AND9640/D

Hardware Design Considerations for Image Sensor Modules

ON Semiconductor®

www.onsemi.com

APPLICATION NOTE

Introduction

This application note is intended to be used as a baseline for design recommendations for image sensor modules. This application note describes layout best practices for image sensor module design and provides a list of recommendations to assist with design decisions in the layout process.

A few fundamental signal integrity (SI) concepts are presented in order to understand the background for the design recommendations. We also cover different types of electrical noise which influence image quality along with key influencing factors and design recommendations to address them. This is not an exhaustive description of a complex subject, but offered to help the module designers in understanding the reasoning for the design guidelines.

Signal Integrity and EMI

Electromagnetic interference (EMI) is defined as unwanted, conducted, or radiated signals of electronic origin that can cause degradation of system performance, while signal integrity refers to methods that ensure electrical signals are of sufficient quality for proper operation. Examples that affect signal integrity include crosstalk, ringing, ground bounce, and power supply noise. Failure to plan for induced noise can cause the final design to work incorrectly, affect image quality, force redesigns and lower yield. Although we are not specifically discussing EMI in this application note, techniques to improve SI will often result in lowering overall system EMI. The next sections provide details about signal integrity and EMI:

- Frequency and Time Domain Relationship
- Mutual Capacitance, Self Inductance and Mutual Inductance
- Thermal Considerations

Frequency and Time Domain Relationship

The first concept is that a digital waveform observed in the time domain is a combination of a sum of multiple harmonics in the frequency domain (see Figures 1 and 2). Non−sinusoidal signals can be described as a combination of multiple sinusoidal frequencies of various amplitudes. One must think of each frequency traveling down the signal path individually and how that signal might be affected by the RLC effects of the signal path and then the sum of all of the frequencies are combined at the endpoint. The result of combining all of the individual frequencies is that if every frequency of concern is unaffected by the signal path, then one would have the same waveform at the endpoint as in the beginning. If any particular frequency is affected by the signal path, then the overall signal becomes distorted. If the resulting waveform is highly distorted, this could affect the proper operation of your system.

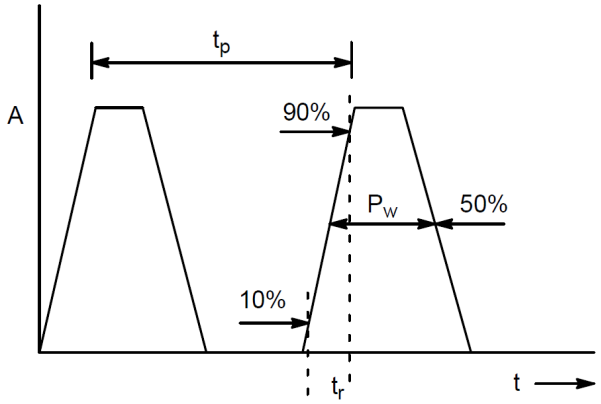


Figure 1. Time Domain of a Trapezoidal Pulse

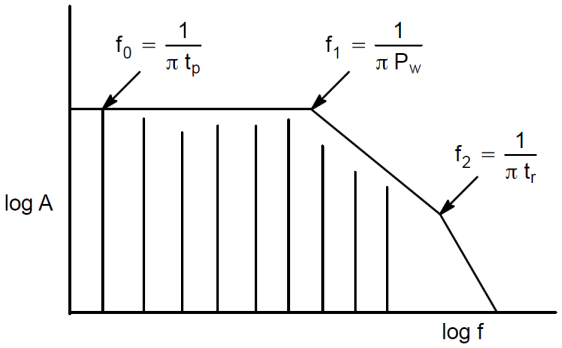


Figure 2. Frequency Domain of a Trapezoidal Pulse

While trying to focus on bandwidth of interest, rise and fall times of involved signals need careful consideration. For a clock square wave with rise time of t_r, Figure 2 could be used as basic rule of thumb to understand bandwidth involved in frequency domain. E.g. Digital signal with 500 ps rise time would generate frequencies of interest up to 636 MHz. Slower rise times will generate less high frequency signals thereby reducing the signal bandwidth. Slew rate control if allowed can also help in mitigating EMI.

Mutual Capacitance, Self−Inductance and Mutual Inductance

Mutual capacitance is intentional or unintentional capacitance which occurs when voltage change on one conductor introduces current in adjacent conductor. When conductors are closely spaced together in a transmission line, the air or material separating the lines acts as dielectric and the conductors act as capacitor plates. The Figure 3 below helps in visualizing crosstalk caused by mutual capacitance where capacitive coupling of two electric fields occurs when current injected in victim line is proportional to dV/dT of aggressor line. A rising edge on aggressor induces a noise current on the victim line introducing positive crosstalk with a time duration equal to rise time at aggressor.

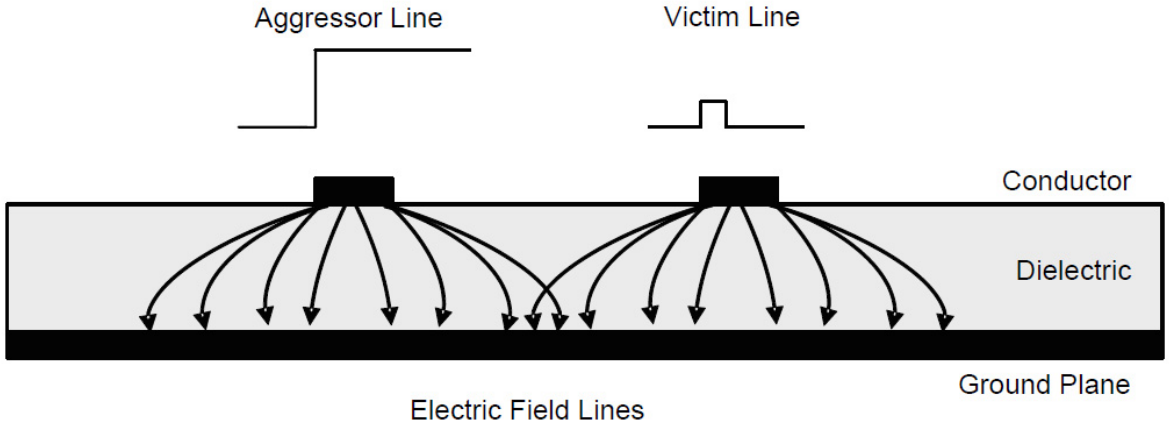


Figure 3. Mutual and Self Capacitance

Self−inductance is the voltage induced in a current carrying wire when current in the wire is changing. Magnetic field created by changing current in a circuit induces a voltage change in the same circuit making the voltage change self−induced.

Mutual inductance is the phenomenon which comes into play when more than one current loop are present. Magnetic field strength is proportional to magnitude and direction of loop current. Mutual inductance causes positive and negative crosstalk. Figure 4 provides a visual example of how magnetic fields interact when two traces are physically brought together. The magnetic field lines begin to interact and fraction of flux from conductor A passes through flux of conductor B. Faradays law states that induced voltage is proportional to rate of change of flux in loop B. The magnitude of inductive coupling depends on direction of current flow in adjacent conductor. If we have a high frequency signal travelling in a wire loop, the effective inductance can be described as:

$$Leff = L1 + L2 \pm 2M$$

M is the mutual inductance which is coupling factor between conductors.

Direction of current decides the polarity of ±M. ‘+’ for currents in same direction and ‘−‘ for opposite direction. Figure 3 shows an example of negative crosstalk.

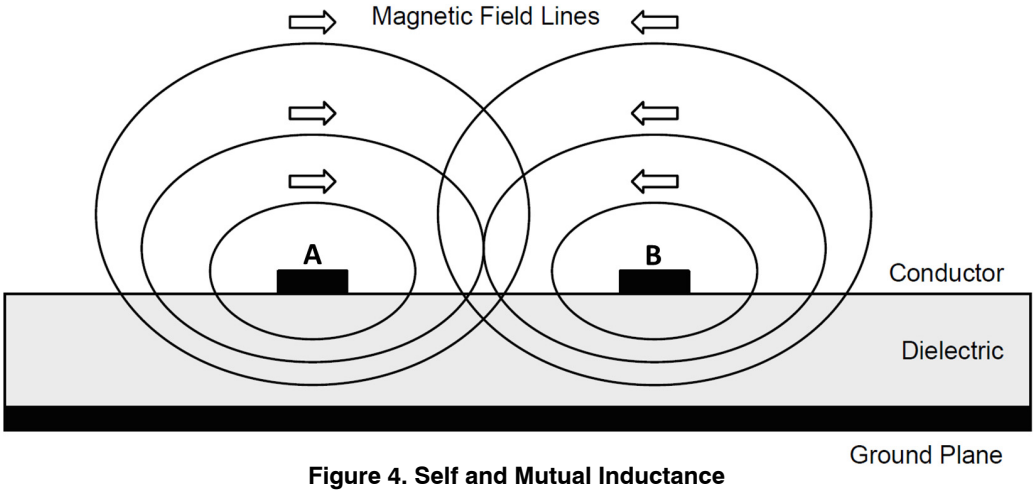


Figure 4. Self and Mutual Inductance

Mutual inductance can be used to our benefit to reduce overall effective inductance in current path. This can be accomplished by bringing the return current path as close as possible to the source path. Mutual inductance is a current flow problem and improving return current path fixes inductive crosstalk. Conversely, if the current is going in the same direction, this increases effective inductance. Ideally we would want to use these techniques to minimize interaction between signals.

A current loop is the path taken by current from Tx to Rx and back to Tx. All designs should target to make current loop area as small as possible.

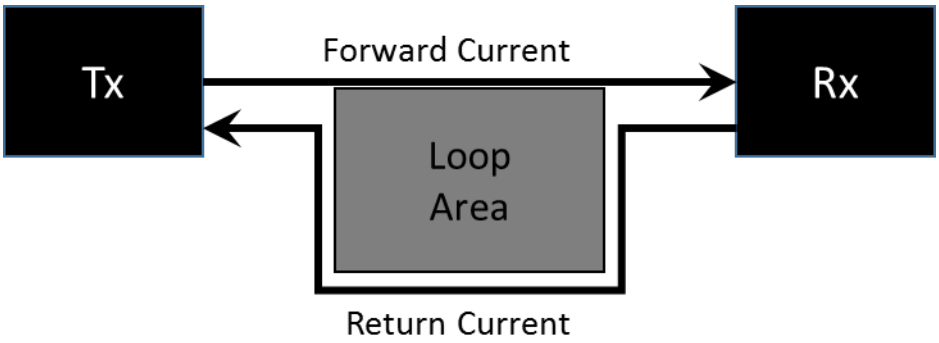


Figure 5. Current Loop and Loop Area

Lower effective inductance can be achieved by keeping the return current path close to the forward current path. Using a ground path under the signal wire can reduce the loop area. For signals going in the same direction, a minimum of 5h separation is desired to avoid positive crosstalk (h− dielectric thickness between signal layer and adjacent ground plane). Smaller loop area helps in avoiding interference into adjacent circuits, thereby reducing EMI.

Current always follows path of least impedance. Resistive effects dominate at lower frequencies and L and C effects dominate at high frequencies. ESR and ESL effects should be considered when high frequency response is critical.

Thermal Considerations:

Image sensor is the primary heat source in an image sensor module. Power delivery to the image sensor can be termed as the next dominant heat source on module. Optimal power conversion on a module while keeping in mind the key sensitivities of the image sensor, can help in optimizing the power loss and hence the thermals on the module. In absence of an external heat sink, PCB is the biggest heat sink available for thermal management. Module layout will have a major influence on the image noise levels of final product as increased PCB temperature increase dark currents thereby raising the noise floor. It is imperative to integrate proper thermal management strategies in system design to prevent degradation in image quality. Maximize ground flood under the image sensor and power supplies and add ground vias as available to maximize thermal transfer from the top layer.

Module Layout: Best Practices

Module layout is very critical to the overall image sensor performance. The content below should be used as a guideline to make educated tradeoffs in an attempt to achieve best performing design with the available design constraints.

This is a wide topic and the key topics can be broken down into following topics:

- General guidelines

- Clocks and high speed traces
- Power supply
- Decoupling capacitor selection

General Guidelines:

The following list provides design guidelines for different areas of PCB layout.

1. Follow ON Semiconductor datasheet and developer guide for information to correctly terminate unused pins
2. To lower inductance and minimize crosstalk, use multilayer boards with solid power and ground plane. At least 4−layer board is desirable. If high speed traces are routed in top and bottom layer, it is advisable to minimize loop area by assuring a low Z ground path is available to the signal when it transitions layers.
3. If solid GND plane is not possible, consider minimizing overall inductance of return current path. Ways to minimize inductance of return path:
   a. Avoid voids on GND layer. Voids are typically caused by vias placed too close together. Avoid any other planes on GND layer
   b. Avoid routing any signal traces on GND layer. This slices the plane and increases path inductance.
4. All high−frequency signals should flow over solid ground plane related to signal to minimize loop area.
5. When using flex cable, use return current path under signal trace where possible. This helps in keeping smaller loop area. This reduces chances of crosstalk.
6. Use a solid GND on flex cable. It provides better impedance matching and favors improved signal integrity
7. If the module has multiple connectors connecting to a host board, place them in proximity to each other to avoid large return current loops which can lead to crosstalk.
8. Vias represent discontinuity in signal path, use them very carefully. When signal traces change layers from top to the bottom of the board the return current should also transition layers. Place GND vias, to facilitate the return current layer change. This helps in keeping smaller loop area and reduces chances for crosstalk.

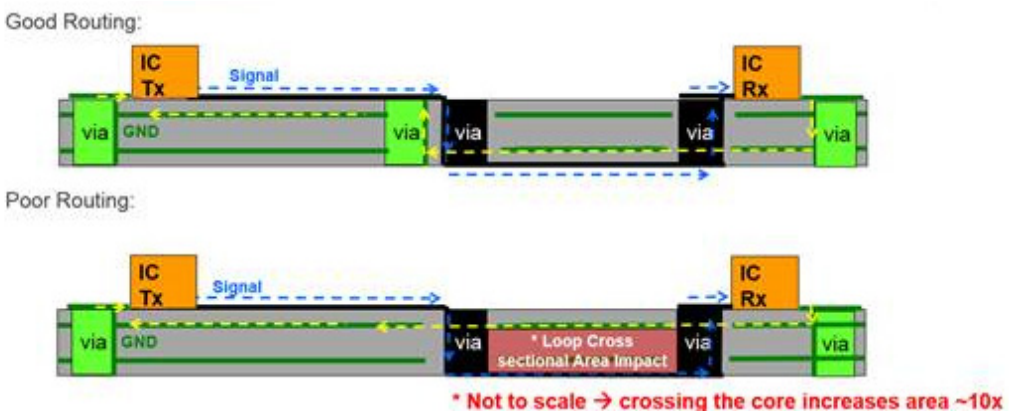
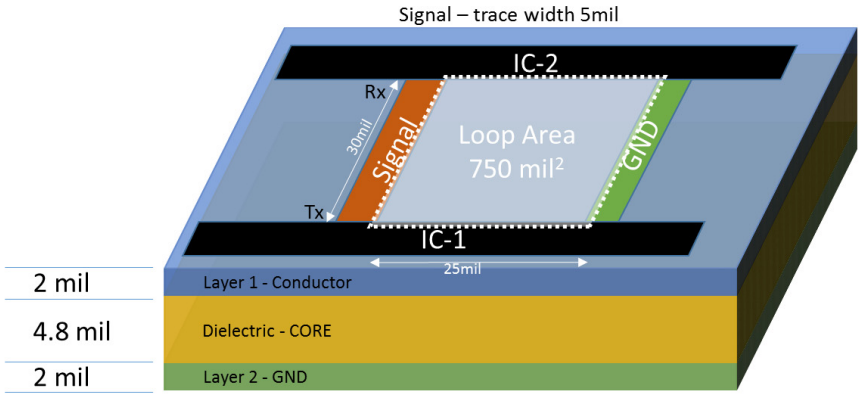
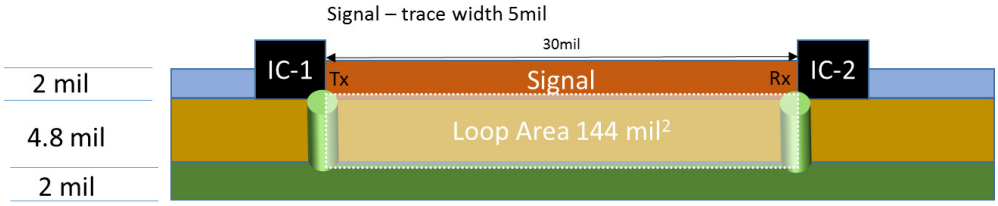


Figure 6. GND and via Signaling

9. Split grounds need to be implemented very cautiously. They create multiple routing channels for return current paths. Typically for image sensor modules splitting analog and digital grounds is not required as the split grounds increase the path inductance of return current path thereby compromising the high speed performance response.
10. If using split grounds, route signal traces over/under respective power/ground return paths. Digital signals over digital ground and analog area over analog ground.
11. Using GND traces to isolate high speed signals and their use as return current path has benefit only in PCB which does not have a dedicated ground plane. If the design has a ground layer using that plane for return current path provides smallest possible loop area. Comparing Option A v/s Option B in Figure 7 will provide an idea on the smaller loop area by using an adjacent ground plane for return current path. Using guard traces take up PCB real estate without much perceivable benefit.



Option A



Option B

Figure 7. Loop Area Comparisons Using Adjacent Ground Layer Recommendations

Clocks and High speed traces:

1. Keep clock traces as short as possible.
2. Discontinuities in a transmission line path degrade the signal quality. Do not use 90 degree ends, 45 degree bends are preferred.
3. Avoid changing layers on the clock trace.
4. When available slew rate control of clock edges allows in minimizing simultaneous pad switching currents and ground bounce and minimize overshoot and undershoot caused by pulse reflections from the load.
5. Follow termination requirements for all signals and use proper termination topologies if required to minimize reflections and ringing on high speed signals.
   a. MIPI requires 50 Ω single ended traces = 100 Ω differential intra−pair
   b. Dielectric thickness between signal and ground layer determines trace width
6. Avoid layer transitions as much as possible to avoid via induced discontinuities. If vias are used in signal path, follow directions mentioned in Figure 6 to keep loop area as small as possible.
7. Match trace length and widths across all high speed data lines to avoid and impedance mismatch. Impedance mismatch will deteriorate signal integrity and cause reflections and ringing. It is recommended to have
   c. Intra−pair length matching ≤ 150 μm
   a. Inter−pair length matching ≤ 300 μm
   a. Parallel length matching ≤ 300 μm
8. Trace spacing is a function of dielectric spacing to adjacent layer GND plane. If h=dielectric thickness, maintain the following guidelines to avoid any crosstalk induced coupling.
   a. MIPI N/P Intra−pair spacing ≥ 3h
      i. 25 μm dielectric = 75μm minimum spacing
   b. MIPI N/P pair spacing to other signals ≥ 5h
      i. 25 μm dielectric = 125 μm minimum spacing
   c. Parallel maintain ≥ 3h spacing between lines and ≥ 5h to other signals

Power Supply

1. Use solid plane to distribute power. This reduces the path impedance
2. Limit the power and ground signal path to as short as possible to avoid any negative impact on the power path impedance.
3. Provide dedicated ground layers adjacent to power layers to minimize the loop area and avoid mutual inductance and capacitance based effects as discussed above.
4. Loading pattern on multiple power blocks is a function of data readout from the image sensor array. Each row read is seen as a load transient for the power supply across all power blocks. It is imperative that the power delivery to image sensor can respond to this load transients by image sensor. Electrical noise is usually translated into

image noise if power supplies are not carefully designed.

5. Power supply topology selection for specific rail should be based on following:
   a. Image sensor sensitivity to electrical noise.
   b. Power consumption

The table below should help in summarizing the pros and cons of each topology:

Table 1. POWER SUPPLY TOPOLOGY COMPARISON

	Linear VR	Sync-Buck VR
DC Accuracy	+/- 1-2%	+/- 1-2%
Ripple	<1mV	5-10mV typ
Transient Response	~5us recovery time	> 10us recovery time
PSRR	High = couple mV impact	Low > 5x LDO pkpk
Efficiency	Fixed = Vout/Vin	Poor < 30mA Good > 30mA
Design Complexity	Stable with recommended decoupling	Need to ensure stability in time and frequency domain in current design configuration
EMI Issues	Lower as lower switching/circulating currents	Potential to create lot of issues if not carefully designed
Solution Size	Small	Bigger
Solution Cost	Low – Includes IC+C	High – Includes Controller + L + C

   c. Linear VR(LDO) preferred for noise sensitive rails like VAA and VAAPIX
      i. Low ripple
      ii. Fast load transient response
   d. Switching VR preferred for less sensitive but higher power rails like VDD, VDDIO
      i. High power efficiency
6. Consider using remote sense to enable the VR to sense the voltage at the sensor. This will enable the VR to respond to the load transients at the sensor by reducing the impact of the power path impedance.
7. For an application which has higher system voltage coming in as the main power rail for image sensor it is recommended to convert to a mid−level before feeding it to the image sensor. This provides the following benefits:
   a. Separates image sensor power from system power – PSRR improvement
   b. Improves efficiency of the sensor system – improved thermals
   c. Helps with tight form factor requirements – Enables use of smaller components
   d. Generally works out to a cost and performance optimized option

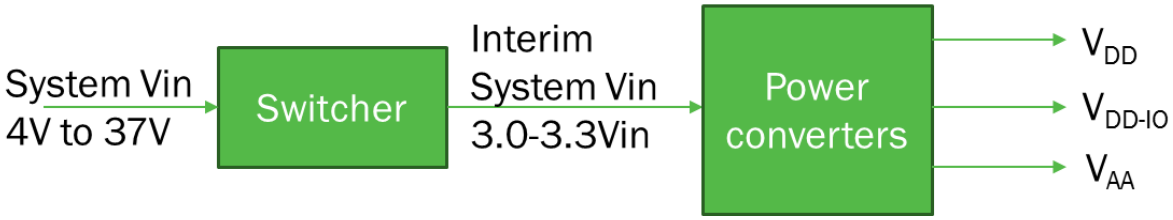


Figure 8. System Power Breakdown Diagram

8. Ferrite beads should not be used in power path between image sensor and power supply. They add path impedance and adversely impact the VR's ability to respond to the load transients on image sensor. The ferrite bead in combination with the capacitance around it adds resonance and high frequency isolation which causes the dynamic currents to resonate and results in higher pk−pk voltages on power supply. The DCR in ferrite beads also introduces a DC drop when placed in power path. A carefully designed system should not need any ferrite beads for noise isolation.

Power Supply Decoupling and Bypass Capacitors

Bypass capacitors are used to reduce high frequency current by shunting and reducing noise current to ground.

Proper bypassing is required for decoupling capacitors as they are the key energy storage elements. The bypass path must provide significantly lower impedance at the frequency of interest. An ideal power supply has zero impedance.

Decoupling capacitors are used to reduce the peak to peak voltage seen by the circuit. Use of good decoupling techniques reduce transmission of energy from one part of circuit to another by storing the energy locally and providing isolation between two circuits to ensure proper operation.

Decoupling and bypass capacitors are usually tied between ground and other power/signals to reduce noise levels.

General capacitor guidelines:

1. Minimum decoupling capacitor must be able to supply current required during worst case switching conditions. I = C dv/dt could be used to calculate the required capacitor sizes.
2. It is extremely important to consider the capacitor response across from 100 Hz up to 100 MHz to understand the capacitor response and effectiveness.
3. In a real system capacitors have parasitic elements associated with the package. A capacitor consists of RLC elements in series. Effectiveness across frequency is determined by the parasitic elements of the capacitor.

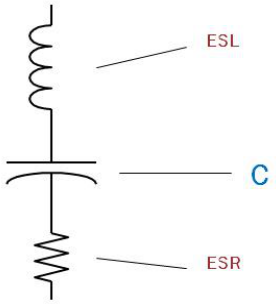
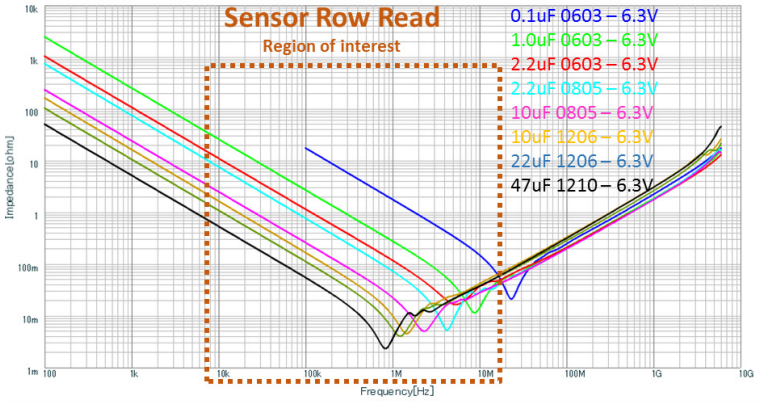


Figure 9. Capacitor Parasitics

4. MLCC are recommended to use on module because of the low ESR and ESL characteristic that they offer across frequency. ESR is major component of the impedance profile at low frequency (<1 MHz) ESL dominates at higher frequencies (>1 Mhz)



Impedance at 200kHz
0.1uF 0603 = 8.639 ohm
1.0uF 0603 = 1.36 ohm
2.2uF 0603 = 0.58 ohm
2.2uF 0805 = 0.382
10uF 0805 = 0.13 ohm
10uF 1206 = 0.082 ohm
22uF 1206 = 0.058 ohm
47uF 1210 = 0.026 ohm

Figure 10. Capacitor Parasitics – (Source−Murata SimSurfing tool)

For similar capacitor value and voltage rating, bigger capacitor size will have improved low frequency impedance profile because of lower ESR and marginally compromised high frequency response because of higher ESL.

5. Multiple capacitors in parallel make it easier for physical distribution by lowering ESR and ESL. 0.1 μF in parallel with a higher value capacitor can be seen as standard recommendation in design guides. The main reason behind that is they offer lower ESL. With a lower ESL, we avoid the possibility of creating a frequency resonant pole caused by lead inductance of capacitor and inter−nplane capacitance. With enhancements in MLCC structures and materials used even the higher value capacitors offer ESL comparable to 0.1uF. Please provide careful attention to the impedance profile of the capacitors in design available from manufacturers and low net impedance at higher frequencies is very critical design parameter to be considered.
6. For higher performance more unique package options like reverse geometry are available which offer up to 4x improvements in ESL profile for improved high frequency response.

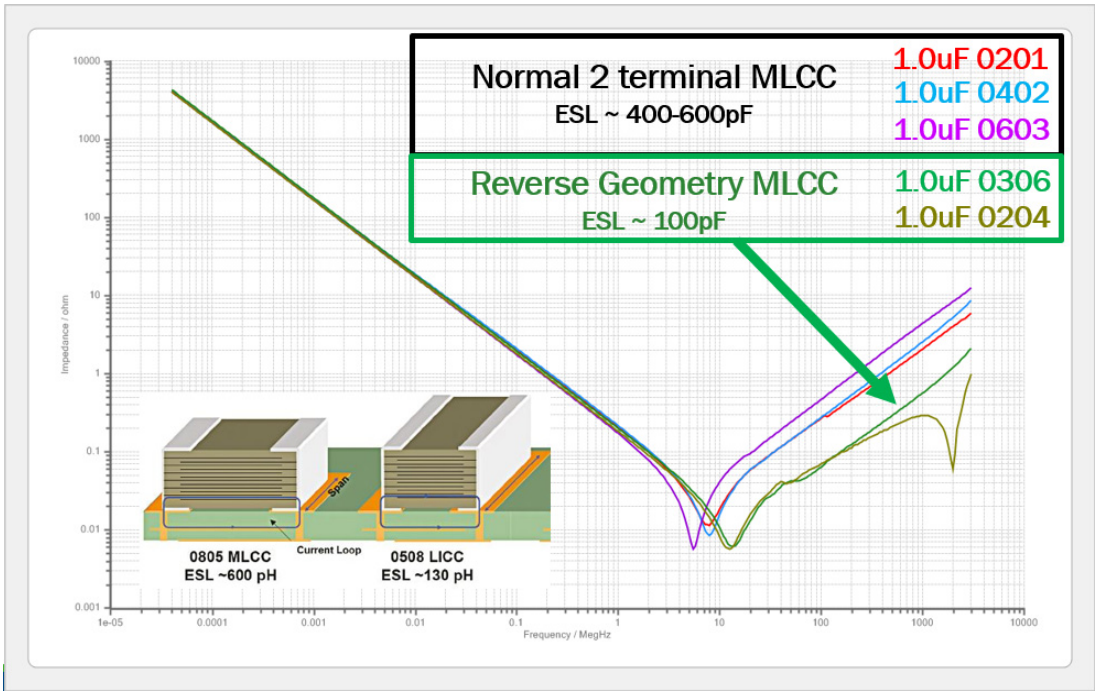


Figure 11. Reverse Geometry Capacitor Parasitics – (Source–Murata SimSurfing tool)

7. Do not use thermal reliefs on bypass capacitors. This increases effective ESL and effects their high frequency response.
8. Distribute the capacitor placement across key locations where sink/source energy is critical.
   a. Some amount of capacitance required by power supply (VR) for stable operation. That should be placed in proximity to the VR. In case of a switching power supply, place a capacitor close to the inductor for ripple currents.
   b. Place capacitance close to the image sensor power pads to provide shorter path for fast transient currents.
9. Use optimal via placements next to the capacitor power and ground pads to transfer current directly to the power and ground planes. This optimizes capacitor performance and also helps in reducing loop area. In Figure 12, the Option B is a desirable configuration to minimize loop area.

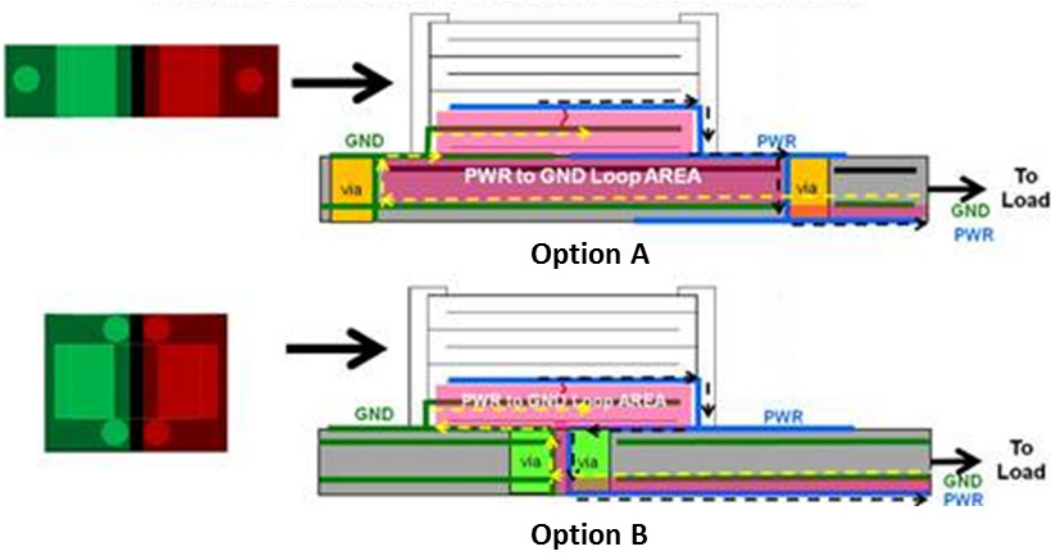


Figure 12. MLCC via Placement Influence on Loop Area

10. When constrained by the total number of capacitors on image sensor module, prioritize the most sensitive rails to have the local decoupling. Vaa and PIX rails should be given the highest priority followed by Vddio and Vdd.

Summary

Careful power architecture selection, component selection and PCB design are very critical to image sensor performance. Following the design outlines highlighted above can limit issues caused due to signal integrity and sub−par quality issues and guarantee that the image sensor can deliver its optimal performance. If caution is exercised upfront, it reduces chances of PCB re-spin due to performance issues.

ON Semiconductor does offer schematic and layout reviews for its customers. Please contact your ON Semiconductor representative for this information.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative