AN2750

USB-to-GPIO Bridging with Microchip USB70xx Hubs

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INTRODUCTION

The USB-to-GPIO bridging feature of Microchip's USB70xx family of hubs provides system designers expanded system control and potential BOM reductions. General Purpose Input/Outputs (GPIOs) may be used for any general 3.3V-level digital control and input functions.

Commands may be sent from the USB Host to the internal Hub Feature Controller (HFC) device in the Microchip hub to perform the following functions:

- Set the direction of the GPIO (input or output)
- Enable a pull-up resistor
- Enable a pull-down resistor
- Read the state
- Set the state

SECTIONS

General Information

Part Number-Specific Information

SDK Implementation

Manual Implementation

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REFERENCES

Consult the following documents for details on the specific parts referred to in this application note:

- *Microchip USB7002 Data Sheet*
- *Microchip USB7050 Data Sheet*
- *Microchip USB7051 Data Sheet*
- *Microchip USB7052 Data Sheet*
- *Microchip USB7056 Data Sheet*
- *Microchip Configuration Options for the USB70xx*

GENERAL INFORMATION

Microchip hub USB Bridging features work via host commands sent to an embedded Hub Feature Controller within the device located on an additional internal USB port. In order for the bridging features to work correctly, this internal Hub Feature Controller must be enabled by default. Table 1 provides details on default Hub Feature Controller settings per device.

TABLE 1: DEFAULT SETTINGS FOR HUB FEATURE CONTROLLER ENABLE

Part Number	Part Summary	Hub Feature Controller Default Setting
USB7002	4-Port USB3.1 Gen1 Hub	Enabled by default on port 6
USB7050	4-Port USB3.1 Gen1 Hub with USB power delivery on 3 ports	Enabled by default on port 6
USB7051	4-Port USB3.1 Gen1 Hub with USB power delivery on 2 ports	Enabled by default on port 6
USB7052	4-Port USB3.1 Gen1 Hub with USB power delivery on 1 port	Enabled by default on port 6
USB7056	6-Port USB3.1 Gen1 Hub with USB power delivery on 1 port	Enabled by default on port 8

The Hub Feature Controller is connected to an extra internal port in the hub. It is mapped to the highest numbered port on the hub by default.

The Hub Feature Controller example for the USB7002 is illustrated in Figure 1, while the Hub Feature Controller example for the USB7050, USB7051, and USB7052 is in Figure 2. A sample of the Hub Feature Controller for USB7056 is shown in Figure 3.

FIGURE 1: USB7002 HUB FEATURE CONTROLLER EXAMPLE

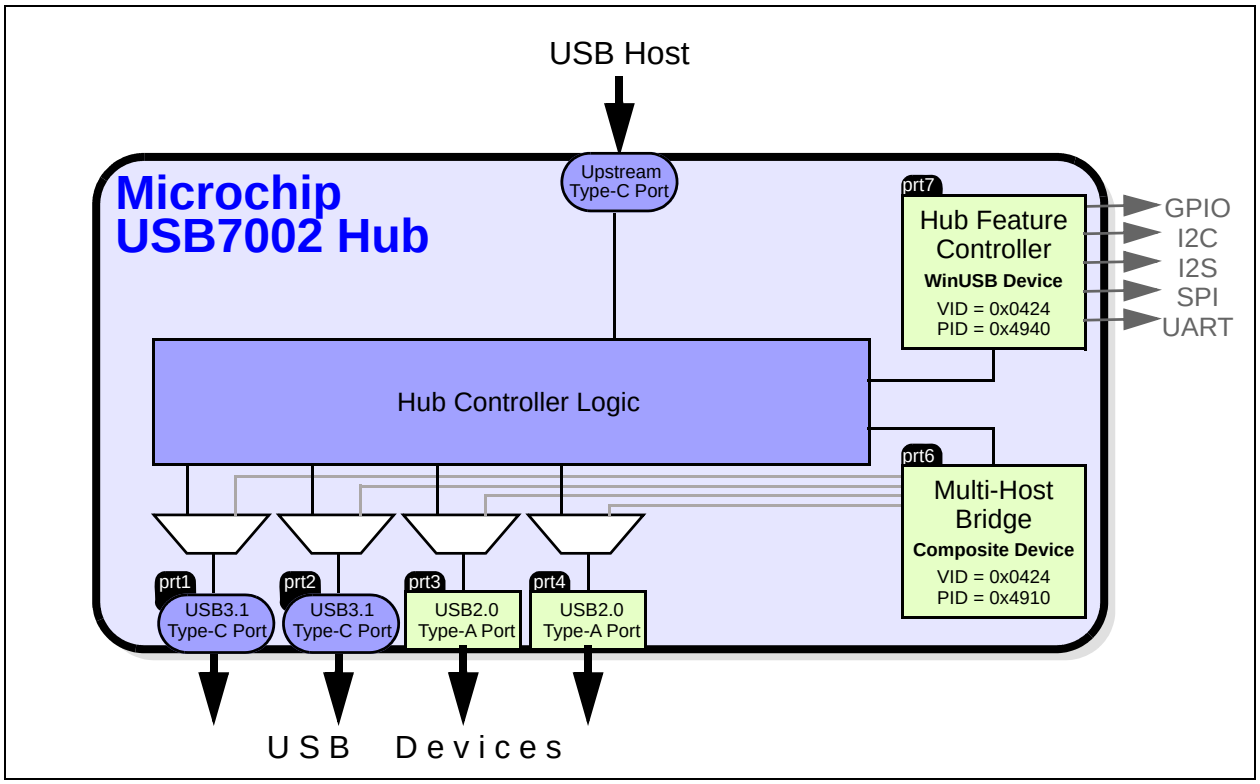


FIGURE 2: USB7050, USB7051, AND USB7052 HUB FEATURE CONTROLLER EXAMPLE

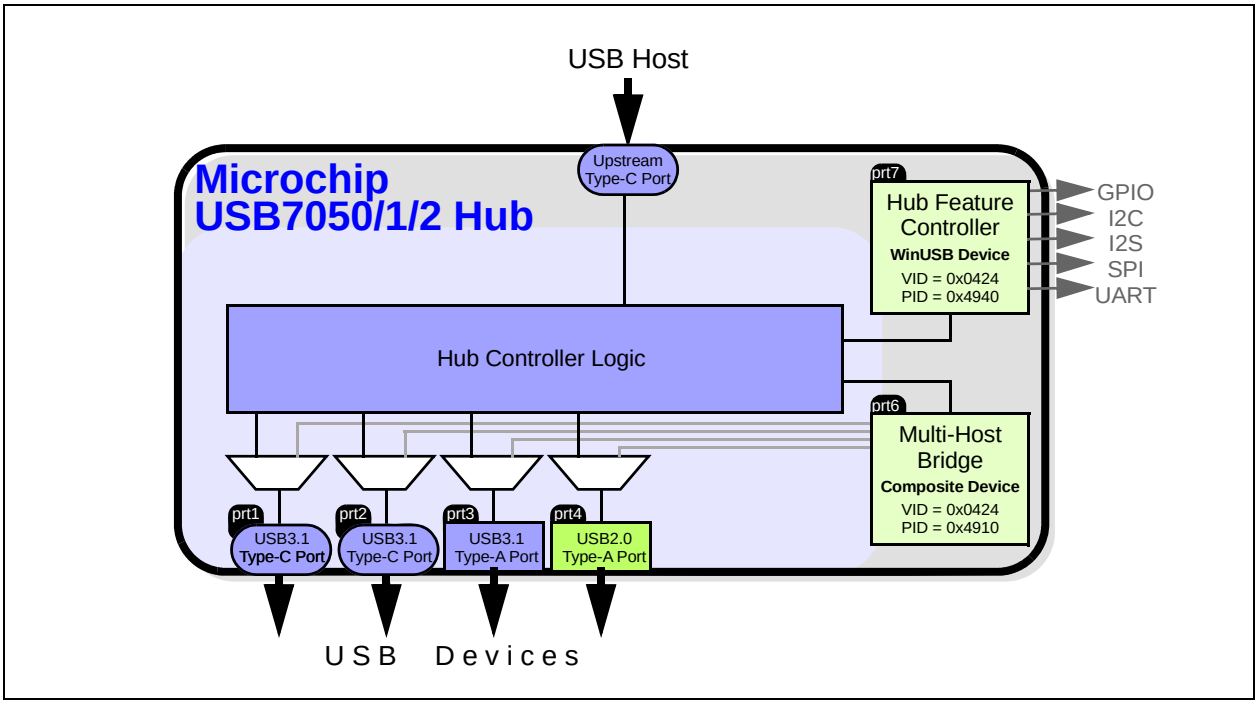
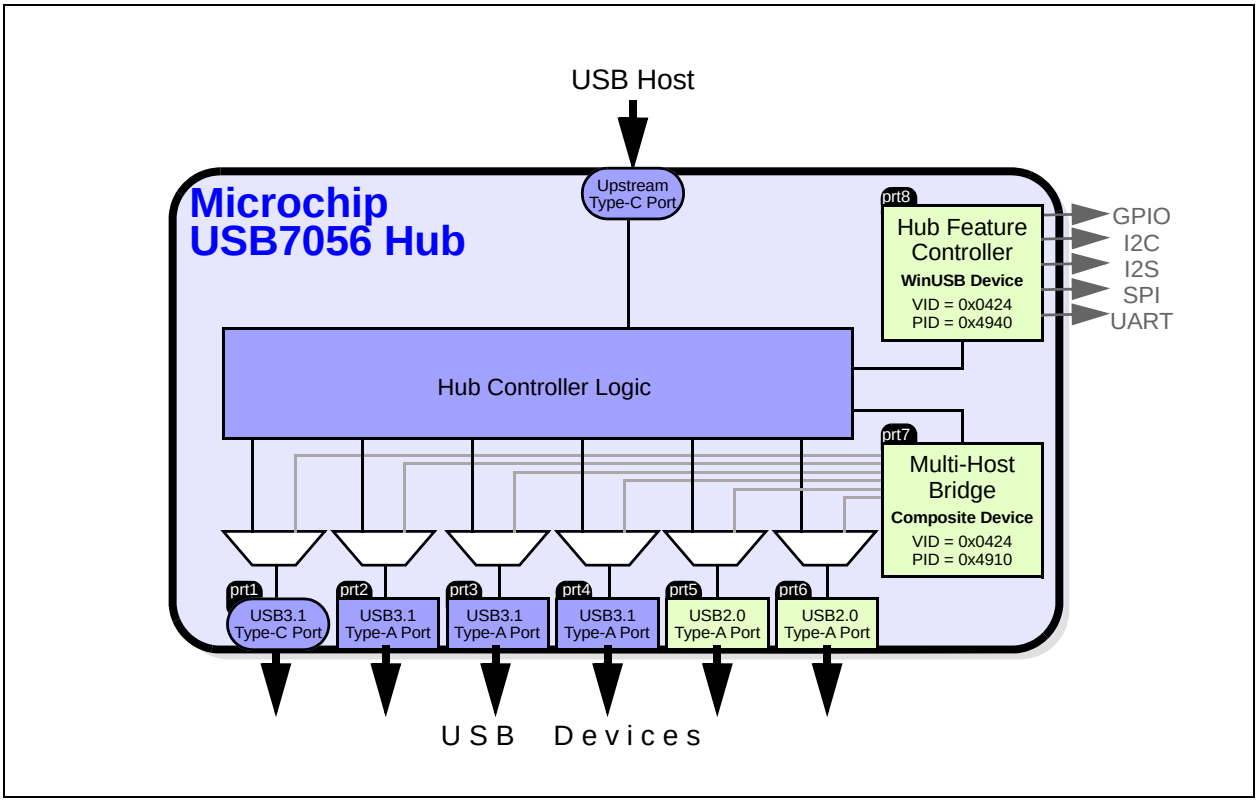


FIGURE 3: USB7056 HUB FEATURE CONTROLLER EXAMPLE



The following GPIO functions are supported:

- Set the GPIO Direction (Input or Output)
- Enable GPIO Internal Pull-up Resistor
- Enable GPIO Internal Pull-down Resistor
- GPIO Read State (Input Mode)
- GPIO Set State (Output Mode)

Set the GPIO Direction (Input or Output)

Each GPIO can be configured as either a Schmitt-triggered input or output with an 8 mA sink/source.

Enable GPIO Internal Pull-up Resistor

Each GPIO can be enabled with a 50 uA (typical) internal pull-up resistor. Internal pull-up resistors prevent unconnected inputs from floating. The pull-up is only 67k, so it may not be strong enough to drive a load of less than 100k. When connected to a load that must be pulled high, an external resistor must be added.

Enable GPIO Internal Pull-down Resistor

Each GPIO can be enabled with a 50 uA (typical) internal pull-down resistor. Internal pull-down resistors prevent unconnected inputs from floating. The pull-down is only 67k, so it may not be strong enough to drive a load of less than 100k. When connected to a load that must be pulled low, an external resistor must be added.

GPIO Read State (Input Mode)

Read a 0: GPIO is below 0.9V.

Read a 1: GPIO is above 1.9V.

Note:	When configured as an input, the GPIOs are digital Schmitt-triggered inputs. The range 0.8V to 2.0V is an indeterminate input state, so 3.3V-to-2.5V signaling is supported.

GPIO Set State (Output Mode)

Set to 0: GPIO Drives to 0.0V. When driven low, an 8 mA sink is enabled, driving the pin to 0.4V or lower.

Set to 1: GPIO Drives to 3.3V. When driven high, an 8 mA source is enabled, driving the pin to VDD33 to 0.4V or higher.

PART NUMBER-SPECIFIC INFORMATION

Part Summary

Table 2 summarizes the total number of available GPIOs by part number. Many of the GPIOs on the hub are only available after configuration. The following methods may be used to configure the hub:

- **ProTouch:** If configuring via internal One-Time Programmable (OTP) memory or SPI EEPROM with a base firmware file
- **SMBus/I^{2}C Configuration:** If using an embedded SoC/I^{2}C EEPROM to configure the hub at each start-up/reset
- **Pin Strapping:** Many of the GPIOs are made available by specific pin strapping or by simply not populating an SPI EEPROM device.

TABLE 2: GPIO AVAILABILITY SUMMARY

	USB7002	USB7050	USB7051	USB7052	USB7056
Minimum GPIOs Available	4 (CONFIG2)	8 (CONFIG1)	4 (CONFIG3)	1 (CONFIG3)	1 (CONFIG2)
Maximum GPIOs Available	12 (CONFIG4)	14 (CONFIG4)	11 (CONFIG4)	8 (CONFIG4)	2 (CONFIG1)

TABLE 3: USB7002 GPIOS

	CONFIG1 (I^{2}C)	CONFIG2 (I^{2}S)	CONFIG3 (UART)	CONFIG4 (FLEX)
PF6	GPIO70	GPIO70	*UART_RX*	GPIO70
PF7	GPIO71	*MIC_DET*	*UART_TX*	GPIO71
PF12	GPIO76	—	—	GPIO76
PF14	GPIO78	*I2S_SDI*	*UART_nCTS*	GPIO78
PF18	*MSTR_I2C_CLK*	*I2S_LRCK*	*UART_nDCD*	GPIO82
PF19	*MSTR_I2C_DATA*	*I2S_SDO*	*UART_nRTS*	GPIO83
PF26	*SLV_I2C_CLK*	*I2S_SCK*	*UART_nDSR*	GPIO90
PF27	*SLV_I2C_DATA*	*I2S_MCLK*	*UART_nDTR*	GPIO91
PF28	GPIO92	GPIO92	GPIO92	GPIO92
PF29	GPIO93	GPIO93	GPIO93	GPIO93
PF30	GPIO94	*MSTR_I2C_CLK*	GPIO94	GPIO94
PF31	GPIO95	*MSTR_I2C_DATA*	GPIO95	GPIO95

TABLE 4: USB7050 GPIOS

	CONFIG1 (I^2C)	CONFIG2 (I^2S)	CONFIG3 (UART)	CONFIG4 (FLEX)	CONFIG5
PF2	GPIO66	GPIO66	*UART_nCTS*	GPIO66	GPIO66
PF3	GPIO67	*I2S_SDI*	*UART_nRTS*	GPIO67	GPIO67
PF4	*PD_SPI_CE_N2*	*I2S_SDO*	*UART_nDSR*	GPIO68	GPIO68
PF5	*PD_SPI_CE_N1*	*I2S_SCK*	*UART_nDTR*	GPIO69	GPIO69
PF6	*PD_SPI_CE_N0*	*I2S_LRCK*	*UART_RX*	GPIO70	GPIO70
PF7	*PD_SPI_CLK*	*I2S_MCLK*	*UART_TX*	GPIO71	GPIO71
PF14	GPIO78	GPIO78	GPIO78	GPIO78	GPIO78
PF19	SLV_I2C_DATA	SLV_I2C_DATA	SLV_I2C_DATA	GPIO83	*SLV_I2C_DATA*
PF26	*SLV_I2C_CLK*	*SLV_I2C_CLK*	*SLV_I2C_CLK*	GPIO90	*SLV_I2C_CLK*
PF27	GPIO91	*MIC_DET*	GPIO91	GPIO91	GPIO91
PF28	GPIO92	GPIO92	GPIO92	GPIO92	GPIO92
PF29	GPIO93	GPIO93	GPIO93	GPIO93	GPIO93
PF30	GPIO94	GPIO94	GPIO94	GPIO94	GPIO94
PF31	GPIO95	GPIO95	GPIO95	GPIO95	GPIO95

TABLE 5: USB7051 GPIOS

	CONFIG1 (I^2C)	CONFIG2 (I^2S)	CONFIG3 (UART)	CONFIG4 (FLEX)
PF4	GPIO68	GPIO68	GPIO68	GPIO68
PF6	GPIO70	GPIO70	*UART_RX*	GPIO70
PF7	GPIO71	*MIC_DET*	*UART_TX*	GPIO71
PF14	GPIO78	*I2S_SDI*	*UART_nCTS*	GPIO78
PF19	SLV_I2C_DATA	I2S_SDO	*UART_nRTS*	GPIO83
PF26	*SLV_I2C_CLK*	I2S_SCK	*UART_nDSR*	GPIO90
PF27	GPIO91	I2S_MCLK	*UART_nDTR*	GPIO91
PF28	GPIO92	I2S_LRCK	*UART_nDCD*	GPIO92
PF29	GPIO93	GPIO93	GPIO93	GPIO93
PF30	GPIO94	GPIO94	GPIO94	GPIO94
PF31	GPIO95	GPIO95	GPIO95	GPIO95

TABLE 6: USB7052 GPIOS

	CONFIG1 (I^2C)	CONFIG2 (I^2S)	CONFIG3 (UART)	CONFIG4 (FLEX)
PF6	GPIO70	GPIO70	*UART_RX*	GPIO70
PF7	GPIO71	*MIC_DET*	*UART_TX*	GPIO71
PF14	GPIO78	*I2S_SDI*	*UART_nCTS*	GPIO78
PF19	SLV_I2C_DATA	I2S_SDO	*UART_nRTS*	GPIO83
PF26	*SLV_I2C_CLK*	I2S_SCK	*UART_nDSR*	GPIO90
PF27	GPIO91	I2S_MCLK	*UART_nDTR*	GPIO91
PF28	GPIO92	I2S_LRCK	*UART_nDCD*	GPIO92
PF29	GPIO93	GPIO93	GPIO93	GPIO93

TABLE 7: USB7056 GPIOS

	CONFIG1 (I^2C)	CONFIG2 (I^2S)
PF6	GPIO70	GPIO70
PF7	GPIO71	*MIC_DET*

SDK IMPLEMENTATION

The simplest method for implementing the USB-to-GPIO Bridging functions is to use the publicly available DLL which is distributed with the MPLAB® Connect Configurator tool. The DLL is compatible with Windows operating systems. Visit the USB705xx product page on microchip.com to download MPLAB Connect with the DLL package. Using the libraries available in the DLL, the Bridging features can be implemented in C-code.

The DLL package contains the following:

- User's guide (*MPLAB Connect DLL User's Guide*) with detailed description of how to use the DLL and call each function
- Release notes
- Library files:
  - For Windows: A ".dll" and a ".lib" file
  - For Linux: A ".cpp" file that can be built into a ".a" file
- Example code

Commands Included in the SDK

- **libMchpUsbGpioConfigureGPIO:** Configures a pin to behave as a GPIO
- **libMchpUsbGpioGet:** Sets the queried GPIO to an input (if not already set as such) and then reads the input state
- **libMchpUsbGpioSet:** Sets the queried GPIO to an output (if not already set as such) and then sets the output state

For additional details on how to use the SDK to implement USB-to-GPIO Bridging, download the SDK package and refer to the user's guide.

MANUAL IMPLEMENTATION

The USB-to-GPIO Bridging features may be implemented at the lowest level if you have the ability to build USB packets. This approach is required if you are not using a Windows or Linux host system and cannot use the SDK.

All USB-to-GPIO Bridging commands are accomplished with internal register writes and reads. Further details can be found in the Microchip application note, *Configuration Options for the USB70xx.* All USB to GPIO bridging commands must be sent directly to Endpoint 0 of the Hub Feature Controller connected to the last downstream port of the Microchip hub.

For details on the register read and write USB SETUP packets, refer to Register Read and Register Write, respectively. The configuration register addresses and contents are detailed in GPIO Configuration Register Map and Register Definitions.

Register Read

To read the state of a GPIO, a register read with the USB SETUP packet in Table 8 must be used:

TABLE 8: REGISTER READ USB SETUP COMMAND

SETUP Parameter	Value	Description
bmRequestType	0xC0	Device-to-host, vendor class, targeted to interface
bRequest	0x04	Register read command: CMD_REG_READ
wValue	Register address LSB	Valid address range: <0x0000> to <0xFFFF> [64KB]
wIndex	Register address MSB	Valid address range: <0x0000> to <0xFFFF> [64KB]
wLength	Data length	Length of the data bytes to be retrieved

REGISTER READ USB TRANSACTION SEQUENCE

Command Phase: The Hub Feature Controller receives the SETUP packet with the parameters specified in Table 8.

Data Phase: The Hub Feature Controller sends the data bytes of length wLength from the specified address.

Status Phase: The Hub Feature Controller sends ACK on the successful completion of register read.

Register Write

To configure the direction of a GPIO, pull-up/pull-down resistor settings, or set the output state of a GPIO, a register write command with the USB SETUP packet in Table 9 must be used:

TABLE 9: REGISTER WRITE USB SETUP COMMAND

SETUP Parameter	Value	Description
bmRequestType	0x40	Host-to-device, vendor class, targeted to interface
bRequest	0x03	Register read command: CMD_REG_WRITE
wValue	Register address LSBs	Last four bytes of the 32-bit register address
wIndex	Register address MSBs	First four bytes of the 32-bit register address
wLength	Data length	Length of data bytes to write

REGISTER WRITE USB TRANSACTION SEQUENCE

Command Phase: The Hub Feature Controller receives the SETUP packet with the parameters specified in Table 9.

Data Phase: The Hub Feature Controller receives the data bytes of length wLength to be written to the register starting from the specified address.

Status Phase: The Hub Feature Controller sends ACK on successful completion of register write.

GPIO Configuration Register Map

TABLE 10: CONFIGURATION REGISTER MEMORY MAP

Address	Name	R/W	Function	Default
BF80 0908	PIO96_OEN	R/W	PIO[95:64] Output Enable Register	00h
BF80 0918	PIO96_IEN	R/W	PIO[95:64] Input Enable Register	00h
BF80 0928	PIO96_OUT	R/W	PIO[95:64] Output State Register	00h
BF80 0938	PIO96_IN	R	PIO[95:64] Input State Register	00h
BF80 0948	PIO96_PUE	R/W	PIO[95:64] Pull-up Enable Register	00h
BF80 0958	PIO96_PDE	R/W	PIO[95:64] Pulldown Enable Register	00h

Register Definitions

TABLE 11: PIO[95:64] OUTPUT ENABLE REGISTER

PIO96_OEN (BF80 0908h)			PIO[95:64] Output Enable Register
Bit	**Name**	**R/W**	**Description**
31	GPIO_95_OE	R/W	Set bit to enable GPIO95 as an output.
30	GPIO_94_OE	R/W	Set bit to enable GPIO94 as an output.
29	GPIO_93_OE	R/W	Set bit to enable GPIO93 as an output.
28	GPIO_92_OE	R/W	Set bit to enable GPIO92 as an output.
27	GPIO_91_OE	R/W	Set bit to enable GPIO91 as an output.
26	GPIO_90_OE	R/W	Set bit to enable GPIO90 as an output.
25:20	Reserved	R	Reserved
19	GPIO_83_OE	R/W	Set bit to enable GPIO83 as an output.
18	GPIO_82_OE	R/W	Set bit to enable GPIO82 as an output.
17:15	Reserved	R	Reserved
14	GPIO_78_OE	R/W	Set bit to enable GPIO78 as an output.
13	Reserved	R	Reserved
12	GPIO_76_OE	R/W	Set bit to enable GPIO76 as an output.
11:8	Reserved	R	Reserved
7	GPIO_71_OE	R/W	Set bit to enable GPIO71 as an output.
6	GPIO_70_OE	R/W	Set bit to enable GPIO70 as an output.
5	GPIO_69_OE	R/W	Set bit to enable GPIO69 as an output.
4	GPIO_68_OE	R/W	Set bit to enable GPIO68 as an output.
3	GPIO_67_OE	R/W	Set bit to enable GPIO67 as an output.
2	GPIO_66_OE	R/W	Set bit to enable GPIO66 as an output.
1:0	Reserved	R	Reserved
Note:	**BF80_0908h:** GPIO66-71; **BF80_0909h:** GPIO76-78; **BF80_090Ah:** GPIO82-83; **BF80_090Bh:** GPIO 90-92		

TABLE 12: PIO[95:64] INPUT ENABLE REGISTER

PIO96_IEN (BF80 0918h)			PIO[95:64] Input Enable Register
Bit	**Name**	**R/W**	**Description**
31	GPIO_95_IE	R/W	Set bit to enable GPIO95 as an input.
30	GPIO_94_IE	R/W	Set bit to enable GPIO94 as an input.
29	GPIO_93_IE	R/W	Set bit to enable GPIO93 as an input.
28	GPIO_92_IE	R/W	Set bit to enable GPIO92 as an input.
27	GPIO_91_IE	R/W	Set bit to enable GPIO91 as an input.
26	GPIO_90_IE	R/W	Set bit to enable GPIO90 as an input.
25:20	Reserved	R	Reserved
19	GPIO_83_IE	R/W	Set bit to enable GPIO83 as an input.
18	GPIO_82_IE	R/W	Set bit to enable GPIO82 as an input.
17:15	Reserved	R	Reserved
14	GPIO_78_IE	R/W	Set bit to enable GPIO78 as an input.
13	Reserved	R	Reserved
12	GPIO_76_IE	R/W	Set bit to enable GPIO76 as an input.
11:8	Reserved	R	Reserved
7	GPIO_71_IE	R/W	Set bit to enable GPIO71 as an input.
6	GPIO_70_IE	R/W	Set bit to enable GPIO70 as an input.
5	GPIO_69_IE	R/W	Set bit to enable GPIO69 as an input.
4	GPIO_68_IE	R/W	Set bit to enable GPIO68 as an input.
3	GPIO_67_IE	R/W	Set bit to enable GPIO67 as an input.
2	GPIO_66_IE	R/W	Set bit to enable GPIO66 as an input.
1:0	Reserved	R	Reserved
Note:	**BF80_0918h:** GPIO66-71; **BF80_0919h:** GPIO76-78; **BF80_091Ah:** GPIO82-83; **BF80_091Bh:** GPIO 90-92		

TABLE 13: PIO[95:64] OUTPUT STATE REGISTER

PIO96_OUT (BF80 0928h)			PIO[95:64] Output State Register
Bit	**Name**	**R/W**	**Description**
31	GPIO_95_OS	R/W	Set bit to drive GPIO95 high. Clear bit to drive GPIO95 low.
30	GPIO_94_OS	R/W	Set bit to drive GPIO94 high. Clear bit to drive GPIO94 low.
29	GPIO_93_OS	R/W	Set bit to drive GPIO93 high. Clear bit to drive GPIO93 low.
28	GPIO_92_OS	R/W	Set bit to drive GPIO92 high. Clear bit to drive GPIO92 low.
27	GPIO_91_OS	R/W	Set bit to drive GPIO91 high. Clear bit to drive GPIO91 low.
26	GPIO_90_OS	R/W	Set bit to drive GPIO90 high. Clear bit to drive GPIO90 low.
25:20	Reserved	R	Reserved
19	GPIO_83_OS	R/W	Set bit to drive GPIO83 high. Clear bit to drive GPIO83 low.
18	GPIO_82_OS	R/W	Set bit to drive GPIO82 high. Clear bit to drive GPIO82 low.
17:15	Reserved	R	Reserved
14	GPIO_78_OS	R/W	Set bit to drive GPIO78 high. Clear bit to drive GPIO78 low.
13	Reserved	R	Reserved
12	GPIO_76_OS	R/W	Set bit to drive GPIO76 high. Clear bit to drive GPIO76 low.
11:8	Reserved	R	Reserved
7	GPIO_71_OS	R/W	Set bit to drive GPIO71 high. Clear bit to drive GPIO71 low.
6	GPIO_70_OS	R/W	Set bit to drive GPIO70 high. Clear bit to drive GPIO70 low.
5	GPIO_69_OS	R/W	Set bit to drive GPIO69 high. Clear bit to drive GPIO69 low.
4	GPIO_68_OS	R/W	Set bit to drive GPIO68 high. Clear bit to drive GPIO68 low.
3	GPIO_67_OS	R/W	Set bit to drive GPIO67 high. Clear bit to drive GPIO67 low.
2	GPIO_66_OS	R/W	Set bit to drive GPIO66 high. Clear bit to drive GPIO66 low.
1:0	Reserved	R	Reserved
Note:	**BF80_0928h:** GPIO66-71; **BF80_0929h:** GPIO76-78; **BF80_092Ah:** GPIO82-83; **BF80_092Bh:** GPIO 90-92		

TABLE 14: PIO[95:64] INPUT STATE REGISTER

PIO96_IN (BF80 0938h)			PIO[95:64] Input State Register
Bit	**Name**	**R/W**	**Description**
31	GPIO_95_IS	R/W	Read bit to determine input state of GPIO95.
30	GPIO_94_IS	R/W	Read bit to determine input state of GPIO94.
29	GPIO_93_IS	R/W	Read bit to determine input state of GPIO93.
28	GPIO_92_IS	R/W	Read bit to determine input state of GPIO92.
27	GPIO_91_IS	R/W	Read bit to determine input state of GPIO91.
26	GPIO_90_IS	R/W	Read bit to determine input state of GPIO90.
25:20	Reserved	R	Reserved
19	GPIO_83_IS	R/W	Read bit to determine input state of GPIO83.
18	GPIO_82_IS	R/W	Read bit to determine input state of GPIO82.
17:15	Reserved	R	Reserved
14	GPIO_78_IS	R/W	Read bit to determine input state of GPIO78.
13	Reserved	R	Reserved
12	GPIO_76_IS	R/W	Read bit to determine input state of GPIO76.
11:8	Reserved	R	Reserved
7	GPIO_71_IS	R/W	Read bit to determine input state of GPIO71.
6	GPIO_70_IS	R/W	Read bit to determine input state of GPIO70.
5	GPIO_69_IS	R/W	Read bit to determine input state of GPIO69.
4	GPIO_68_IS	R/W	Read bit to determine input state of GPIO68.
3	GPIO_67_IS	R/W	Read bit to determine input state of GPIO67.
2	GPIO_66_IS	R/W	Read bit to determine input state of GPIO66.
1:0	Reserved	R	Reserved
Note:	**BF80_0938h:** GPIO66-71; **BF80_0939h:** GPIO76-78; **BF80_093Ah:** GPIO82-83; **BF80_093Bh:** GPIO 90-92		

TABLE 15: PIO[95:64] PULL-UP ENABLE REGISTER

PIO96_PUE (BF80 0948h)			PIO[95:64] Pull-Up Resistor Register
Bit	**Name**	**R/W**	**Description**
31	GPIO_95_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO95.
30	GPIO_94_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO94.
29	GPIO_93_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO93.
28	GPIO_92_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO92.
27	GPIO_91_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO91.
26	GPIO_90_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO90.
25:20	Reserved	R	Reserved
19	GPIO_83_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO83.
18	GPIO_82_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO82.
17:15	Reserved	R	Reserved
14	GPIO_78_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO78.
13	Reserved	R	Reserved
12	GPIO_76_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO76.
11:8	Reserved	R	Reserved
7	GPIO_71_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO71.
6	GPIO_70_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO70.
5	GPIO_69_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO69.
4	GPIO_68_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO68.
3	GPIO_67_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO67.
2	GPIO_66_PUE	R/W	Set bit to enable ~62k pull-up resistor on GPIO66.
1:0	Reserved	R	Reserved
Note:	**BF80_0948h:** GPIO66-71; **BF80_0949h:** GPIO76-78; **BF80_094Ah:** GPIO82-83; **BF80_094Bh:** GPIO 90-92		

TABLE 16: PIO[95:64] PULLDOWN ENABLE REGISTER

PIO96_PDE (BF80 0958h)			PIO[95:64] Pull-Down Resistor Register
BIT	**Name**	**R/W**	**Description**
31	GPIO_95_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO95.
30	GPIO_94_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO94.
29	GPIO_93_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO93.
28	GPIO_92_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO92.
27	GPIO_91_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO91.
26	GPIO_90_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO90.
25:20	Reserved	R	Reserved
19	GPIO_83_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO83.
18	GPIO_82_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO82.
17:15	Reserved	R	Reserved
14	GPIO_78_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO78.
13	Reserved	R	Reserved
12	GPIO_76_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO76.
11:8	Reserved	R	Reserved
7	GPIO_71_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO71.
6	GPIO_70_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO70.
5	GPIO_69_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO69.
4	GPIO_68_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO68.
3	GPIO_67_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO67.
2	GPIO_66_PDE	R/W	Set bit to enable ~62k pull-down resistor on GPIO66.
1:0	Reserved	R	Reserved
Note:	**BF80_0958h:** GPIO66-71; **BF80_0959h:** GPIO76-78; **BF80_095Ah:** GPIO82-83; **BF80_095Bh:** GPIO 90-92		

EXAMPLES

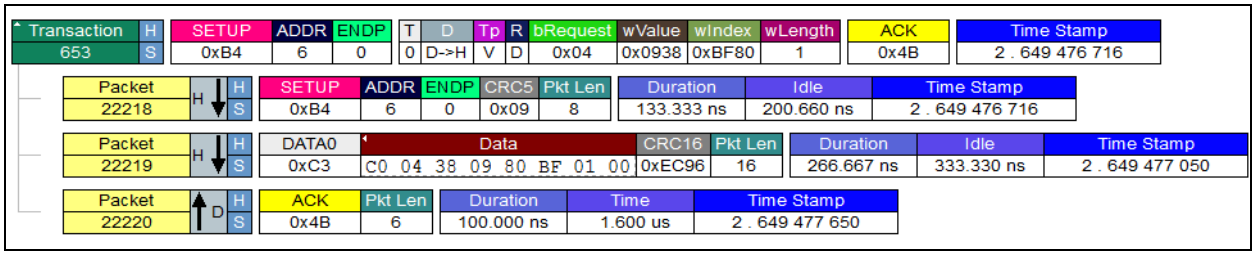
Read the Input State of PF7/GPIO71

1. **Command Phase (SETUP Transaction):** Send the following SETUP Register Read Command to Endpoint 0 of the Hub Feature Controller to read the contents of registers 0xBF80_0938 (PIO[95:64] Input State Register) which contains the input state information for PF7/GPIO71 (assuming that the GPIO was already configured as an input in a previous command). See Table 17 and Figure 4.

TABLE 17: REGISTER READ SETUP COMMAND EXAMPLE

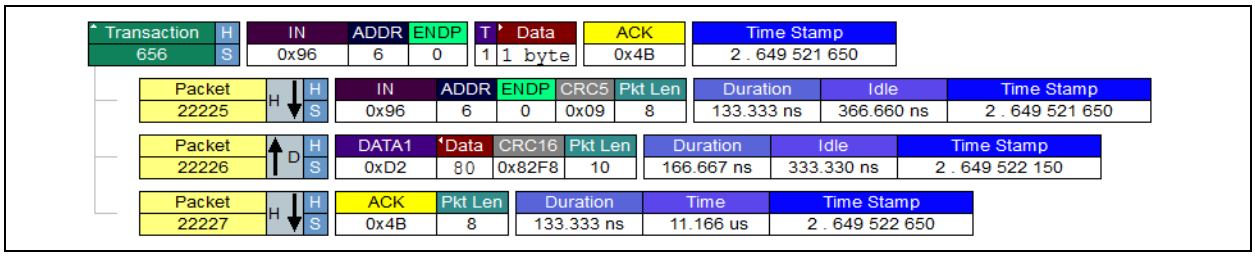
SETUP Parameter	Value	Note
bmRequestType	0xC0	—
bRequest	0x04	—
wValue	0x0938	Last four bytes of the register address
wIndex	0xBF80	First four bytes of the register address
wLength	0x0001	One register to be read

FIGURE 4: REGISTER READ SETUP TRANSACTION EXAMPLE



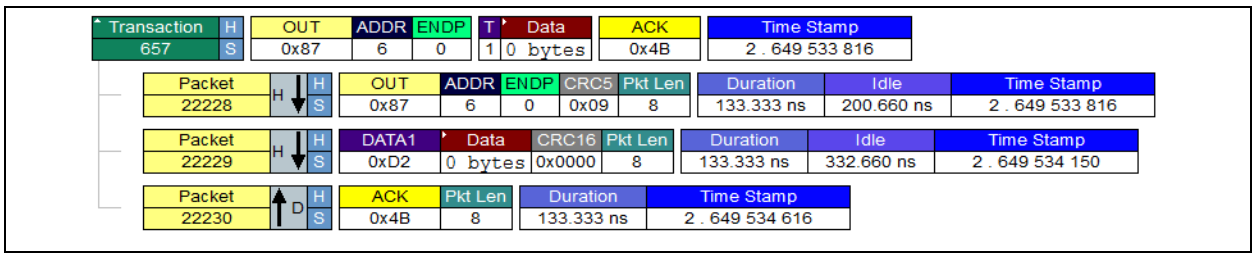
2. **Data Phase (IN Transaction):** The Hub Feature Controller sends the data bytes of length wLength starting from the specified address after receiving an IN packet. The returned value is 0x80, which indicates that PF7/GPIO71 is high. See Figure 5.

FIGURE 5: REGISTER READ IN TRANSACTION EXAMPLE



3. **Status Phase (OUT Transaction):** The Host sends an OUT packet to complete the USB Transfer. The Hub Feature Controller responds with a zero-length data packet. Refer to Figure 6.

FIGURE 6: REGISTER READ OUT TRANSACTION EXAMPLE



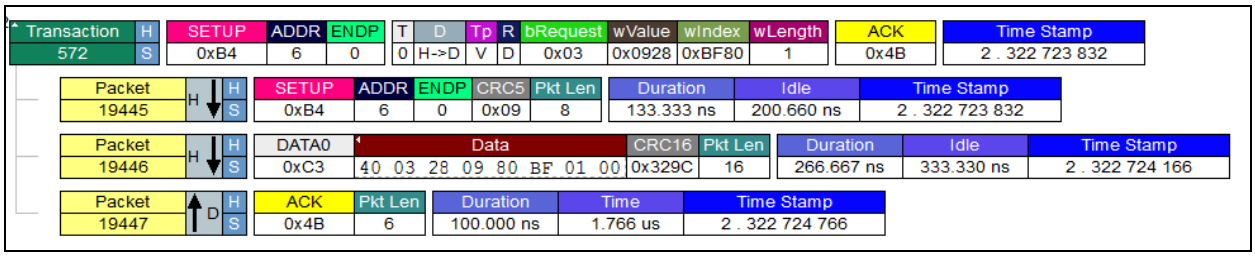
Write Registers to Set PF7/GPIO71 Output State as High

1. **Command Phase (SETUP Transaction):** Send the following SETUP Register Write Command to Endpoint 0 of the Hub Feature Controller to write the contents of register 0xBF80_0928 (PIO[95:64] Output State Register). In this example, PF7/GPIO71 is set high (assuming that the GPIO was already configured as an output in a previous command). See Table 18 and Figure 7.

TABLE 18: REGISTER WRITE SETUP COMMAND EXAMPLE

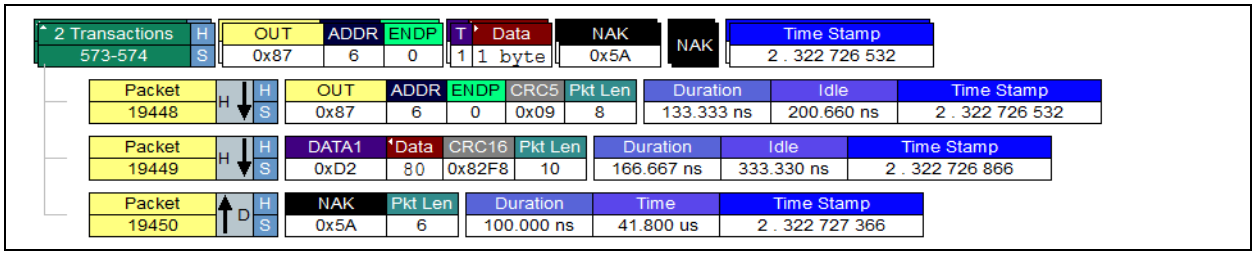
SETUP Parameter	Value	Note
bmRequestType	0x40	—
bRequest	0x03	—
wValue	0x0928	Last 4 bytes of the register address
wIndex	0xBF80	First 4 bytes of the register address
wLength	0x0001	One register is to be read

FIGURE 7: REGISTER WRITE SETUP TRANSACTION EXAMPLE



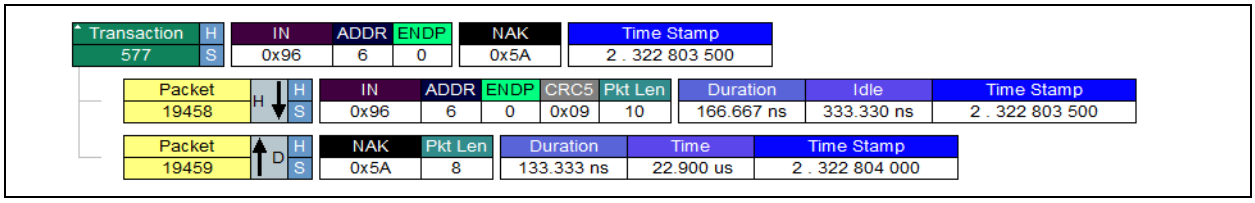
2. **Data Phase (OUT Transaction):** The Host sends the data byte to set 0xBF80_0928 = 0x80 from the specified address after sending the OUT packet to set the PF7/GPIO71 output as high. Refer to Figure 8.

FIGURE 8: REGISTER WRITE OUT TRANSACTION EXAMPLE



3. **Status Phase (OUT Transaction):** The Host sends an IN packet to complete the USB Transfer. The Hub Feature Controller responds with a zero-length data packet. See Figure 9.

FIGURE 9: REGISTER WRITE IN TRANSACTION EXAMPLE



NOTES:

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level and Date	Section/Figure/Entry	Correction
DS00002750A (07-13-18)	All	Initial release

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