

Application Note:

Designing for High Efficiency

and Low-Harmonic Emissions

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1 Introduction

To reduce the cost of wireless Internet of Things (IoT) connectivity the Bill of Materials (BoM) of a product must be continuously re-evaluated for potential savings. This is increasingly the case for external RF shielding which also adds undesirable size and weight to miniaturized designs.

Screening is typically employed to improve device sensitivity and reduce spurious emissions (for examples see [\[1, 2\]](#)). However, there are many cost sensitive applications where the unscreened device performance is sufficient provided that radiated spurious emissions limits can be met.

For reasons that will be described here, a screen-less design cannot systematically be guaranteed. However, in this Note, we present both the PCB design and PA optimization methodologies used to reduce likelihood that board level screening will be required. It is presented here in the form of a screen-less reference design for SX1272 in typical European LoRaWAN configuration [\[5\]](#).

2 Harmonic Radiation

2.1 The Source of Harmonic Radiation

A real amplifier can only deliver a finite amount of power, so at some input power, the output power ceases to be a linear function of the input. Every actively amplified signal therefore contains distortions due to this nonlinearity.

We define this as shown below:

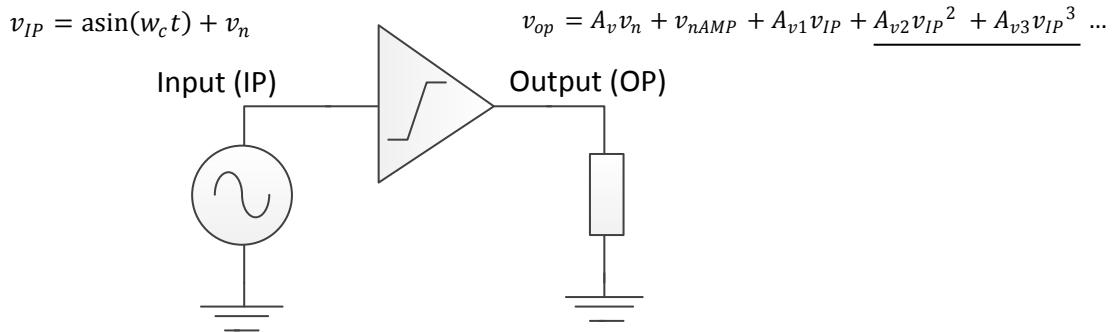


Figure 1: Input and Output Power Functions

The input voltage v_{IP} applied to the amplifier also includes a noise voltage v_n , the signal is amplified by the voltage gain of the amplifier A , which also adds some noise v_{nAMP} in the process of amplification.

In addition to the various noise terms, the underlined power terms indicate that distortions of the injected signal manifest themselves as additional components at integer multiples of the input (fundamental) frequency, termed harmonics.

It is well understood that all transmitters produce harmonics and, as such, they are subject to regulatory control (see [3] and [4] for Europe and the USA respectively). Consequently, a harmonic filter is mandated in a practical design to remove harmonics before they reach the antenna. The figure below shows a simplification of this process. The limited linearity of the amplifier introduces distortion, which is then removed by the harmonic filter.

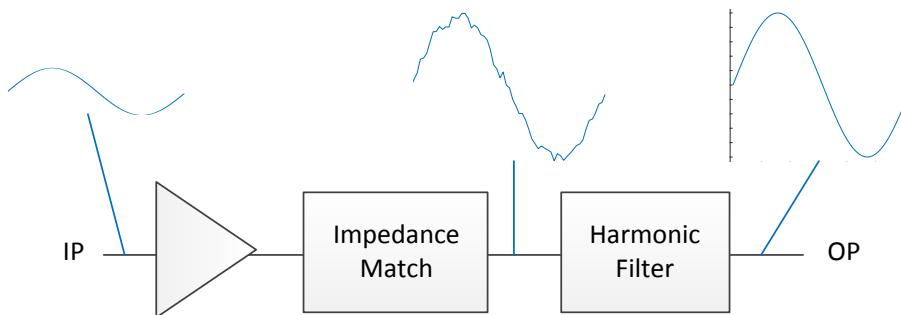


Figure 2: Removal of Harmonic Distortion in a Tx Chain by Filtering

In reality the most efficient amplifiers are switching amplifiers. In which case the impedance match is also responsible for recovery of a more sinusoidal output with an even greater filtering burden placed on the harmonic filtering. Due to the high frequencies of harmonics (in the GHz range for a PA operating in the 868 MHz or 915 MHz bands), even with such filtering, radiation may occur from PCB metallization either connected, or closely coupled, to the PA output.

So although the source of these harmonics is the amplifier, harmonic radiation originates from unintentional antennas formed by metallic board and enclosure elements.

Table 1: Harmonic Frequencies and Dimensions of a Half-Wavelength of PCB Trace on FR4 Substrate [6]

Harmonic	Frequency	L/2
H2	1.73 GHz	47 mm
H3	2.60 GHz	31 mm
H4	3.47 GHz	23 mm
H5	4.34 GHz	19 mm
H6	5.21 GHz	15 mm

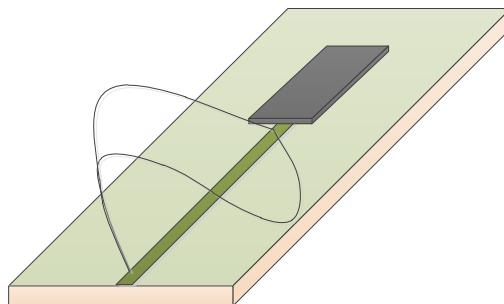


Figure 3: Hypothetical Unintentional Radiation from a PCB Trace Half-wave & Full-wave Resonances

The figure above shows an idealized picture of this scenario, but is instructive in highlighting just how short a length of PCB can become resonant at harmonic frequencies.

In reality, the picture is more complicated than this, as even non-resonant lengths of PCB can radiate harmonics. The figure below shows a more realistic view. Here the radio couples a range of harmonic emissions into the surrounding PCB (left hand plot). The PCB has some propensity to act as an unintentional antenna as a function of frequency, i.e. it acts as an antenna with a certain efficiency (center plot). The resulting radiation seen is the combination of these two effects (rightmost plot).

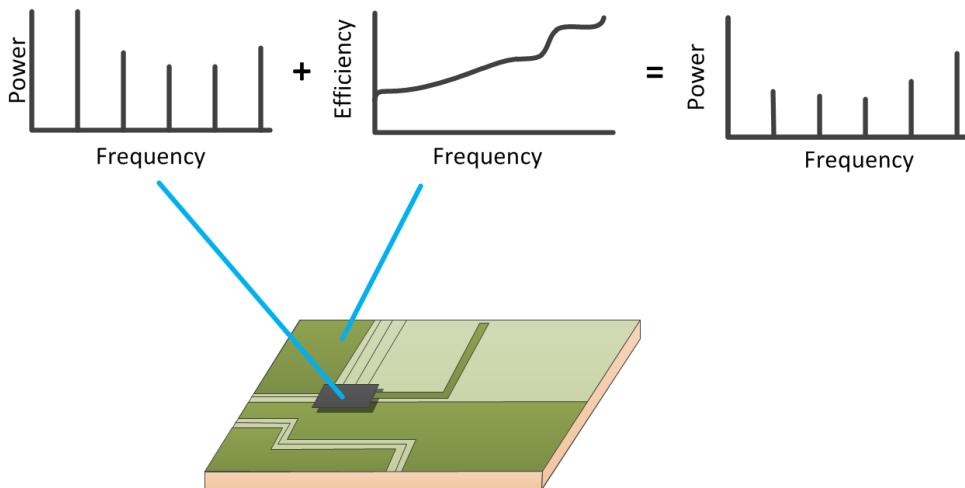


Figure 4: A More Realistic View of Unintentional Radiation from a Radio PCB

With this understanding it is clear that to attenuate the radiated spurious (harmonic) radiation, our design must seek to minimize one, or both, mechanisms - chiefly:

- Reduce the harmonic powers generated by the PA
- Avoid the creation of unintentional antennas to radiate those harmonics

2.2 Best Design Practices to Avoid Harmonic Radiation

Board level screening, or a screening can, is the best method by which to prevent radiation from the PBC, however there are some caveats to this advice.

- **Slots:** Care must be taken to ensure that slots are not formed at the interface between the PCB and the screen. Slots can be very effective radiators.
- **IO Traces:** Any trace (even a digital or supply trace) that leaves area covered by the shield can still potentially then go on to radiate spurious emissions that have coupled to it within the shield. One of the best techniques to avoid this is the resistive isolation of such PCB traces.

Resistive isolation, particularly of digital lines, is consistent with general RF design best practices.

Although ordinarily employed to reduce noise coupling from the digital to the RF portion of a design, separation of RF and digital portions of the design can also be used to help provide more predictable board performance at RF and, with resistive isolation of digital lines, reduce the likelihood of spurious radiation from digital traces.

The principle is shown in the image below, analogue (RF) and digital grounds are joined by a 'bridge' of ground. Any signals traversing domains are made over this bridge. In the case of digital signals (such as SPI) typically by a value of $1\text{ k}\Omega$ is used to provide effective RF filtering. Supply planes are connected in a similar fashion but with a suitable ferrite or inductance.

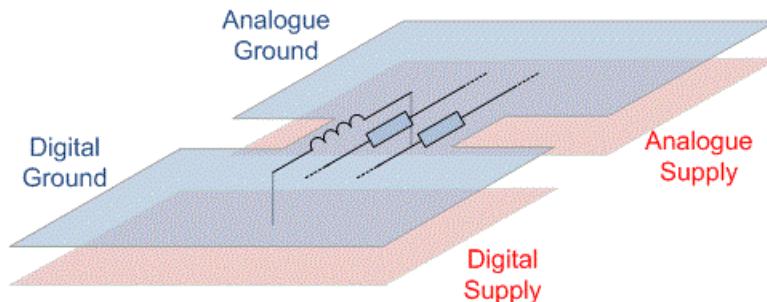


Figure 5: Separation of Analogue (RF) and Digital Ground

The figure above shows that separation of analogue (RF) and digital ground can help reduce unpredictable PCB effects at RF.

For more information on design RF design practices, please see our application note [\[7\]](#). For more information on noise coupling and mitigation see the definitive reference on the subject [\[8\]](#).

For the remainder of this document we focus on ways of reducing harmonic radiation from a design where neither a screen cannot be accommodated nor can best design practices be adhered to due to application size or cost constraints. Given the unpredictability of PCB-based radiation mechanisms, we begin by looking at the harmonic power output of the radio.

3 SX1232/SX1272 High Efficiency Power Amplifier

3.1 RFO Amplifier Connection

Here we consider the example of the SX1272 (also equivalent to SX1232). The SX1272 features a linear, high-efficiency PA on the RFO pin that can be used for applications demanding RF output power up to +14 dBm with lower current consumption than the +20 dBm PA_BOOST output.

The following Figure shows the connectivity of the SX1272 when using the high efficiency switching amplifier. Internally the RFO amplifier features 3 separate stages of parallel amplification (labeled 1, 2 and 3 below) of increasing geometry to supply increasing output power.

As an aside, note that the receiver (RFI) path can be routed through a shared impedance match with the RFI pin or independently, see [9] for more details.

The amplifiers are biased through an external inductance by a shared regulated bias (VR_PA) voltage programmed by a DAC. As shown below, the regulation feedback path switches between PA_BOOST and RFO amplifier depending upon the amplifier selected. The voltage reference for the regulator also switches (not shown) between a fixed voltage reference in PA_BOOST mode and one derived from VBAT in RFO mode.

The amplifier duty cycle (conduction angle) can also be varied programmatically.

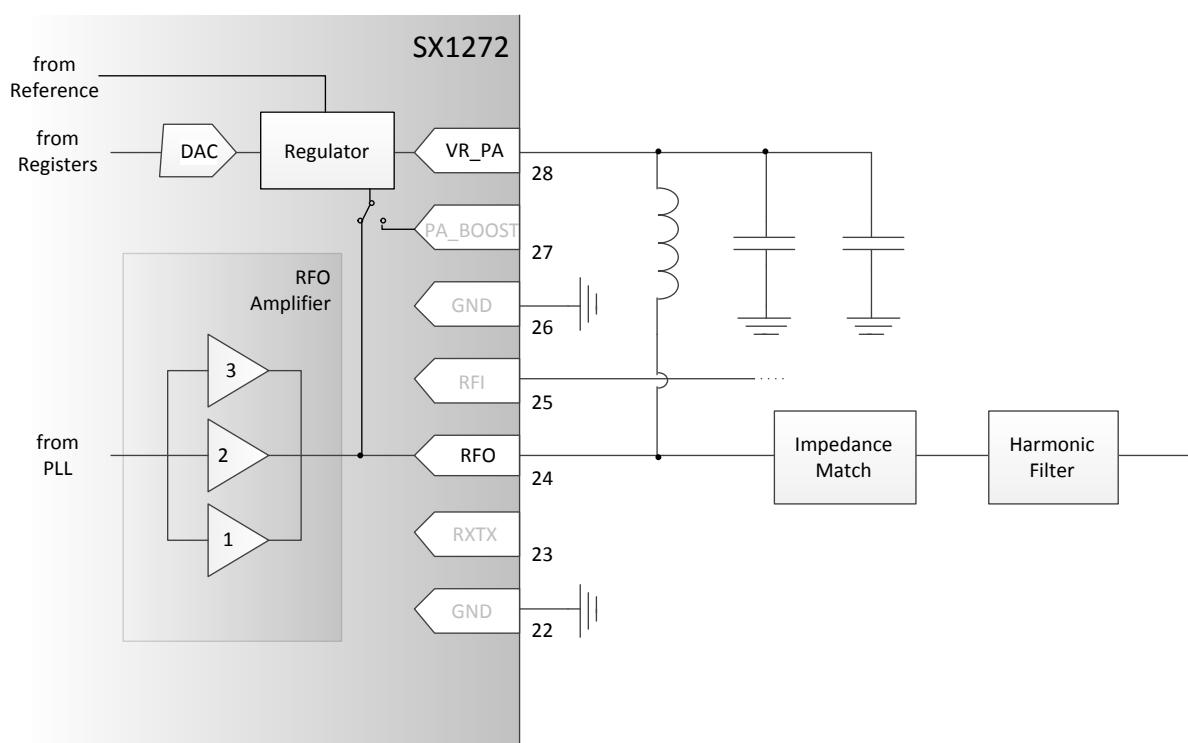


Figure 6: Connection of the RFO High Efficiency Amplifier

In normal (automatic) operation, the amplifier output is set to a specific output power corresponding to the programmed power level. Each programmed power level in fact generates a fixed combination of:

- Number of amplifiers used
- PA duty cycle
- DC bias

These default settings are adequate for the majority of applications, however, where we require fine control over the PA output to precisely control the contribution of each harmonic tone and find intermediate PA configurations with advantageous performance, we can manipulate their settings directly.

3.2 RFO Amplifier Control

Three programmable settings are at our disposal to configure the power amplifier.

3.2.1 VR_PA DAC Bias

The DAC word programmed is directly proportional to the bias voltage applied to the power amplifier. Extreme care must be taken not to exceed the maximum bias voltage word of 0xE7. Values within the range 0x00 to 0xE7 are hence valid and have a nonlinear relationship to the RF output power.

3.2.2 PA Duty Cycle

The principle of PA duty cycle is shown below. It indicates the fraction of a period at the RF frequency for which the PA is in the ON state. This influences not only the power output and efficiency of the power amplifier, but also the magnitude of the harmonic components present at the output so has a critical role in reducing the harmonics generated by the SX1272.

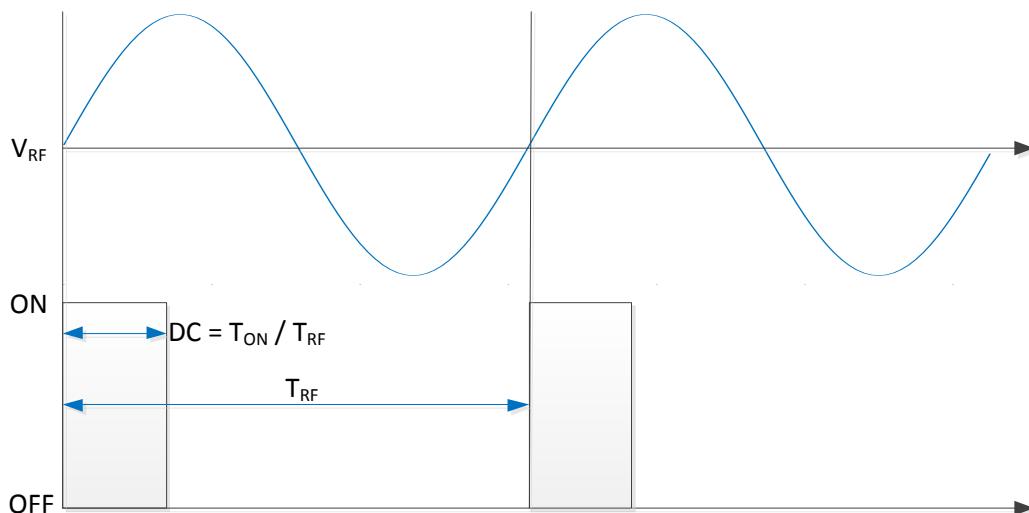


Figure 7: Definition of PA Duty Cycle

The duty cycle (expressed as a percentage) is programmable in the LSB of register 0x4B. The value 0xF corresponds to a duty cycle of 20%. Each subsequent integer step represents a 4% increase in PA duty cycle. The maximum useable value is 0x9 which corresponds to a programmed duty cycle of 44%.

3.2.3 Number of Amplifier Stages

The value programmed to the LSB of register 0x4C corresponds to the number of amplifiers enabled.

3.2.4 Register Summary

To enable manual control of the power amplifier, it is necessary to modify the contents of four configuration registers shown below:

Table 2: SX1272 Manual PA Configuration Registers

Register	Bits	Manual PA	Min	Max	Description
0x63	7-5	0x0			Reserved
	4	0x1			Enable manual PA control (active high)
	3-0	0x0			Reserved
0x4B	7-4	0x7			Manual PA supply configuration
	3-0		0xF	0x9	PA Duty cycle control
0x4C	7-0		0x00	0xE7	Manual PA DAC bias
0x4D	7-2	0x00			Reserved
	1-0		0x1	0x3	Number of amplifier stages enabled, range 1 to 3

CAUTION!

Settings programmed beyond the minimum and maximum values stated above can result in permanent damage to the amplifier and affect device reliability.

4 Minimising Unintentional Radiation

As was illustrated in Figure 6, due to the pin arrangement of the SX1272, it is necessary to traverse the LNA input line, RFI, of the receiver with the RFO amplifier bias from VR_PA. Understanding that the PA output is a source of harmonic energy the layout of this portion of the RF layout is critical in minimizing radiated harmonic emissions.

Here we use a combination of 4-layer design and short trace lengths to minimize harmonic radiation. The following figure shows the full board layout and the inset image, detail of the RFO connection.

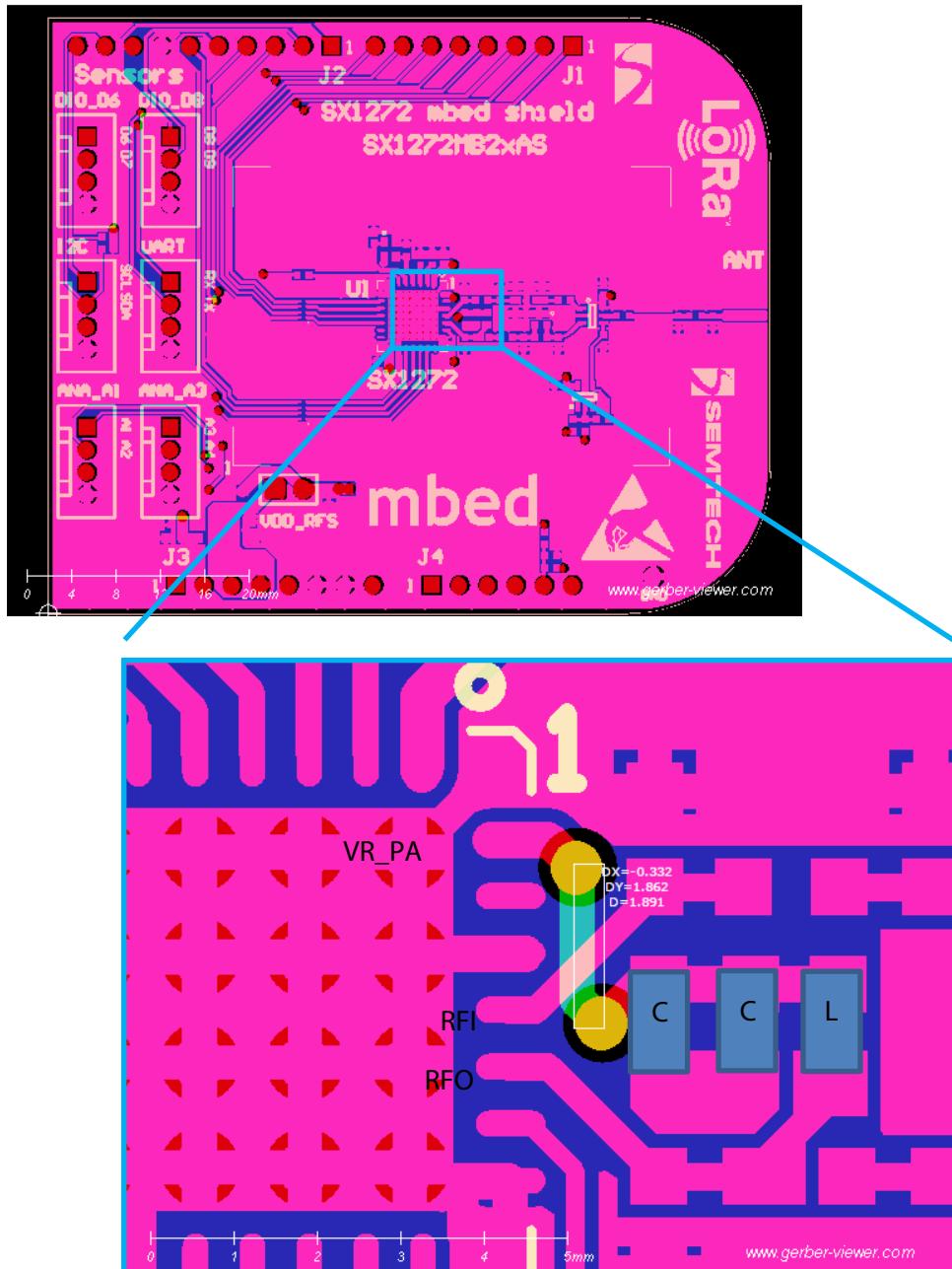


Figure 8: The Reference Design Layout

Here we see the top 3 layers of the 4 layer design. The top layer (red) has a full ground plane (blue) on the next layer (pink where top and bottom layers overlap). The third layer (green) is the layer upon which the VR_PA signal is routed. A final bottom ground layer (layer 4) is also included but not shown here for clarity.

The two decoupling capacitors and series inductance used to attenuate the fundamental and any harmonics are located as close as possible to the RFO trace. The bias line is less than 2 mm in length and is sandwiched between the two ground layers (2 and 4).

Such layout considerations should be taken into account to help reduce the probability of having radiated emission problems in the final design.

5 Minimizing Harmonics within the Power Amplifier

Given the SX1272 amplifier switches with a programmable duty cycle, the harmonics generated by the SX1272 can be controlled by varying the duty cycle. For a perfect rectangle wave pulse, a duty cycle of 50% suppresses even order harmonics whilst lower duty cycles will suppress the $1 / \text{duty cycle}^{\text{th}}$ harmonic. For a good explanation of this see [\[10\]](#). Note the reduction in the fundamental power as the duty cycle is reduced.

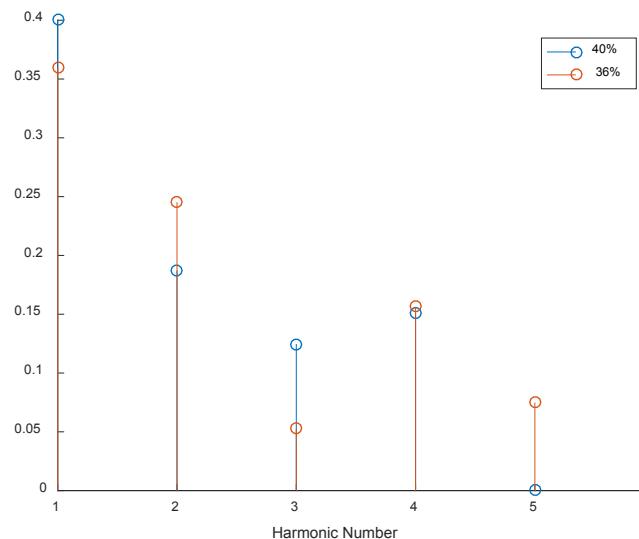


Figure 9: Harmonic Level Changes Between 40% and 36% Duty Cycle for a Rectangle Wave

Given the output waveform is a switched sinusoid with additional distortion the same harmonic relationship as for a rectangle wave does not hold, but can be used as the basis for empirical design improvement. To be certain that a reduction in the conducted harmonic output of the SX1272 results in a radiated improvement, we must perform a radiated measurement.

6 Practical Implementation

Whilst the preceding information can be used during the design phase to reduce the likelihood of harmonic radiation, in a practical product design there is often little time or scope to change PCB board size and packaging. A harmonic compliance issue may also only be found late in the design process during the regulatory test phase. For this reason a bench-top method is shown below that can be used to measure relative harmonic levels, so permitting optimization of a design prior to anechoic chamber measurement.

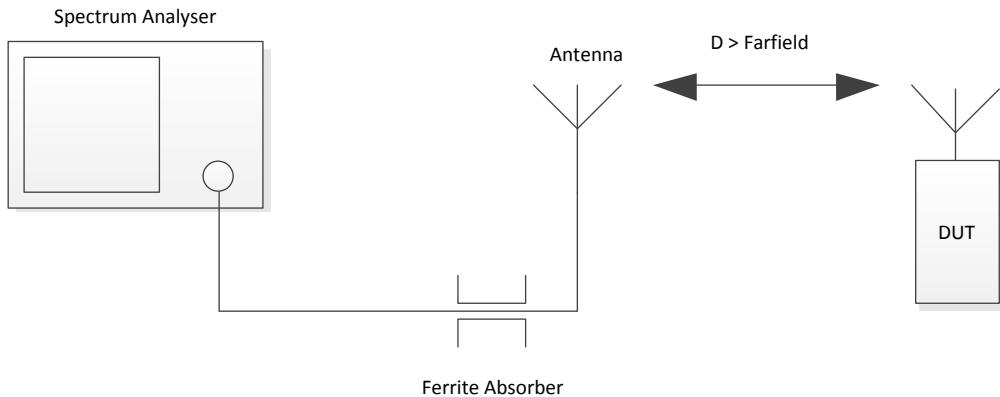


Figure 10: Block Diagram of the Bench-top Setup for Optimization of the PA Settings

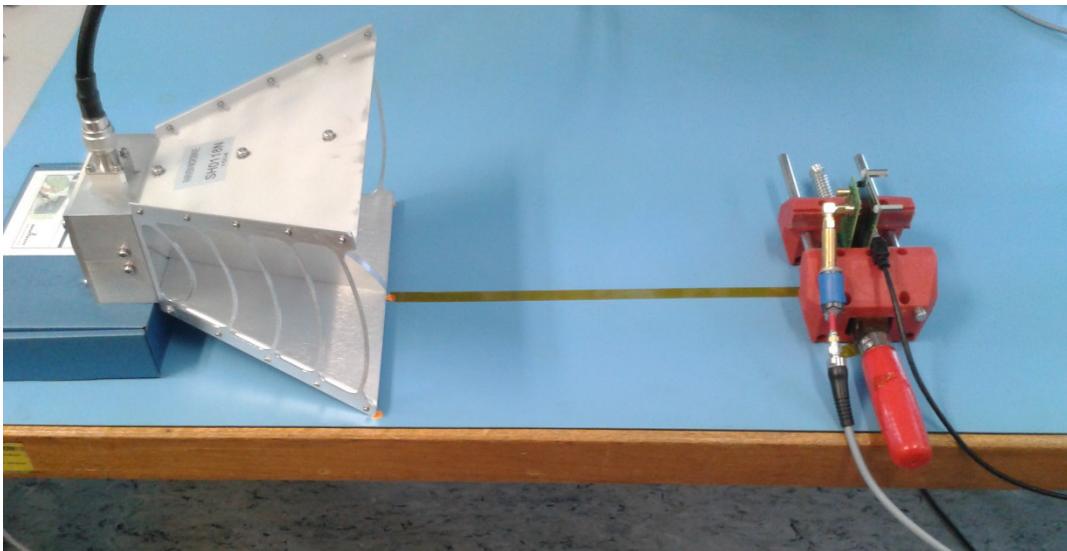


Figure 11: Photograph of Bench-top Setup used for Optimization of the PA Settings

This setup features an antenna that will receive all harmonic frequencies, which are measured by spectrum analyzer. All wire connections to the antenna and device under test (DUT) should be isolated by ferrite absorber cores to prevent the connecting wires contributing to the radiated field measurements.

This setup was used to produce the following optimized settings for our screen-less SX1272 reference design (note that all four registers must be modified for the manual settings control to be effective).

Table 3: Register Settings Used in the Optimized Design

Register	Content	Description
0x63	0x10	Enable manual PA configuration
0x4B	0x7B	Manual PA configuration supply and duty cycle
0x4C	0xE7	Manual PA DAC bias
0x4D	0x03	Manual setting number of amplifier stages enabled

7 Anechoic Chamber Measurement

The images below show the setup of the SX1272 in the anechoic chamber in accordance with the EN 300 220 measurement procedure.

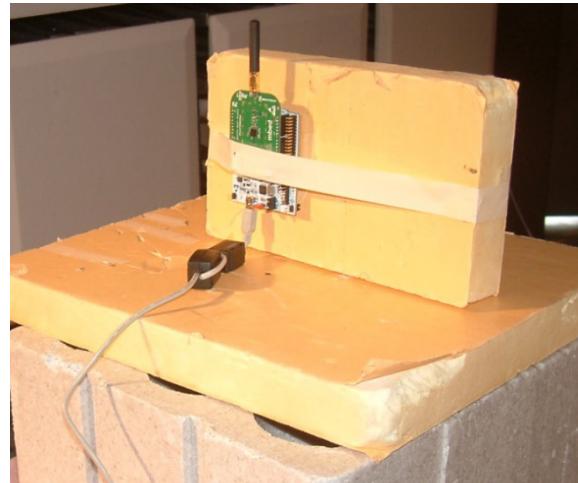
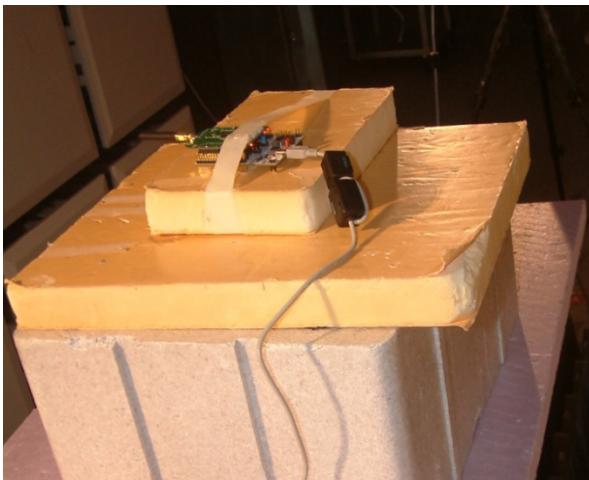


Figure 12: Clockwise from Top Left: DUT Horizontal Orientation, Vertical Orientation, Receiver Antenna at 3 m Distance in the Chamber and DUT Edge Orientation

These settings minimized the harmonic output power, without any board level shielding employed whilst maintaining over 13 dBm of RF output power. These settings were then used in a full radiated power and harmonic measurement process.

The recorded results for each orientation of the PCB are shown in the following table. Here we see that the design passes the regulatory limit of -30 dBm with a margin of 2.2 dB.

Table 4: Measured Radiated Harmonic Results

DUT (SX1272) Position	Rx Antenna Polarization	Conducted	Radiated				
		Carrier level (dBm)	H2 (dBm)	H3 (dBm)	H4 (dBm)	H5 (dBm)	H6 (dBm)
Vertical	Horizontal	13.4	-49.1	-43.2	-34.6	-39.7	-37.2
Vertical	Vertical	13.4	-48.4	-41.0	-32.4	-38.5	-37.2
Horizontal	Horizontal	13.4	-51.0	-43.9	-37.3	-44.7	-42.4
Horizontal	Vertical	13.4	50.7	-44.9	-34.8	-43.6	-40.7
Edge	Horizontal	13.4	-47.0	-39.8	-32.2	-37.3	-35.9
Edge	Vertical	13.4	-50.1	-46.1	-35.1	-42.0	-37.4

8 Conclusion

A fully compliant SX1272 reference design has been presented. However, because the harmonic emissions of the SX1272 are a function of both PA configuration and unintentional radiation that is dependent upon the PCB on which the device is mounted - the instructions for full control of the RFO high efficiency amplifier, together with a design methodology have also been presented to allow optimization of an individual design.

9 References

[1] Screening to improve sensitivity example at:

http://www.keysight.com/upload/cmc_upload/All/MWJ_Webcast_RIM-Agilent_10-06-2011.pdf?&cc=CH&lc=ger

[2] Screening to reduce spurious emissions example at:

http://www.digikey.ch/Web%20Export/Supplier%20Content/Laird_776/PDF/Laird_EMI_Shielding_Design_Calculation.pdf

[3] ETSI Regulations:

http://www.etsi.org/deliver/etsi_en/300200_300299/30022001/02.04.01_40/en_30022001v020401o.pdf

[4] FCC Regulations:

http://www.ecfr.gov/cgi-bin/text-idx?tpl=/ecfrbrowse/Title47/47cfr15_main_02.tpl

[5] The LoRaWAN Channel Plan:

<https://www.lora-alliance.org/portals/0/specs/LoRaWAN%20Specification%201R0.pdf>

[6] Microstripline calculations from:

I. J. Bahl and D. K. Trivedi, "A Designer's Guide to Microstrip Line", Microwaves, May 1977

[7] Semtech RF Design Guide:

http://www.semtech.com/images/datasheet/rf_design_guidelines_semtech.pdf

[8] Henry Walter Ott, "Noise Reduction Techniques in Electronic Systems", 2nd Edition, John Wiley & Sons, Inc. 1988

[9] SX1272 Reference available at the time of writing from:

<http://www.semtech.com/wireless-rf/rf-transceivers/sx1272/>

[10] <http://www.dspguide.com/ch13/4.htm>



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Contact Information

Semtech Corporation
Wireless & Sensing Products
200 Flynn Road, Camarillo, CA 93012
E-mail: sales@semtech.com
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com