PCB Layout Guidelines for QFN Package

Abstract

This Application Note provides PCB designers with a set of guidelines for successful board mounting of Active-Semi's widely used QFN. It includes example PCB land patterns, thermal via designs, stencils, and solder mask openings.

Introduction

The QFN package is a leadless package which makes electrical contact to the PCB by soldering the bottom surface of the package to the PCB (Figure 1 and Figure 2). The QFN package's Exposed Pad enhances the thermal and electrical properties of the package. The die pad attaches to the Exposed Pad on the bottom of the package, providing excellent thermal conduction between die and exterior of the package. Proper footprint and thermal design is critical for reliable mechanical connection of the package to the PCB and for taking full advantage of the QFN thermal properties.

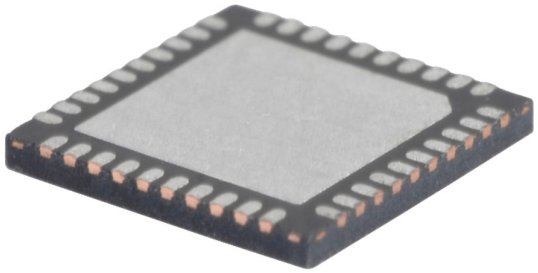


Figure 1. Bottom view of a QFN55-40 package

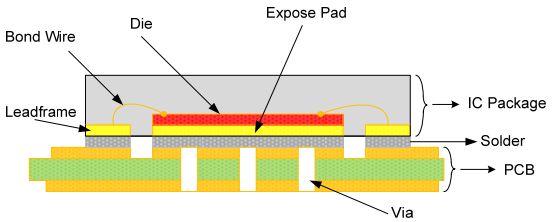


Figure 2. Section view of QFN55-40 package soldered onto a PCB

PACKAGE DIMENSION

For robust board assembly and board level reliability, the PCB layout and stencil designs are critical to ensure sufficient solder coverage between package and PCB. When designing the PCB layout, please refer to the Active-Semi's package Outline and Dimension drawing in the datasheet to obtain the package dimensions and tolerances. **Figure 3** shows an example of a QFN55-40, 0.4mm pitch package outline drawing. The D, E, b, e, L, D2, E2 dimensions are critical to design and layout the PCB.

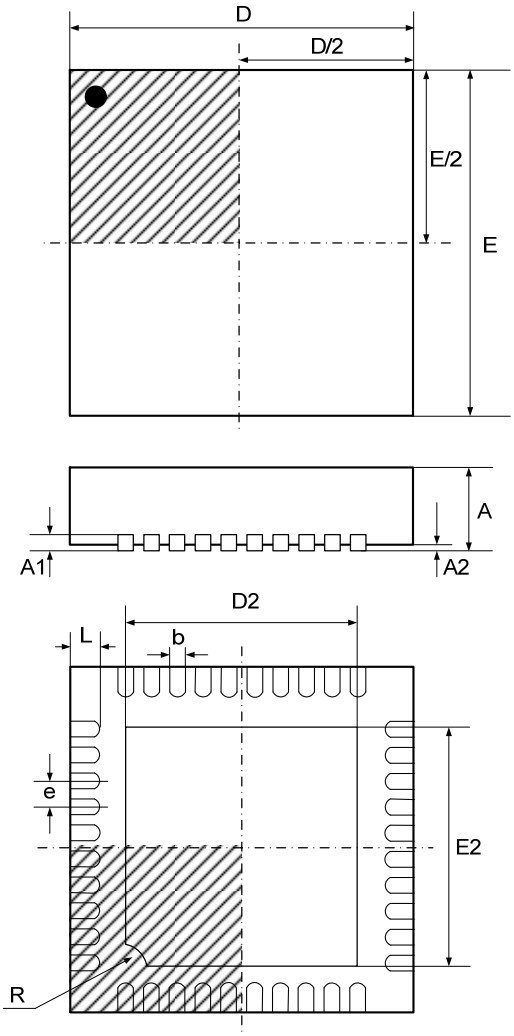


Figure 3. QFN55-40 Package Outline Drawing

PCB LAYOUT GUIDELINES

Figure 4 below demonstrates how to design the PCB landing pattern for a 5 x 5 mm - 40-pin, 0.4mm -pitch package. The PCB designer needs to design the Pads and Thermal Pad according to the Package Outlines and Dimensions provided in the Active-Semi datasheet. Below are recommended basic calculation for each dimension:

$ZD_{min} = D_{max} + 2(0.25)$

$ZE_{min} = E_{max} + 2(0.25)$

$GD_{min} = D_{min} - 2L_{max} - 0.1$

$GE_{min} = E_{min} - 2L_{max} - 0.1$

$PD_{max} = GD_{min} - 2C_{PL}$ where $C_{PL} = 0.15$

$PE_{max} = GE_{min} - 2C_{PL}$ where $C_{PL} = 0.15$

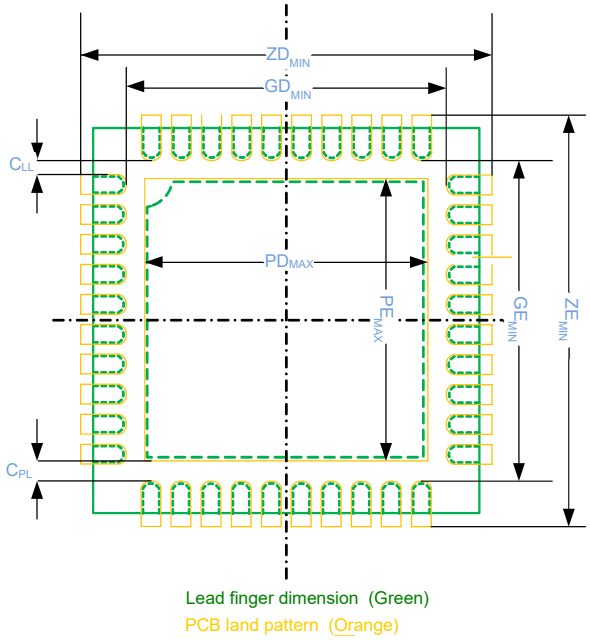


Figure 4. PCB land pattern of a QFN40L Package

PCB Lead Figure Land Pattern Design

In general, the **PCB** lead finger pad should be designed slightly wider and longer than the IC Exposed Leads.

The Pad length (Y) should be designed at least 0.3mm longer than the package terminal length (L) for good filleting. The pad length should be extended 0.05mm towards the center line of the package.

The Pad width (X) should be a minimum 0.05mm wider (0.025mm each side) than the package terminal width (b) as shown in **Figure 5** below.

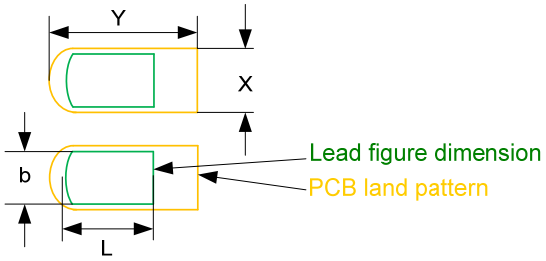


Figure 5. Lead Pads

Notice: PCB designer must keep enough clearance between Lead Pads (C_{LL}) and from Lead Pads to Thermal Pad (C_{PL}) to be minimum 0.15mm to prevent solder bridging.

PCB Thermal Pad Land Pattern Design

The PCB's Thermal Pad is the exposed copper area which is not covered by the solder mask. This Thermal Pad must be soldered directly to the Exposed Pad on the bottom of the IC. This thermal Pad should be made as large as possible to improve the thermal and electrical characteristics.

Thermal Pad Via Design

Active-Semi highly recommends using multiple vias inside the thermal pad area to conduct heat from the top layer to the inner or bottom layers. Correct layout of these vias greatly improves the thermal characteristics of the IC as well as electrical performance. Figure 6 shows example via placement. The following are dimensional rules for thermal pad area vias:

Pitch: 1mm to 1.2mm pitch

Diameter: 0.3mm to 0.33mm

The number of vias included in a PCB layout is application-specific and depends upon the package power dissipation and electrical conductivity requirements. Thermal and electrical analysis and/or testing are recommended to determine the minimum number of vias required. Figure 7 shows Active-Semi's recommendations for solid vias which directly connect to copper. Active-Semi does not recommend thermal relief vias.

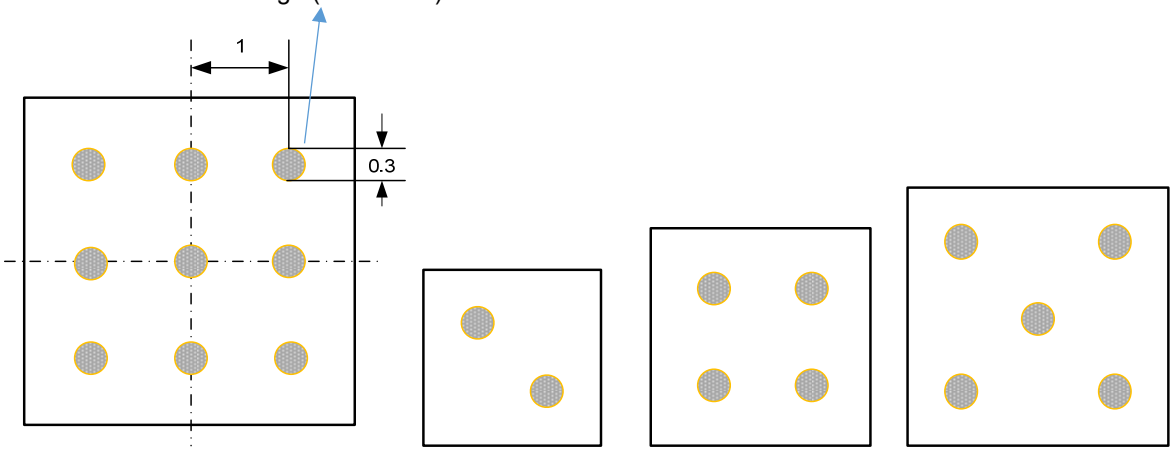
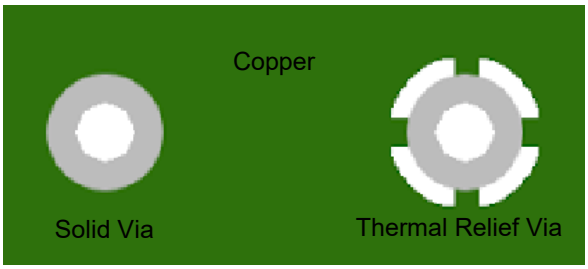


Figure 6. Thermal Via Placement



(Recommended) (Not Recommended)

Figure 7. Solid vs Thermal Relief Via

Solder Mask Openings

Pads can be either Non-solder mask defined (NSMD) or solder mask defined (SMD). A NSMD pad is defined by having a metal pad on the PCB that is smaller than the solder mask opening. A SMD pad is defined where the copper is larger than the solder mask opening. In this case, the solder mask opening is smaller than the copper and defines the size of the pad.

Active-Semi recommends Non Solder Mask Defined (NSMD) pads when possible. NSMD pads provide better solder joint reliability. Solder mask should surround each pad, with masking pattern 60 - 70µm larger than the pad size. The solder mask can be designed around each individual lead pad for lead pitches greater than 0.65mm. However, most of the Active-Semi QFN package products use lead-to-lead pitch equal to 0.5mm or smaller. For these packages it is recommended to design the solder mask around all pads on each side. In order to maximize the solder mask between adjacent sides, it is necessary to round the inner corner on each row. This will ensure sufficient solder mask in the corner of the PCB footprint design as shown in the **Figure 8** below.

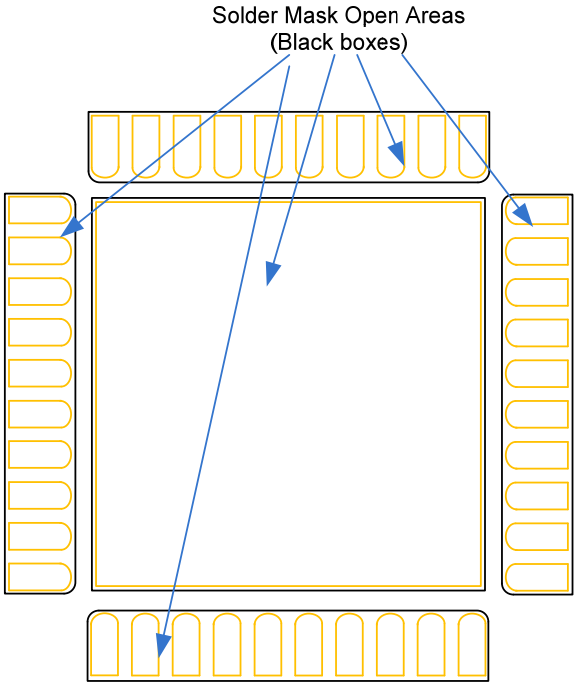


Figure 8. PCB Pads and Solder Mask Opening Design

SOLDER PASTE AND STENCIL

Solder Paste Type

Active-Semi highly recommends customer to use type3 or type 4 solder paste in mounting QFNs to archive high assembly yield. Follow JEDEC/IPC J-STD-20D.1 for standard reflow procedure recommendations.

Solder Stencil for Lead Pads

The stencil aperture opening should be designed to maximum paste release. This is typically accomplished by considering the following two ratios:

- AREA RATIO = Area of Aperture opening / Aperture Wall Area
- ASPECT RATIO = Aperture Width / Stencil Thickness

Area Ratio should be greater than 0.66.

Aspect Ratio should be greater than 1.5.

Solder Stencil for Thermal Pads

For large Thermal Pad area with the size larger than 25mm^2, Active-Semi recommends using cross-hatching in the thermal pads stencil opening of a QFN package (as shown in **Figure 9**). Cross-hatching will prevent excessive amount of applied solder paste, thus reducing the risk of solder bridging.

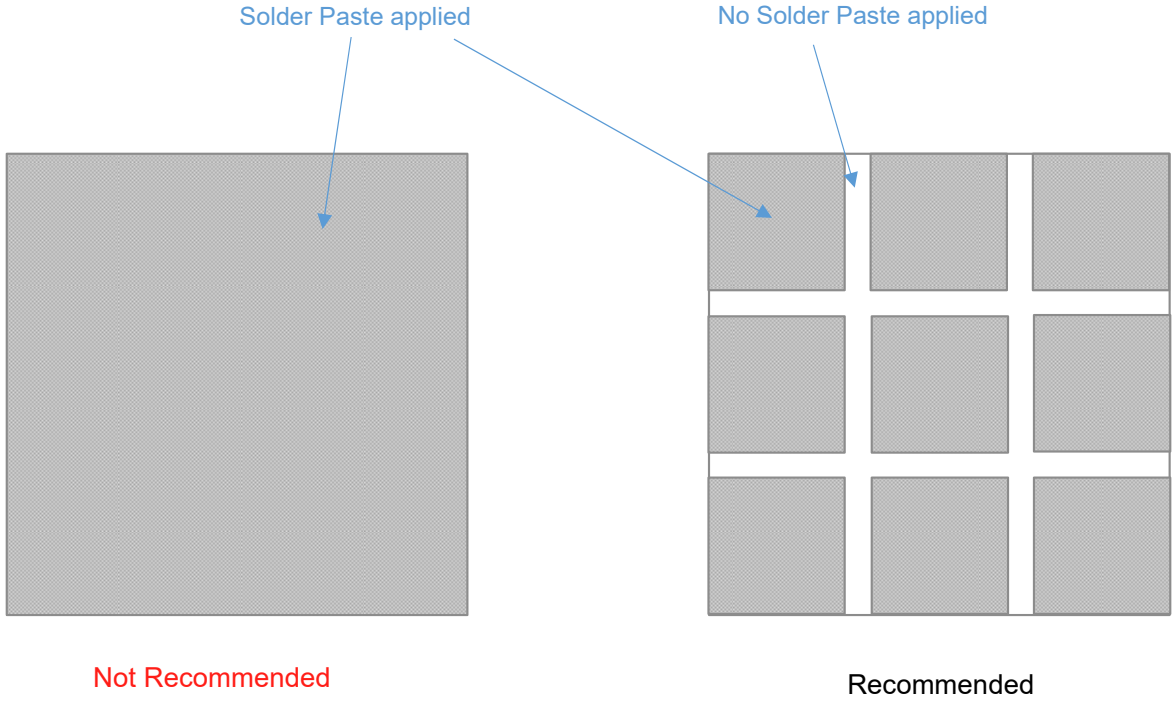
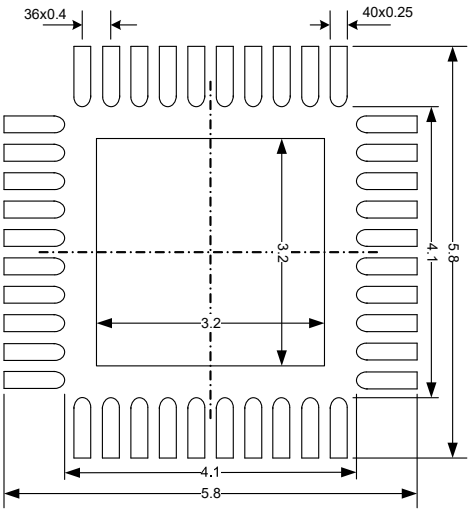


Figure 9. Thermal Pad Stencil Opening for Large Thermal Pad

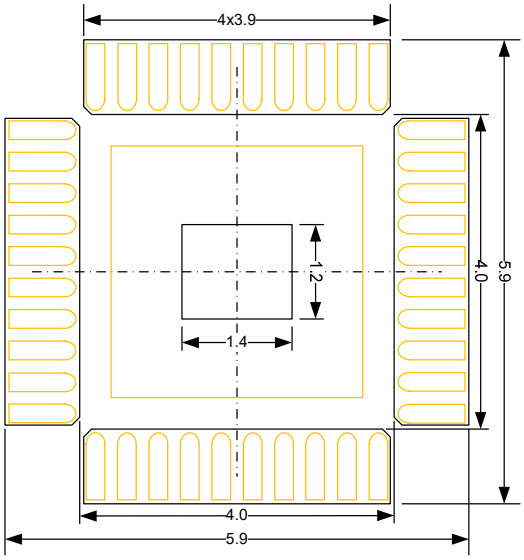
Layout Guideline Examples

The following pages provide recommended PCB land pattern, thermal vias, solder mask opening, and stencil design for different packages.

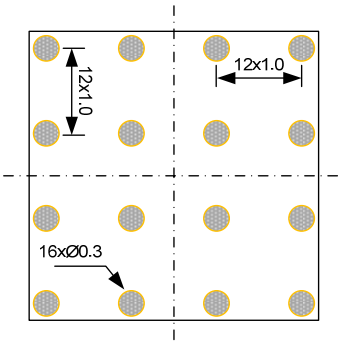
40L-FCSLP EXAMPLE



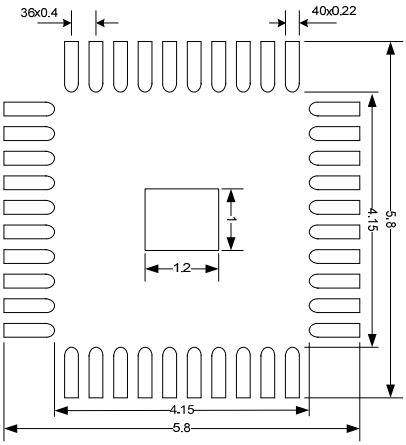
PCB Layout Pattern



Solder Mask Opening



Thermal Vias Design

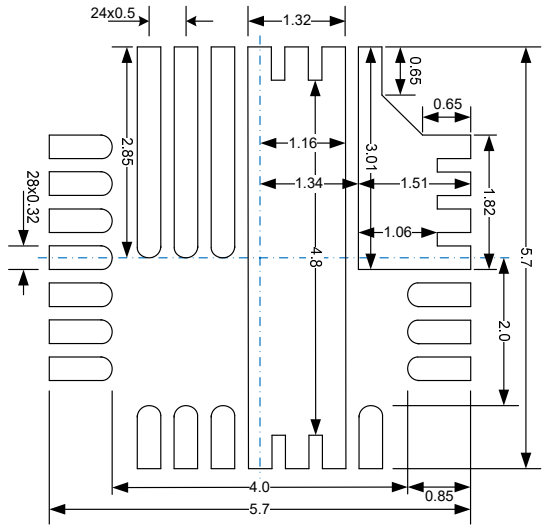


Stencil Design

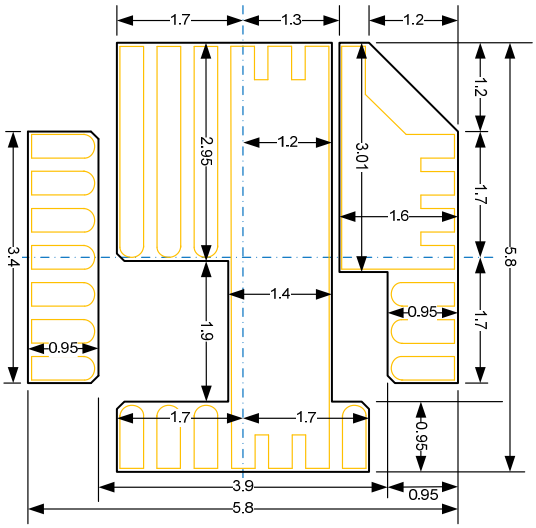
Note1: All dimensions in mm

Note2: The ACT8870 uses this special package

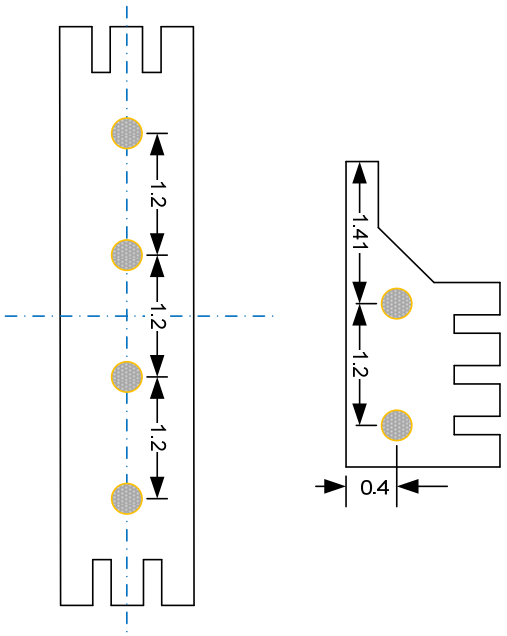
28L-FCSLP EXAMPLE



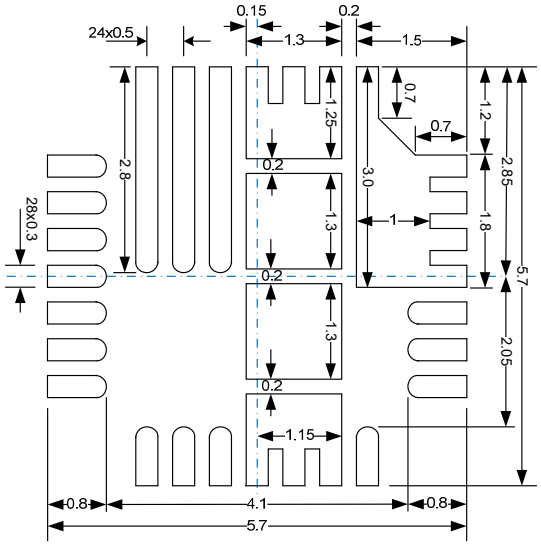
PCB Layout Pattern



Solder Mask Opening



Thermal Vias Design

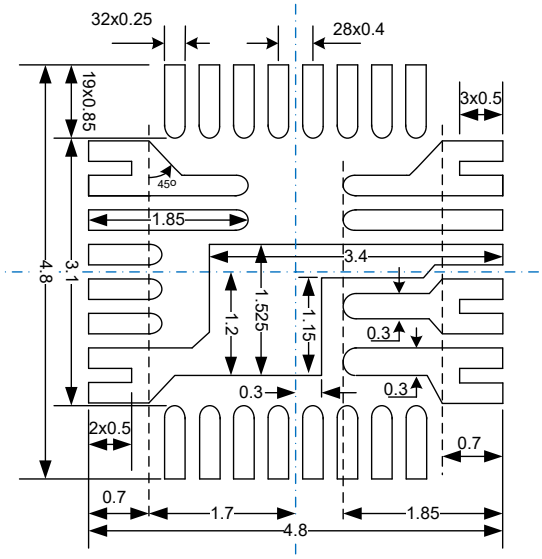


Stencil Design

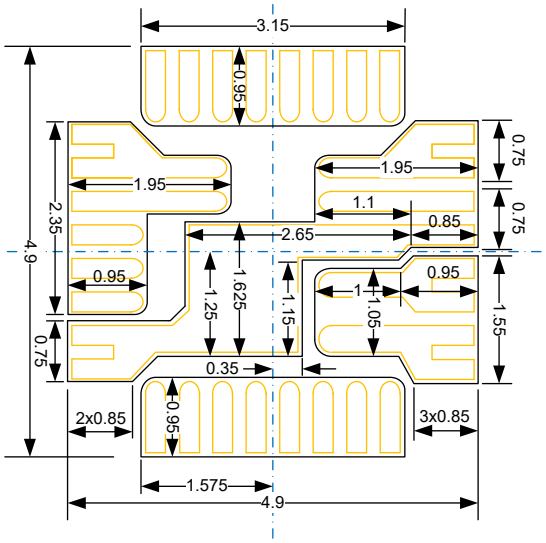
Note1: All dimensions in mm

Note2: The ACT4910 uses this special package

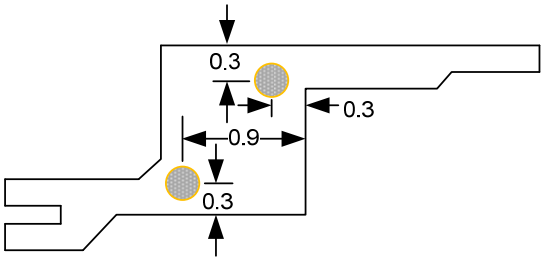
32L-FCSLP EXAMPLE



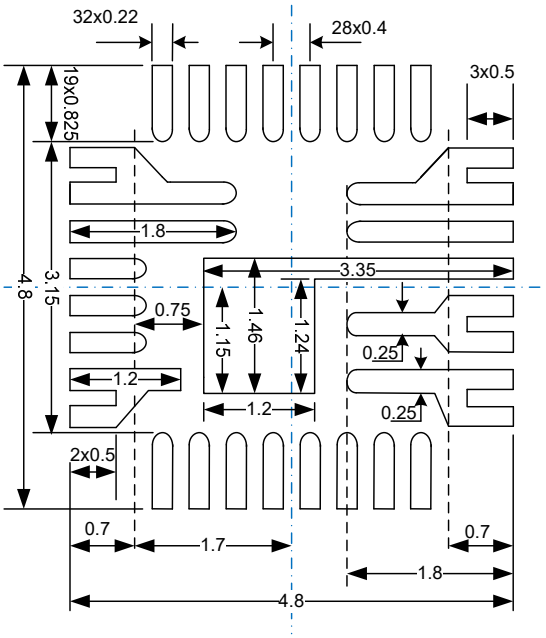
PCB Layout Pattern



Solder Mask Opening



Thermal Vias Design



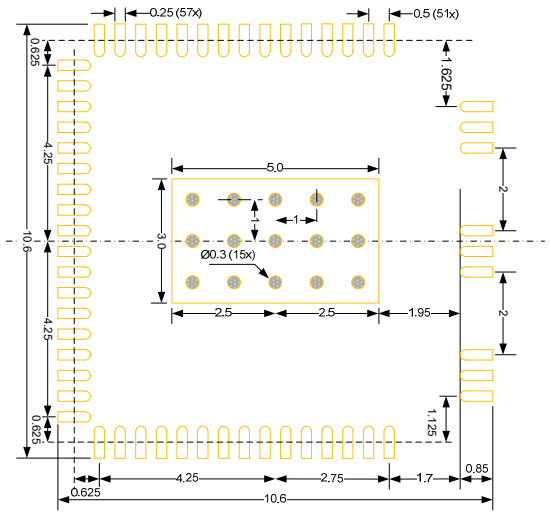
Stencil Design

For the Thermal Via Design, the PCB designer may put 4x of 0.3mm vias in the middle pad.

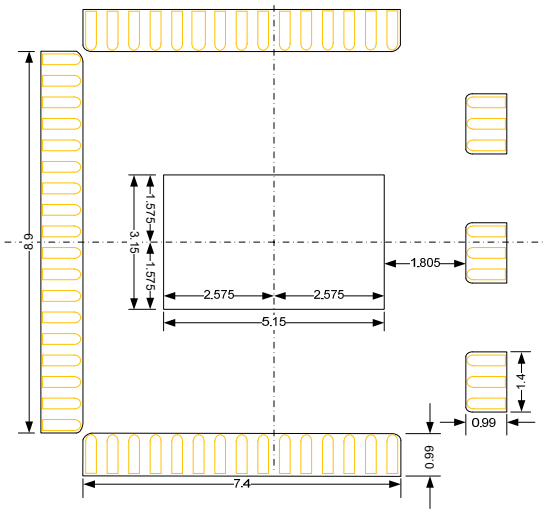
Note1: All dimensions in mm

Note2: The ACT88320 uses this special package

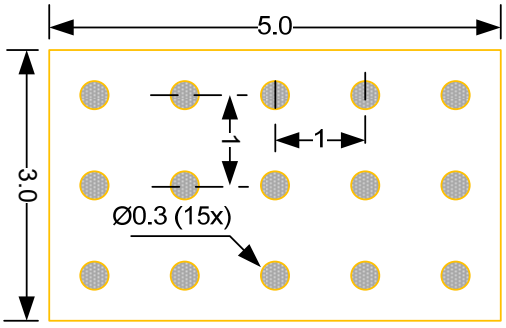
TQFN1010-57 EXAMPLE



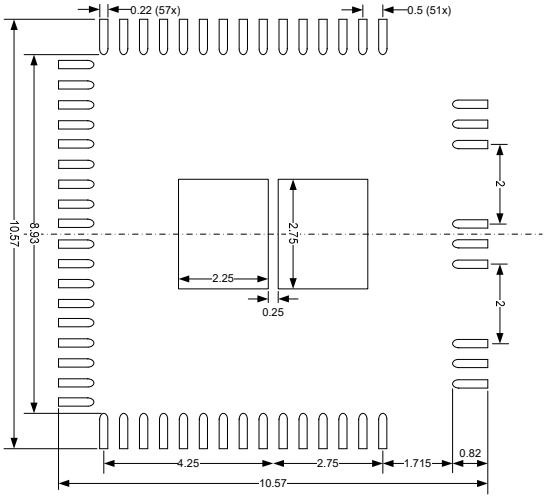
PCB Layout Pattern



Solder Mask Opening



Thermal Vias Design

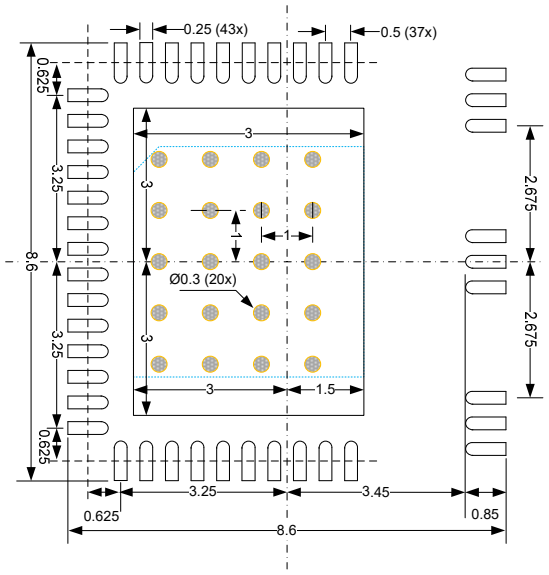


Stencil Design

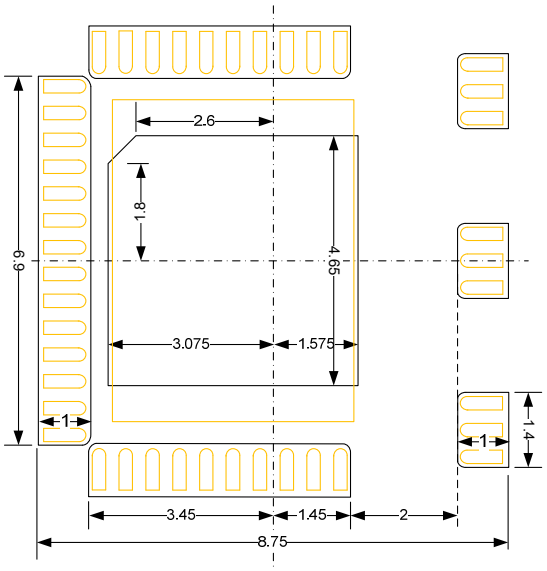
Note1: All dimensions in mm

Note2: The PAC5250 uses this special package

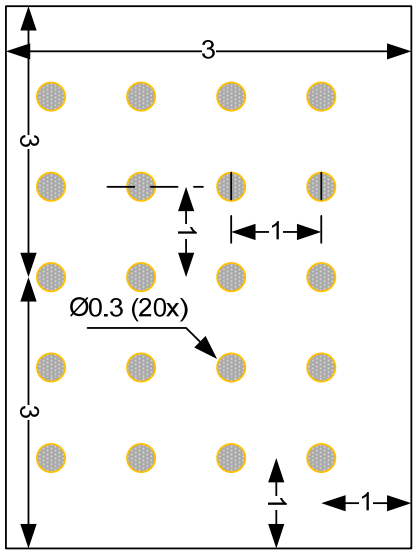
TQFN88-43 EXAMPLE



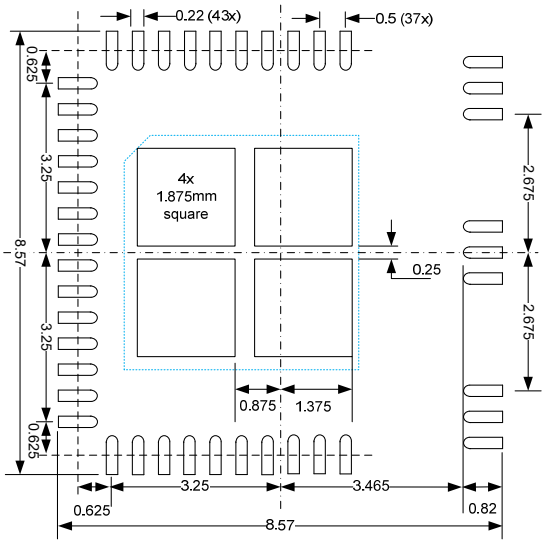
PCB Layout Pattern



Solder Mask Opening



Thermal Vias Design



Stencil Design

Note1: All dimensions in mm

Note2: The PAC5253 uses this special package