0.2 µV/°C Offset Drift, 105 MHz Low Power, Low Noise, Rail-to-Rail Amplifier

Data Sheet

ADA4805-1

FEATURES

- Low input offset voltage: 125 µV (maximum)
- Low input offset voltage drift
  - 0.2 µV/°C (typical)
  - 1.5 µV/°C (maximum)
- Ultralow supply current: 495 µA/amplifier
- Wide supply voltage range: 3 V to 10 V
- High speed performance
  - −3 dB bandwidth: 105 MHz
  - Slew rate: 160 V/µs
  - 0.1% settling time: 35 ns
- Rail-to-rail outputs
- Input common-mode range: $-V_S - 0.1$ V to $+V_S - 1$ V
- Low noise: 5.9 nV/√Hz at 100 kHz; 0.6 pA/√Hz at 100 kHz
- Low distortion: −102 dBc/−116 dBc HD2/HD3 at 100 kHz
- Low input bias current: 470 nA (typical)
- Dynamic power scaling
  - High speed turn-on time: 3 µs (maximum) fully settled
- Small packaging
  - 6-lead SC70, 6-lead SOT-23

APPLICATIONS

- High resolution, high precision ADC drivers
- Battery-powered instrumentation
- Micropower active filters
- Portable point of sales terminals
- Active RFID readers
- Photo multipliers
- ADC reference buffers

GENERAL DESCRIPTION

The ADA4805-1 is a high speed voltage feedback rail-to-rail output amplifier with an exceptionally low quiescent current of 495 µA, making it ideal for low power, high resolution data conversion systems. Despite being low power, this amplifier provides excellent overall performance. It offers a high bandwidth of 105 MHz at a gain of 1, high slew rate of 160 V/µs, and a low input offset voltage of 125 µV maximum.

A shutdown pin allows further reduction of the quiescent supply current to 3 µA. For power sensitive applications, the shutdown mode offers very fast turn-on time of 3 µs from shutdown to fully on (output settled to 16 bits). This allows the user to dynamically manage the power of the amplifier by turning the amplifier off between ADC samples.

The Analog Devices, Inc., proprietary extra fast complementary bipolar (XFCB) process allows for both low voltage and low current noise (5.9 nV/√Hz, 0.6 pA/√Hz). The ADA4805-1 operates over a wide range of supply voltages from ±1.5 V to ±5 V, as well as from single 3 V and 5 V supplies, making it ideal for high speed, low power instruments.

The ADA4805-1 amplifier is available in both a 6-lead SOT-23 and a 6-lead SC70 package. These amplifiers are rated to work over the industrial temperature range of −40°C to +125°C.

TYPICAL APPLICATIONS CIRCUIT

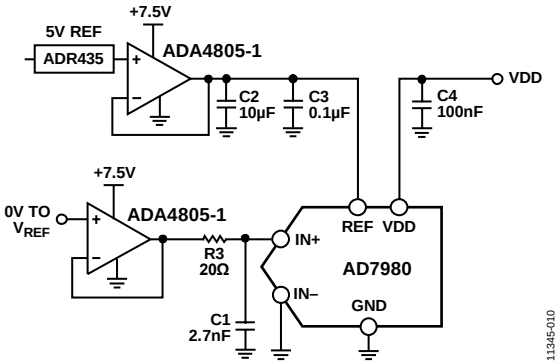

Figure 1. Driving the AD7980 with the ADA4805-1

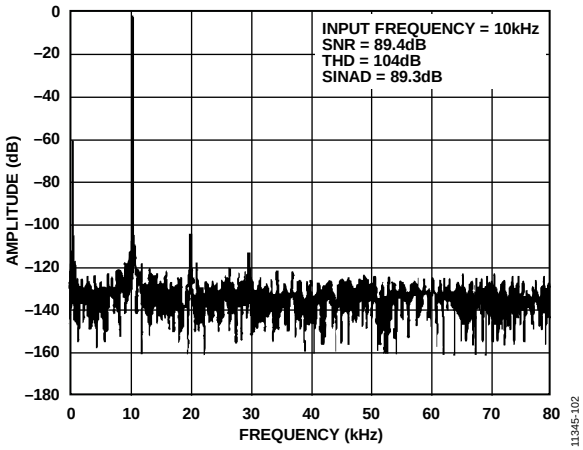

Figure 2. FFT Plot for the Circuit Configuration in Figure 1

Table 1. Complementary Products to the ADA4805-1

Product	Power (mW)	Throughput (MSPS)	Resolution (Bits)	SNR (dB)
AD7982	7.0	1	18	98
AD7984	10.5	1.33	18	98.5
AD7980	4.0	1	16	91
AD7685	10	0.25	16	88

Rev. 0 Document Feedback

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REVISION HISTORY

7/14—Revision 0: Initial Version

SPECIFICATIONS

±5 V SUPPLY

V_S = ±5 V at T_A = 25°C; R_F = 0 Ω for G = +1; otherwise, R_F = 1 kΩ; R_L = 2 kΩ to ground; unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		120		MHz
	G = +1, V_{OUT} = 2 V p-p		40		MHz
Bandwidth for 0.1 dB Flatness	G = +1, V_{OUT} = 0.02 V p-p		18		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step		190		V/µs
	G = +2, V_{OUT} = 4 V step		250		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 2 V step		35		ns
	G = +2, V_{OUT} = 4 V step		78		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3[1]	f_C = 20 kHz, V_{OUT} = 2 V p-p		−114/−115		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−102/−115		dBc
	f_C = 20 kHz, V_{OUT} = 4 V p-p, G = +1		−109/−119		dBc
	f_C = 100 kHz, V_{OUT} = 4 V p-p, G = +1		−93/−113		dBc
	f_C = 20 kHz, V_{OUT} = 4 V p-p, G = +2		−113/−120		dBc
	f_C = 100 kHz, V_{OUT} = 4 V p-p, G = +2		−96/−104		dBc
Input Voltage Noise	f = 100 kHz		5.2		nV/√Hz
Input Voltage Noise 1/f Corner Frequency			8		Hz
0.1 Hz to 10 Hz Voltage Noise			44		nV rms
Input Current Noise	f = 100 kHz		0.7		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			13	125	µV
Input Offset Voltage Drift[2]	T_{MIN} to T_{MAX}, 4 σ		0.2	1.5	µV/°C
Input Bias Current			550	800	nA
Input Offset Current			2.1	25	nA
Open-Loop Gain	V_{OUT} = −4.0 V to +4.0 V	107	111		dB
INPUT CHARACTERISTICS					
Input Resistance					
Common Mode			50		MΩ
Differential Mode			260		kΩ
Input Capacitance			1		pF
Input Common-Mode Voltage Range		−5.1		+4	V
Common-Mode Rejection Ratio	$V_{IN, CM}$ = −4.0 V to +4.0 V	103	130		dB
$\overline{\text{SHUTDOWN}}$ PIN					
$\overline{\text{SHUTDOWN}}$ Voltage					
Low	Powered down		<−1.3		V
High	Enabled		>−0.9		V
$\overline{\text{SHUTDOWN}}$ Current					
Low	Powered down		20		nA
High	Enabled		195		nA
Turn-Off Time	50% of $\overline{\text{SHUTDOWN}}$ to <10% of enabled quiescent current		2		µs
Turn-On Time	50% of $\overline{\text{SHUTDOWN}}$ to >90% of final V_{OUT}		2	3	µs
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = +6 V to −6 V, G = +2		95/100		ns
Output Voltage Swing	R_L = 2 kΩ	−4.98		+4.98	V
Short-Circuit Current	Sinking/sourcing		85/73		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Linear Output Current	<1% THD at 100 kHz, V_{OUT} = 2 V p-p		±58		mA
Off Isolation	V_{IN} = 0.5 V p-p, f = 1 MHz, $\overline{SHUTDOWN}$ = low		41		dB
Capacitive Load Drive	30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		10	V
Quiescent Current	Enabled		570	625	µA
	$\overline{SHUTDOWN}$ = $-V_S$		7.4	12	µA
Power Supply Rejection Ratio					
Positive	$+V_S$ = 3 V to 5 V, $-V_S$ = −5 V	100	119		dB
Negative	$+V_S$ = 5 V, $-V_S$ = −3 V to −5 V	100	122		dB

[1] f_C is the fundamental frequency.
[2] Guaranteed, but not tested.

5 V SUPPLY

V_S = 5 V at T_A = 25°C; R_F = 0 Ω for G = +1; otherwise, R_F = 1 kΩ; R_L = 2 kΩ to midsupply; unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		105		MHz
	G = +1, V_{OUT} = 2 V p-p		35		MHz
Bandwidth for 0.1 dB Flatness	G = +1, V_{OUT} = 0.02 V p-p		20		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step		160		V/µs
	G = +2, V_{OUT} = 4 V step		220		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 2 V step		35		ns
	G = +2, V_{OUT} = 4 V step		82		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3[1]	f_C = 20 kHz, V_{OUT} = 2 V p-p		−114/−119		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−102/−116		dBc
	f_C = 20 kHz, G = +2, V_{OUT} = 4 V p-p		−107/−118		dBc
	f_C = 100 kHz, G = +2, V_{OUT} = 4 V p-p		−90/−109		dBc
Input Voltage Noise	f = 100 kHz		5.9		nV/√Hz
Input Voltage Noise 1/f Corner			8		Hz
0.1 Hz to 10 Hz Voltage Noise			54		nV rms
Input Current Noise	f = 100 kHz		0.6		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			9	125	µV
Input Offset Voltage Drift[2]	T_{MIN} to T_{MAX}, 4 σ		0.2	1.5	µV/°C
Input Bias Current			470	720	nA
Input Offset Current			0.4		nA
Open-Loop Gain	V_{OUT} = 1.25 V to 3.75 V	105	109		dB
INPUT CHARACTERISTICS					
Input Resistance					
Common Mode			50		MΩ
Differential Mode			260		kΩ
Input Capacitance			1		pF
Input Common-Mode Voltage Range		−0.1		+4	V
Common-Mode Rejection Ratio	$V_{IN, CM}$ = 1.25 V to 3.75 V	103	133		dB
$\overline{SHUTDOWN}$ PIN					
$\overline{SHUTDOWN}$ Voltage					
Low	Powered down		<1.5		V
High	Enabled		>1.9		V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
$\overline{\text{SHUTDOWN}}$ Current					
Low	Powered down		10		nA
High	Enabled		74		nA
Turn-Off Time	50% of $\overline{\text{SHUTDOWN}}$ to <10% of enabled quiescent current		1.5		µs
Turn-On Time	50% of $\overline{\text{SHUTDOWN}}$ to >90% of final V_{OUT}		3	4	µs
OUTPUT CHARACTERISTICS					
Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = −1 V to +6 V, G = +2		130/145		ns
Output Voltage Swing	R_L = 2 kΩ	0.02		4.98	V
Short-Circuit Current	Sinking/sourcing		73/63		mA
Linear Output Current	<1% THD at 100 kHz, V_{OUT} = 2 V p-p		±47		mA
Off Isolation	V_{IN} = 0.5 V p-p, f = 1 MHz, $\overline{\text{SHUTDOWN}}$ = $-V_S$		41		dB
Capacitive Load Drive	30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		10	V
Quiescent Current	Enabled		495	520	µA
	$\overline{\text{SHUTDOWN}}$ = $-V_S$		2.9	4	µA
Power Supply Rejection Ratio					
Positive	$+V_S$ = 1.5 V to 3.5 V, $-V_S$ = −2.5 V	100	120		dB
Negative	$+V_S$ = 2.5 V, $-V_S$ = −1.5 V to −3.5 V	100	126		dB

[1] f_C is the fundamental frequency.
[2] Guaranteed, but not tested.

3 V SUPPLY

V_S = 3 V at T_A = 25°C; R_F = 0 Ω for G = +1; otherwise, R_F = 1 kΩ; R_L = 2 kΩ to midsupply; unless otherwise noted. All specifications are per amplifier.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		95		MHz
	G = +1, V_{OUT} = 1 V p-p, $+V_S$ = 2 V, $-V_S$ = −1 V		30		MHz
Bandwidth for 0.1 dB Flatness	G = +1, V_{OUT} = 0.02 V p-p		35		MHz
Slew Rate	G = +1, V_{OUT} = 1 V step, $+V_S$ = 2 V, $-V_S$ = −1 V		85		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 1 V step		41		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3[1]	f_C = 20 kHz, V_{OUT} = 1 V p-p, $+V_S$ = 2 V, $-V_S$ = −1 V		−123/−121		dBc
	f_C = 100 kHz, V_{OUT} = 1 V p-p, $+V_S$ = 2 V, $-V_S$ = −1 V		−107/−121		dBc
Input Voltage Noise	f = 100 kHz		6.3		nV/√Hz
Input Voltage Noise 1/f Corner			8		Hz
0.1 Hz to 10 Hz Voltage Noise			55		nV rms
Input Current Noise	f = 100 kHz		0.8		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			7	125	µV
Input Offset Voltage Drift[2]	T_{MIN} to T_{MAX}, 4 σ		0.2	1.5	µV/°C
Input Bias Current			440	690	nA
Input Offset Current			0.5		nA
Open-Loop Gain	V_{OUT} = 1.1 V to 1.9 V	100	107		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Resistance					
Common Mode			50		MΩ
Differential Mode			260		kΩ
Input Capacitance			1		pF
Input Common-Mode Voltage Range		−0.1		+2	V
Common-Mode Rejection Ratio	$V_{IN, CM}$ = 0.5 V to 2 V	89	117		dB
$\overline{\text{SHUTDOWN}}$ PIN					
$\overline{\text{SHUTDOWN}}$ Voltage					
Low	Powered down		<0.7		V
High	Enabled		>1.1		V
$\overline{\text{SHUTDOWN}}$ Current					
Low	Powered down		6.4		nA
High	Enabled		32		nA
Turn-Off Time	50% of $\overline{\text{SHUTDOWN}}$ to <10% of enabled quiescent current		1		µs
Turn-On Time	50% of $\overline{\text{SHUTDOWN}}$ to >90% of final V_{OUT}		7	8	µs
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = −1 V to +4 V, G = +2		135/175		ns
Output Voltage Swing	R_L = 2 kΩ	0.02		2.98	V
Short-Circuit Current	Sinking/sourcing		65/47		mA
Linear Output Current	<1% THD at 100 kHz, V_{OUT} = 1 V p-p		±40		mA
Off Isolation	V_{IN} = 0.5 V p-p, f = 1 MHz, $\overline{\text{SHUTDOWN}}$ = $-V_S$		41		dB
Capacitive Load Drive	30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		10	V
Quiescent Current	Enabled		470	495	µA
	$\overline{\text{SHUTDOWN}}$ = $-V_S$		1.3	3	µA
Power Supply Rejection Ratio					
Positive	$+V_S$ = 1.5 V to 3.5 V, $-V_S$ = −1.5 V	96	119		dB
Negative	$+V_S$ = 1.5 V, $-V_S$ = −1.5 V to −3.5 V	96	125		dB

[1] f_C is the fundamental frequency.
[2] Guaranteed, but not tested.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$-V_S - 0.7$ V to $+V_S + 0.7$ V
Differential Input Voltage	±1 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages. Table 6 lists the θ_{JA} for the ADA4805-1.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
6-Lead SC70	224	°C/W
6-Lead SOT-23	209	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the ADA4805-1 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4805-1. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the ADA4805-1 output load drive.

The quiescent power dissipation is the voltage between the supply pins ($\pm V_S$) multiplied by the quiescent current (I_S).

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = \left(V_S \times I_S\right) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = \left(V_S \times I_S\right) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

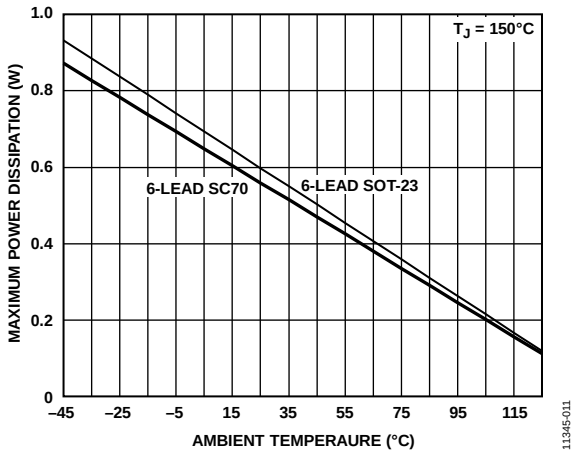


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

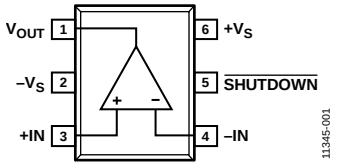


Figure 4. 6-Lead SC70 Pin Configuration

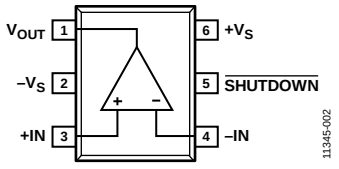


Figure 5. 6-Lead SOT-23 Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT}	Output.
2	$-V_S$	Negative Supply.
3	+IN	Noninverting Input.
4	–IN	Inverting Input.
5	$\overline{\text{SHUTDOWN}}$	Active Low Power-Down.
6	$+V_S$	Positive Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

R_L = 2 kΩ, unless otherwise noted. When G = +1, R_F = 0 Ω.

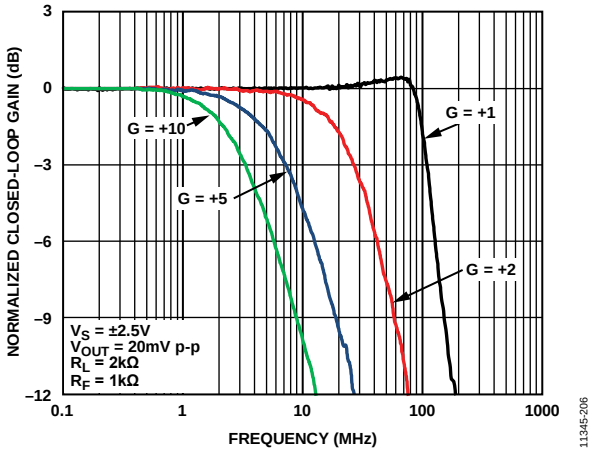


Figure 6. Small Signal Frequency Response vs. Frequency for Various Gains

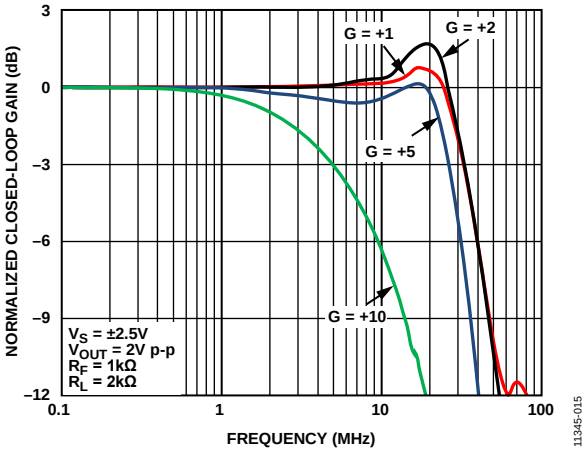


Figure 9. Large Signal Frequency Response vs. Frequency for Various Gains

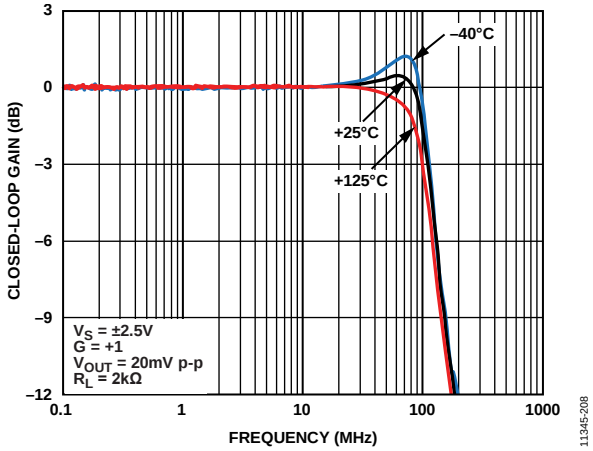


Figure 7. Small Signal Frequency Response vs. Frequency for Various Temperatures

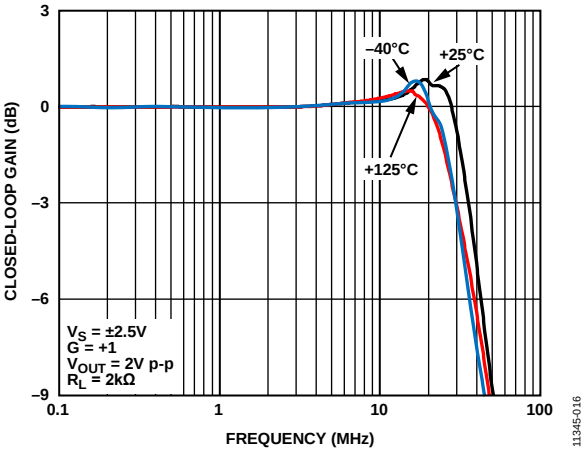


Figure 10. Large Signal Frequency Response vs. Frequency for Various Temperatures

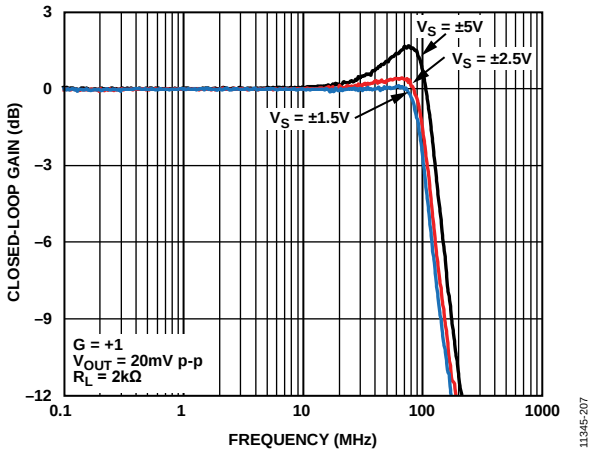


Figure 8. Small Signal Frequency Response vs. Frequency for Various Supply Voltages

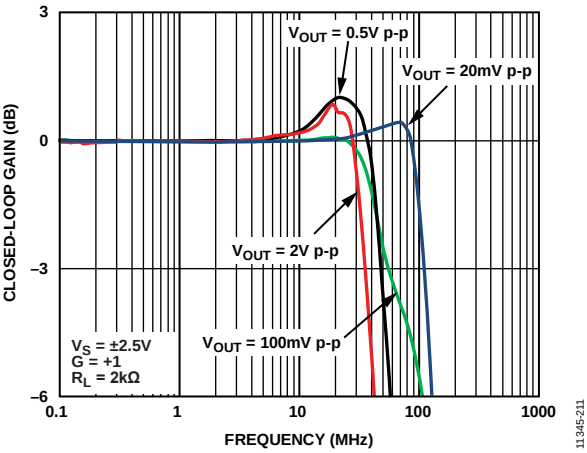


Figure 11. Frequency Response for Various Output Voltages

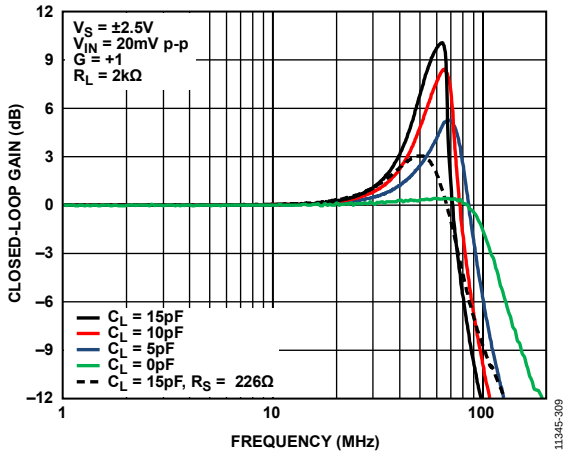


Figure 12. Small Signal Frequency Response vs. Frequency for Various Capacitive Loads (See Figure 42)

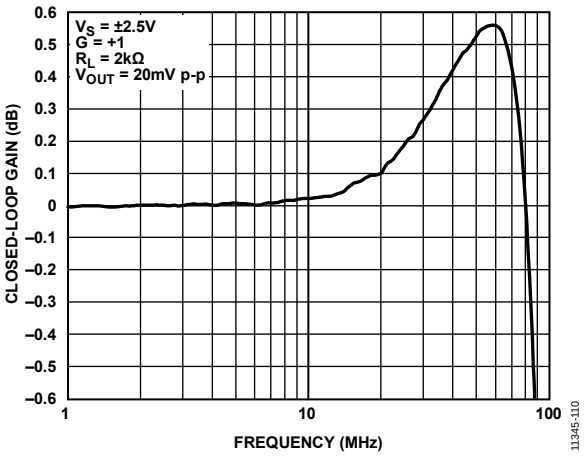


Figure 15. Small Signal 0.1 dB Bandwidth

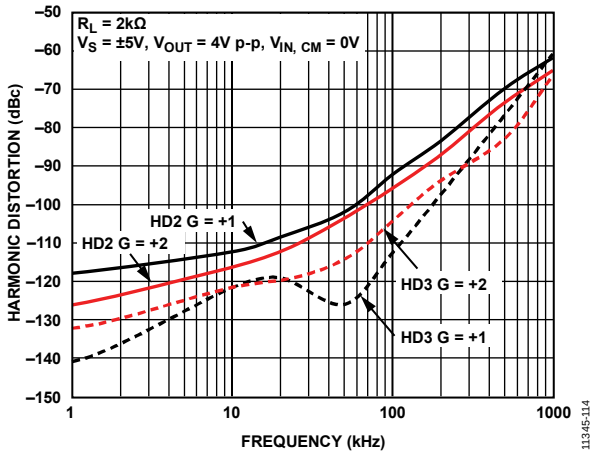


Figure 13. Harmonic Distortion vs. Frequency for Various Gains

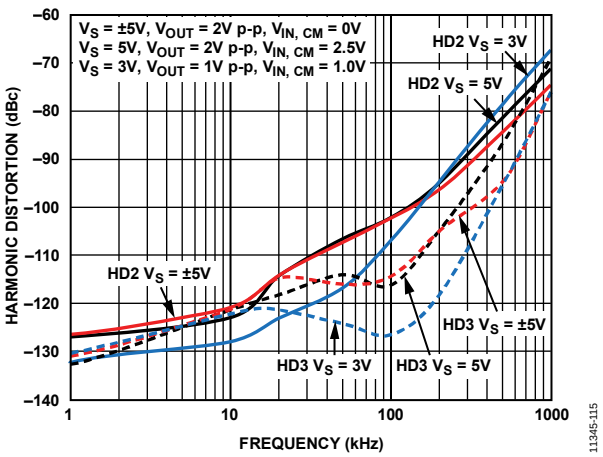


Figure 16. Harmonic Distortion vs. Frequency for Various Supplies, G = +1

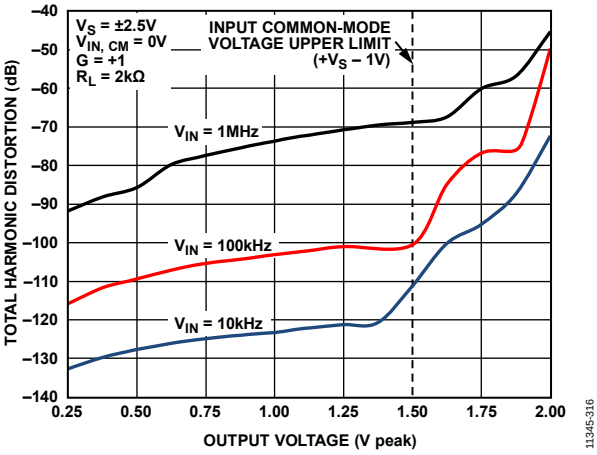


Figure 14. Total Harmonic Distortion Vs. Output Voltage For Various Frequencies

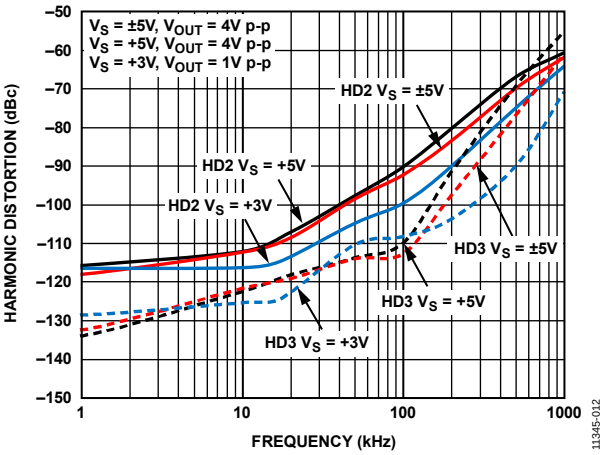


Figure 17. Harmonic Distortion vs. Frequency, G = +2

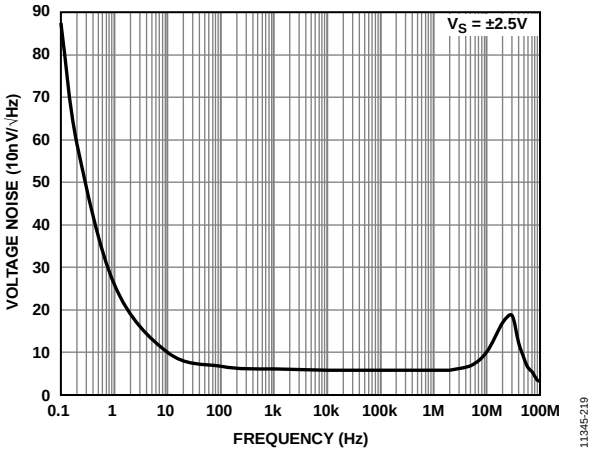


Figure 18. Voltage Noise vs. Frequency

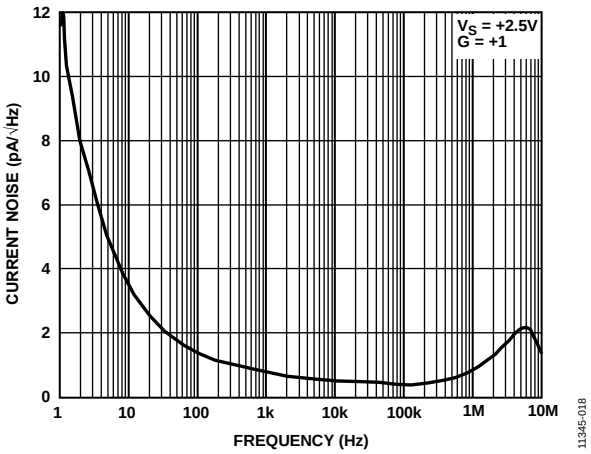


Figure 21. Current Noise vs. Frequency (See Figure 43)

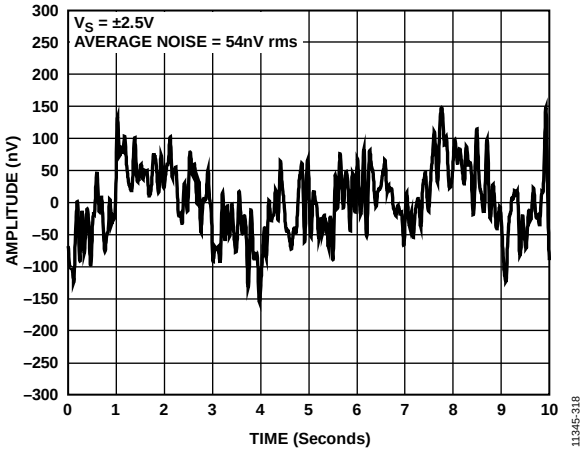


Figure 19. 0.1 Hz to 10 Hz Voltage Noise

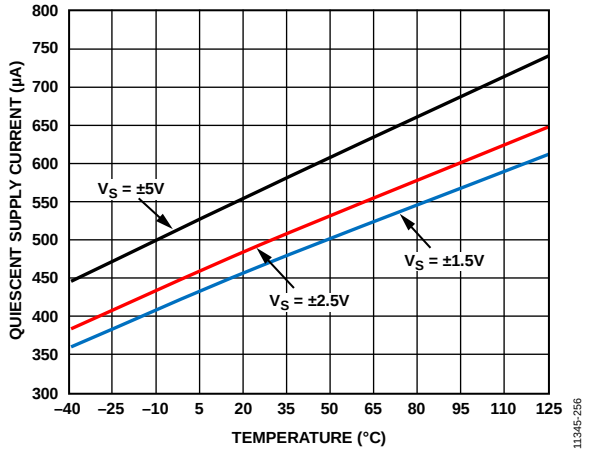


Figure 22. Quiescent Supply Current vs. Temperature for Various Supplies

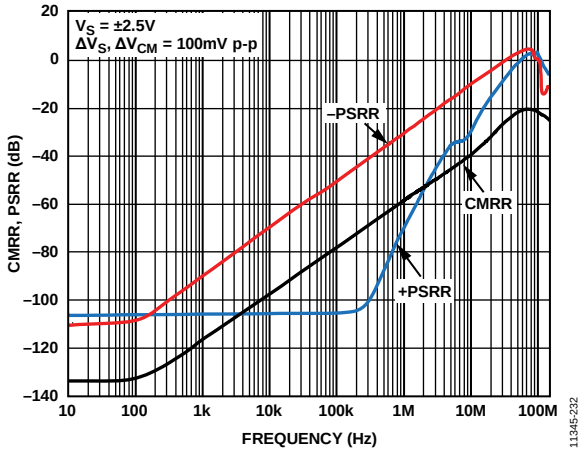


Figure 20. CMRR, PSRR vs. Frequency

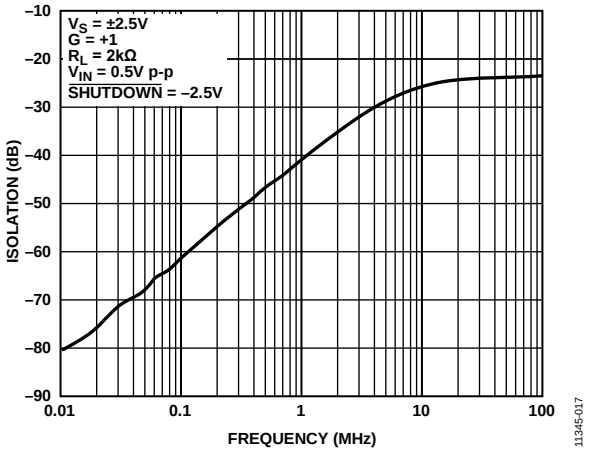


Figure 23. Forward/Off Isolation vs. Frequency

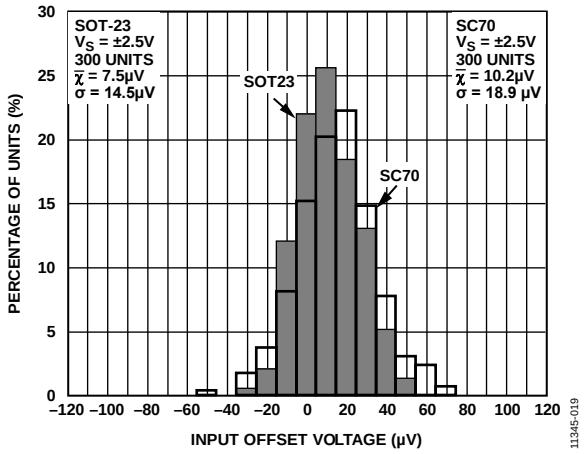


Figure 24. Input Offset Voltage Distribution

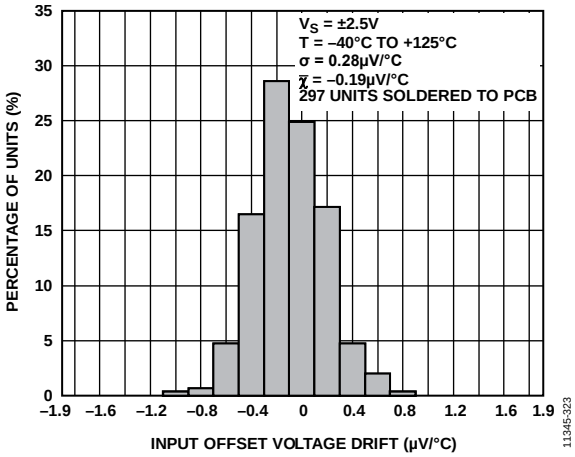


Figure 27. Input Offset Voltage Drift Distribution

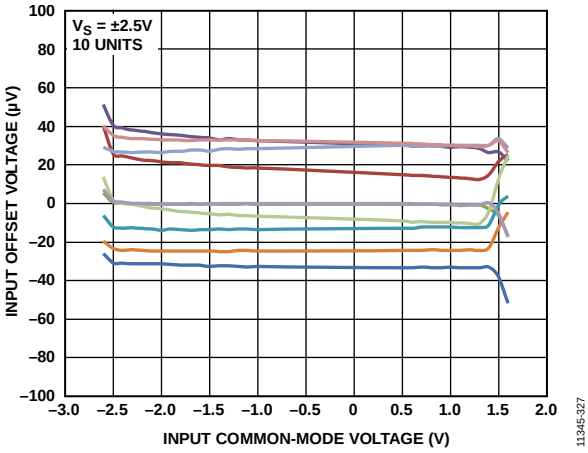


Figure 25. Input Voltage Offset vs. Input Common-Mode Voltage

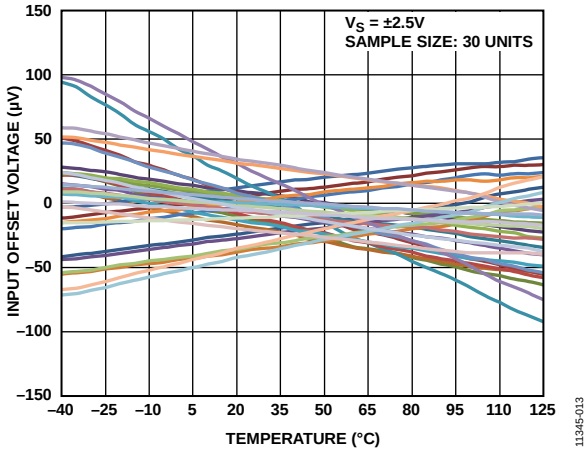


Figure 28. Input Offset Voltage vs. Temperature

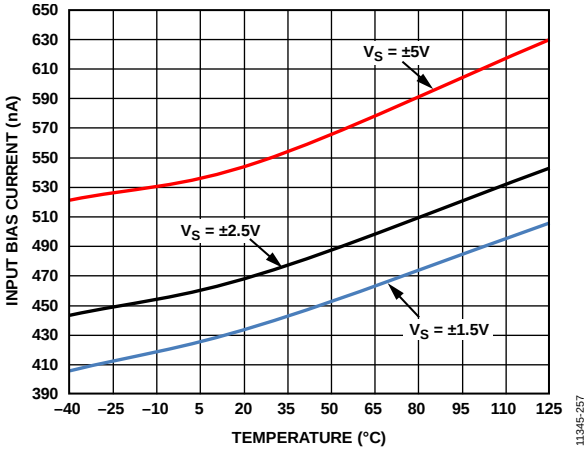


Figure 26. Input Bias Current vs. Temperature for Various Supplies (See Figure 44)

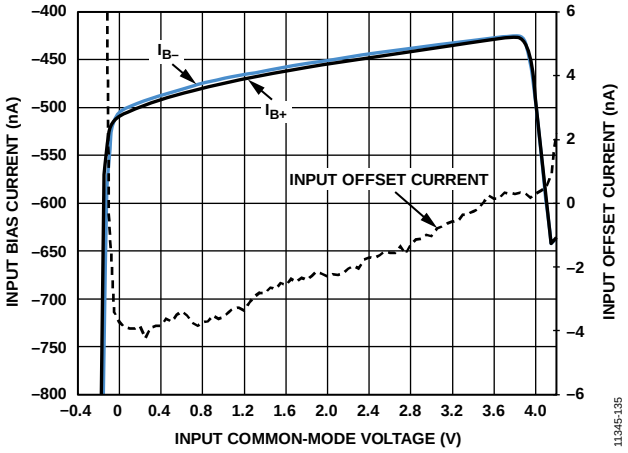


Figure 29. Input Bias Current and Input Offset Current vs. Input Common-Mode Voltage

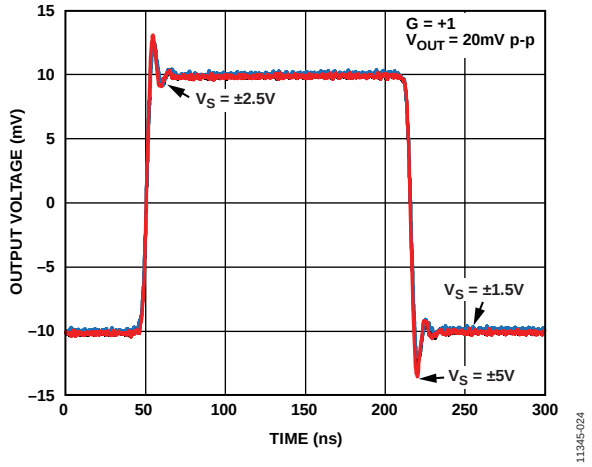


Figure 30. Small Signal Transient Response for Various Supplies, G = +1

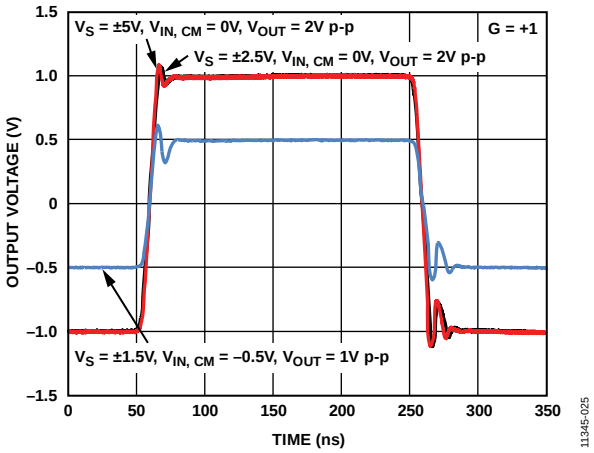


Figure 33. Large Signal Transient Response for Various Supplies, G = +1

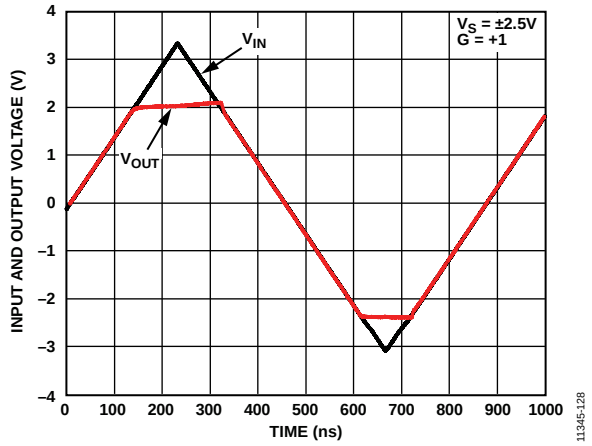


Figure 31. Input Overdrive Recovery Time, G = +1

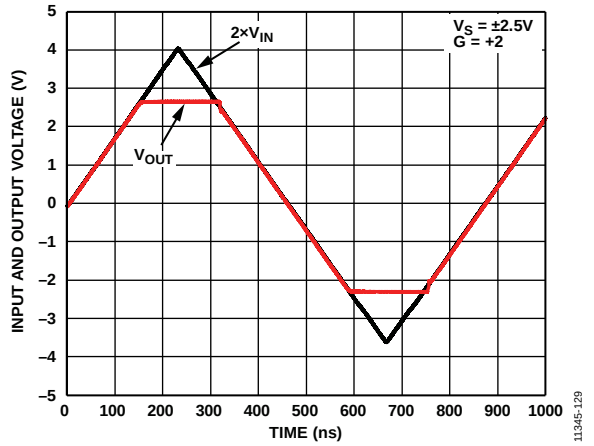


Figure 34. Output Overdrive Recovery Time, G = +2

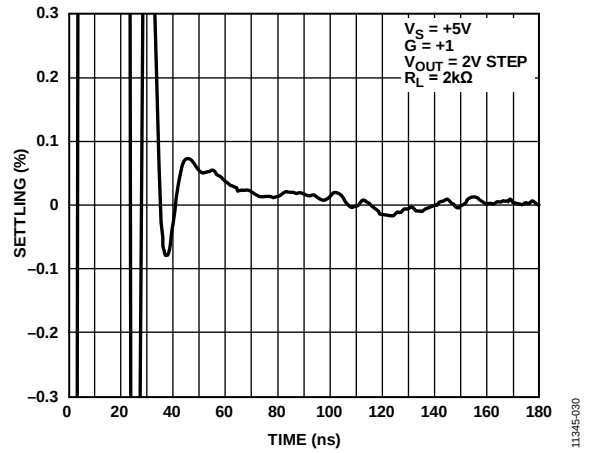


Figure 32. Settling Time to 0.1%

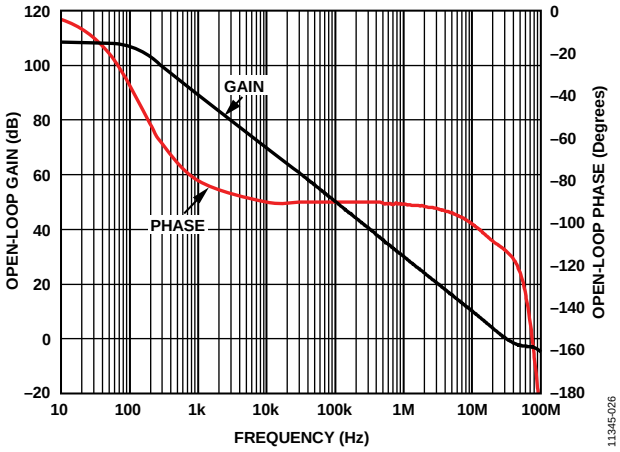


Figure 35. Open-Loop Gain and Phase Margin

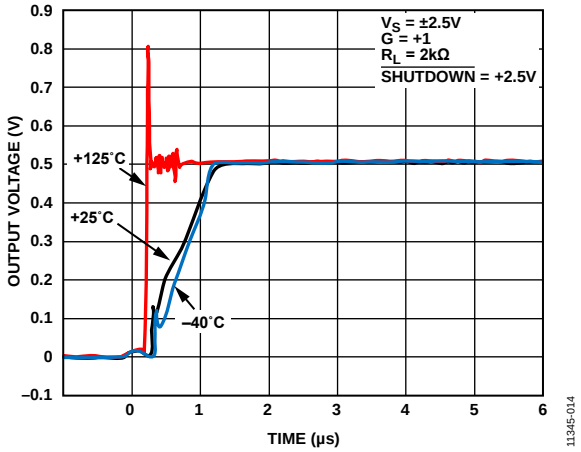


Figure 36. Turn-On Response Time for Various Temperatures (See Figure 45)

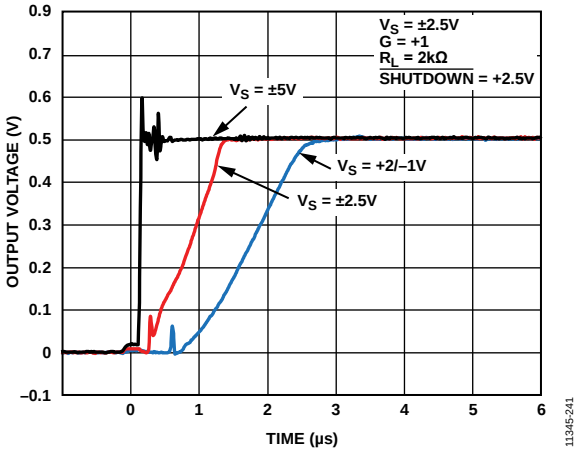


Figure 39. Turn-On Response Time for Various Supplies (See Figure 45)

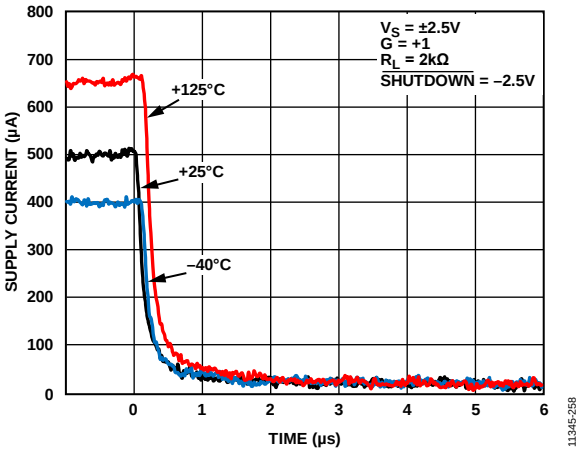


Figure 37. Turn-Off Response Time for Various Temperatures (See Figure 46)

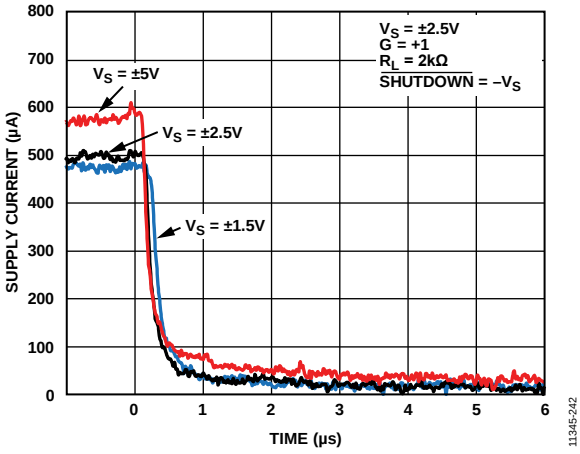


Figure 40. Turn-Off Response Time for Various Supplies (See Figure 46)

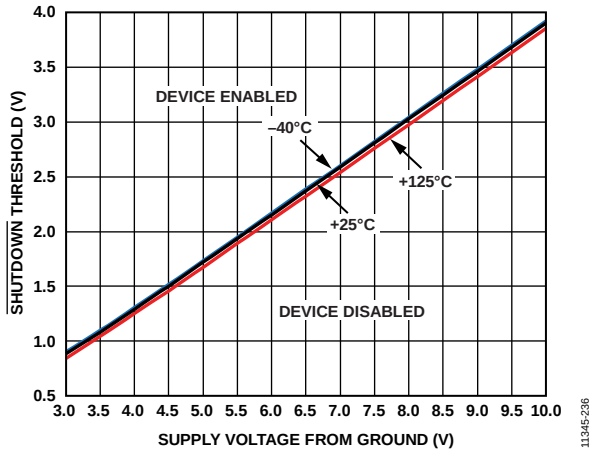


Figure 38. $\overline{SHUTDOWN}$ Threshold vs. Supply Voltage from Ground for Various Temperatures

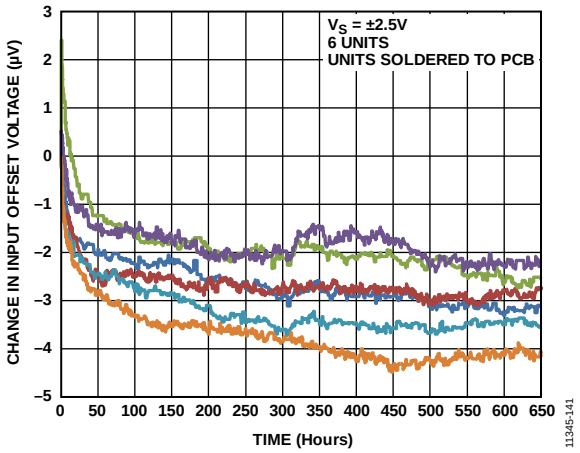


Figure 41. Long-Term V_{OS} Drift

TEST CIRCUITS

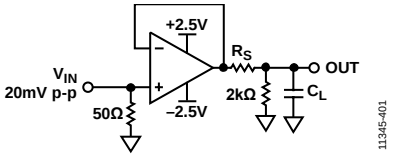


Figure 42. Output Capacitive Load Behavior Test Circuit (See Figure 12)

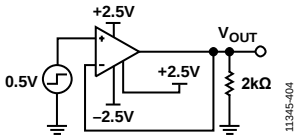


Figure 45. Turn-On Response Test Circuit (See Figure 36 and Figure 39)

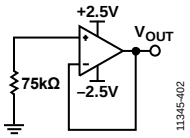


Figure 43. Current Noise Test Circuit (See Figure 21)

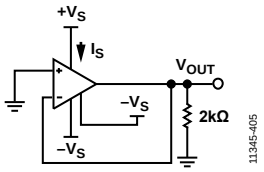


Figure 46. Turn-Off Response Test Circuit (See Figure 37 and Figure 40)

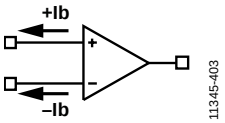


Figure 44. Input Bias Current Temperature Test Circuit (See Figure 26)

THEORY OF OPERATION

AMPLIFIER DESCRIPTION

The ADA4805-1 has a bandwidth of 105 MHz and a slew rate of 160 V/µs. It has an input referred voltage noise of only 5.9 nV/√Hz. The ADA4805-1 operates over supply voltages from 3 V to 10 V and consumes only 495 µA of supply current at 5 V. The amplifiers are unity-gain stable, and the input structure results in an extremely low input 1/f noise. The ADA4805-1 uses a slew enhancement architecture, as shown in Figure 47. The slew enhancement circuit detects the absolute difference between the two inputs. It then modulates the tail current, I_{TAIL}, of the input stage to boost the slew rate. The architecture allows higher slew rate and fast settling time with low quiescent current while maintaining low noise.

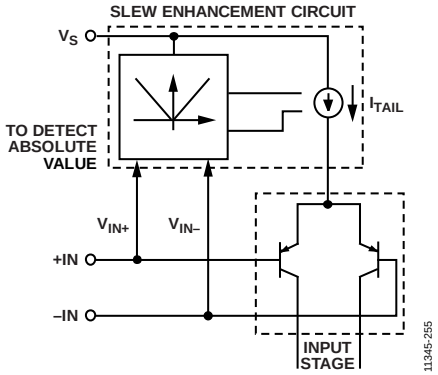


Figure 47. Slew Rate Enhancement Circuit

INPUT PROTECTION

The ADA4805-1 is fully protected from ESD events, withstanding human body model ESD events of ±3.5 kV and charged-device model events of ±1.25 kV with no measured performance degradation. The precision input is protected with an ESD network between the power supplies and diode clamps across the input device pair, as shown in Figure 48.

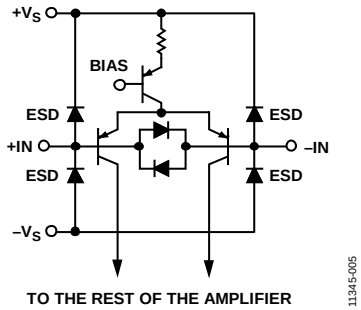


Figure 48. Input Stage and Protection Diodes

For differential voltages above approximately 1.2 V at room temperature, and 0.8 V at 125°C, the diode clamps begin to conduct. Too much current can cause damage due to excessive heating. If large differential voltages must be sustained across the input terminals, it is recommended that the current through the input clamps be limited to less than 10 mA. Series input resistors that are sized appropriately for the expected differential overvoltage provide the needed protection.

The ESD clamps begin to conduct for input voltages that are more than 0.7 V above the positive supply and input voltages more than 0.7 V below the negative supply. If an overvoltage condition is expected, it is recommended that the input current be limited to less than 10 mA.

SHUTDOWN OPERATION

Figure 49 shows the ADA4805-1 shutdown circuitry. To maintain very low supply current in shutdown mode, no internal pull-up resistor is supplied; therefore, the $\overline{\text{SHUTDOWN}}$ pin must be driven high or low externally and not be left floating. Pulling the $\overline{\text{SHUTDOWN}}$ pin to ≥1 V below midsupply turns the device off, reducing the supply current to 2.9 µA for a 5 V voltage supply. When the amplifier is powered down, its output enters a high impedance state. The output impedance decreases as frequency increases. In shutdown mode, a forward isolation of 62 dB can be achieved at 100 kHz (see Figure 49).

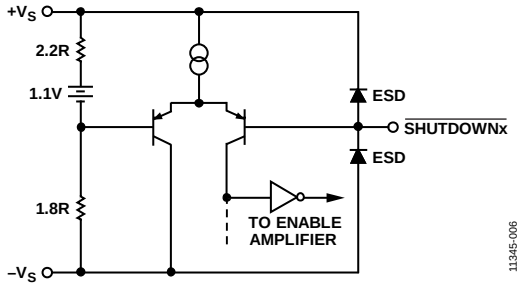


Figure 49. Shutdown Circuit

The $\overline{\text{SHUTDOWN}}$ pin is protected by ESD clamps, as shown in Figure 49. Voltages beyond the power supplies cause these diodes to conduct. For protection of the $\overline{\text{SHUTDOWN}}$ pin, ensure that the voltage to this pin does not exceed 0.7 V above the positive supply or 0.7 V below the negative supply. If an overvoltage condition is expected, it is recommended that the input current be limited with a series resistor to less than 10 mA. Table 8 summarizes the threshold voltages for the powered down and enabled modes for various supplies.

Table 8. Threshold Voltages for Powered Down and Enabled Modes

Mode	+3 V	+5 V	+5 V/–5 V	+7 V/–2 V
Enabled	>1.1 V	>1.9 V	>–0.9 V	>1.52 V
Powered Down	<0.7 V	<1.5 V	<–1.3 V	<1.52 V

NOISE CONSIDERATIONS

Figure 50 illustrates the primary noise contributors for the typical gain configurations. The total rms output noise is the root-mean-square of all the contributions.

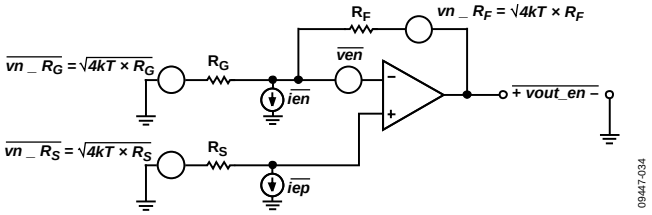


Figure 50. Noise Sources in Typical Connection

The output noise spectral density can be calculated by

$$\overline{VOUT\_EN} = \sqrt{4kTR_F + \left(1+\frac{R_F}{R_G}\right)^2\left[4kTRs + \overline{IEP}^2 R_S{}^2 + \overline{VEN}^2\right] + \left(\frac{R_F}{R_G}\right)^2 4kTR_G + \overline{IEN}^2 R_F{}^2}$$

where:

k is Boltzmann's constant.

T is the absolute temperature (degrees Kelvin).

$\overline{iep}$ and $\overline{ien}$ represent the amplifier input current noise spectral density (pA/√Hz).

$\overline{ven}$ is the amplifier input voltage noise spectral density (nV/√Hz).

R_S is the source resistance, as shown in Figure 50.

R_F and R_G are the feedback network resistances, as shown in Figure 50.

Source resistance noise, amplifier input voltage noise ($\overline{ven}$), and the voltage noise from the amplifier input current noise ($\overline{iep} \times R_S$) are all subject to the noise gain term ($1 + R_F/R_G$).

Figure 51 shows the total referred to input (RTI) noise due to the amplifier vs. the source resistance. Note that with a 5.9 nV/√Hz input voltage noise and 0.6 pA/√Hz input current noise, the noise contributions of the amplifier are relatively small for source resistances from approximately 2.6 kΩ to 47 kΩ.

The Analog Devices SiGe bipolar process makes it possible to achieve a low noise of 5.9 nV/√Hz for the ADA4805-1. This noise is much improved compared to other similar low power amplifiers with a supply current in the hundreds of microampere range.

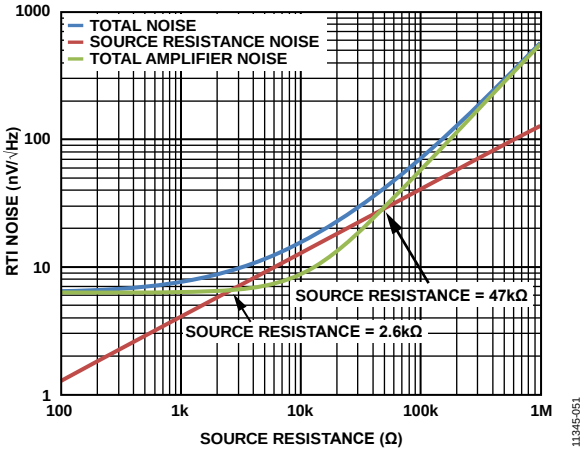


Figure 51. RTI Noise vs. Source Resistance

APPLICATIONS INFORMATION

SLEW ENHANCEMENT

The ADA4805-1 has an internal slew enhancement circuit that increases the slew rate as the feedback error voltage increases. This circuit allows the amplifier to settle a large step response faster, as shown in Figure 52. This is particularly useful in ADC applications where multiple input signals are multiplexed. The impact of the slew enhancement can also be seen in the large signal frequency response, where larger input signals cause a slight increase in peaking, as shown in Figure 53.

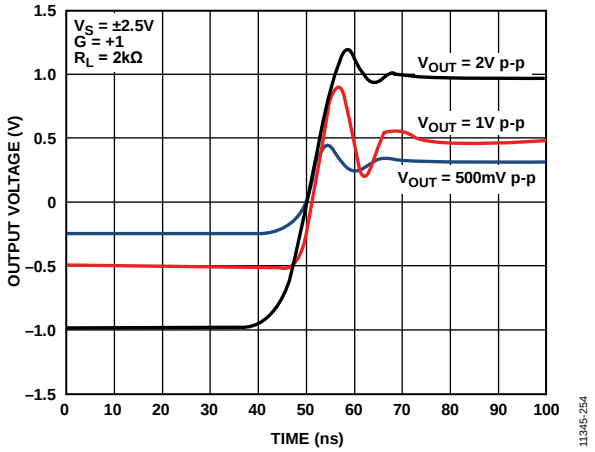


Figure 52. Step Response with Selected Output Steps

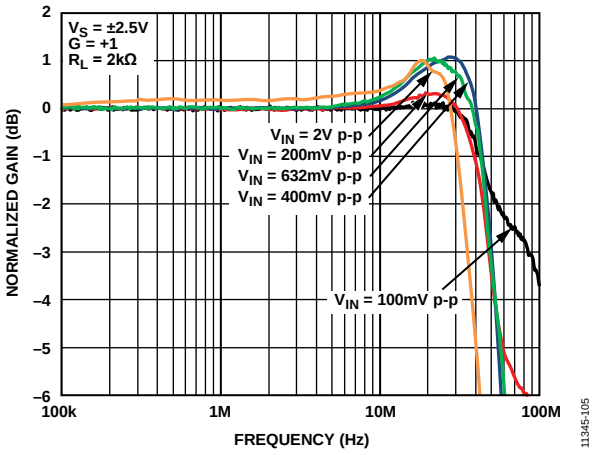


Figure 53. Peaking in Frequency Responses as Signal Level Changes, G = +1

EFFECT OF FEEDBACK RESISTOR ON FREQUENCY RESPONSE

Large feedback resistor contributes to peaking in the frequency response. This is due to the reduced phase margin imposed by the pole formed by the input capacitance of the amplifier, and the feedback network. Figure 54 shows the effect of peaking at selected feedback resistor values when the amplifier is configured as a gain of +2. This effect is easily mitigated by putting a feedback capacitor across the feedback resistor of the amplifier.

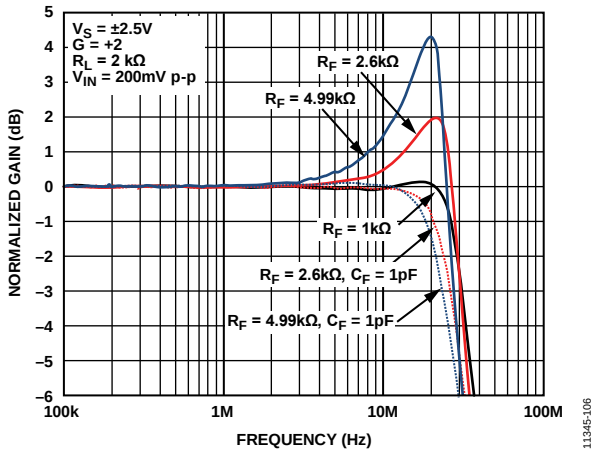


Figure 54. Peaking in Frequency Response at Selected R_F Values

COMPENSATING PEAKING IN LARGE SIGNAL FREQUENCY RESPONSE

Due to the slight peaking effect of the slew enhancement circuit at large outputs at higher frequencies, caution must be used when the amplifier is configured as a gain of +2 or higher because the feedback resistor R_F contributes to additional peaking (see the Effect of Feedback Resistor on Frequency Response section). Figure 55 shows that when the peaking is due to both the slew enhancement effect and the feedback resistor, the peaking can still be effectively reduced by a feedback capacitor.

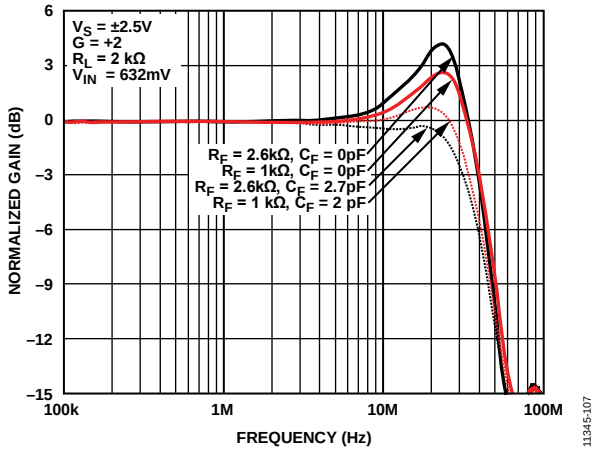


Figure 55. Using Feedback Capacitors to Mitigate Peaking

DRIVING LOW POWER, HIGH RESOLUTION SAR ADC

The main challenge of driving a low power, high resolution SAR ADC is to select a low power amplifier that can work in a single supply configuration and has noise and distortion such that it is capable of delivering the required linearity that is compatible with the chosen ADC. The ADA4805-1 has a noise of 5.9 nV/√(Hz) and a rail-to-rail output stage that helps minimizing distortion at large output. With its low power of 495 µA, it consumes power that is compatible with the low power SAR ADCs, which is usually in the microwatt (µW) to milliwatt (mW) range.

Furthermore, it supports a single-supply configuration; its input common range extends to 0.1 below the negative supply, and 1 V below the positive supply. These features make the ADA4805-1 a suitable candidate for driving low power, high resolution SAR ADCs.

Figure 56 shows a typical 16-bit single-supply application. The ADA4805-1 drives the AD7980, a 16-bit, 1 MSPS SAR ADC in a low power configuration. The AD7980 operates on a 2.5 V supply and supports an input from 0 V to V_{REF}. In this case, the ADR435 provides a 5 V reference. The ADA4805-1 is used both as a driver for the AD7980 and as a reference buffer for the ADR435.

The low-pass filter between the ADC driver and the ADC further limits the noise to the ADC (see Figure 56). The designer can reduce the corner frequency of the filter to remove additional noises, but note that this impacts the maximum input frequency allowed.

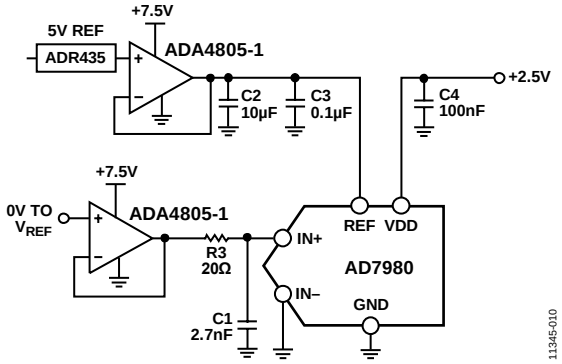


Figure 56. Driving the AD7980 with the ADA4805-1

In this configuration, the two ADA4805-1 consume 7.2 mW of quiescent power. The measured SNR, SINAD, and THD of the whole system for a 10 kHz signal are 89.9 dB, 103 dB, and 89.7 dB, respectively. This translates to an effective number of bits (ENOB) of 14.6 at 10 kHz, which is compatible with the AD7980 performance. Table 9 shows the performance of this setup at selected input frequencies.

DYNAMIC POWER SCALING

One of the merits of an SAR ADC like the AD7980 is that its power scales with the sampling rate. This makes it very power efficient, especially when the ADC runs at a low sampling frequency. However, the ADC driver used with the SAR ADC traditionally consumes constant power regardless of the sampling frequency. In other words, the power of the driver typically does not scale with the sampling rate of the system.

Figure 57 demonstrates how to scale the quiescent power of the driver with the sampling rate of the system. The conversion (CNV) signal is used as a trigger to generate a timing waveform that controls the $\overline{\text{SHUTDOWN}}$ pin of the ADA4805-1.

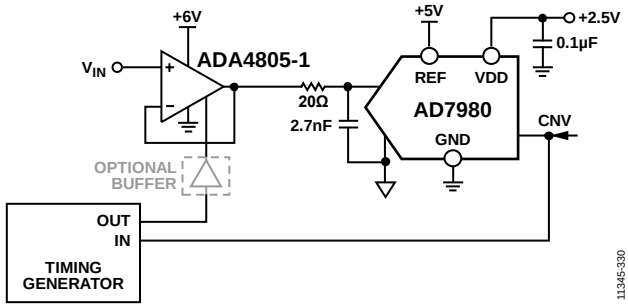


Figure 57. ADA4805-1/AD7980 Power Management Circuitry

Figure 58 illustrates the relative signal timing for power scaling the ADA4805-1 and the AD7980. To prevent any degradation in the performance of the ADC, the ADA4805-1 must exit its shutdown mode and have a fully settled output into the ADC input prior to the activation of the ADC CNV start signal. In this example, the amplifier is turned on to full power mode 3 µs prior to the start of the conversion signal, which is the minimum time needed for the amplifier output/ADC input to fully settle to 16 bits in acquisition mode. The $\overline{\text{SHUTDOWN}}$ pin of the ADA4805-1 is pulled low when the ADC input is inactive in between samples. The quiescent current of the amplifier falls to 10% of the normal operating value within 600 ns typically and settles to its final value of 3 µA by 1 µs maximum. Its output impedance is high in shutdown mode. This process is then repeated immediately after the amplifier is powered on again.

Table 9. System Performance at Selected Input Frequency for Driving the AD7980 Single-Ended

	ADC Driver		Reference Buffer		Results		
Input Frequency (kHz)	**Supply (V)**	**Gain**	**Supply (V)**	**Gain**	**SNR (dB)**	**THD (dBc)**	**SINAD (dB)**
1	7.5 and 0	1	7.5	1	89.8	103	89.6
10	7.5 and 0	1	7.5	1	89.4	104	89.3
20	7.5 and 0	1	7.5	1	89.9	103	89.7
50	7.5 and 0	1	7.5	1	88.5	99	88.1
100	7.5 and 0	1	7.5	1	86.3	93.7	85.6

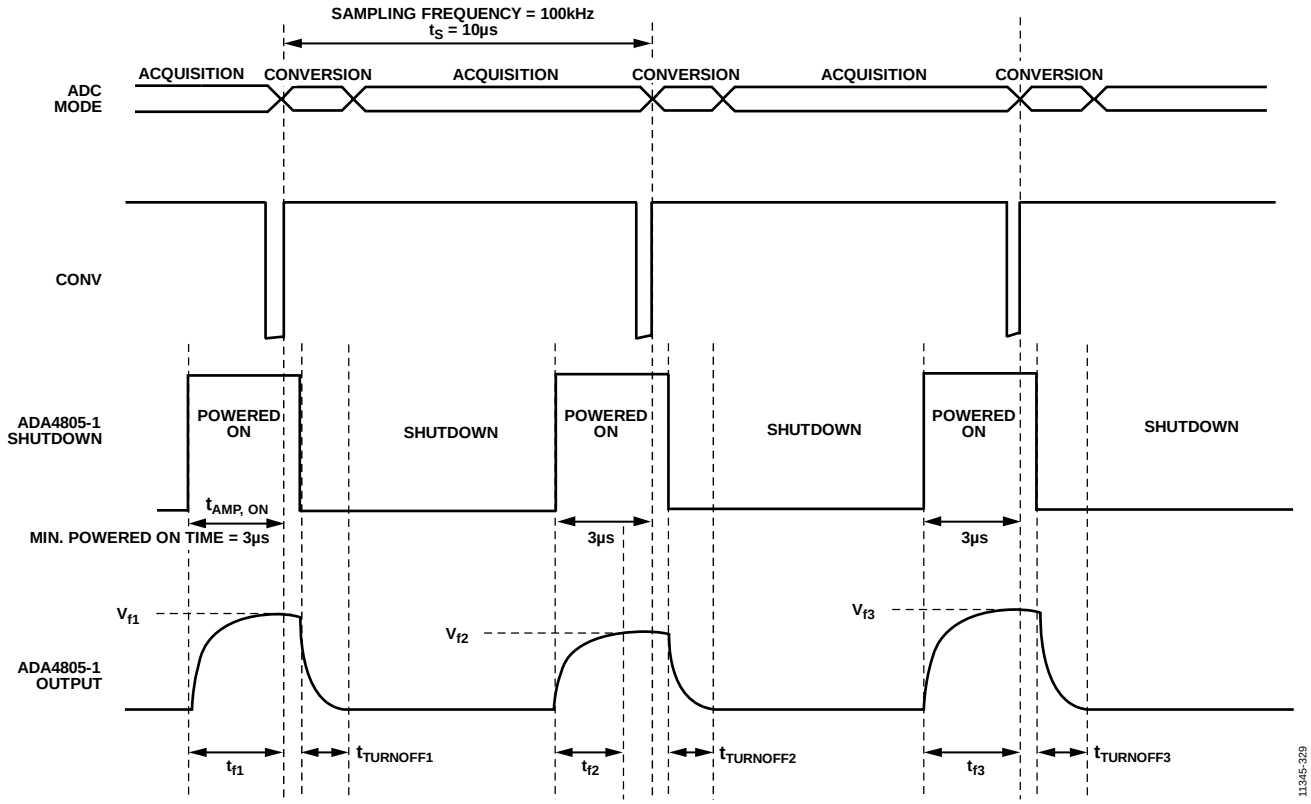


Figure 58. Timing Waveforms

Figure 59 shows the quiescent power of the ADA4805-1 with and without the power scaling. Without power scaling, the ADA4805-1 consumes constant power regardless of the sampling frequency as shown in Equation 1.

$$P_Q = I_Q \times V_S \quad (1)$$

With power scaling, the quiescent power becomes proportional to the ratio between the amplifier on time, $t_{AMP, ON}$, and the sampling time, t_S.

$$P_Q = I_Q \times V_S \times \frac{t_{AMP,ON}}{t_S} \quad (2)$$

Thus, by dynamically switching the ADA4805-1 between shutdown and full power modes between consecutive samples, the quiescent power of the driver scales with the sampling rate.

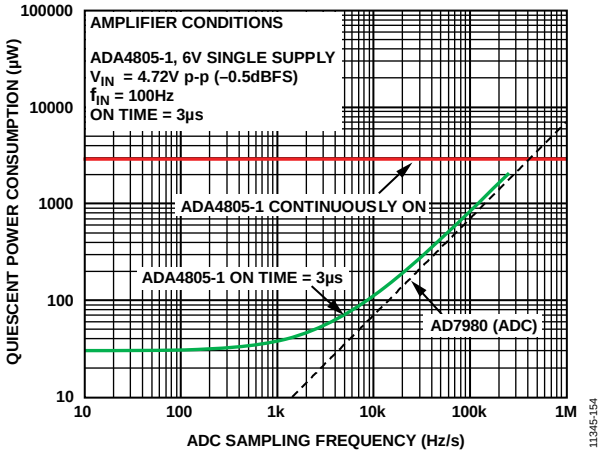


Figure 59. Quiescent Power Consumption of the ADA4805-1 vs. ADC Sampling Frequency

SINGLE-ENDED TO DIFFERENTIAL CONVERSION

Most high resolution ADCs have differential inputs to reduce common-mode noise and harmonic distortion. Therefore, it is necessary to use an amplifier to convert a single-ended signal into a differential signal to drive the ADCs.

There are two common ways the user can convert a single-ended signal into a differential signal: either use a differential amplifier, or configure two amplifiers as shown in Figure 60. The use of a differential amplifier yields better performance, whereas the 2-op-amp solution results in a lower system cost. The ADA4805-1 solves this dilemma of choosing between the two methods by combining the advantages of both. Its low harmonic distortion, low offset voltage, and low bias current means that it is able to produce a differential output that is well matched with the performance of the high resolution ADCs.

Figure 60 shows how the ADA4805-1 converts a single-ended signal into a differential output. The first ADA4805-1 is configured in a gain = +1 configuration. Its output is then inverted to produce the complementary signal. The differential output then drives the AD7982, an 18-bit, 1 MSPS SAR ADC. To further reduce noise, the user can reduce the values of R1 and R2. However, note that this increases the power consumption. The low-pass filter between the ADC driver and the ADC also limits the noise to the ADC. The user can reduce the corner frequency of the filter to remove additional noise, but note that this has an impact on the maximum input frequency allowed.

The measured SNR, THD, and SINAD of the whole system for a 10 kHz signal are 93 dB, 113 dB, and 93 dB, respectively. This translates to an effective number of bits (ENOB) of 15.2 at 10 kHz, which is compatible with the performance of the AD7982. Table 10 shows the performance of this setup at selected input frequencies.

Table 10. System Performance at Selected Input Frequency for Driving the AD7982 Differentially

	Results		
Input Frequency (kHz)	**SNR (dB)**	**THD (dBc)**	**SINAD (dB)**
1	93	104	93
10	93	113	93
20	93	110	93
50	92	102	91
100	89	96	88

LAYOUT CONSIDERATIONS

To ensure optimal performance, careful and deliberate attention must be paid to the board layout, signal routing, power supply bypassing, and grounding.

Ground Plane

It is important to avoid ground in the areas under and around the input and output of the ADA4805-1. Stray capacitance created between the ground plane and the input and output pads of a device is detrimental to high speed amplifier performance. Stray capacitance at the inverting input, together with the amplifier input capacitance, lowers the phase margin and can cause instability. Stray capacitance at the output creates a pole in the feedback loop, which can reduce phase margin and cause the circuit to become unstable.

Power Supply Bypassing

Power supply bypassing is a critical aspect in the performance of the ADA4805-1. A parallel connection of capacitors from each power supply pin to ground works best. Smaller value ceramic capacitors offer better high frequency response, whereas larger value ceramic capacitors offer better low frequency performance.

Paralleling different values and sizes of capacitors helps to ensure that the power supply pins are provided with a low ac impedance across a wide band of frequencies. This is important for minimizing the coupling of noise into the amplifier—especially when the amplifier PSRR begins to roll off—because the bypass capacitors can help lessen the degradation in PSRR performance.

Place the smallest value capacitor on the same side of the board as the amplifier and as close as possible to the amplifier power supply pins. Connect the ground end of the capacitor directly to the ground plane.

It is recommended that a 0.1 µF ceramic capacitor with a 0508 case size be used. The 0508 case size offers low series inductance and excellent high frequency performance. Place a 10 µF electrolytic capacitor in parallel with the 0.1 µF capacitor. Depending on the circuit parameters, some enhancement to performance can be realized by adding additional capacitors. Each circuit is different and must be analyzed individually for optimal performance.

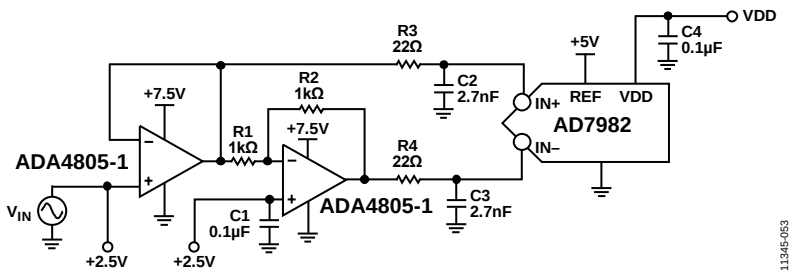
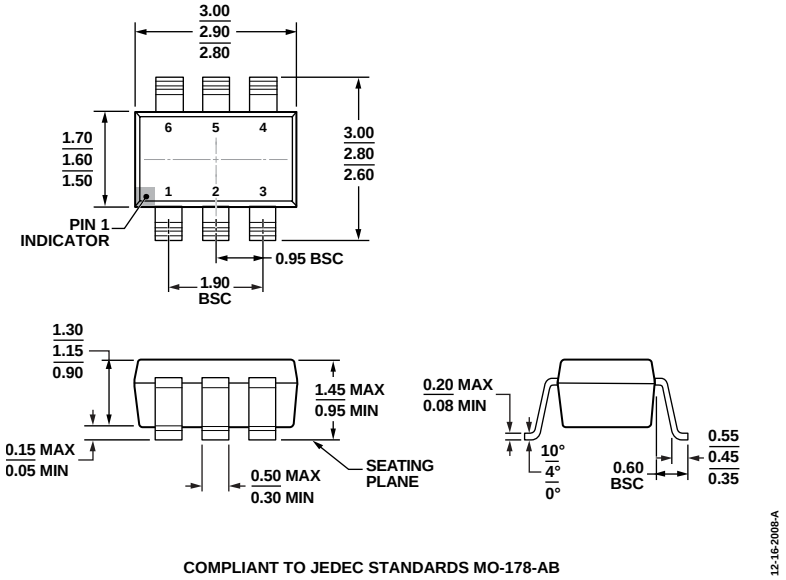


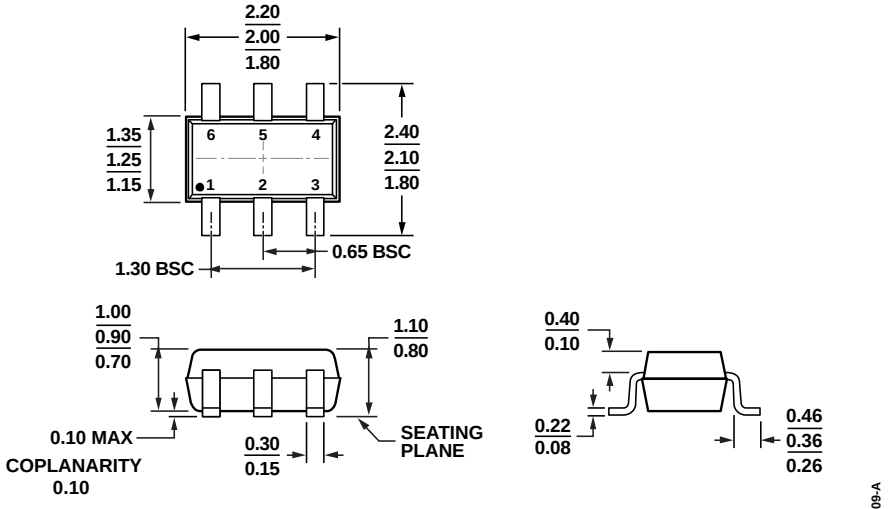
Figure 60. Driving the AD7982 with the ADA4805-1

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 61. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-203-AB

Figure 62. 6-Lead Plastic Surface-Mount Package [SC70]
(KS-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4805-1ARJZ-R2	−40°C to +125°C	6-Lead SOT-23	RJ-6	H3H
ADA4805-1ARJZ-R7	−40°C to +125°C	6-Lead SOT-23	RJ-6	H3H
ADA4805-1ARJZ-EBZ		Evaluation Board for 6-Lead SOT-23		H3H
ADA4805-1AKSZ-R2	−40°C to +125°C	6-Lead SC70	KS-6	H3H
ADA4805-1AKSZ-R7	−40°C to +125°C	6-Lead SC70	KS-6	H3H
ADA4805-1AKSZ-EBZ		Evaluation Board for 6-Lead SC70		

[1] Z = RoHS Compliant Part.

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ADA4805-1ARJZ-R7 ADA4805-1ARJZ-EBZ ADA4805-1AKSZ-EBZ