AD9162-FMC-EBZ Evaluation Board Quick Start Guide

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Getting Started with the AD9162-FMC-EBZ Evaluation Board and Software

WHAT'S IN THE BOX

AD9162-FMC-EBZ OR AD9162-FMCB-EBZ Evaluation Board(1)
Mini USB cable
Evaluation Board DVD

(1) The difference between these two version boards can be found in the boards difference section.

RECOMMENDED EQUIPMENT LIST

+12Vdc Power Supply
Dual Sinusoidal Clock Source (5GHz, <0.5ps RMS jitter)
Spectrum Analyzer

INTRODUCTION

The AD9162-FMC(B)-EBZ EVB connects to an ADS7-V1 or ADS7-V2 Pattern Generator to allow for quick evaluation of the AD9162, a high-speed, RF Digital to Analog converter (RF DAC). The ADS7 automatically formats the data and sends it to the AD9162 EVB, simplifying evaluation of the device. The Evaluation Board (EVB) runs from the FMC power supply.

The AD9162-FMC(B)-EBZ EVB can be driven by an external clock or the on-board clock, the ADF4355, as shown in Figure 1. There is one single pole, double throw (SPDT) switch on the board for selecting the clock source.

Figure 2 is an image of the top side of the AD9162-FMC(B)-EBZ. The board includes a clock buffer, the AD9508, which provides the reference clock and SYSREF to the ADS7 and the SYSREF signal to DAC.

AD9162-FMC(B)-EBZ EVALUATION SOFTWARE

The AD9162-FMC(B)-EBZ Evaluation Board software has an easy-to-use graphical user interface (GUI) called ACE (Analysis, Control, Evaluation). It is included on the Evaluation Board CD. This will install DPG Downloader (for loading vectors into the ADS7) and the AD9162 ACE SPI programmer application. The SPI programmer enables full access to the AD9162's register map, and has additional functionality such as the ability to record, load, and save macros, or register sequences, to ease programming of the device. The ADF4355 and AD9508 are also configured by ACE. Several macros or register sequences will be used by this guide to demonstrate the usefulness of the function and to ease the setup of the device. ACE also controls the SPDT switch for selecting the clock source.

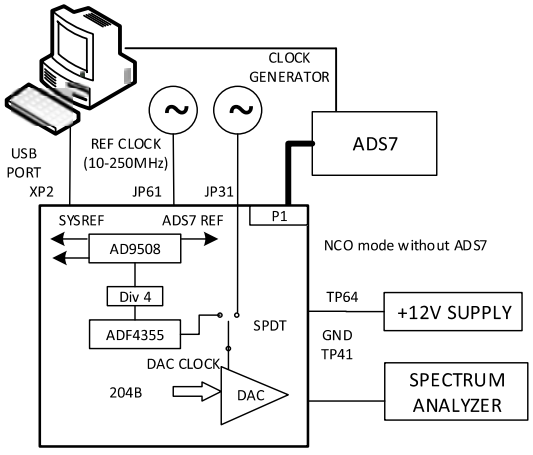

Figure 1. Block diagram of the AD9162-FMC(B)-EBZ lab bench set-up

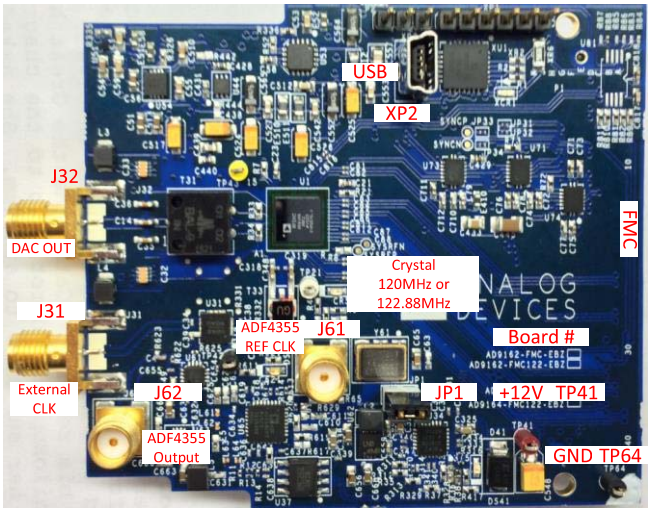

Figure 2. Top view of AD9162-FMC(B)-EBZ Evaluation Board

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HARDWARE SETUP

1. Use external signal generator as clock source

Remove the jumper on JP1. A low phase noise, high frequency clock source should be connected to the SMA connector, J31; and output level set to 0dBm. A second low phase noise, high frequency clock source (10MHz to 250MHz) with 0 dBm output level that is the reference clock of the ADF4355 should be connected to the SMA connector J61; the two clock sources should be synchronized. A unit such as the Rohde and Schwarz SMA100 has a convenient option for a secondary signal source, and using it will ensure the two clocks are synchronized. Or, the 10 MHz reference output of the signal generator can be used as the reference input. The spectrum analyzer should be connected to the SMA connector, J32.

Affix the AD9162-FMC(B)-EBZ Eval board to the ADS7-V1 using the connector circled in Figure 3. The ADS7-V2 has a single FMC connector and the AD9162-FMC(B)-EBZ Eval board should be connected to it.

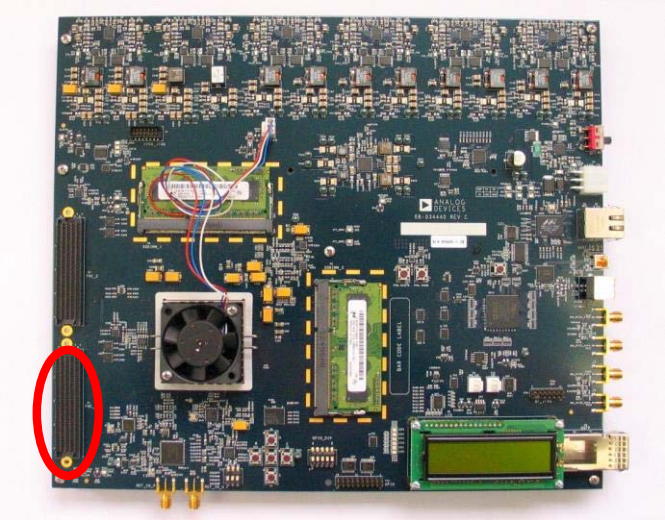

Figure 3. View of the top of the ADS7-V1 pattern generator board

2. Use on-board ADF4355 as clock source

Put the jumper on JP1. And connect the spectrum analyzer to the SMA connector, J32

Affix the AD9162-FMC(B)-EBZ Eval board to the ADS7-V1 using the connector circled in Figure 3. The ADS7-V2 has a single FMC connector and the AD9162-FMC(B)-EBZ Eval board should be connected to it.

3. DC TEST/NCO mode without ADS7

The AD9162 can work in DC TEST/NCO mode without ADS7, but it has to run from an external power supply. Connect +12V to TP64 (red), GND to TP41 (black). The external power supply should have capacity for 1A of current. Put the jumper on JP1 if using the on-board ADF4355 as the clock source. If using an external clock source, connect a low phase noise, high frequency clock source to J31. And connect the spectrum analyzer to the SMA connector, J32

The PC should be connected to the EVB using the mini-USB connector XP2 after installation of the Evaluation Board software. The PC also should be connected to the ADS7 through its USB connector. **Do not connect these USB connectors until after the software has been loaded onto the PC.**

GETTING STARTED

The PC software comes on the included Evaluation Board DVD. The installation will include an updated version of the DPG Downloader software as well as all the necessary AD9162-FMC(B)-EBZ files including schematic, board layout, data sheet, SPI programmer, and other files.

Initial Set-Up

Install the DPG Downloader and AD9162 software and support files on your PC by running the "autorun.exe" program. It will appear as in Figure 4. Run both of the indicated files, one for the DAC Software Suite and the other for the ACE installer.

Figure 4. Entry screen of the installer program for the DAC Software Suite and ACE installer

It is suggested that the basic set-up is verified before making any modifications to the evaluation board.

Several different configurations and scenarios will be described in this Quick Start guide, with step-by-step instructions for each one of them. Not all need to be completed, but rather choose the scenario(s) which is/are desired to be evaluated and follow the instructions. A summary software User's Guide is at the end of the start-up scenarios.

DC TEST/NCO MODE

Configure Hardware

The spectrum analyzer can be configured with Start Frequency = 50 MHz, Stop Frequency 5 GHz, and Resolution Bandwidth of 300 kHz. Use an Average/RMS detector setting, and choose Input Attenuation to be 6 dB. This can be adjusted later if indications are that the analyzer is causing degradations (warnings on the analyzer itself, or third order products appearing on the output spectrum.).

Configure the AD9162-FMC(B)-EBZ Evaluation Board

1. Open the ACE software, which is located in Start->Programs->Analog Devices->ACE->ACE. The screen will appear similar to Figure 5 below. ACE is the software that is used to load the registers in the AD9162. The ACE software enables full access to the AD9162 register map, and also has several views and features that simplify its use. Many of the ACE software features will be covered in the ACE Software User's Guide section. This section will focus on what is necessary to start-up the AD9162 in DC TEST/NCO mode.

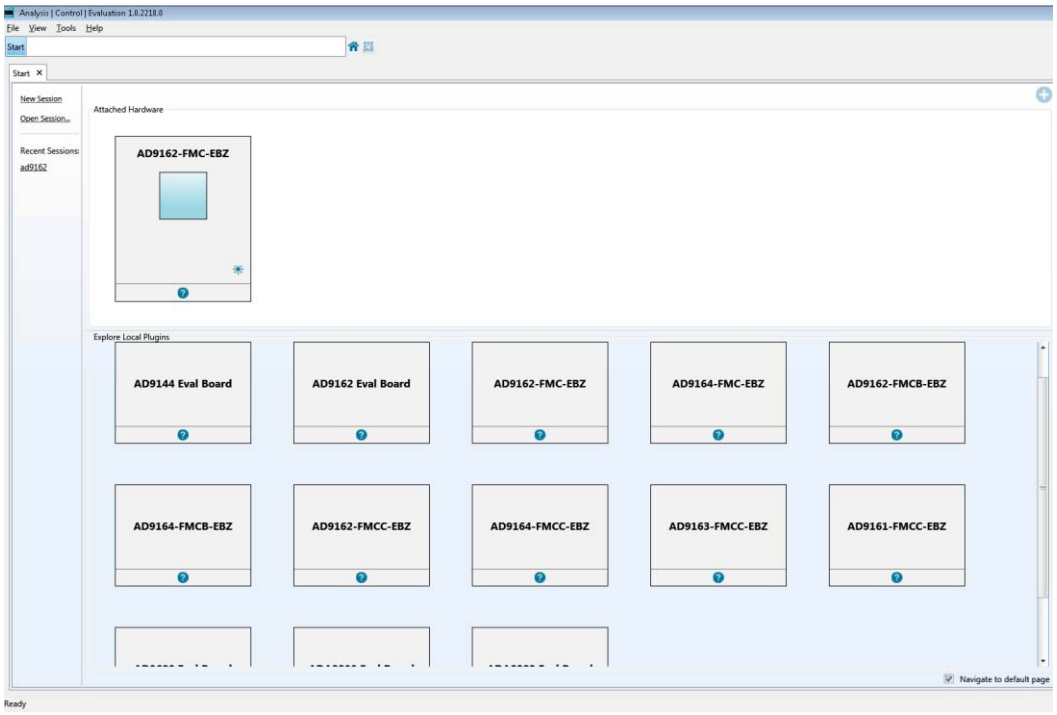

Figure 5. The entry screen of the ACE SPI programmer software

2. Open the board view by double clicking on the AD9162 Eval Board area, then select clock source as shown in Figure 6.

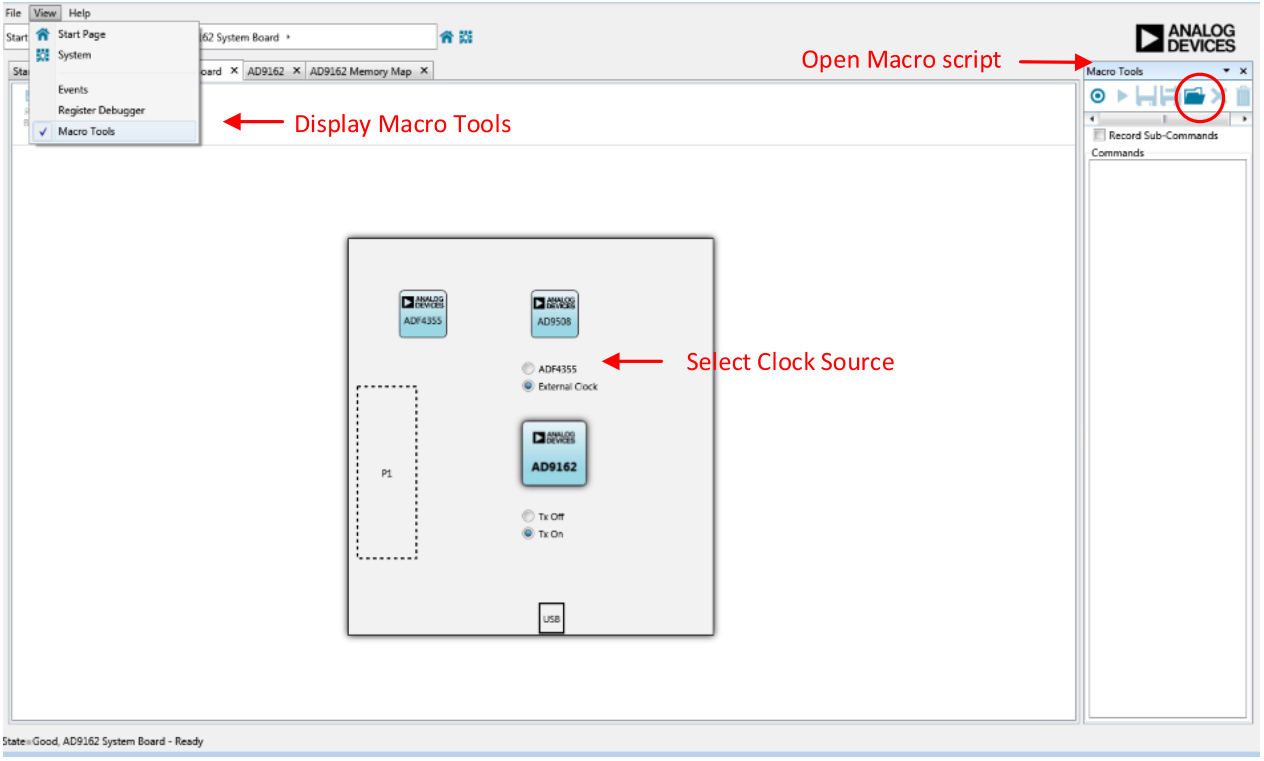

Figure 6. AD9162 Eval Board View and Clock Source Selection in ACE

3. Open the file called "AD916x_Initial_Worksheet.xlsx". It will look like Figure 7 . Follow the three steps in the file and save the Macro script into one file (file name example: AD9162_Script.adimacro). Notes that correct board number MUST be selected

in step 1. DC TEST mode can be enabled by setting register 0x150[1] to 1. And interpolation ratio must be 1 in DC TEST mode. The output amplitude can be changed by register 0x14F and 0x14E. The output frequency is set by NCO.

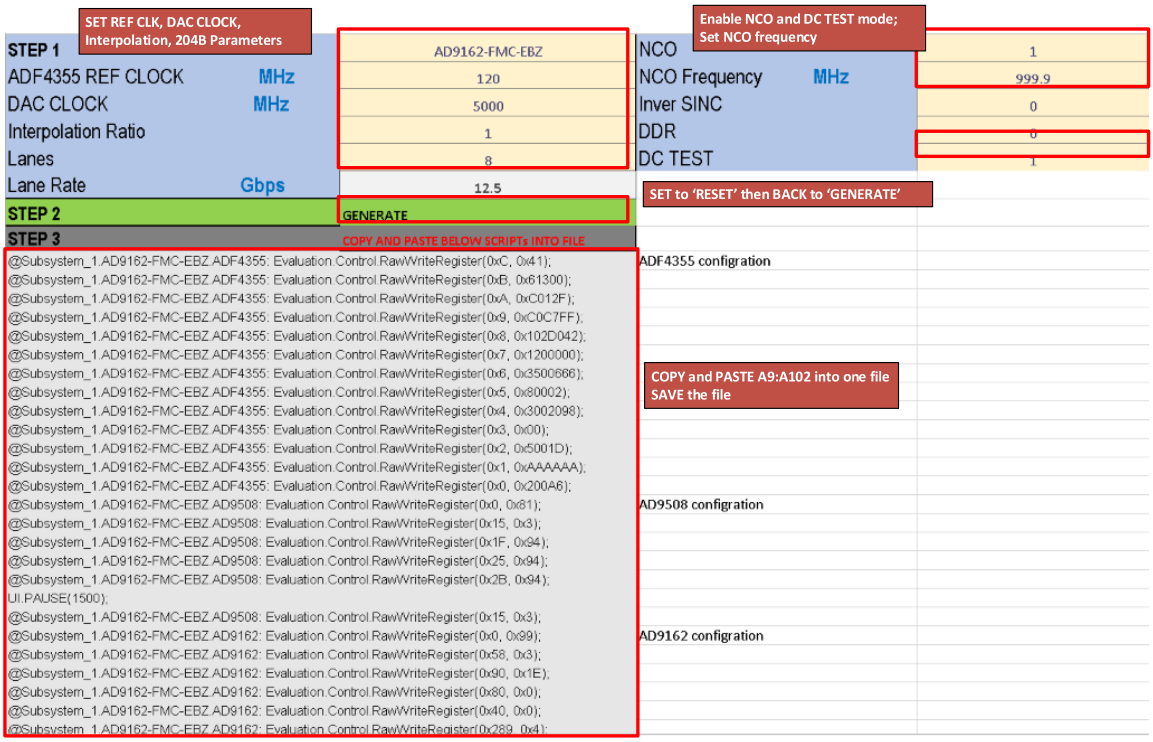

Figure 7. AD9162 Initialization Worksheet

4. Go to the macro section on the right and click on the "Open Macro" icon (folder opening) as shown in Figure 6. In the Open Macro dialog, navigate to the file that is saved in step 3, and click "Open". A series of register writes will appear below the control.
5. Press the "Play" (right-pointing triangle) button, and all of the black register writes should turn green as they are successfully executed as shown in Figure 8.

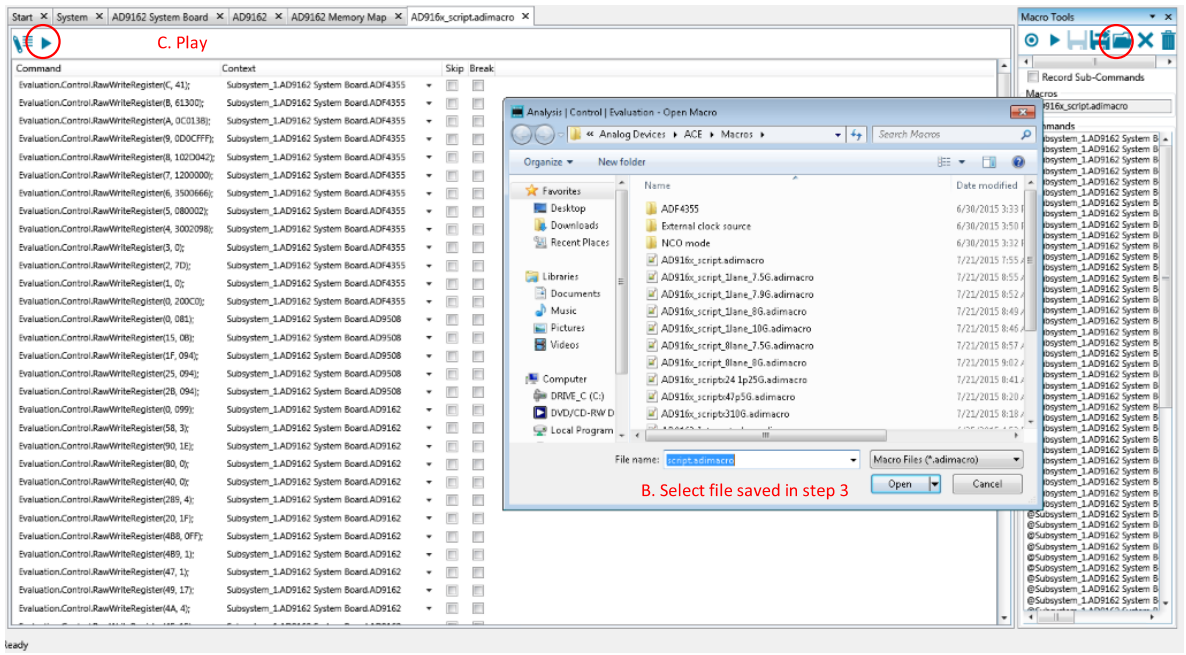

Figure 8. Run Macro Script

6. A 1 GHz single tone should now appear on the spectrum analyzer as shown in Figure 9. Change the NCO frequency and repeat step 3 to step5 for getting different DAC output.

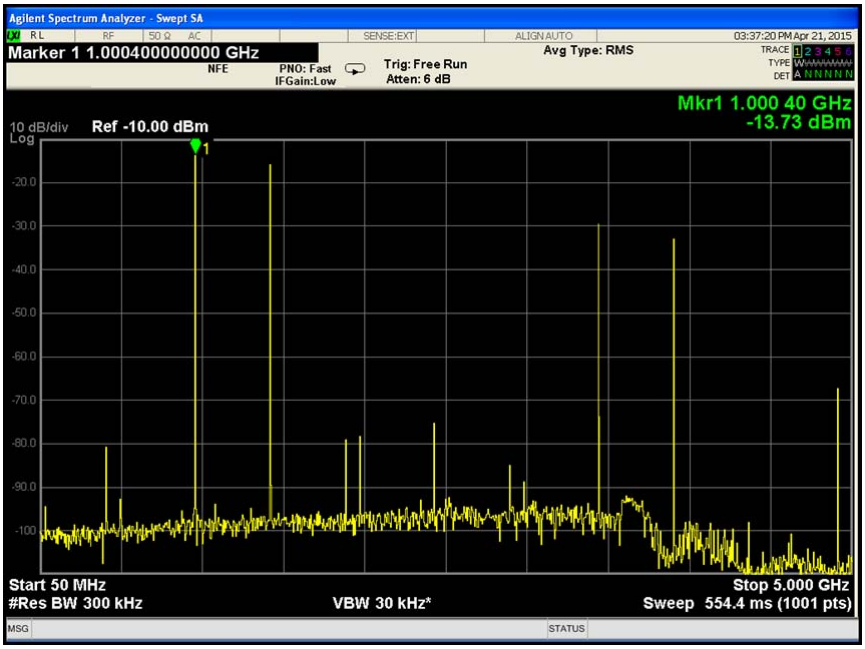

Figure 9. Spectrum Analyzer plot of DAC output in NCO mode, showing single tone at 1 GHz

USING THE ADS7 TO PLAY A PATTERN TO THE AD9162-FMC(B)-EBZ

Configure Hardware

Configure the hardware according to the hardware set-up instructions given in the Hardware Setup section above.

The spectrum analyzer can be configured with Start Frequency = 50 MHz, Stop Frequency 5 GHz, and Resolution Bandwidth of 300 kHz. Use an Average/RMS detector setting, and choose Input Attenuation to be 6 dB. This can be adjusted later if indications are that the analyzer is causing degradations (warnings on the analyzer itself, or third order products appearing on the output spectrum.).

Load and Play Pattern to the ADS7

Open DPGDownloader (Start > Programs > Analog Devices > DPG > DPGDownloader). Ensure that the program detects the AD9162, as indicated in the "Evaluation Board" drop-down list, and select it. For this evaluation board, JESD204B is the only valid Port Configuration, and it will be selected automatically. The "Lane Rate" window may not yet show a clock frequency, but it normally does. In the lower portion of the screen, choose Subclass '0'. The screen should look like Figure 10. The SYNC Status may show a Green check mark or a Red "X". It is irrelevant at this point.

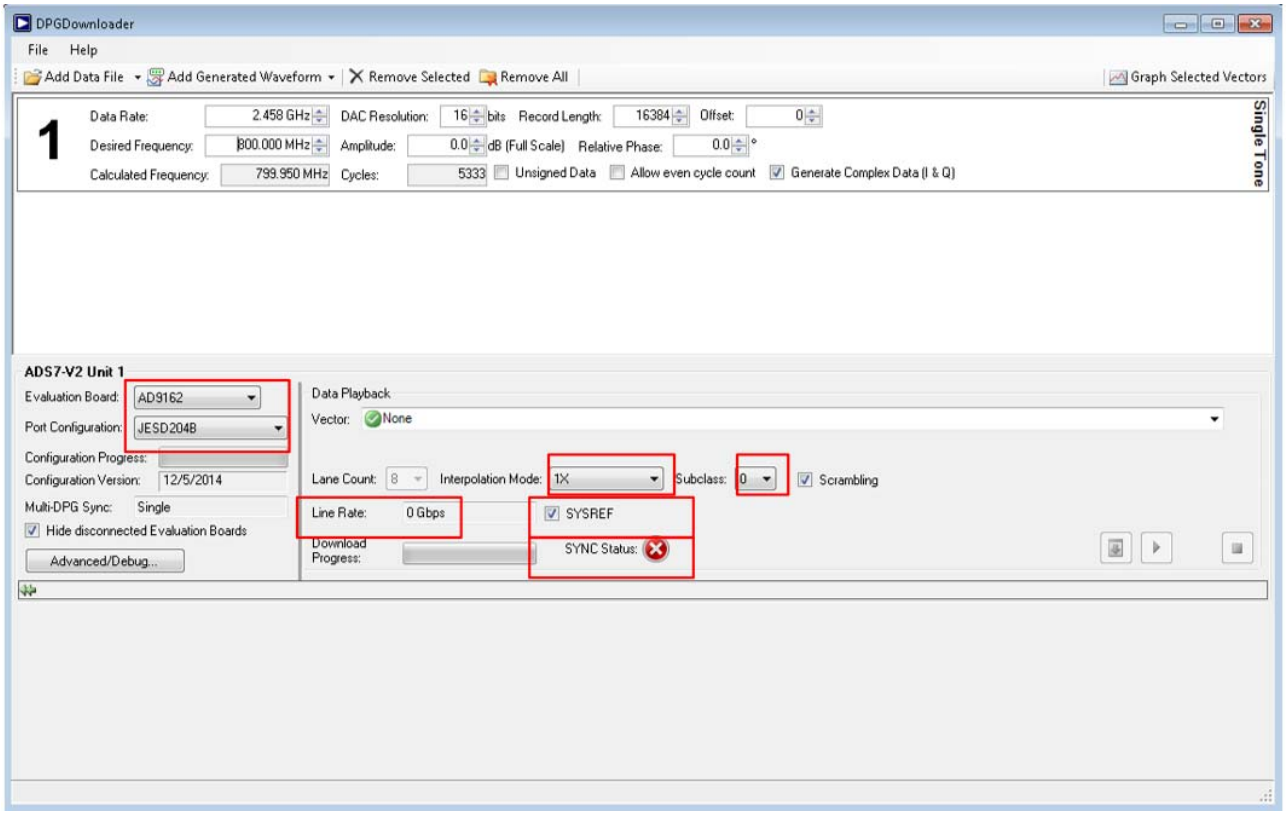

Figure 10. Initial screen of DPG Downloader when configured for AD9162

Click on "Add Generated Waveform", and then "Single Tone", as shown in Figure 11. A single tone panel will be added to the vector list. Enter the sample rate, or DAC clock frequency in this case, 2.4576 GHz. Next, choose the "Resolution" to be 16 bits. Choose a center frequency of 800 MHz. Keep "Amplitude" as 0 dB. Uncheck the "Unsigned Data" check box because the AD9162 only accepts 2's Complement data. The signal should appear on the list of signals as shown in.

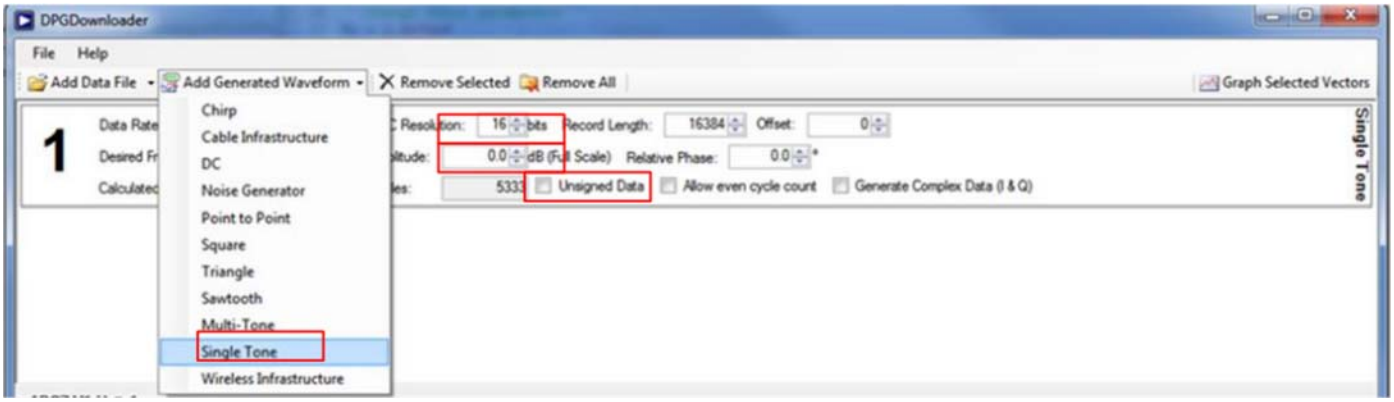

Figure 11. Choose "Single Tone" as the vector type

Next, in the lower portion of the screen, select ""1: Single Tone – 799.950 MHz; 0.0 dB; 0.0°" as the Data Vector. The other options can be left at their default values. The "SYNC Status" may show as the red "X" as in Figure 12.

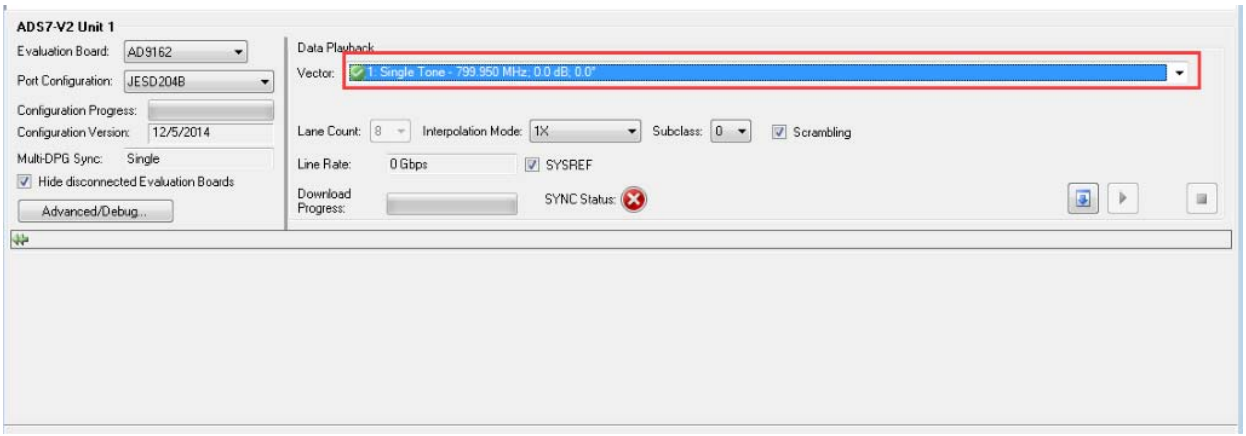

Figure 12. DPG Downloader Lower section, used to select the desired vector and download it to the ADS7 unit

Make sure the ADS7 unit is powered up and the AD9162 eval board is plugged into it correctly. Click the button to download the pattern from the computer to the ADS7 unit, wait for the Play ( ) button to become active, and then click the Play ( ) button to begin vector playback to the AD9162.

Configure the AD9162-FMC(B)-EBZ Evaluation Board

1. Open the ACE software, which is located in Start->Programs->Analog Devices->ACE->ACE. The screen will appear similar to Figure 13 as below. ACE is the software that is used to load the registers in the AD9162. The ACE software enables full access to the AD9162 register map, and also has several views and features that simplify its use. Many of the ACE software features will be covered in the ACE Software User's Guide. This section will focus on what is necessary to start-up the AD9162 in JESD mode.

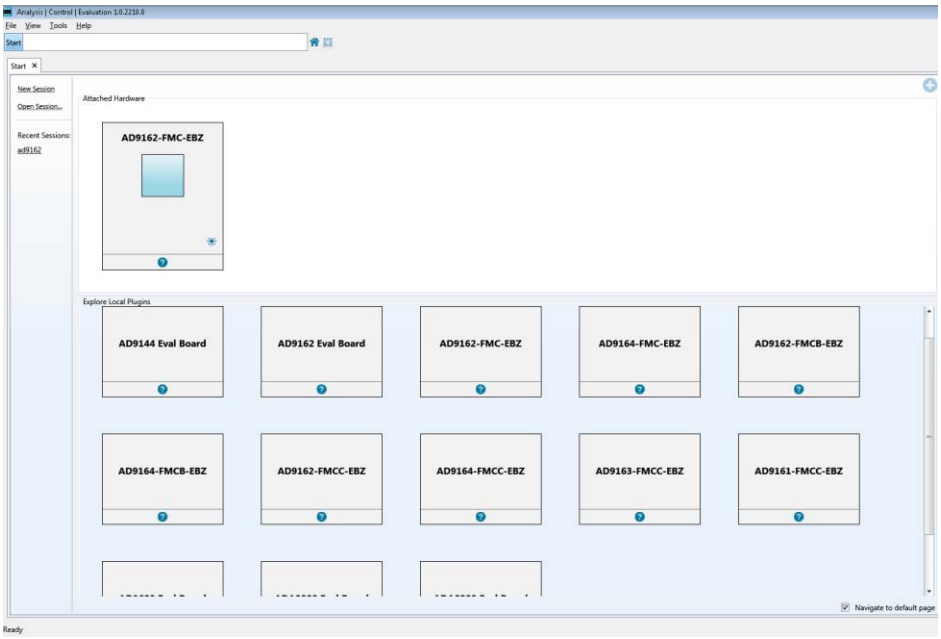

Figure 13. The entry screen of the ACE SPI programmer software

1. Open the board view by double clicking on the AD9162 Eval Board area, then select clock source as shown in Figure 14.

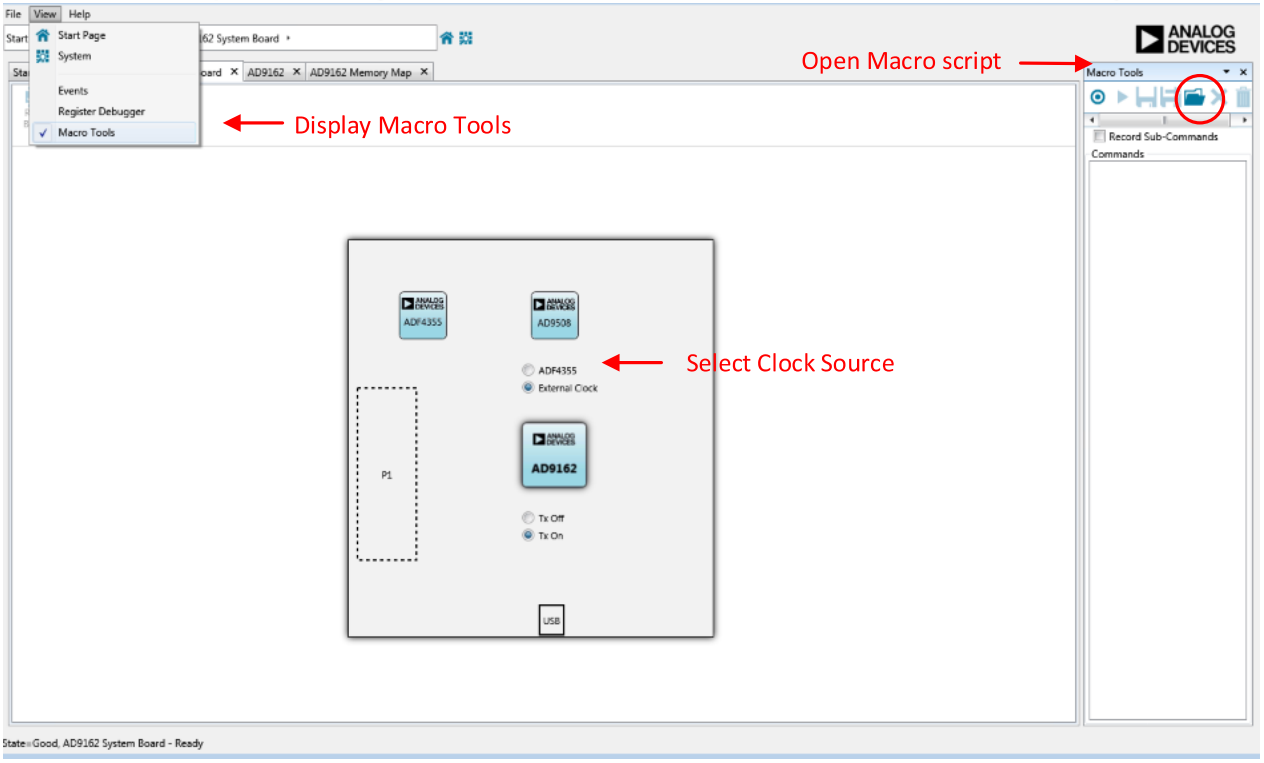

Figure 14. AD9162 Eval Board View and Clock Source Selection in ACE

2. Open the file called "AD916x_Initial_Worksheet.xlsx". It will look like Figure 15. Follow 3 steps in the file and save Macro script into one file (file name example: AD9162_Script.adimacro).

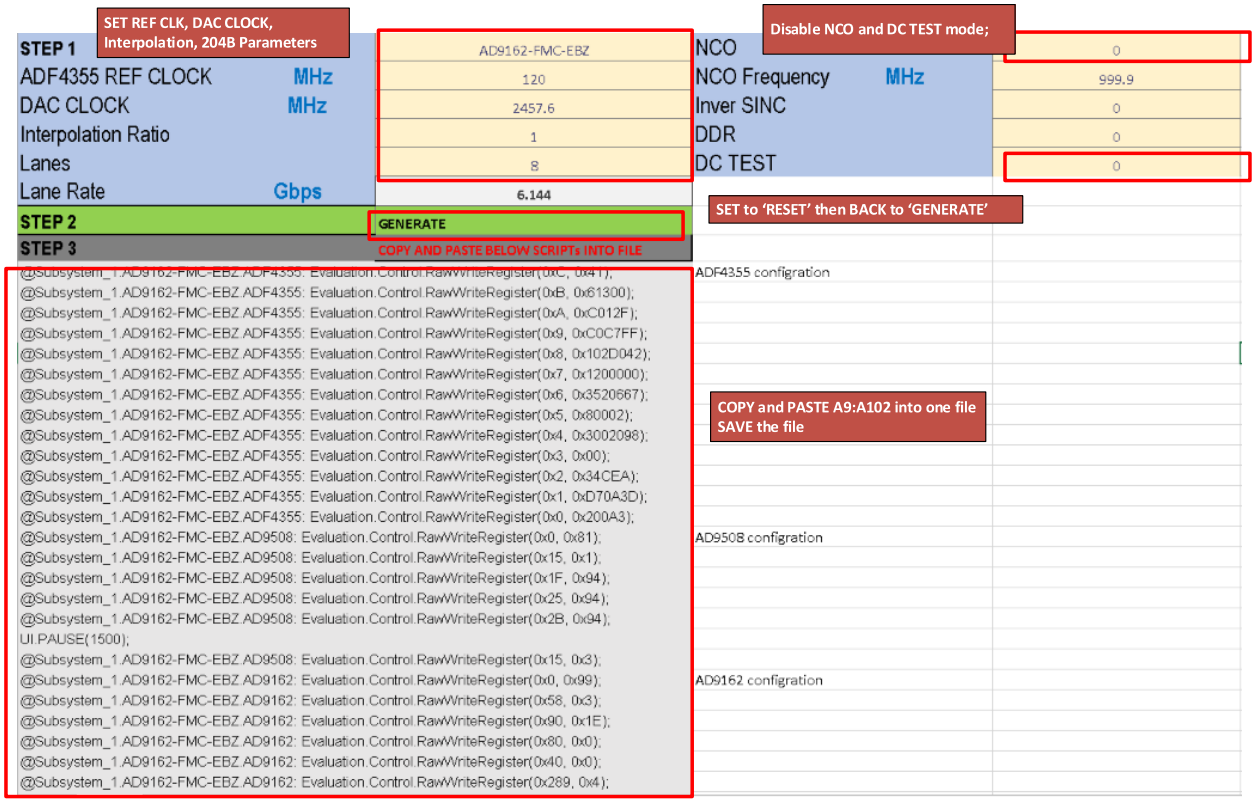

Figure 15. AD9162 Initialization Worksheet

3. Go to the macro section on the right and click on the "Open Macro" icon (folder opening) as shown in Figure 16. In the Open Macro dialog, navigate to the file that was saved in the last step, and click "Open". A series of register writes will appear below the control.
4. Press the "Play" (right-pointing triangle) button, and all of the black register writes should turn green as they are successfully executed as shown in Figure 16.

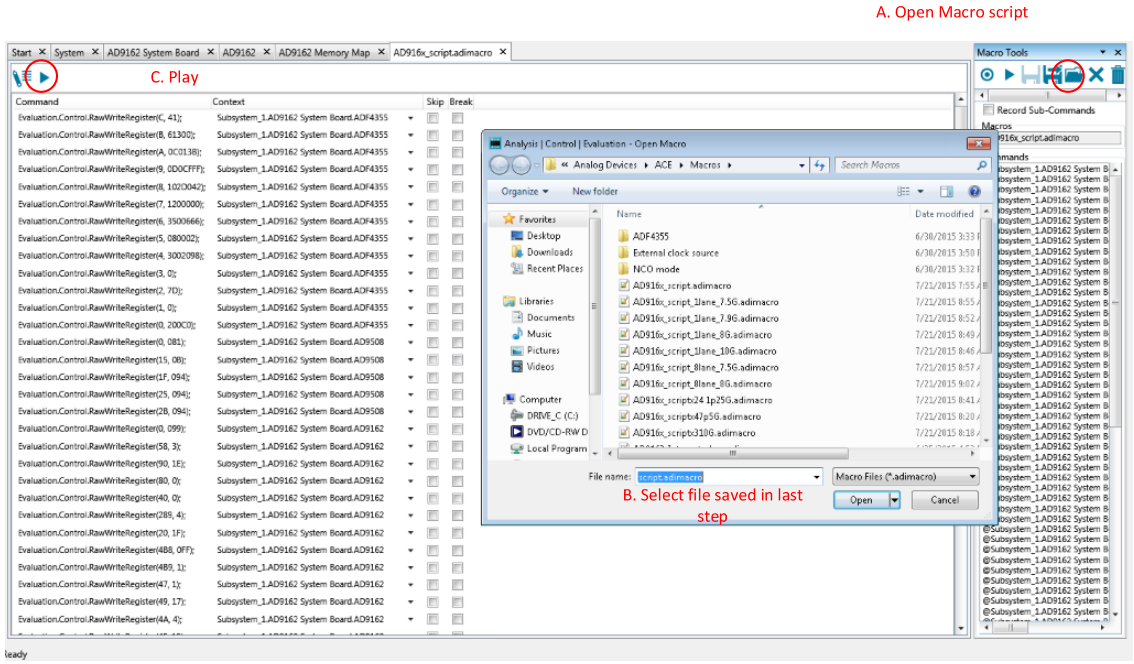

Figure 16. Run Macro Script

5. At this point, the session can be saved using File->Save Session so that this view can be opened directly in future.
6. The Lane Rate frequency from the AD9162 should be reported as 6.144 Gbps as shown in Figure 17. The "SYNC Status" should show as the green check mark.

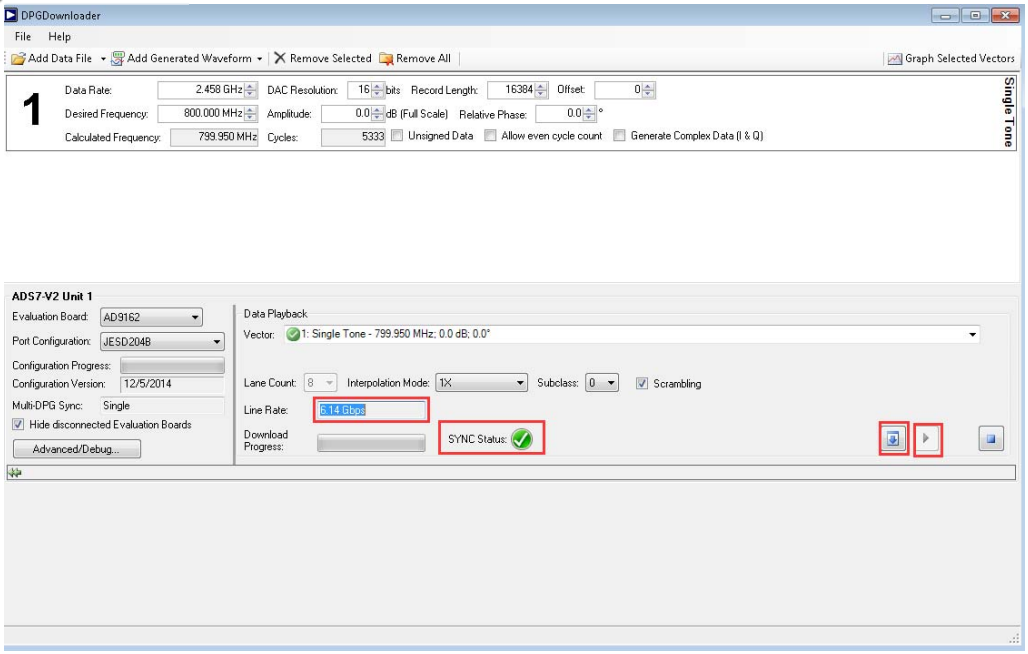

Figure 17. Download single tone and play it

7. An 800 MHz single tone should now appear on the spectrum analyzer as shown in Figure 18.

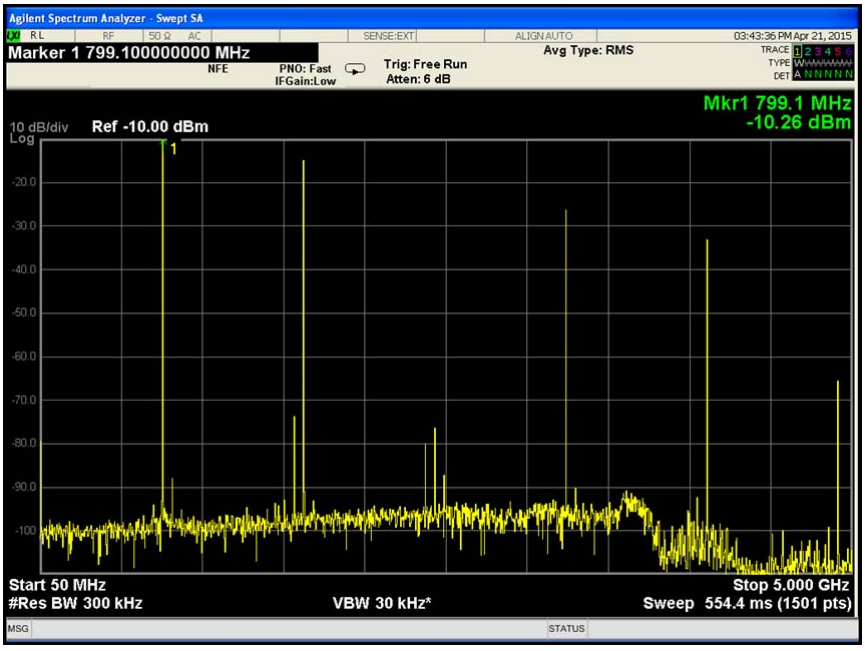

Figure 18. Spectrum Analyzer plot of DAC output in JESD 8-lane, 1x mode, showing single tone at 800 MHz

8. The frequency of the tone can be changed either by
   a. enabling the NCO in register 0x111 and
   b. entering a frequency tuning word in registers 0x114 – 0x119 and
   c. setting the "FTW update" bit in register 0x113, or

d. the user can choose a new frequency for the DPG Downloader vector generator to create, and re-download the vector.

The re-download may momentarily bring the JESD link down, but the link should recover and re-sync and the new output frequency should be observed on the spectrum analyzer.

9. Other vectors can also be generated and downloaded in a similar manner once the JESD link is up.
10. If the user want to run new setting like different clock rate, interpolation ratio, lanes and reference clock, just go to "AD916x_Initial_Worksheet.xlsx", repeat step 2 to step 7.
11. For debugging suggestions in case the link does not come up, see the Errors section.
12. If the interpolation ratio configured in the "AD916x_Initial_Worksheet.xlsx" is bigger than 1, DPG Downloader configuration shall be changed as well as shown in Figure 19 . The data type is complex and interpolation mode is set to ">1x".

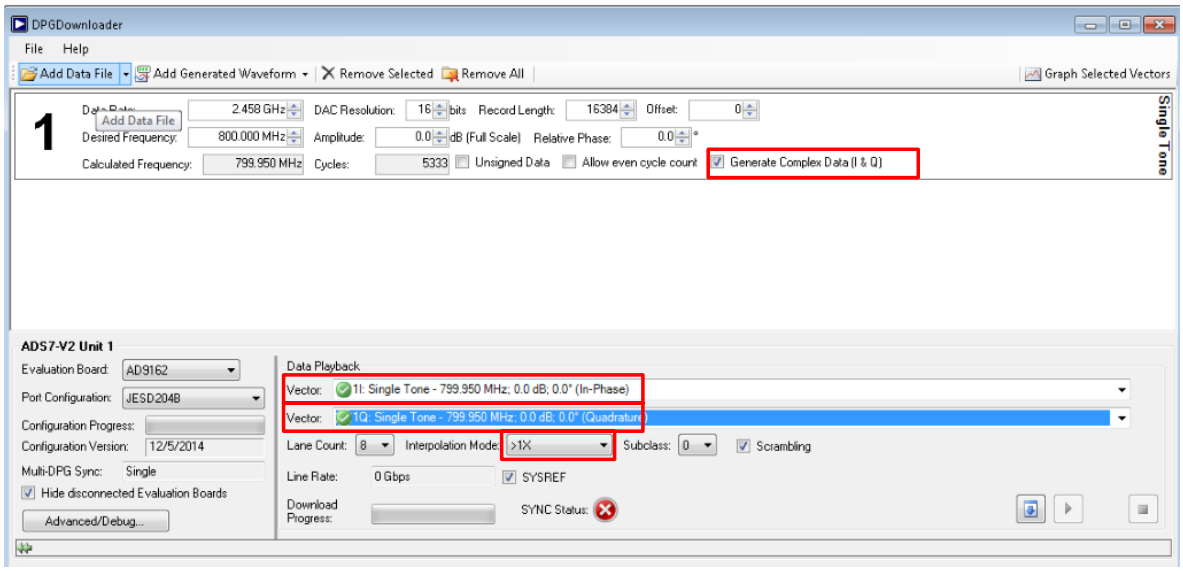

Figure 19. DPG Downloader when configured for interpolation ratio >1

EVALUATION BOARDS DIFFERENCE

The difference between AD9162-FMC-EBZ and AD9162-FMCB-EBZ is DAC output Balun. AD9162-FMC-EBZ uses Marki BAL-0009SMG.AD9162-FMCB-EBZ uses Mini-Circuits TC1-1-13MA+ or TC1-1-43A+. The insertion loss, phase mismatch and amplitude mismatch of these Baluns are different at same frequency, so the DAC output fundamental amplitude response and spurs level can be slightly different. The Typical fundamental amplitude responses (without cable calibration) are shown in Figure 20.

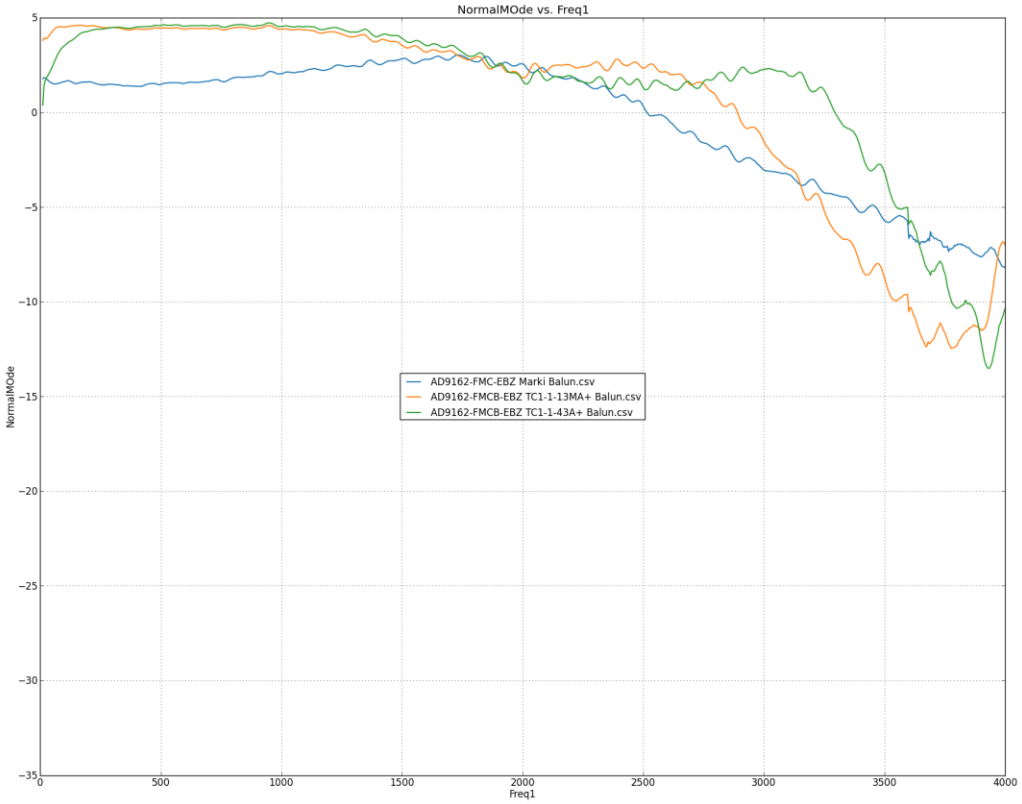

Figure 20 Typical fundamental amplitude responses of AD9162-FMC(B)-EBZ boards

ADF4355 PEFORMANCE OPTIMIZATION

The user can measure the ADF4355 performance by the SMA J62 as shown in Figure 2. The loop filter on the board is standard Type II, third order low pass filter. The user can customize and optimize the filter by ADIsimPLL.
https://form.analog.com/Form_Pages/RFComms/ADISimPll.aspx

The ADF4355 register setting generated by "AD916x_Initial_Worksheet.xlsx" is a typical one. The user can use standalone ADF4355 tools (http://www.analog.com/media/en/evaluation-boards-kits/evaluation-software/ADF4355_v0_53_3.zip) to regenerate new ADF4355 settings and put them into the Macro script. How to update ADF4355 configuration is shown in Figure 21.

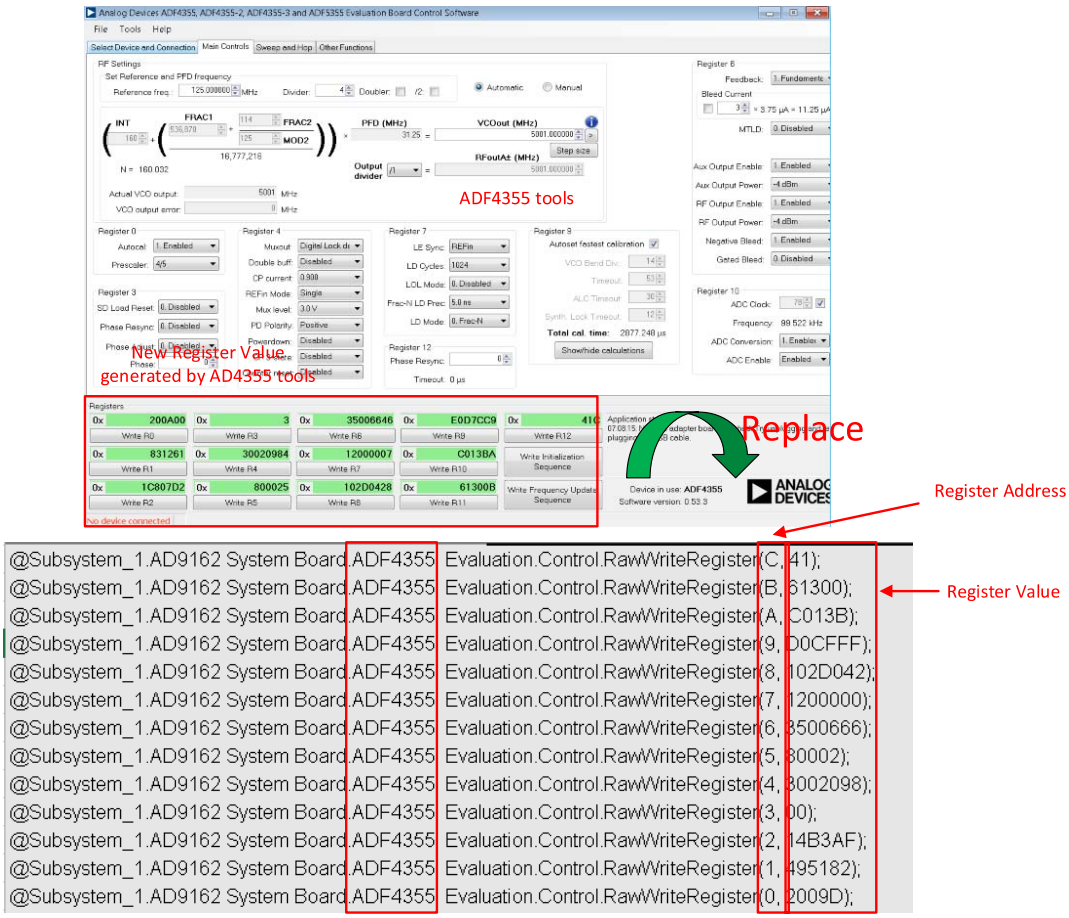

Figure 21. Optimize ADF4355 performance

The ADF4355 PFD spur level is PFD frequency related. Lower PFD frequency can help reduce PFD spur, which also narrows the loop filter bandwidth and affects PLL output phase noise. The PFD frequency used in 'AD916x_Initial_Worksheet.xlsx 'is from 20MHz to 50MHz. The user can choose the PFD frequency according to the phase noise requirement and PFD spur requirement.

KNOWN ISSUES

There is a divide- by-4 divider (HMC362) on the board for providing reference clock to FPGA. The divider causes ½ DAC clock rate spur to be shown on the ADF4355 output. i.e. there is a 2.5GHz spur on ADF4355 output if DAC clock rate is set to 5GHz. The spur level is around -55 dBc. The ½ DAC clock rate spur can mix with DAC output to generate two new spurs (Fout+/- ½ CLK) if using ADF4355 as clock source.

The user may see these two additional spurs (Fout+/- ½ CLK) at DAC output. But these two spurs are not caused by DAC. They disappear with external clock instead. Figure 22 is one example to show DAC spur differences between on-board clock ADF4355 and external clock. The spur in the red circle is at ½ FDAC-Fout.

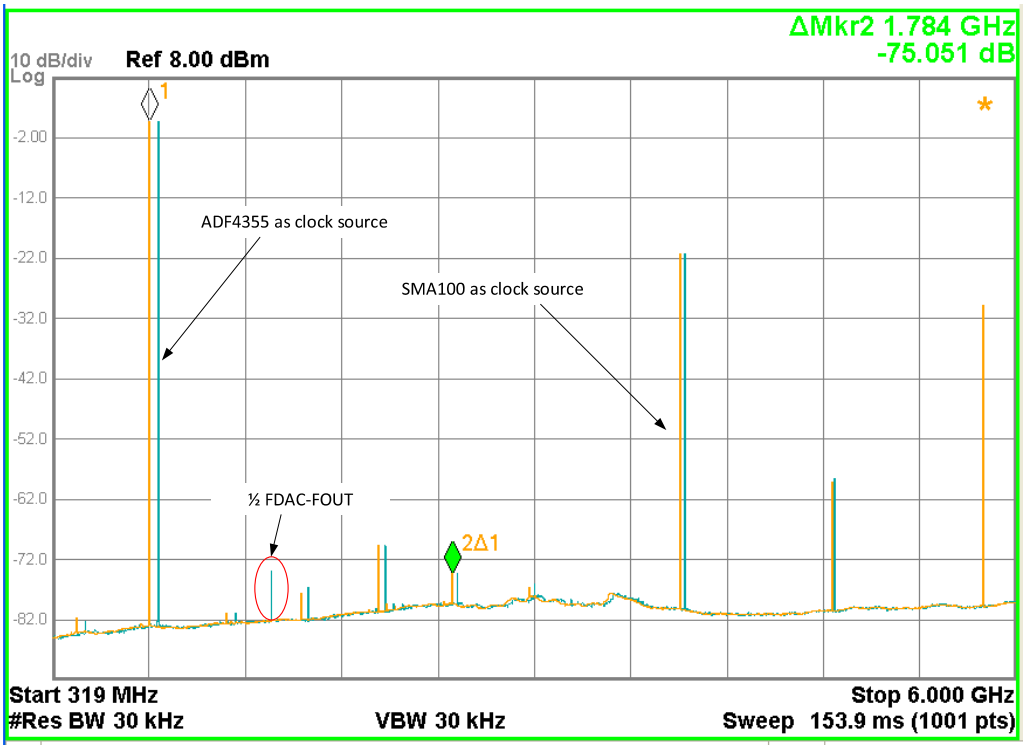

Figure 22. DAC output spur differences with different clock sources, ADF4355 and external clock SMA100

ACE USER'S GUIDE

A comprehensive User's Guide for the ACE software can be found on Analog Devices' Wiki site here: http://wiki.analog.com/resources/tools-software/ace .

A quick guide to the AD9162 "plug-in" for ACE is given here. For any general information relating to the ACE tool itself, please consult the ACE user's guide on the ADI Wiki.

A picture of the ACE software screen is shown in Figure 23. In this view, the tabs for the ADS7+AD9162 eval boards, the AD9162-FMC(B)-EBZ eval board, the AD9162 device, and the AD9162 Memory Map are shown near the red (1) in a circle, along with three tabs for each of the start-up scripts used in this Quick Start guide. The user can click on each tab to navigate to the various windows.

At the red (2) in a circle, the memory map view as registers or bit fields can be chosen. In Registers view, the full registers are shown, and in the area below the red (4), some registers have been expanded to show the bit field names and the detail that is possible to see. In the Bit Field view, the bit fields are listed alphabetically and have some "widgets" to control them and set bits, whereas in the Register view, the control is by bit or hex word. Both views can program the registers and it is merely user preference which is more convenient to use.

At the red (3) is the Functional Group view. Because the AD9162 has a large register map, the Functional Group view is useful to reduce the number of registers to view at a time. For example, Figure 23 shows the "JESD_Control" Functional Group, which is useful because the four needed registers to configure the JESD link are all in that group. By selecting this group and expanding the registers, the user can quickly find the registers and update their values. **The "Apply Selected" or "Apply Changes" button, above the red (2), MUST be clicked after a register is changed to commit the change and program it to the device.**

The Bit Fields view can be used in conjunction with Functional Groups. In that case, the Bit Fields associated with the selected Functional Group will be shown.

The red (5) is in the Macro Tools area, and is above the list of macros that are currently open in the session. The user can click the name of the desired macro to make it active in the screen. The "Play" button (right-pointing triangle) can be clicked and the selected macro played.

The red (6) is on the search field, which can be used to find a desired bit field.

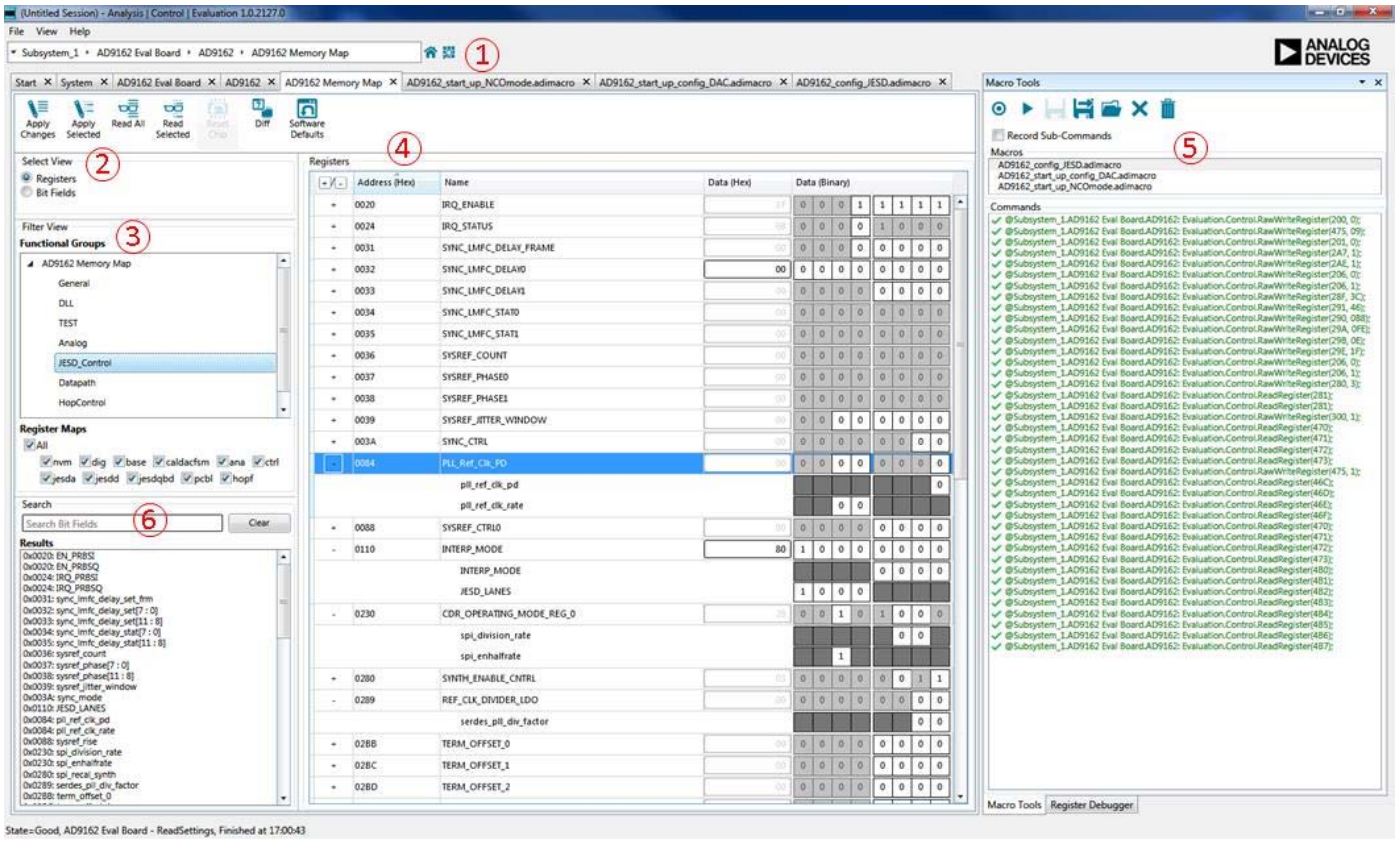

Figure 23. JESD_Control Functional Group view of AD9162 in ACE

The Macro Tools window can be enabled by going to the "View" menu from the main menu bar and checking "Macro Tools".

JESD CONFIGURATION

The ADS7 is based on a Xilinx Virtex7 FPGA device. It is possible to configure another Xilinx Virtex7-based evaluation board to drive the AD9162 EVB. Some items to note are given in this section to assist the customer in configuring the JESD204B transmitters. These can also be found in the AD9162 data sheet rev PrE or later.

JESD Parameters

The JESD204B parameters for the AD9162-FMC(B)-EBZ EVB are given below.

Table 1. JESD Parameters for Interpolation Rate and Number of Lanes

Interp	Lanes	M	F	S	PCLK period (DAC clocks)	LMFC period (DAC clocks)	Lane Rate @ 5GHz DACCLK
1	8	1	1	4	16	128	12.5
2	6	2	2	3	12	192	16.66 (NOTE 1)
2	8	2	1	2	16	128	12.5
3	6	2	2	3	18	288	11.11
3	8	2	1	2	24	192	8.33
4	3	2	4	3	12	384	16.66 (NOTE 1)
4	4	2	1	1	16	128	12.5
4	6	2	2	3	24	384	8.33
4	8	2	1	2	32	256	6.25
6	3	2	4	3	18	576	11.11
6	4	2	1	1	24	192	8.33
6	6	2	2	3	36	576	5.55

6	8	2	1	2	48	384	4.16
8	2	2	2	1	16	256	12.5
8	3	2	4	3	24	768	8.33
8	4	2	1	1	32	256	6.25
8	6	2	2	3	48	768	4.16
8	8	2	1	2	64	512	3.12
12	2	2	2	1	24	384	8.33
12	3	2	4	3	36	1152	5.55
12	4	2	1	1	48	384	4.16
12	6	2	2	3	72	1152	2.77
12	8	2	1	2	96	768	2.08
16	1	2	4	1	16	512	12.5
16	2	2	2	1	32	512	6.25
16	3	2	4	3	48	1536	4.16
16	4	2	1	1	64	512	3.12
16	6	2	2	3	96	1536	2.08
16	8	2	1	2	128	1024	1.56
24	1	2	4	1	24	768	8.33
24	2	2	2	1	48	768	4.16
24	3	2	4	3	72	2304	2.77
24	4	2	1	1	96	768	2.08
24	6	2	2	3	144	2304	1.38
24	8	2	1	2	192	1536	1.04

NOTE 1: Maximum lane rate is 12.5 GHz, these modes must be run with the DAC rate below 3.75 GHz

Table 2. JESD parameters with fixed values

Parameter	Value	Notes
K	32	
N	16	
NP	16	
CF	0	
HD	1	
CS	0	

JESD Lane Mapping and EVB connections to FMC Connector and Use with the Xilinx JESD204B Transmitter IP

The physical lanes on the FMC connector are not necessarily connected to the same lanes on the AD9162. The AD9162 does have a cross bar switch on the JESD204B link, but in the case of the ADS7 and AD9162, the switch is done using the crossbar in the Xilinx JESD Transmitter. Here is the mapping between the FMC lanes and the AD9162 lanes on the AD9162-FMC(B)-EBZ evaluation board. The mapping to the Xilinx JESD204B IP is also given for reference.

- Physical lane 0 on the FMC connector (DP0_C2M) is also lane 0 on AD9162 (lane 0 out of the Xilinx JESD204 IP)
- Physical lane 1 on the FMC connector (DP1_C2M) is also lane 1 on AD9162 (lane 1 out of the Xilinx JESD204 IP)
- Physical lane 2 on the FMC connector (DP2_C2M) is also lane 2 on AD9162 (lane 2 out of the Xilinx JESD204 IP)
- Physical lane 3 on the FMC connector (DP3_C2M) is also lane 3 on AD9162 (lane 3 out of the Xilinx JESD204 IP)
- Physical lane 4 on the FMC connector (DP4_C2M) is lane 5 on AD9162 (lane 5 out of the Xilinx JESD204 IP)
- Physical lane 5 on the FMC connector (DP5_C2M) is lane 7 on AD9162 (lane 7 out of the Xilinx JESD204 IP)
- Physical lane 6 on the FMC connector (DP6_C2M) is also lane 6 on AD9162 (lane 6 out of the Xilinx JESD204 IP)
- Physical lane 7 on the FMC connector (DP7_C2M) is lane 4 on AD9162 (lane 4 out of the Xilinx JESD204 IP)

There is also some P/N inversion between Tx and Rx on the AD9162-FMC(B)-EBZ EVB to ease lay out. They can easily be inverted in the Xilinx physical layer

- Physical lanes 4-7 (DP4_C2M – DP7_C2M) on the FMC connector are inverted (P/N swapped)

When getting the JESD link up and running, a few debug ideas are below. Watch the Sync lane

- If Sync lane stays low, the 204B reference frequency needs to be adjusted
- Sync lane toggles: P/N lanes needs to be adjusted (K character pass but not ILS with inverted polarity creating Sync toggling)
- Sync stays high but not a good spectrum: Transport or mapping of lane is wrong

Single Tone Record Length in 3 lanes / 6 lanes mode

Record length shall be multiple of 3 in 3 lane/6lanes mode, otherwise the output spectrum isn't correct. One example is shown in Figure 24.

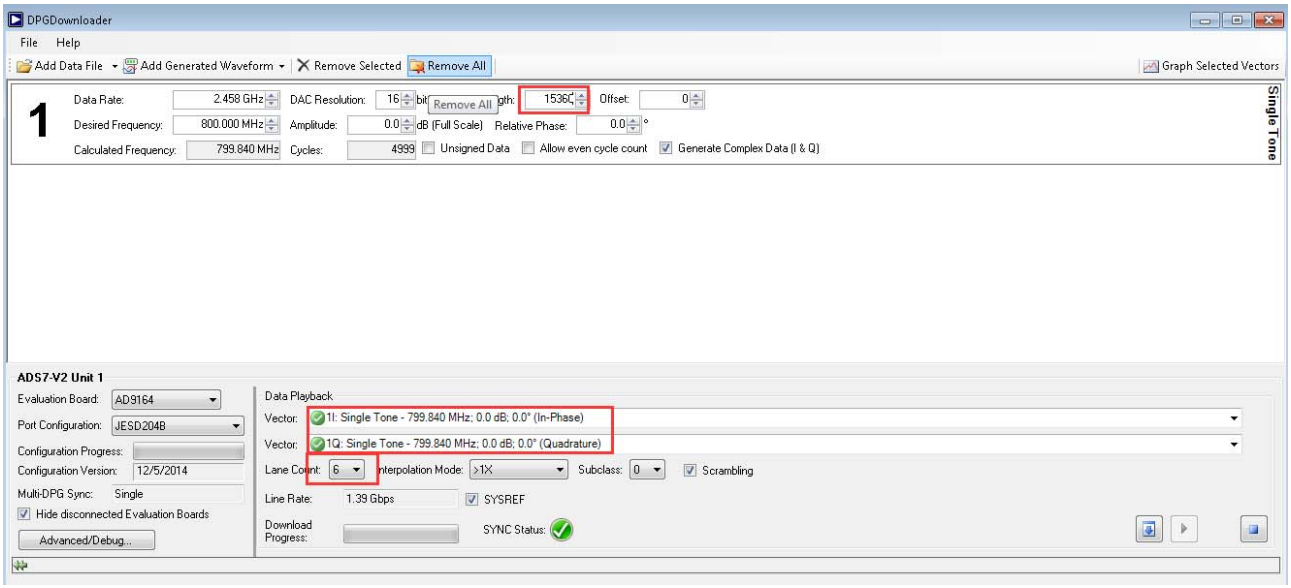

Figure 24. Record length in 3/6 lanes mode

ERRORS

Basic Hardware Issues

There are five LEDs on the Eval board which are the 12v power supply LED, the ADF4355 locked LED, the USB connected LED, the AD9162 PWR_BAD LED and the AD9162 interruption LED. These LED are shown in Figure 25 . If the Eval board is configured correctly, 12v power LED, ADF4355 locked LED and USB connected LED shall be lit. PWR_BAD LED is lit when AD9162 isn't powered properly.

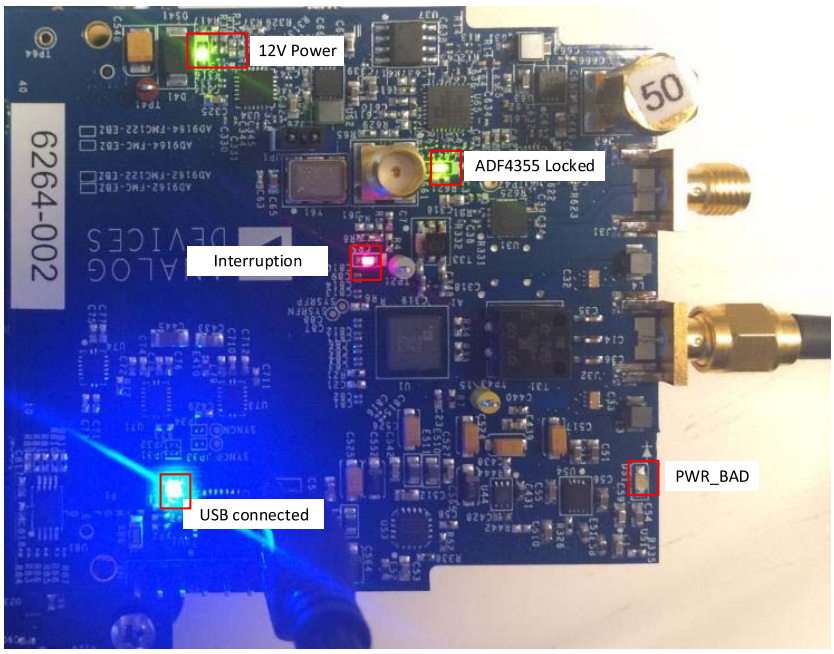

Figure 25. Five LEDs on the Eval Board

The AD9162-FMC(B)-EBZ eval board can be run with or without an ADS7. To download a valid image to the FPGA, open DPG Downloader with the USB cable connected to the PC and the ADS7. DPG Downloader will recognize the ADS7 and read the board ID of the AD9162-FMC(B)-EBZ (if it is connected) through the FMC connector. It will then download a valid image and power on the AD9162-FMC(B)-EBZ automatically.

There may be cases that one or the other software does not recognize the Eval boards. DPG Downloader can be open and a simple unplug-plug of the USB cable is normally sufficient. In the case of ACE, the ACE software will need to be closed, the USB cable plugged into the AD9162 Eval board, power applied to the AD9162 Eval board, and then ACE opened. This is an issue in ACE that will be addressed in a future release.

DPG Downloader Does Not Recognize an ADS7

It can occur that the DPG Downloader software does not recognize the ADS7 board. Unplug the USB cable from the ADS7 and re-plug it in to the ADS7, and the DPG Downloader software should recognize the ADS7. If it does, it will download a Generic image to the FPGA. If the AD9162-FMC(B)-EBZ board is plugged into the ADS7 with the FMC connector prior to the USB cable being plugged into the ADS7, the DPG Downloader software should recognize the ADS7 and also read the AD9162-FMC(B)-EBZ identifier through the FMC connector, and download an AD9162 image to the Eval board.

JESD204B Link Does Not Come up

The start-up sequences referenced in this document have been tested in ADI's lab on the AD9162-FMC(B)-EBZ evaluation board and are known working. There can be cases or situations when the JESD204B link does not come up. This section has several suggestions to debug the situation, but it is not an exhaustive list covering every possible scenario. When in doubt, power-cycle all hardware, re-open the ACE software, re-open the DPG Downloader software, and follow one of the Quick Start routines given in this guide. Then, notice the differences from the routines in this document as compared to the desired set-up, and carefully make the changes step-by-step and observe where the issue is created.

Some debugging suggestions for times when the SERDES link does not come up:

- If the SERDES PLL is locked (0x281[0]=1), then it may be necessary to reset the deframer by toggling bit 0x475[3] = 1, then 0.

- If that doesn't resolve the issue, it may be necessary to do a SERDES PLL re-calibration. To do this, set and reset 0x280[2], then do the de-framer reset toggle of 0x475[3] = 1, then 0.

If these don't work, check to make sure the DPG Downloader has a pattern selected and the pattern is playing, i.e., sending data to the AD9162-FMC(B)-EBZ. The link will NOT come up if there is no data being sent to the DAC. Also, be sure to check that sub-class 0 is

selected. This is the default sub-class and the Quick Start Guide examples all use sub-class 0. Finally, check that the JESD lane rate reported by DPG Downloader is what is expected based on the chosen JESD parameters.

If the board was previously configured for NCO mode, reset the board by doing a power cycle or writing 0x99 to register 0x000, then writing 0x18 to register 0x000. If the board was previously configured in a JESD mode, write the below sequence to disable the JESD204B interface:

a. Reg 0x300 = 0x00 #Disable JESD204B links
b. Reg 0x280 = 0x00 #Disable SERDES PLL

This must be done before the SERDES configuration is changed. After disabling the JESD204B link, the below steps can be followed.

ACE Doesn't recognize the AD9162-FMC(B)-EBZ Eval Board

One of two possible errors can be generated, as shown in Figure 26 and Figure 27. Both of these indicate that the ACE software hasn't recognized the AD9162-FMC(B)-EBZ. These can occur if the ACE software is started before powering up and connecting the AD9162-FMC(B)-EBZ Eval board to the PC, or if the Eval board is power-cycled and ACE is not re-started. This is a bug in ACE and will be corrected in a future release of ACE.

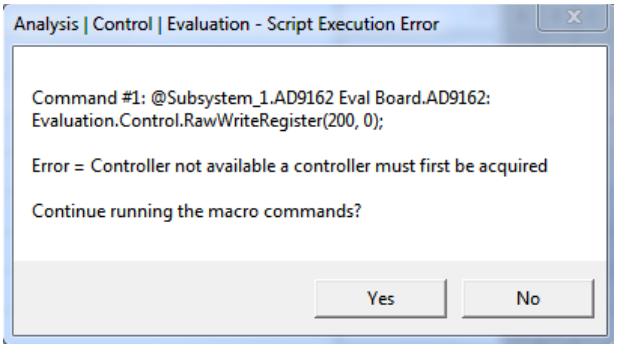

Figure 26. Script error window indicating ACE does not recognize the AD9162-FMC(B)-EBZ eval board

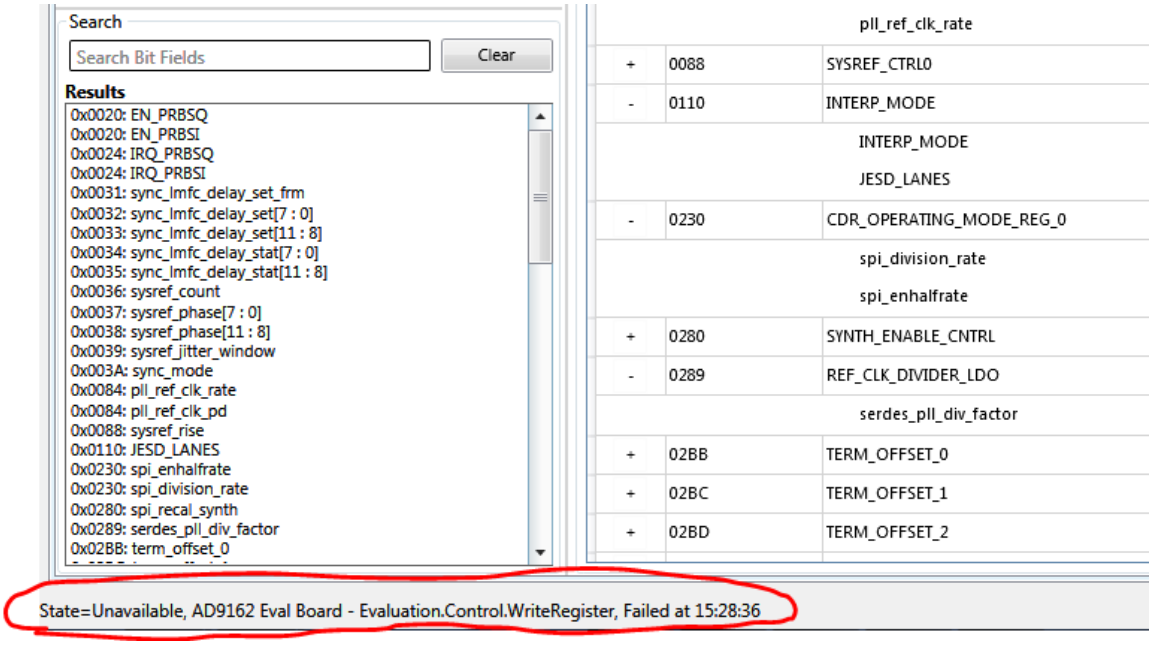

Figure 27. Register Write error indicating ACE does not recognize the AD9162-FMC(B)-EBZ Eval board

The most basic remedy for this issue is to close ACE and re-open it (re-start). As long as the AD9162-FMC(B)-EBZ is powered up and connected to the PC, ACE will recognize the Eval board and scripts and register writes will work again.

ADF4355 output frequency or DAC output frequency isn't correct

Check the board crystal, it can be 120MHz or 122.88MHz. The reference clock in the 'AD916x_Initial_Worksheet.xlsx' should be set to the crystal frequency.

ADS7 Firmware Update Needed

The ADS7 firmware was updated at the factory prior to shipping. However, it is possible that a further update to the firmware was made after that time. If a firmware update is needed, a dialog stating that will be displayed and the user will not be able to use DPGDownloader until a firmware update is completed.

To update the ADS7 firmware, open the DPG Downloader application and select the Advanced Debug button, as shown in Figure 28. Then, choose the "update" button. The updater should run and install the firmware update. It may be necessary to power cycle the ADS7 board, and to close and re-open DPG Downloader to recognize the update happened.

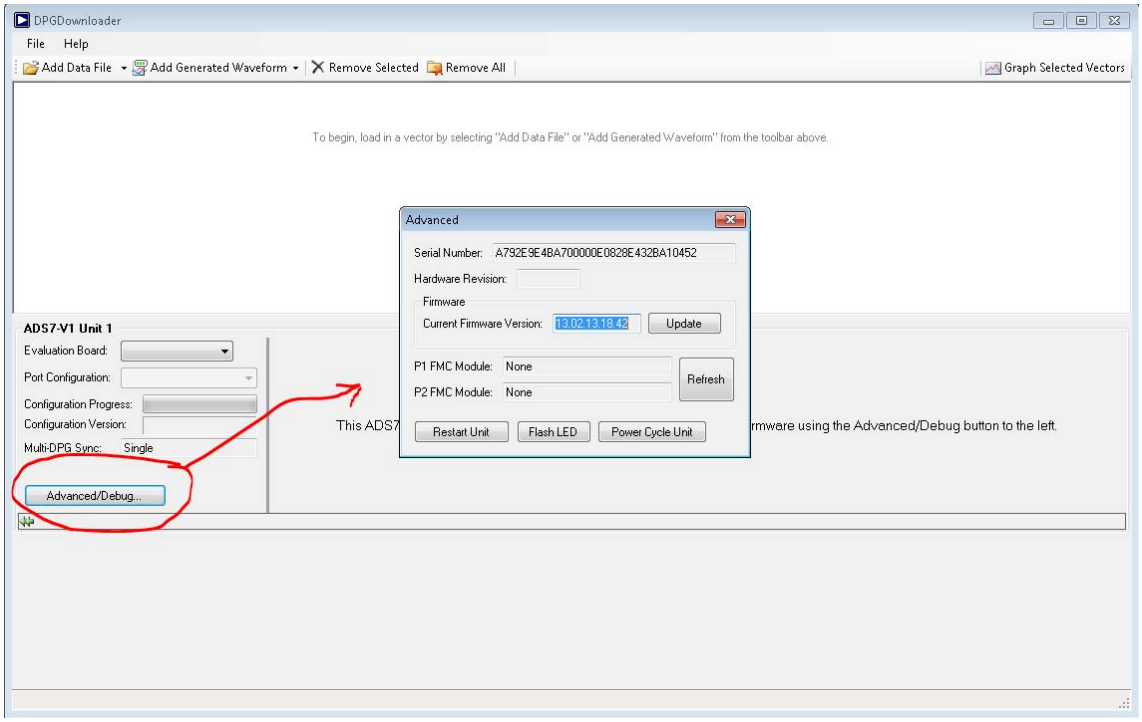

Figure 28. Updating the ADS7 firmware version