12Bit, 2.5GSPS, 1.3/2.5V ADC

Preliminary Technical Data

AD9625

FEATURES

12-bit 2.5GSPS ADC with no missing codes
SFDR = 75 dBc w/ Ain up to 1GHz, @-1dBFS, 2.5GSPS
SFDR = 70 dBc w/ Ain up to 2GHz, @-1dBFS, 2.5GSPS
SNR = 57.2 dBFS w/ Ain up to 1GHz, @-1dBFS, 2.5GSPS
Noise Floor = -147.5dBFS/Hz @ 2.5GSPS
Power Consumption: 3.7W at 2.5GSPS
Conversion Error Rate = 1e-15
Differential Analog Input: 1.2V pk-pk
Differential Clock Input
High-speed 6 or 8-lane JESD-204B serial output
- Sub class 1: 6.25Gbps at 2.5GSPS

Two Independent divide by 8 and 16 decimation filters with 10-bit NCOs
Supply voltages: 1.3V, 2.5V
Serial Port control
Flexible digital output modes
Built-In selectable digital test patterns

APPLICATIONS

Spectrum Analyzers
Military Communications
RADAR
High performance digital storage oscilloscopes
Active Jamming/Anti-Jamming
Electronic Surveillance & Countermeasures

PRODUCT HIGHLIGHTS

- High performance: exceptional SFDR in high sample rate applications.
- Direct RF sampling
- Ease of use:
  - On-chip reference
  - Flexible digital data output formats based on JESD204B specification
- A control-path SPI interface port supports various product features and functions, such as data formatting, gain and offset calibration values, as well as power-down modes.

FUNCTIONAL BLOCK DIAGRAM

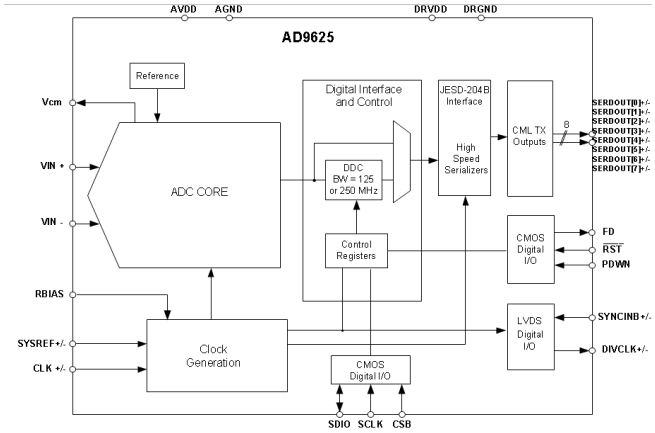


Figure 1.

GENERAL DESCRIPTION

The AD9625 is a 12-bit monolithic sampling analog-to-digital converter (ADC) that operates at conversion rates up to 2.5 giga-samples-per-second (2.5GSPS). This product is designed for sampling wide bandwidth analog signals and can be used up to the third Nyquist zones. The AD9625's combination of wide input bandwidth, high sampling rate and excellent linearity are ideally suited for spectrum analyzers, data acquisition systems and a wide assortment of military electronics applications such as RADAR and jamming/anti-jamming measures.

The analog input, clock and SYSREF signals are differential inputs. Users can configure the JESD204B based high-speed serialized output in a variety of 6-lane and 8-lane configurations. The product is specified over the industrial temperature ranges of (-40C to +85C).

Rev. PrM

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

10/28/10—Advanced Info Version (Rev PrA) available.

06/20/11 – Advanced Info Version (Rev PrB) available.

07/06/11 – Advanced Info Ver (Rev PrC) –corrected heading label, changed WO Spur, 4GHz IF in Product Highlights

07/07/11 – Advanced Info Ver (Rev PrD) – updated functional block diagram

08/16/11 – Advanced Info Ver (Rev PrE) – updated aperture delay, aperture uncertainty, copyright indicator in footer

12/10/11 - Advanced Info Ver (Rev PrF) – updated pin out, specs, absolute max table, function descriptions

12/19/11 – Advanced Info Version (Rev PrG) – updated ballout, power rating

01/20/12 – Advanced Info Version (RevPrH) – updated functional block diagram, digital specifications, equivalent circuits, memory map, JESD204B interface descriptions

01/26/12 – Advanced Info Version (RevPrI) – updated ball map and ADC specifications

04/13/12 – Advanced Info Version (RevPrJ) – updated specifications

04/19/12 – Advanced Info Version (RevPrK) – updated ballmap

02/26/13 – Advanced Info Version (RevPrL) – Added ordering guide

07/10/13 – Advanced Info Version (RevPrM)

SPECIFICATIONS

AVDD1 = DVDD1 = DRVDD1 = 1.3V, AVDD2 = DVDD2 = DRVDD2 = 2.5V, specified maximum sampling rate, 1.2V internal reference, AIN = -1.0dBFS, default SPI settings, unless otherwise noted.

Table 1.

Parameter	Temp	AD9625 2500MSPS			Unit
		Min	Typ	Max	
RESOLUTION		12			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full		± 1		LSB
Gain Error	Full		± 3		%FSR
Differential Nonlinearity (DNL)	Full		± 0.5		LSB
Integral Non-Linearity (INL)	Full		± 1.0		LSB
TEMPERATURE DRIFT					
Offset Error	Full		TBD		ppm/°C
Gain Error	Full		TBD		ppm/°C
ANALOG INPUTS					
Differential Input Voltage Range (Internal VREF = xV)	Full		1.2		V p-p
Internal Common-Mode Voltage(Vcm)	Full		525		mV
Differential Input Resistance	25C		100		Ω
Differential Input Capacitance	25C		1.5		pF
Analog Full-Power Bandwidth (100 ohm diff termination)[1]	25C		2		GHz
Analog Full-Power Bandwidth (50 ohm diff termination)[1]	25C		3.5		GHz
Input Referred Noise	25C		4.0		LSB
POWER SUPPLY					
AVDD1	Full	1.28	1.3	1.32	V
AVDD2	Full	2.4	2.5	2.6	V
DRVDD1	Full	1.28	1.3	1.32	V
DRVDD2	Full	2.4	2.5	2.6	V
DVDD1	Full	1.28	1.3	1.32	V
DVDD2	Full	2.4	2.5	2.6	V
DVDDIO	Full	2.5		3.3	V
SPI_VDDIO	Full	2.5		3.3	V
IAVDD1	Full		1190	TBD	mA
IAVDD2	Full		470	TBD	mA
IDRVDD1	Full		470	TBD	mA
IDRVDD2	Full		4	TBD	mA
IDVDD1 (With Direct Digital Down Conversion)	Full		430	TBD	mA
IDVDD1 (Without Direct Digital Down Conversion)	Full		300	TBD	mA
IDVDD2	Full		1	TBD	mA
IDVDDIO	Full		1	TBD	mA
ISPI_VDDIO	Full		1	TBD	mA
Power Dissipation (Without Direct Digital Down Conversion)	Full		3.7	TBD	W
Power Dissipation (With Direct Digital Down Conversion)	Full		TBD	TBD	W
Power-down Dissipation	Full		123	TBD	mW

[1]Full power bandwidth does not always equate to usable bandwidth

AC SPECIFICATIONS

AVDD1 = DVDD1 = DRVDD1 = 1.3V, AVDD2 = DVDD2 = DRVDD2 = 2.5V, specified maximum sampling rate, 1.2V internal reference, AIN = -1.0dBFS, default SPI settings, unless otherwise noted.

Table 2.

Parameter	Temp	AD9625 2500MSPS			Unit
		Min	Typ	Max	
ANALOG INPUT FULL SCALE	Full		1.2		V p-p
NOISE DENSITY	25C		-150		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 100 MHz	25C		57.8		dBFS
f_{IN} = 500 MHz	25C		57.7		dBFS
f_{IN} = 1000 MHz	25C		57.2		dBFS
f_{IN} = 1800 MHz	25C		56.0		dBFS
f_{IN} = 2000 MHz	Full		55.8		dBFS
SINAD					
f_{IN} = 100 MHz	25C		56.6		dBFS
f_{IN} = 500 MHz	25C		56.6		dBFS
f_{IN} = 1000 MHz	25C		56.1		dBFS
f_{IN} = 1800 MHz	25C		56.0		dBFS
f_{IN} = 2000 MHz	Full		55.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 100 MHz	25C		9.1		Bits
f_{IN} = 500 MHz	25C		9.1		Bits
f_{IN} = 1000 MHz	25C		9.0		Bits
f_{IN} = 1800 MHz	25C		9.0		Bits
f_{IN} = 2000 MHz	Full		9.0		Bits
SPURIOUS FREE DYNAMIC RANGE (SFDR) (including 2nd or 3rd Harmonic)					
f_{IN} = 100 MHz	25C		76.3		dBFS
f_{IN} = 500 MHz	25C		76.3		dBFS
f_{IN} = 1000 MHz	25C		76.2		dBFS
f_{IN} = 1800 MHz	25C		70.4		dBFS
f_{IN} = 2000 MHz	Full		68.7		dBFS
WORST OTHER (Excluding 2nd or 3rd Harmonic)					
f_{IN} = 100 MHz	25C		78.0		dBFS
f_{IN} = 500 MHz	25C		77.3		dBFS
f_{IN} = 1000 MHz	25C		81.8		dBFS
f_{IN} = 1800 MHz	25C		76.3		dBFS
f_{IN} = 2000 MHz	Full		76.8		dBFS
TWO-TONE INTERMODULATION DISTORTION (IMD) @ -7dBFS per tone					
f_{IN1} = 999 MHz, f_{IN2} = 1001 MHz	25C		-73		dBc
f_{IN1} = 1999 MHz, f_{IN2} = 2001 MHz	25C		-68		dBc

DIGITAL SPECIFICATIONS

AVDD1 = DVDD1 = DRVDD1 = 1.3V, AVDD2 = DVDD2 = DRVDD2 = 2.5V, specified maximum sampling rate, 1.2V internal reference, AIN = -1.0dBFS, default SPI settings, unless otherwise noted.

Table 3.

Parameter	Temp	AD9625 2500MSPS			Unit
		Min	Typ	Max	
CLOCK INPUTS (CLK+, CLK-)					
Differential Input Voltage	Full	250		TBD	mV p-p
Input Common Mode Voltage	Full		0.85		V
Input Common Mode Range	Full				
Input Resistance (Differential)	Full		57k		kΩ
Input Capacitance	Full		2.5		pF
SYSREF INPUTS (DSYSREF+, DSYSREF-)					
Differential Input Voltage	Full	250		TBD	mV p-p
Input Common Mode Voltage	Full		0.85		V
Input Common Mode Range	Full				
Input Resistance (Differential)	Full		100		Ω
Input Capacitance	Full		2.5		pF
LOGIC INPUTS (SDIO, SCLK, CSB)					
Logic Compliance			CMOS		
Logic 1 Voltage	Full	0.8XSPI_DVDDIO			V
Logic 0 Voltage	Full			0.5	V
Input Resistance	Full		30		kΩ
Input Capacitance	Full		0.5		pF
LOGIC INPUTS (PWDN)					
Logic Compliance			CMOS		
Logic 1 Voltage	Full	0.8XDVDDIO			V
Logic 0 Voltage	Full			0.5	V
Input Resistance	Full		30		kΩ
Input Capacitance	Full		0.5		pF
SYNCINB INPUT					
Logic Compliance			LVDS		
Differential Input Voltage	Full	250		TBD	mV p-p
Input Common Mode Voltage	Full		1.2		V
Input Resistance (Differential)	Full		20		kΩ
Input Capacitance	Full		2.5		pF
LOGIC OUTPUT (SDIO)					
Logic Compliance			CMOS		
Logic 1 Voltage (IOH = 800μA)	Full		0.8XSPI_VDDIO		V
Logic 0 Voltage (IOL = 50 μA)	Full		0.3		V
DIGITAL OUTPUTS					
Compliance	Full		CML		
Differential Output Voltage	Full		800		mV p-p
Output Offset Voltage	Full		650		mV p-p
RESETS (RST~,ARST,DRST)					
Logic 1 Voltage	Full	0.8XDVDDIO			V
Logic 0 Voltage	Full			0.5	V
Input Resistance (Differential)	Full		20		kΩ
Input Capacitance	Full		2.5		pF
FAST DETECT (FD) and INTERRUPT (IRQ)					
Logic Compliance			CMOS		
Logic 1 Voltage	Full	0.8XDVDDIO			V
Logic 0 Voltage	Full			0.5	V

Input Resistance (Differential)	Full	20	kΩ
Input Capacitance	Full	2.5	pF

SWITCHING SPECIFICATIONS

AVDD1 = DVDD1 = DRVDD1 = 1.3V, AVDD2 = DVDD2 = DRVDD2 = 2.5V, specified maximum sampling rate, 1.2V internal reference, AIN = -1.0dBFS, default SPI settings, unless otherwise noted.

Table 4.

Parameter	Temp	AD9625 2500MSPS Min	Typ	Max	Unit
CLOCK (CLK)					
Maximum Clock Rate	Full			2500	MSPS
Minimum Clock Rate	Full	325[1]			MSPS
Clock Pulse Width High	Full	50+/-5			% duty cycle
Clock Pulse Width Low	Full	50+/-5			% duty cycle
SYSREF (SYSREF)[2]					
Setup Time (t_{SSREF})	Full	-160			pS
Hold Time (t_{HSREF})	Full	+225			pS
OUTPUT PARAMETERS (SERDOUT[n])					
Rise Time	Full		TBD		pS
Fall Time	Full		TBD		pS
Power-up Time	Full		TBD		mS
Wake-Up Time (from Power Down)	Full		TBD		mS
Pipeline Latency (Generic 8-lane Mode)[3]	Full		232		Clock Cycles
DIVIDE CLOCK (DIVCLK)					
Power-up Time	Full		TBD		mS
Wake-Up Time (from Power Down)	Full		TBD		mS
APERTURE					
Aperture Delay	Full		180		pS
Aperture Uncertainty (Jitter)	Full		40		fs RMS
Out-of-range Recovery Time	Full		3		Clock Cycles

[2] SYSREF setup and hold times are defined with respect to rising sysref edge and rising clock edge

[3] Please refer to DIGITAL OUTPUT section for latency of all JESD modes

Timing Diagrams

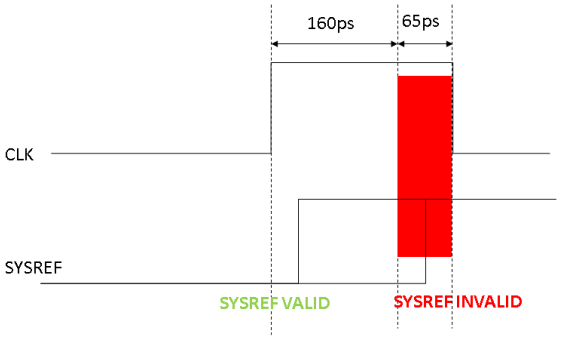


Figure X. Sysref setup and hold time

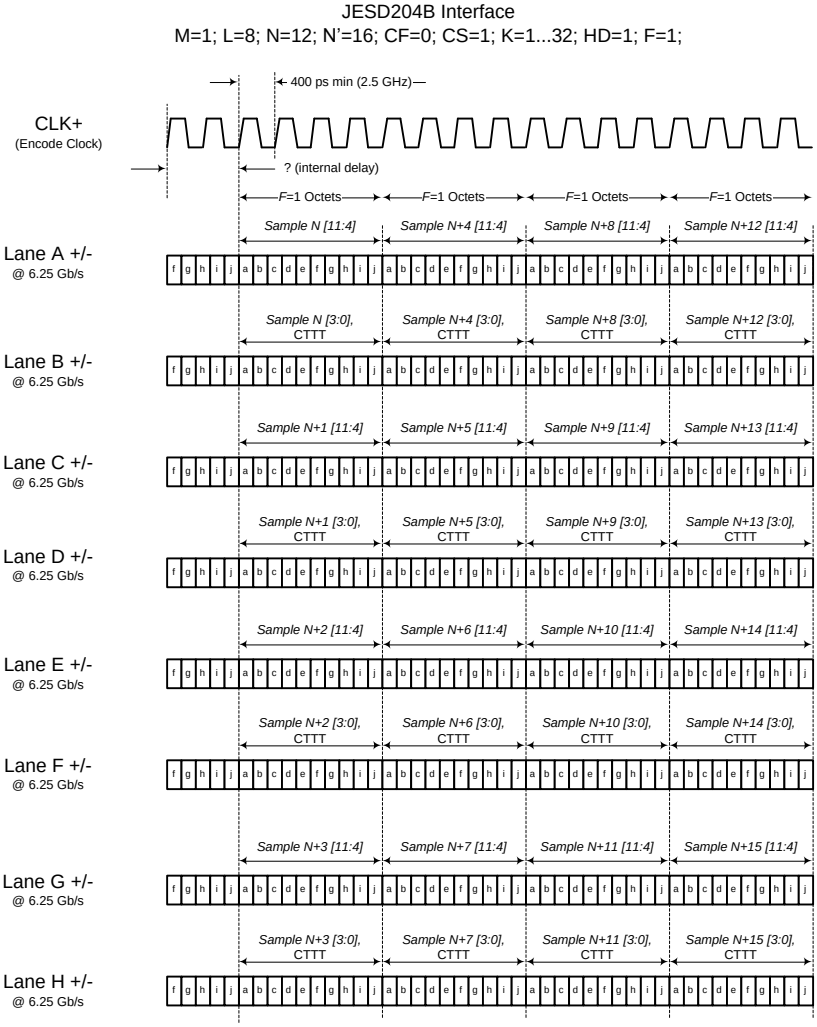


Figure X. CLK Input and DOUT Timing Relationship (Generic 8-Lane Mode)

On power up, reset AD9625 to ensure proper operation. To reset AD9625, follow the initialization sequence specified below. Note that DRST and ARST can share a common signal.

1. Drive ARST high, DRST high, and RSTB low
2. Wait for at least 40 ns
3. Drive ARST low, DRST low, and RSTB low
4. Wait for at least 40 ns
5. Drive ARST low, DRST low, and RSTB high

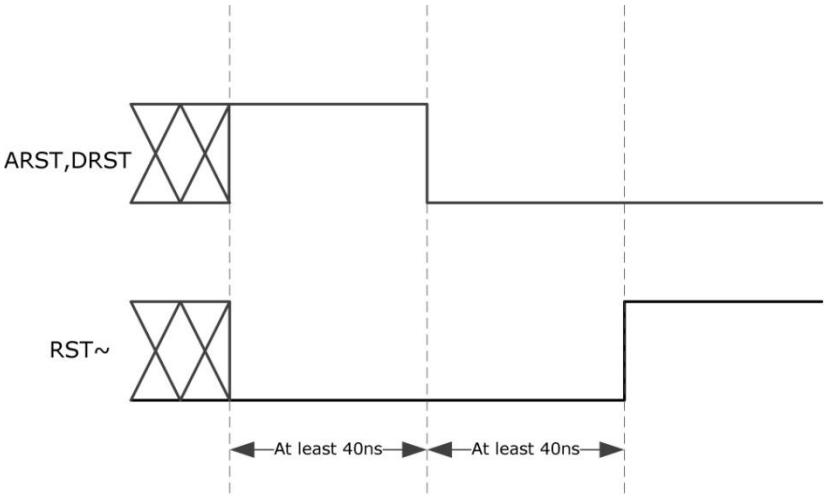


Figure X. Reset Cycle

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Electrical	
AVDD1to AGND	-0.3V to +1.32V
AVDD2 to AGND	-0.3V to +2.75V
DRVDD1 to DRGND	-0.3V to +1.32V
DRVDD2 to DRGND	-0.3V to +2.75V
DVDD1 to DGND	-0.3V to +1.32V
DVDD2 to DGND	-0.3V to +2.75V
DVDDIO to DGND	-0.3V to +3.63V
SPI_VDDIO to DGND	-0.3V to +3.63V
AGND to DRGND	-0.3V to +0.3V
VIN± to AGND	-0.3V to AVDD1+ 0.2V
VCM to AGND	-0.3V to AVDD1+ 0.2V
VMON to AGND	-0.3V to AVDD1+ 0.2V
CLK± to AGND	-0.3V to AVDD1+ 0.2V
DSYSREF± to AGND	-0.3V to AVDD1+ 0.2V
SYNCINB± to DRGND	-0.3V to DRVDD2 + 0.2V
SCLK to DRGND	-0.3V to SPI_VDDIO + 0.2V
SDIO to DRGND	-0.3V to SPI_VDDIO + 0.2V
IRQ to DRGND	-0.3V to DVDDIO + 0.2V
PDWN to DRGND	-0.3V to DVDDIO + 0.2V
$\overline{RST}$ to DRGND	-0.3V to DVDDIO + 0.2V
CSB to DRGND	-0.3V to SPI_VDDIO + 0.2V
FD to DRGND	-0.3V to DVDDIO + 0.2V
DIVCLK± to DRGND	-0.3V to DRVDD2 + 0.2V
SERDOUT[n]± to DRGND	-0.3V to DRVDD1 + 0.2V
Environmental	
Operating temperature range	-40°C to +85°C
Maximum junction temperature	125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

PCB	Power (W)	T_A (°C)	T_J (°C)	Θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	Ψ_{JB} (°C/W)	Θ_{JC} (°C/W)
4L	3.7	85.0	135.5	18.7	0.61	6.1	1.4
10L	3.7	85.0	127.5	11.5	0.61	4.1	--

Table xx. Thermal Resistance

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE PLOTS

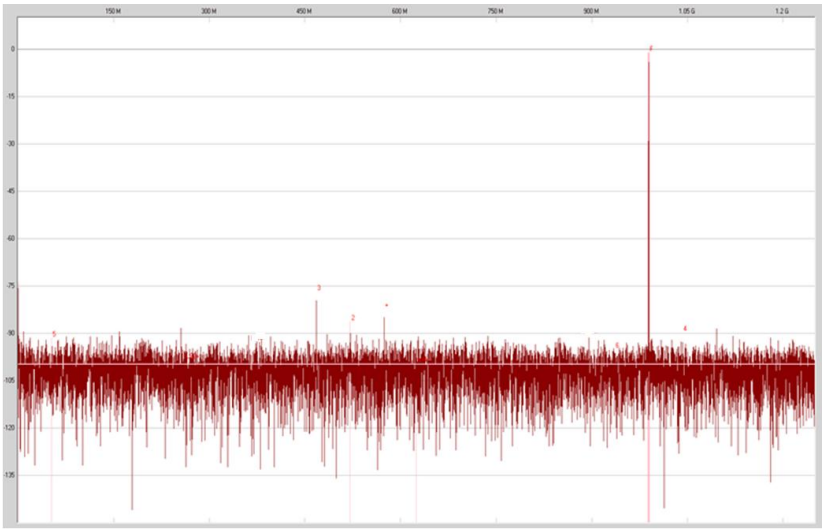


Figure X. FFT Plot at 2.5GSPS, 1GHz Ain (SFDR=75.8dBc, SNR=57.5dBFS)

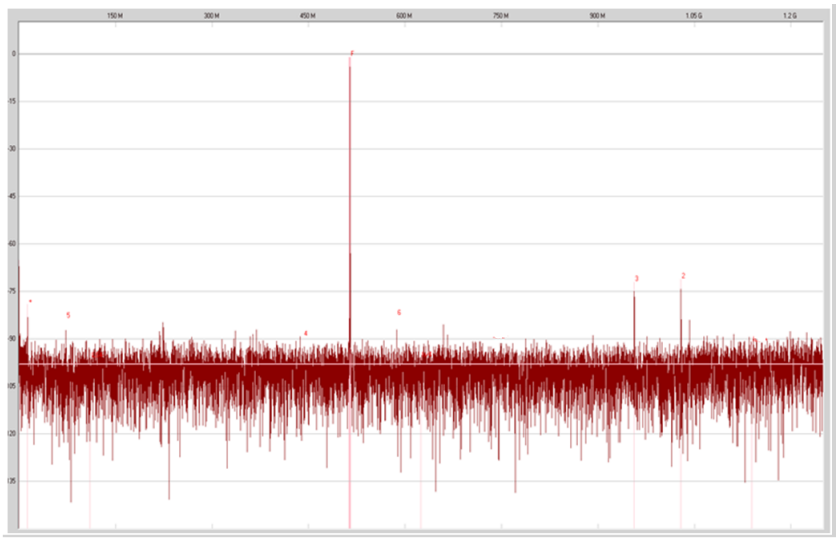


Figure X. FFT Plot at 2.5GSPS, 2GHz Ain (SFDR=70.3dBc, SNR=55.9dBFS)

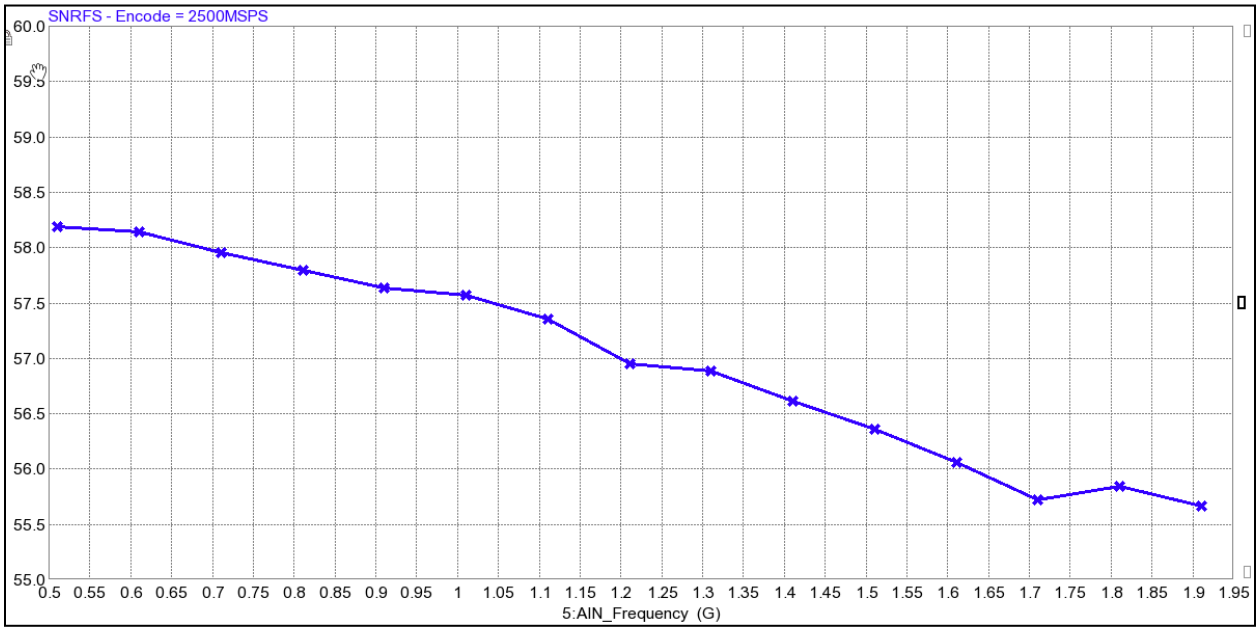


Figure X. SNR versus Analog Input at 2.5GSPS

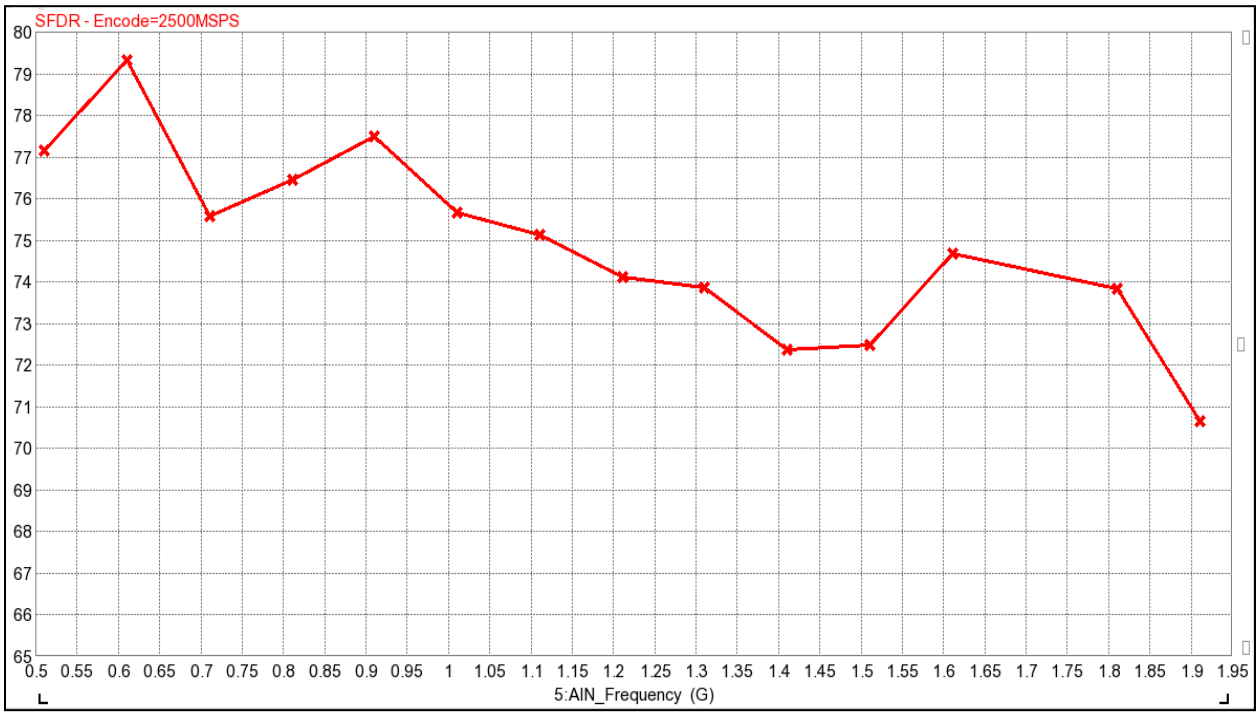


Figure X. SFDR versus Analog Input at 2.5GSPS

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	AVDD2	AVDD1	DVDD2	DVDD1	DRVDD2	DRVDD1	DVDDIO SPI_VDDIO	AGND	DGND	DRGND	DNC or Bypass /w Cap

•	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AGND	AGND	AGND	AVDD1	AGND	AVDD2	VCM	AGND	VIN+	VIN-	AGND	VM_BYP	AVDD2	AVDD2
B	AGND	AGND	AGND	AGND	AVDD1	AGND	AVDD2	AGND	AGND	AGND	AGND	AVDD2	AGND	AGND
C	AGND	AGND	AGND	AGND	AGND	AVDD1	AGND	AVDD2	AGND	AGND	AVDD2	AGND	AGND	AVDD1
D	DVDD1	DVDD1	DVDD1	DNC	AGND	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AVDD1	AVDD1
E	DGND	DGND	DGND	DVDD2	VMON	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	AGND
F	DVDD1	DVDD1	DVDD1	SPI_VDDIO	DVDDIO	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	CLK+
G	DGND	DGND	DGND	CSB	DVDDIO	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	CLK-
H	DVDD1	DVDD1	DVDD1	SCLK	IRQ	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	AGND
J	DGND	DGND	DGND	SDIO	FD	RBIAS_EXT	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	SYSREF+
K	DVDD1	DVDD1	RSTB	PDWN	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	SYSREF-
L	DGND	DNC	SYNCINB-	SYNCINB+	DGND	DGND	DGND	DGND	ARST	DNC	DNC	DNC	AGND	AGND
M	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRVDD1	REXT	DRST	DRGND
N	DRVDD1	SERDOUT[7]+	SERDOUT[6]+	SERDOUT[5]+	SERDOUT[4]+	DRVDD1	SERDOUT[3]+	SERDOUT[2]+	SERDOUT[1]+	SERDOUT[0]+	DRVDD1	VP_BYP	DRVDD2	DRVDD2
p	DRVDD1	SERDOUT[7]-	SERDOUT[6]-	SERDOUT[5]-	SERDOUT[4]-	DRVDD1	SERDOUT[3]-	SERDOUT[2]-	SERDOUT[1]-	SERDOUT[0]-	DRVDD1	DRGND	DIVCLK-	DIVCLK+

Pin Number	Name	Type	Description
General Power / Ground Supply			
J6	RBIAS	Input	Reference Bias (External Resister, 10kOhm to Ground)
*	AGND	Ground	ADC Analog Ground
CLOCK PINS			
F14	CLK +	Input	ADC Clock Input - True
G14	CLK -	Input	ADC Clock Input - Complement
ADC Analog Power / Ground Supplies			
A14, A13, B12, C11, D11, E11, F11, G11, H11, J11, J8, H8, G8, F8, E8, D8, C8, B7, A6	AVDD2	Power	ADC Analog Power Supply (2.50 V)
D14, C14, D13, D12, E12, F12, G12, H12, J12, J7, H7, G7, F7, E7, D7, C6, B5, A4	AVDD1	Power	ADC Analog Power Supply (1.275 V)
A12	VM_BYP	Input	Voltage Bypass
*	AGND	Ground	ADC Analog Ground Supply
ADC Analog			
A9	VIN+	Input	Differential Analog Input Pin (+)
A10	VIN-	Input	Differential Analog Input Pin (+)
A7	VCM	Output	Analog Input Common Mode (0.525V)
E5	VMON	Output	CTAT voltage monitor output (diode temperature sensor)
JESD204B High Speed Serial Power/Gnd			
P11, P6, P1, N11, N6, N1	DRVDD1	Power	Serializer Digital Power Supply (1.275V)
**	DRGND	Ground	Digital Ground Supply
N14, N13	DRVDD2	Power	Power Supply (2.5V) Ref. Clk Div., DSYNC+/- ,DIVCLK+/-
M11	DRVDD1	Power	
N12	VP_BYP	Input	Power Supply (1.275V) Ref. Clk. Div., VCO, Synthesizer
L2	DNC	DNC	Voltage Bypass Do Not Connect
JESD204B High Speed Serial I/O			
J14	SYSREF+	Input	System Reference Chip Synchronization – True
K14	SYSREF-	Input	System Reference Chip Synchronization – False
L4	SYNCINB+	Input	SYNCINB LVDS Input (active low) – True
L3	SYNCINB-	Input	SYNCINB LVDS Input (active low) – Compliment
N10	SERDOUT[0]+	Output	Lane A CML Output Data – True
P10	SERDOUT[0]-	Output	Lane A CML Output Data – Compliment
N9	SERDOUT[1]+	Output	Lane B CML Output Data – True
P9	SERDOUT[1]-	Output	Lane B CML Output Data – Compliment
N8	SERDOUT[2]+	Output	Lane C CML Output Data – True
P8	SERDOUT[2]-	Output	Lane C CML Output Data – Compliment
N7	SERDOUT[3]+	Output	Lane D CML Output Data – True
P7	SERDOUT[3]-	Output	Lane D CML Output Data – Compliment
N5	SERDOUT[4]+	Output	Lane E CML Output Data – True
P5	SERDOUT[4]-	Output	Lane E CML Output Data – Compliment
N4	SERDOUT[5]+	Output	Lane F CML Output Data – True
P4	SERDOUT[5]-	Output	Lane F CML Output Data – Compliment
N3	SERDOUT[6]+	Output	Lane G CML Output Data – True
P3	SERDOUT[6]-	Output	Lane G CML Output Data – Compliment
N2	SERDOUT[7]+	Output	Lane H CML Output Data – True
P2	SERDOUT[7]-	Output	Lane H CML Output Data – Compliment
P14	DIVCLK+	Output	Divide by 4/5 Reference Clk LVDS – True
P13	DIVCLK-	Output	Divide by 4/5 Reference Clk LVDS - Compliment
Digital Supply/Ground			
D1, D2, D3, F1, F2, F3, H1, H2, H3, K1, K2	DVDD1	Power	ADC Digital Power Supply (1.275V)
***	DGND	Ground	ADC Digital Ground Supply
G5, F5	DVDDIO	Power	Digital I/O Power Supply (2.5-3.3V)

Pin Number	Name	Type	Description
F4	SPI_VDDIO	Power	SPI Digital Power Supply (2.5V-3.3V)
E4	DVDD2	Power	ADC Digital Power Supply (2.5V)
D4	DNC	DNC	Do Not Connect
Digital Control			
K4	PDWN	Input	Chip Power-Down/Standby Input
K3	$\overline{RST}$	Input	Chip Digital Reset (active low)
M13	DRST	Input	Reset (active high)
L9	ARST	Input	Reset (active high)
H4	SCLK	Input	SPI Serial Clock CMOS Input
G4	CSB	Input	SPI Chip Select (active low) CMOS Input
J4	SDIO	I/O	SPI Serial Data CMOS Input/Output; Scan Output #1
J5	FD	Output	Fast Detect Output (External Resister, 10kOhm to Ground)
M12	REXT	Input	External Resister, 10kOhm to Ground
H5	IRQ	Output	Interrupt Request Output Signal
L12, L11, L10	DNC	DNC	Do Not Connect
* connected to Analog Ground plane A1, A2, A3, A5, A8, A11, B1, B2, B3, B4, B6, B8, B9, B10, B11, B13, B14, C1, C2, C3, C4, C5, C7, C9, C10, C12, C13, D5, D6, D9, D10, E6, E9, E10, E13, E14, F6, F9, F10, F13, G6, G9, G10, G13, H6, H9, H10, H13, H14, J9, J10, J13, K5, K6, K7, K8, K9, K10, K11, K12, K13, L13, L14	AGND	Ground	ADC Analog Ground Supply
** connected to Digital Driver Ground Plane M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M14, P12	DRGND	Ground	Digital Driver Ground Supply
*** connected to Digital Ground Plane E1, E2, E3, G1, G2, G3, J1, J2, J3, L1, L5, L6, L7, L8	DGND	Ground	Digital Control Ground Supply

EQUIVALENT CIRCUITS

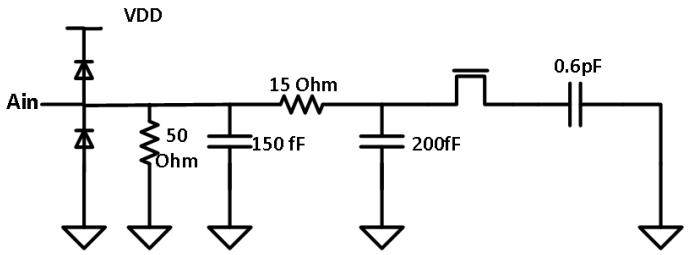


Figure X. Equivalent Analog Input Circuit

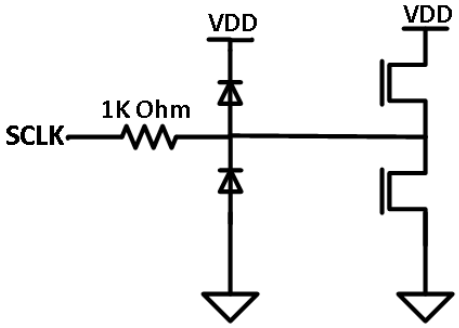


Figure X. Equivalent SCLK Circuit

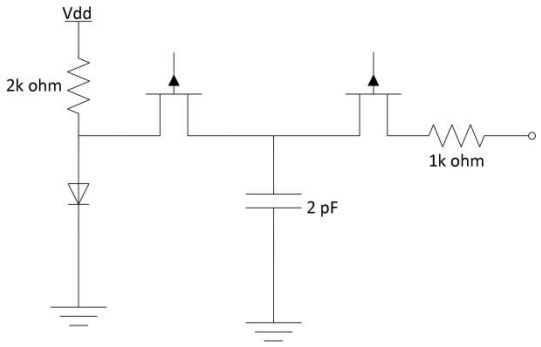


Figure X. Equivalent Temperature Sensor Circuit

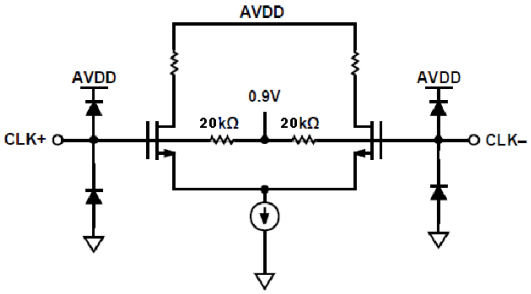


Figure X. Equivalent Clock Input Circuit

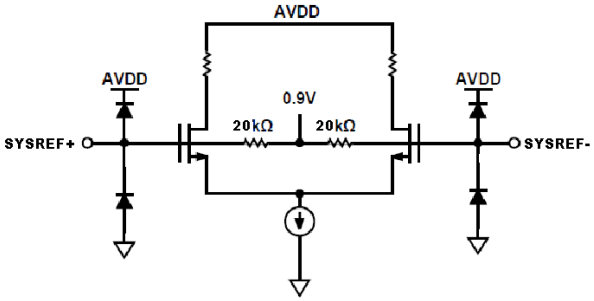


Figure X. Equivalent SYSREF Input Circuit

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into three sections: the chip configuration registers (Address 0x000 to Address 0x002); the transfer register Address 0x0FF); and the ADC functions registers, including setup, control, and test (Address 0x008 to Address 0x13A).

The memory map register table (see Table XX) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x14, the output mode register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This document details the functions controlled by Register 0x00 to Register 0x25. The remaining registers, Register 0x2C and Register 0x13A, are documented in the Memory Map Register Description section.

Open and Reserved Locations

All address and bit locations that are not included in Table XX are not currently supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x15). If the entire address location is open (for example, Address 0x13), this address location should not be written.

Default Values

After the AD9625 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table XX.

Logic Levels

An explanation of logic level terminology follows:

• "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."

• "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Transfer Register Map

Address 0x08 to Address 0x20 are shadowed. Writes to these addresses do not affect part operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set, and then the bit autoclears.

MEMORY MAP REGISTER TABLE

All address and bit locations that are not included in Table XX are not currently supported for this device.

TableXX. Memory Map Registers

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Registers											
0x000	SPI port configuration	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0X18	The nibbles are mirrored so that LSB first mode or MSB first mode registers correctly, regardless of shift mode.
0x001	Chip ID	8-bit chip ID[7:0] (AD9625 = 0x??) (default)								N/A	Read only.
0x002	Chip grade	Open	Open	Speed grade ID 00 = 2.5 GSPS		Open	Open			N/A	Speed grade ID used to differentiate devices; read only.
Transfer Register											
0x0FF	Transfer	Open	Open	Open	Open	Open	Open	Open	Transfer	0x00	Synchronously transfers data from the master shift register to the slave.
ADC Functions											
0x008	Power modes	External power-down pin enable 0=ignored 1=enabled	Open	External power-down pin function 0 = power-down 1 = standby	Open	Open	Open	Internal power-down mode 00 = normal operation 01 = full power-down 10 = standby 11 = reserved		0x80	Determines various generic modes of chip operation.
0x00A	PLL status	PLL locked status 0=not locked 1=locked	Open	Open	Open	Open	Open	Open	Open	0x00	
0x00D	ADC Test Control Register	Data path user test mode control 0=Continuous pattern mode 1=Single pattern mode	Open	Reset PN long gen 0=enabled 1=held in reset	Reset PN short gen 0=enabled 1=held in reset	Data output test generation mode 0000: Off - Normal Operation 0001: Midscale short 0010: Positive Full-Scale 0011: Negative Full-Scale 0100: Alternating Checker Board 0101: PN Sequence - Long 0110: PN Sequence - Short 0111: 1/0 Word Toggle 1000: User Test Mode 1001-1110: Reserved 1111: Ramp Output				0x00	When this register is set, the test data is placed on the output pins in place of normal data.

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0x00E	BIST enable	Open	Open	Open	Open	Open	BIST init 0=Cascade mode 1=Single mode	Open	BIST enable	0x00	
0x010	Offset adjust	Open	Open	Offset adjust in LSBs from +31 to −32 (twos complement format)						0x00	
0x014	Output mode	Open	Open	Open	Output enable bar	Open	Output invert 0 = normal (default) 1 = inverted	Output format 00 = offset binary 01 = twos complement (default) 10 = Reserved 11 = reserved		0x01	Configures the outputs and the format of the data.
0x015	Output Adjust	Open	Serializer output polarity 0=normal 1=inverted	Serializer emphasis amplitude control 00: 0 mV emphasis differential p-p 01: 40 mV emphasis differential p-p 10: 80 mV emphasis differential p-p 11: 160 mV Amplitude differential p-p		Open	Open	Serializer driver amplitude control 00: 320 mV Amplitude differential p-p 01: 160 mV Amplitude differential p-p 10: 80 mV Amplitude differential p-p 11: 40 mV Amplitude differential p-p		0x00	
0x019	User Test Pattern 1 LSB	User Test Pattern 1[7:0]								0x00	
0x01A	User Test Pattern 1 MSB	User Test Pattern 1[15:8]								0x00	
0x01B	User Test Pattern 2 LSB	User Test Pattern 2[7:0]								0x00	
0x01C	User Test Pattern 2 MSB	User Test Pattern 2[15:8]								0x00	
0x01D	User Test Pattern 3 LSB	User Test Pattern 3[7:0]								0x00	
0x01E	User Test Pattern 3 MSB	User Test Pattern 3[15:8]								0x00	
0x01F	User Test Pattern 4 LSB	User Test Pattern 4[7:0]								0x00	
0x020	User Test Pattern 4 MSB	User Test Pattern 4[15:8]								0x00	
0x024	BIST signature LSB	BIST signature[7:0]								0x00	Read only.
0x025	BIST signature MSB	BIST signature[15:8]								0x00	Read only.

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
0x02C ADC Analog Input Control Register	7:3			
	2	rw	0x0	Analog Input DC Coupling control 0: Analog Input is optimized for AC coupling 1: Analog Input is optimized for DC coupling
	1:0			
0x03A SYSREF Control Register	7	rw	0x0	SYSREF Replace LSB 0: Normal Mode. 1: SYSREF will replace the least significant bit from the converter.

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
	6	rw	0x0	SYSREF Flag Reset 0: Normal Flag Operation 1: SYSREF Flags Held in Reset (setup/hold error flags cleared) Note: SYSREF must be enabled in order for the flags to be used.
	5			
	4	rw	0x0	SYSREF Transition Selection 0: SYSREF is valid on LOW to HIGH transitions using selected CLK edge. 1: SYSREF is valid on HIGH to LOW transitions using selected CLK edge.
	3	rw	0x0	SYSREF Capture Edge Selection 0: Captured on Rising Edge on CLK input 1: Captured on Falling Edge on CLK input
	2	rw	0x0	SYSREF Next Mode 0: Continuous mode 1: Next SYSREF mode - only the next valid edge of SYSREF pin will be used. Subsequent edges of the SYSREF pin will be ignored. Once the next SYSREF has been found, the SYSREF enable bit is cleared.
	1	rw	0x0	SYSREF Enable 0: SYSREF Disabled 1: SYSREF Enabled. If Next SYSREF mode is selected, only the next valid edge of the SYSREF pin will be used. Subsequent edges of the SYSREF pin will be ignored. Once the next SYSREF has been received, this bit will be cleared.
	0			
0x045 Fast Detect Control Register	7:4			
	3	rw	0x0	Force the FD output pin 0: Normal operation of Fast Detect Pin 1: Force a value on FD Pin (see bit[2] below)
	2	rw	0x0	The FD output pin for this channel is set to this value when the output is forced.
	1			
	0	rw	0x0	Enable Fast Detect on Corrected ADC Data 0: Fine Fast Detect Disabled 1: Fine Fast Detect Enabled
0x047 Fast Detect Upper Threshold Register	7:0	rw	0x0	LSBs of Fast Detect Upper Threshold 8 LSBS of the Programmable 12-bit upper threshold that is compared to the fine ADC magnitude
0x048 Fast Detect Upper Threshold Register	7:4			
	3:0	rw	0x0	MSBs of Fast Detect Upper Threshold 4 MSBS of the Programmable 12-bit upper threshold that is compared to the fine ADC magnitude

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
0x049 Fast Detect Lower Threshold Register	7:0	rw	0x0	LSBs of Fast Detect Lower Threshold 8 LSBS of the Programmable 12-bit lower threshold that is compared to the fine ADC magnitude
0x04A Fast Detect Lower Threshold Register	7:4			
	3:0	rw	0x0	MSBs of Fast Detect Lower Threshold 4 MSBS of the Programmable 12-bit lower threshold that is compared to the fine ADC magnitude
0x04B Fast Detect Dwell Time Counter Threshold Register	7:0	rw	0x0	LSBs of Fast Detect Dwell Time Counter Target This is a load value for a 16-bit counter that determines how long the ADC data must remain below the lower threshold before the FD pin is reset to 0
0x04C Fast Detect Dwell Time Counter Threshold Register	7:0	rw	0x0	MSBs of Fast Detect Dwell Time Counter Target.This is a load value for a 16-bit counter that determines how long the ADC data must remain below the lower threshold before the FDDx pins are reset to 0 Note: Fast Detect pin will deassert after the ADC codes stay below the lower target for this number of samples.

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
0x05E JESD204B Quick Configuration Register	7:0	rw	0x0	JESD204B Serial Quick Configuration (self clearing) 0x00: Configuration determined by other registers. Since register is self-clearing, it will always return to this value after each write. 0x02: Generic 2 Lane 0x04: Generic 4 Lane Config 0x06: Generic 6 Lane Config 0x08: Generic 8 Lane Config 0x48: FSx2 Mode - 8 Lanes 0x81: 1 WBT (High BW) 1 Lane 0x82: 1 WBT (High BW) 2 Lanes 0x91: 1 WBT (Low BW) 1 Lane 0xC1: 2 WBTs (High BW) 1 Lane 0xC2: 2 WBTs (High BW) 2 Lanes 0xC4: 2 WBTs (High BW) 4 Lanes 0xD1: 2 WBTs (Low BW) 1 Lane 0xD2: 2 WBTs (Low BW) 2 Lanes 0xE1: 2 WBTs (Mixed BW) 1 Lane 0xE2: 2 WBTs (Mixed BW) 2 Lanes. 0xE4: 2 WBTs (Mixed BW) 4 Lanes. All other values have no effect. Note: This register is self-clearing and does not control anything in the AD9625 directly. It only changes the value of the other registers which control the chip. Since this register is self-clearing, it will always return to 000 after each write. To use the quick configuration feature, write to this register first, then if there are any changes that need to be made to the settings above, write to the other registers. Finally to update the device with the configuration, write to the transfer bit.
0x05F JESD204B Link Control Register #1	7			
	6	rw	0x0	JESD204B Serial Tail Bit PN Enable 0: Serial Tail Bit PN Disabled. Unused extra tail bits will be padded with zeros. 1: Serial Tail Bit PN Enabled. Unused extra tail bits will be padded with a Psuedo-Random Number Sequence from a 31-bit LFSR. Note: The following equation can be used to determine the number of tail bits sent per sample = N' - N - CS
	5	rw	0x0	JESD204B Serial Test Sample Enable 0: JESD204B Test Samples Disabled 1: JESD204B Test Samples Enabled – Long Transport Layer Test Sample Sequence sent on all link lanes.

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
	4	rw	0x1	JESD204B Serial Lane Synchronization Enable 0: Lane Synchronization Disabled. Both sides do NOT perform lane sync, Frame Alignment Character Insertion always uses /K28.7/ control characters 1: Lane Synchronization Enabled. Both sides perform lane sync, Frame Alignment Character Insertion uses either /K28.3/ or /K28.7/ control characters Note: Frame Character Insertion must be enabled in order to enable lane synchronization.
	3:2	rw	0x1	JESD204B Serial Initial Lane Alignment Sequence Mode 00: Initial Lane Alignment Sequence Disabled 01: Initial Lane Alignment Sequence Enabled 10: Reserved 11: Initial Lane Alignment Sequence Always On Test Mode - JESD204B Data Link Layer Test Mode uses repeated lane alignment sequence sent on all lanes.
	1	rw	0x0	JESD204B Serial Frame Alignment Character Insertion (FACI) Disable 0: Frame Alignment Character Insertion Enabled 1: Frame Alignment Character Insertion Disabled - For Debug Only
	0	rw	0x0	JESD204B Serial Transmit Link Power Down (active high) 0: JESD204B Serial Transmit Link Enabled. Transmission of the /K28.5/ characters for code group synchronization will be controlled by the SYNCINB pin. 1: JESD204B Serial Transmit Link Powered Down (held in reset and clock gated). Note: The JESD204B transmitter link MUST be powered down while changing any of the Link Configuration Bits.
0x060 JESD204B Link Control Register #2	7:6	rw	0x0	JESD204B Serial Sync Mode 00: Normal Mode. 01: Reserved 10: SYNCINB Active Mode. SYNCINB signal is forced - force code group synchronization. 11: SYNCINB Pin Disabled.
	5	rw	0x0	JESD204B Serial Sync Pin Invert 0: SYNCINB Pin NOT inverted. 1: SYNCINB Pin Inverted.
	4:3			
	2	rw	0x0	JESD204B Serial 8b/10b Bypass (Test Mode Only) 0: 8b/10b enabled 1: 8b/10b bypassed (Most significant 2 bits are 0)
	1	rw	0x0	JESD204B 10b Serial Transmit Bit Invert 0: Normal 1: Invert "a b c d e f g h i j" bits. Note: this will effectively invert the differential outputs from the PHY in case the CML signals are reversed.

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
	0	rw	0x0	JESD204B 10b Serial Transmit Bit Mirror 0: 10b serial bits are Not mirrored. Transmit bit order is "a b c d e f g h i j". 1: 10b Serial bits are are mirrored. Transmit bit order is "j i h g f e d c b a".
0x061 JESD204B Link Control Register #3	7	rw	0x0	JESD204B Checksum Disable 0: CHKSUM enabled in link configuration parameter. Normal operation. 1: CHKSUM disabled in link configuration parameter (set to zero). For testing purposes only.
	6			
	5:4	rw	0x0	JESD204B Serial Test Generation Input Selection 00: 16-bit Test Generation Data injected at sample input to the link 01: 10-bit Test Generation Data injected at output of 8b/10b encoder (at input to PHY) 10: 8-bit Test Generation Data injected at Input of Scrambler 11: Reserved
	3:0	rw	0x0	JESD204B Serial Test Generation Mode 0000: Normal Operation (test mode disabled) 0001: Alternating Checker Board 0010: 1/0 Word Toggle 0011: PN Sequence - Long 0100: PN Sequence - Short 0101: Continuous/Repeat User Test Mode - Most significant bits from User Pattern (1,2,3,4) placed on the output for 1 clock cycle and then repeat. (Output User Pattern 1, 2, 3, 4, 1, 2, 3, 4, 1, 2, 3, 4, ...etc.) 0110: Single User Test Mode - Most significant bits from User Pattern (1,2,3,4) placed on the output for 1 clock cycle and then output all zeros. (Output User Pattern 1, 2, 3, 4, then output all zeros) 0111: Ramp Output 1000: Modified RPAT Test Sequence - 10bit value. Must be used with reg 0x061(5:4) = 01 (output of 8b/10b) 1001: Unused 1010: JSPAT Test Sequence - 10bit value. Must be used with reg 0x061(5:4= 01 (output of 8b/10b) 1011: JTSPAT Test Sequence - 10bit value. Must be used with reg 0x061(5:4_sel = 01 (output of 8b/10b) 1100-1111: Unused
0x062 JESD204B Link Control Register #4	7:0	rw	0x0	Initial Lane Alignment Sequence Repeat Count Specifies the number of times the Initial Lane Alignment Sequence is repeated.
0x063 JESD204B Link Control Register #5	7			
	6:4			

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
	3:0	rw	0x0	JESD204B Application Layer Mode 0000: Generic - No application layer used. 0001-0011: Unused 0100: FSx2 Mode 0101-0111: Unused 1000: Single Wide Band Tuner Mode - High Bandwidth Mode (only WBT0 used) 1001: Single Wide Band Tuner Mode - Low Bandwidth Mode (only WBT0 used) 1010-1011: Unused 1100: Dual (2) Wide Band Tuner Mode - High Bandwidth Mode (both WBT0 and WBT1 used) 1101: Dual (2) Wide Band Tuner Mode - Low Bandwidth Mode (both WBT0 and WBT1 used) 1110: Dual (2) Wide Band Tuner Mode - Mixed Bandwidth Mode (WBT0 High Bandwidth Mode, WBT1 Low Bandwidth Mode - samples repeated) 1111: Unused Wideband Tuner Bandwidth Modes: High Bandwidth - Decimate by 8 (Effective Output Bandwidth = Fs/10) Low Bandwidth - Decimate by 16 (Effective Output Bandwidth = Fs/20)
0x064 JESD204B Configuration Register	7:0	rw	0x0	JESD204B Serial Device IDentification (DID) number. Updated whenever the CHIP_ID_ENG register is written.
0x065 JESD204B Configuration Register	7:4			
	3:0	rw	0x0	JESD204B Serial Bank IDentification (BID) number. (extension to DID)
0x066 JESD204B Configuration Register	7:5			
	4:0	rw	0x0	JESD204B Serial Lane IDentification (LID) number for Lane 0. (Only valid with 8 lane JESD204B output)
0x067 JESD204B Configuration Register	7:5			
	4:0	rw	0x1	JESD204B Serial Lane IDentification (LID) number for Lane 1. (Only valid with 8 lane JESD204B output)
0x068 JESD204B Configuration Register	7:5			
	4:0	rw	0x2	JESD204B Serial Lane IDentification (LID) number for Lane 2. (Only valid with 8 lane JESD204B output)
0x069 JESD204B Configuration Register	7:5			
	4:0	rw	0x3	JESD204B Serial Lane IDentification (LID) number for Lane 3. (Only valid with 8 lane JESD204B output)
0x06A JESD204B Configuration Register	7:5			
	4:0	rw	0x4	JESD204B Serial Lane IDentification (LID) number for Lane 4. (Only valid with 8 lane JESD204B output)
0x06B	7:5			

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
JESD204B Configuration Register	4:0	rw	0x5	JESD204B Serial Lane IDentification (LID) number for Lane 5. (Only valid with 8 lane JESD204B output)
0x06C	7:5			
JESD204B Configuration Register	4:0	rw	0x6	JESD204B Serial Lane IDentification (LID) number for Lane 6. (Only valid with 8 lane JESD204B output)
0x06D	7:5			
JESD204B Configuration Register	4:0	rw	0x7	JESD204B Serial Lane IDentification (LID) number for Lane 7. (Only valid with 8 lane JESD204B output)
0x06E JESD204B Configuration Register	7	rw	0x1	JESD204B Serial Scrambler Mode 0:JESD204B Scrambler Disabled. 1:JESD204B Scrambler Enabled.
	6:5			
	4:0	rw	0x7	JESD204B Serial Lane Control 0: One Lane per Link. (L=1) 1: Two Lanes per Link. (L=2) 2: Unused 3: Four Lanes per Link. (L=4) 4: Unused 5: Six Lanes per Link. (L=6) 6: Unused 7: Eight Lanes per Link. (L=8) 8-31: Unused
0x06F JESD204B Configuration Register	7:0	ro	0x0	JESD204B Number of Octets per frame - Read only bits. For the chip, these bits are calculated based on the following equation: F= (N')/(2*L) Note: The following table shows the valid values of F: M=1;S=4;N'=16;L=1; F=8 M=1;S=4;N'=16;L=2; F=4 M=1;S=4;N'=16;L=4; F=2 M=1;S=4;N'=12;L=6; F=1 M=1;S=4;N'=16;L=8; F=1 (default)
0x070	7:5			
JESD204B Configuration Register	4:0	rw	0x1F	JESD204B Number of frames per multiframe. Only values which are divisible by 4 can be used.
0x071 JESD204B Configuration	7:0	ro	0x0	JESD204B Number of converters per link/device 0: Link connected to one ADC. (M=1) 1-255: Unused

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
Register				
0x072 JESD204B Configuration Register	7:6	rw	0x0	JESD204B Number of control bits per sample. 00: No control bits sent per sample 01: One control bits sent per sample - Over-Range Bit Enabled. 10: Two control bits sent per sample - Over-Range + Timestamp SYSREF Bit 11: Three control bits sent per sample - Over-Range + Timestamp SYSREF Bit + Data Valid - Debug Only
	5			
	4:0	rw	0xB	JESD204B Converter Resolution 0x0-0x6: Reserved 0x07: N=8-bit ADC Converter Resolution 0x08: Reserved 0x09: N=10-bit ADC Converter Resolution 0x0A: Reserved 0x0B: N=12-bit ADC Converter Resolution 0x0C: Reserved 0x0D: N=14-bit ADC Converter Resolution 0x0E: Reserved 0x0F: N=16-bit ADC Converter Resolution (used in WBT modes) 0x10-0x1F: Reserved
0x073 JESD204B Configuration Register	7:5	rw	0x1	JESD204B Device Subclass Version 0x0: Subclass 0 0x1: Subclass 1 (default) 0x2: Subclass 2 (not supported) 0x3: Undefined
	4:0	rw	0xF	JESD204B Total number of bits per sample 0x0-0xA: Unused 0xB: N'=12 (L must be = 6) 0xC-0xE: Unused 0xF: N'=16 (L must be = 1,2,4, or 8)
0x074 JESD204B Configuration Register	7:5	rw	0x1	JESD204B Version 0x0: JESD204A - SYNCINB Input is internally gated by Frame Clock. SYNCINB must be low for at least 2 Frame Clock cycles to be interpreted as a synchronization request. 0x1: JESD204B - SYNCINB Input is internally gated by Local Multi-Frame Clock. SYNCINB must be low for at least 4 Frame Clock cycles to be interpreted as a synchronization request. 0x2-0x7: Undefined
	4:0	ro	0x3	JESD204B Samples Per Converter Frame Cycle Read only bits. Always S=4 for AD9625.

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
0x075 JESD204B Configuration Register	7	ro	0x1	JESD204B High Density Format (HD) - Read only bit. 0: High Density Format Disabled 1: High Density Format Enabled High density mode is automatically enabled based on the values of N' and L. Note: The following table shows the values of HD for the AD9625: N'=16;L=1; HD=0 N'=16;L=2; HD=0 N'=16;L=4; HD=0 N'=12;L=6; HD=1 N'=16;L=8; HD=1 (default)
	6:5			
	4:0	ro	0x0	JESD204B Number of control words per frame clock cycle per link (CF) - Read only bits. Always CF=0 for the AD9625.
0x076 JESD204B Configuration Register	7:0	rw	0x0	JESD204B Serial Reserved Field #1 (RES1)
0x077 JESD204B Configuration Register	7:0	rw	0x0	JESD204B Serial Reserved Field #2 (RES2)
0x078 JESD204B Configuration Register	7:0	ro	0xC3	JESD204B Serial Checksum Value for Lane 0. Automatically calculated for each lane. Sum(all link configuration parameters for Lane 0) mod 256. Checksum is disabled by setting the reg 0x061 (7) = 1.
0x079 JESD204B Configuration Register	7:0	ro	0xC4	JESD204B Serial Checksum Value for Lane 1. Automatically calculated for each lane. Sum(all link configuration parameters for Lane 1) mod 256. Checksum is disabled by setting the reg 0x061 (7) = 1.
0x07A JESD204B Configuration Register	7:0	ro	0xC5	JESD204B Serial Checksum Value for Lane 2. Automatically calculated for each lane. Sum(all link configuration parameters for each lane) mod 256. Checksum is disabled by setting the reg 0x061 (7) = 1.
0x07B JESD204B Configuration Register	7:0	ro	0xC6	JESD204B Serial Checksum Value for Lane 3. Automatically calculated for each lane. Sum(all link configuration parameters for Lane 3) mod 256. Checksum is disabled by setting the reg 0x061 (7) = 1.
0x07C JESD204B Configuration Register	7:0	ro	0xC7	JESD204B Serial Checksum Value for Lane 4. Automatically calculated for each lane. Sum(all link configuration parameters for Lane 4) mod 256. Checksum is disabled by setting the reg 0x061 (7) = 1.

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
0x07D JESD204B Configuration Register	7:0	ro	0xC8	JESD204B Serial Checksum Value for Lane 5. Automatically calculated for each lane. Sum(all link configuration parameters for Lane 5) mod 256. Checksum is disabled by setting the reg 0x061 (7) = 1.
0x07E JESD204B Configuration Register	7:0	ro	0xC9	JESD204B Serial Checksum Value for Lane 6. Automatically calculated for each lane. Sum(all link configuration parameters for Lane 6) mod 256. Checksum is disabled by setting the reg 0x061 (7) = 1.
0x07F JESD204B Configuration Register	7:0	ro	0xCA	JESD204B Serial Checksum Value for Lane 7. Automatically calculated for each lane. Sum(all link configuration parameters for Lane 7) mod 256. Checksum is disabled by setting the reg 0x061 (7) = 1.
0x080 JESD204B Lane Power Down	7	rw	0x0	Physical Lane SERDOUT[7] Power Down 0: Lane SERDOUT[7] Enabled 1: Lane SERDOUT[7] Powered Down
	6	rw	0x0	Physical Lane SERDOUT[6] Power Down 0: Lane SERDOUT[6] Enabled 1: Lane SERDOUT[6] Powered Down
	5	rw	0x0	Physical Lane SERDOUT[5] Power Down 0: Lane SERDOUT[5] Enabled 1: Lane SERDOUT[5] Powered Down
	4	rw	0x0	Physical Lane SERDOUT[4] Power Down 0: Lane SERDOUT[4] Enabled 1: Lane SERDOUT[4] Powered Down
	3	rw	0x0	Physical Lane SERDOUT[3] Power Down 0: Lane SERDOUT[3] Enabled 1: Lane SERDOUT[3] Powered Down
	2	rw	0x0	Physical Lane SERDOUT[2] Power Down 0: Lane SERDOUT[2] Enabled 1: Lane SERDOUT[2] Powered Down
	1	rw	0x0	Physical Lane SERDOUT[1] Power Down 0: Lane SERDOUT[1] Enabled 1: Lane SERDOUT[1] Powered Down
	0	rw	0x0	Physical Lane SERDOUT[0] Power Down 0: Lane SERDOUT[0] Enabled 1: Lane SERDOUT[0] Powered Down
0x082	7			

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
JESD204B Lane Control Register #1 (Only valid with 8 lane JESD204B output)	6:4	rw	0x1	Physical Lane SERDOUT[1] Assignment 000: Logical Lane 0 001: Logical Lane 1 (default) 010: Logical Lane 2 011: Logical Lane 3 100: Logical Lane 4 101: Logical Lane 5 110: Logical Lane 6 111: Logical Lane 7
	3			
	2:0	rw	0x0	Physical Lane SERDOUT[0] Assignment 000: Logical Lane 0 (default) 001: Logical Lane 1 010: Logical Lane 2 011: Logical Lane 3 100: Logical Lane 4 101: Logical Lane 5 110: Logical Lane 6 111: Logical Lane 7
0x083 JESD204B Lane Control Register #2 (Only valid with 8 lane JESD204B output)	7			
	6:4	rw	0x3	Physical Lane SERDOUT[3] Assignment 000: Logical Lane 0 001: Logical Lane 1 010: Logical Lane 2 011: Logical Lane 3 (default) 100: Logical Lane 4 101: Logical Lane 5 110: Logical Lane 6 111: Logical Lane 7
	3			
	2:0	rw	0x2	Physical Lane SERDOUT[2] Assignment 000: Logical Lane 0 001: Logical Lane 1 010: Logical Lane 2 (default) 011: Logical Lane 3 100: Logical Lane 4 101: Logical Lane 5 110: Logical Lane 6 111: Logical Lane 7
0x084	7			

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
JESD204B Lane Control Register #3 (Only valid with 8 lane JESD204B output)	6:4	rw	0x5	Physical Lane SERDOUT[5] Assignment 000: Logical Lane 0 001: Logical Lane 1 010: Logical Lane 2 011: Logical Lane 3 100: Logical Lane 4 101: Logical Lane 5 (default) 110: Logical Lane 6 111: Logical Lane 7
	3			
	2:0	rw	0x4	Physical Lane SERDOUT[4] Assignment 000: Logical Lane 0 001: Logical Lane 1 010: Logical Lane 2 011: Logical Lane 3 100: Logical Lane 4 (default) 101: Logical Lane 5 110: Logical Lane 6 111: Logical Lane 7
0x085 JESD204B Lane Control Register #4 (Only valid with 8 lane JESD204B output)	7			
	6:4	rw	0x7	Physical Lane SERDOUT[7] Assignment 000: Logical Lane 0 001: Logical Lane 1 010: Logical Lane 2 011: Logical Lane 3 100: Logical Lane 4 101: Logical Lane 5 110: Logical Lane 6 111: Logical Lane 7 (default)
	3			
	2:0	rw	0x6	Physical Lane SERDOUT[6] Assignment 000: Logical Lane 0 001: Logical Lane 1 010: Logical Lane 2 011: Logical Lane 3 100: Logical Lane 4 101: Logical Lane 5 110: Logical Lane 6 (default) 111: Logical Lane 7
0x088 JESD204B	7:0	rw	0x67	Frame Sync. Bits 7:4: Unused

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
Frame Sync Least Significant Byte Register				Bits 3:0: Used in application layer FSx2
0x089 Unused	7:0	rw	0xF0	Unused
0x08A JESD204B SYSREF Control Register	7:6			
	5:4	rw	0x0	JESD204B SYSREF Serializer Reset Control 00: JESD SYSREF Serializer Reset Enabled Mode - SYSREF Resets Output Lane Serializers and Lane FIFOs. SYSREF cannot be used as a periodic signal at integer multiples of the LMFC rate. Delay uncertainty through the chip is minimized. 01: JESD SYSREF Serializer Reset Gated Mode - SYSREF Resets Output Lane Serializers and Lane FIFOs only when SYNCINB is low. 10: JESD SYSREF Serializer Reset Disabled Mode - SYSREF Does Not Reset Output Lane Serializers or Lane FIFOs. SYSREF can be used as a periodic signal at integer multiples of the LMFC rate. However, delay uncertainty is increased. 11: Reserved
	3:2			
	1:0	rw	0x0	JESD204B SYSREF Clock Reset Mode 00: JESD SYSREF Clock Reset Enabled Mode - Local Multi-Frame Clock (LMFC) and Frame Clock are reset whenever SYSREF comes in. Frame alignment variable delay buffer enabled. 01: JESD SYSREF Clock Reset Gated Mode - LMFC and Frame Clock are reset only when SYNCINB is low. This may help a system integrator if they choose to have LMFC reset only when the link is being established. Frame alignment variable delay buffer enabled when SYNCINB is low. 10: JESD SYSREF Clock Reset Disabled Mode - LMFC and Frame Clock are never reset by a SYSREF event. This mode is used by the ramp test mode for deterministic latency or if the system designer wants to simply use SYSREF as a timestamp and not for deterministic latency. While in this mode, the Frame alignment variable delay buffer is disabled. 11: Reserved
0x08B	7:5			
JESD204B Local Multi-Frame Clock Offset Control Register	4:0	rw	0x00	Local Multi-Frame Clock (LMFC) Phase Offset Value. Reset value for LMFC Phase counter when SYSREF is asserted. Used for deterministic delay applications.
0x08C JESD204B Local Frame Clock Offset Control Register	7:0	rw	0x00	Local Frame Clock Phase Offset Value. Reset value for Frame Clock Phase counter when SYSREF is asserted. For the AD9625, only values from 0-7 are valid. Used for deterministic delay applications.
0x0F0	7:5			

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
JESD204B Link Built-In Self Test Control Register	4	rw	0x0	JESD204B Built-In Self Test Length 0: 512 Cycles 1: 1024 Cycles
	3			
	2	rw	0x0	JESD204B Built-In Self Test Initialization0: Cascade Mode. CRC are not cleared before each BIST cycle. This mode makes it possible to cascade multiple tests together and view the final results.1: Single Mode. CRC cleared before each BIST cycle.
	1			
	0	rw	0x0	JESD204B Link Built-In Self Test Enable 0: BIST Disabled 1: BIST Enabled. Self-cleared after BIST has completed.
0x0F1 JESD204B Link CRC LSB Register	7:0	ro	0x00	Least Significant Cyclic Redundancy Check (CRC) Bits These bits are used in conjunction with the Built-In Self Test (BIST) inside the design.
0x0F2 JESD204B Link CRC MSB Register	7:0	ro	0x00	Most Significant Cyclic Redundancy Check (CRC) Bits These bits are used in conjunction with the Built-In Self Test (BIST) inside the design.
0x0F8 Customer Spare Register	7:0	rw	0x0	Spare Customer Register.
0x0F9 Customer Spare Register	7:0	rw	0x0	Spare Customer Register.
0x0FF Device Update Register	7:1			
	0	rw	0x0	Register Map Master/Slave Transfer bit Self-clearing bit used to synchronize the transfer of data from the master to the slave registers. 0: No effect 1: Transfer data from the master registers written by the register maps to the slave registers.
0x100 Interrupt Request (IRQ) Status Register	7	ro	0x0	Interrupt Request PLL Lock Error 1: The PLL is unlocked. Note: this bit is ignored if the corresponding mask bit is set in register 0x101.
	6			
	5	ro	0x0	Interrupt Request - Background Digital Calibration Routine is running 1: Background Digital Calibration Routine is running. Note: this bit is ignored if the corresponding mask bit is set in register 0x101.
	4	ro	0x0	Interrupt Request - Foreground Digital Calibration Routine is running1: Foreground Digital Calibration Routine is running.

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
				Note: this bit is ignored if the corresponding mask bit is set in register 0x101.
	3	ro	0x0	Interrupt Request SYSREF Hold Error 1: A hold error has occurred with the last SYSREF signal received. To clear this error, reg 0x03A(6) must be 1. Note: this bit is ignored if the corresponding mask bit is set in register 0x101.
	2	ro	0x0	Interrupt Request SYSREF Setup Error 1: A setup error has occurred with the last SYSREF signal received. To clear this error, reg 0x03A(6) must be 1. Note: this bit is ignored if the corresponding mask bit is set in register 0x101.
	1			
	0	ro	0x0	Interrupt Request Fatal Error 1: A fatal error has occurred and the validity of the output data cannot be guaranteed. The only way to recover from this error is to reset the device. Note: this bit is ignored if the corresponding mask bit is set in register 0x101.
0x101 Interrupt Request (IRQ) Mask Control Register	7	rw	0x1	Interrupt Request PLL Lock Error Masked 1: PLL unlocked events will be masked.
	6			
	5	rw	0x1	Interrupt Request - Mask Background Digital Calibration Routine 1: Background Digital Calibration Routine status will be masked
	4	rw	0x1	Interrupt Request - Foreground Digital Calibration Routine is running 1: Foreground Digital Calibration Routine is running.
	3	rw	0x1	Interrupt Request SYSREF Hold Error 1: A hold error has occurred with the last SYSREF signal received. To clear this error, resend the SYSREF signal.
	2	rw	0x1	Interrupt Request SYSREF Setup Error 1: A setup error has occurred with the last SYSREF signal received. To clear this error, resend the SYSREF signal.
	1			

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
	0	rw	0x0	Interrupt Request Fatal Error Mask1: A fatal error has occurred and the validity of the output data cannot be guaranteed. The only way to recover from this error is to reset the device.
0x102 Digital Calibration Background Control Register	7:6	rw	0x1	Background Channel Gain Calibration Mode 0x0: Reserved 0x1: Calibration estimation based on relative internal gain. 0x2: Calibration estimation based on relative external gain 0x3: Reserved
	5:4	rw	0x0	Background Channel Offset Calibration Mode 0x0: Calibration estimation based on absolute offset. 0x1: Calibration estimation based on relative internal offset. 0x2: Calibration estimation based on relative external 0x3: Reserved
	3:2	rw	0x1	Foreground Channel Gain Calibration Mode 0x0: Reserved 0x1: Calibration estimation based on relative internal gain. 0x2: Calibration estimation based on relative external gain 0x3: Reserved
	1:0	rw	0x0	Foreground Channel Offset Calibration Mode 0x0: Calibration estimation based on absolute offset. 0x1: Calibration estimation based on relative internal offset. 0x2: Calibration estimation based on relative external offset 0x3: Reserved
0x103 Digital Calibration Reference Channel Selection Register	7:2			
	1:0	rw	0x0	Digital Calibration Reference Channel Selection 0x0: Channel A Selected as Reference Channel 0x1: Channel B Selected as Reference Channel 0x2: Channel C Selected as Reference Channel 0x3: Channel D Selected as Reference Channel
0x104 Digital Calibration Foreground Force Control Register	7	rw	0x0	Foreground Stage 3 DAC Calibration Force1: Force Foreground Calibration On (rising edge detected - design checks for disabled to enabled transition)0: Normal operation.
	6	rw	0x0	Foreground Stage 2 DAC Calibration Force 1: Force Foreground Calibration On (rising edge detected - design checks for disabled to enabled transition) 0: Normal operation.
	5	rw	0x0	Foreground Stage 1 DAC Calibration Force 1: Force Foreground Calibration On (rising edge detected - design checks for disabled to enabled transition) 0: Normal operation.

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
	4	rw	0x0	Foreground Stage 3 Gain Error Calibration Force 1: Force Foreground Calibration On (rising edge detected - design checks for disabled to enabled transition) 0: Normal operation.
	3	rw	0x0	Foreground Stage 2 Gain Error Calibration Force 1: Force Foreground Calibration On (rising edge detected - design checks for disabled to enabled transition) 0: Normal operation.
	2	rw	0x0	Foreground Stage 1 Gain Error Calibration Force 1: Force Foreground Calibration On (rising edge detected - design checks for disabled to enabled transition) 0: Normal operation.
	1	rw	0x0	Foreground Channel Gain Calibration Force 1: Force Foreground Calibration On (rising edge detected - design checks for disabled to enabled transition) 0: Normal operation.
	0	rw	0x0	Foreground Channel Offset Calibration Force1: Force Foreground Calibration On (rising edge detected - design checks for disabled to enabled transition)0: Normal operation
0x105 Digital Calibration Background Control Register	7:5			
	4	rw	0x1	Background Stage 3 Gain Error Calibration Disable 1: Calibration Disabled. 0: Calibration Enabled.
	3	rw	0x0	Background Stage 2 Gain Error Calibration Disable 1: Calibration Disabled. 0: Calibration Enabled.
	2	rw	0x0	Background Stage 1 Gain Error Calibration Disable 1: Calibration Disabled. 0: Calibration Enabled.
	1	rw	0x0	Background Channel Gain Calibration Disable 1: Calibration Disabled. 0: Calibration Enabled.
	0	rw	0x0	Background Channel Offset Calibration Disable 1: Calibration Disabled. 0: Calibration Enabled.
0x106 Digital Calibration Offset Estimate Register	7:0	rw	0x0	Relative Customer Offset estimate for digital calibration routines.

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
0x107 Digital Calibration Offset Estimate Register	7:0	rw	0x0	Relative Customer Offset estimate for digital calibration routines.
0x108 Digital Calibration Gain Estimate Register	7:0	rw	0x0	Relative Customer Gain estimate for digital calibration routines.
0x109 Digital Calibration Gain Estimate Register	7:0	rw	0x40	Relative Customer Gain estimate for digital calibration routines.
0x10A Digital Calibration Threshold Control Register (TBD)	7			
	6	rw	0x0	Enable sample timeout logic for bgnd ch
	5	rw	0x0	Enable sample threshold logic for bgnd ch
	4	rw	0x0	Enable data set threshold logic for bgnd ch
	3			
	2	rw	0x0	Enable sample timeout logic for fgnd ch gain
	1	rw	0x0	Enable sample threshold logic for fgnd ch gain
	0	rw	0x0	Enable data set threshold logic for fgnd ch
0x10B Digital Calibration Data Set Threshold Register	7:0	rw	0x0	Data set threshold for fgnd ch gain cal
0x10C Digital Calibration Data Set Threshold Register	7:0	rw	0x0	Data set threshold for fgnd ch gain cal
0x10D Digital Calibration Data Set Threshold Register	7:0	rw	0x0	Data set threshold for bgnd ch gain cal
0x10E Digital Calibration Data Set	7:0	rw	0x0	Data set threshold for bgnd ch gain cal

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
Threshold Register				
0x10F Digital Calibration Sample Threshold Register	7:0	rw	0x0	Sample threshold for fgnd ch gain cal
0x110 Digital Calibration Sample Threshold Register	7:0	rw	0x0	Sample threshold for fgnd ch gain cal
0x111 Digital Calibration Sample Threshold Register	7:0	rw	0x0	Sample threshold for bgnd ch gain cal
0x112 Digital Calibration Sample Threshold Register	7:0	rw	0x0	Sample threshold for bgnd ch gain cal
0x113 Digital Calibration Sample Timeout Register	7:0	rw	0x0	Sample timeout count for fgnd ch gain cal
0x114 Digital Calibration Sample Timeout Register	7:0	rw	0x0	Sample timeout count for fgnd ch gain cal
0x115 Digital Calibration Sample Timeout Register	7:0	rw	0x0	Sample timeout count for bgnd ch gain cal
0x116 Digital Calibration	7:0	rw	0x0	Sample timeout count for bgnd ch gain cal

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
Sample Timeout Register				
0x118 Digital Calibration Foreground Status Register	7	ro	0x0	Foreground Stage 3 DAC Calibration Status 1: Calibration currently running. 0: Calibration finished or not started.
	6	ro	0x0	Foreground Stage 2 DAC Calibration Status 1: Calibration currently running. 0: Calibration finished or not started.
	5	ro	0x0	Foreground Stage 1 DAC Calibration Status 1: Calibration currently running. 0: Calibration finished or not started.
	4	ro	0x0	Foreground Stage 3 Gain Error Calibration Status 1: Calibration currently running. 0: Calibration finished or not started.
	3	ro	0x0	Foreground Stage 2 Gain Error Calibration Status 1: Calibration currently running. 0: Calibration finished or not started.
	2	ro	0x0	Foreground Stage 1 Gain Error Calibration Status 1: Calibration currently running. 0: Calibration finished or not started.
	1	ro	0x0	Foreground Channel Gain Calibration Status 1: Calibration currently running. 0: Calibration finished or not started.
	0	ro	0x0	Foreground Channel Offset Calibration Status1: Calibration currently running.0: Calibration finished or not started.
0x119 Digital Calibration Background Status Register	7:5			
	4	ro	0x0	Background Stage 3 Gain Error Calibration Status 1: Calibration currently running. 0: Calibration finished or not started.
	3	ro	0x0	Background Stage 2 Gain Error Calibration Status 1: Calibration currently running. 0: Calibration finished or not started.
	2	ro	0x0	Background Stage 1 Gain Error Calibration Status 1: Calibration currently running. 0: Calibration finished or not started.
	1	ro	0x0	Background Channel Gain Calibration Status 1: Calibration currently running. 0: Calibration finished or not started.

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
	0	ro	0x0	Background Channel Offset Calibration Status 1: Calibration currently running. 0: Calibration finished or not started.
0x11F ADC Spare Customer Control Register	7:0	rw	0x0	Spare Customer Register.
0x120 Clock Divider Output Control Register	7:5			
	4	rw	0x0	Clock Divider Output Disable 0: CLKDIV output is disabled. 1: CLKDIV output is enabled.
	3	rw	0x0	Clock Divider Output Termination Selection 0: CLKDIV output uses an external 100 ohm resistive termination 1: CLKDIV output uses no external resistive termination
	2			
	1:0	rw	0x1	Control the differential swing for the CLKDIV output. 00 = 1/4*Full Swing 01 = 1/2*Full Swing 10 = 3/4*Full Swing 11 = Full Swing
0x130 Wideband Tuner 0 Gain Control Register	7:6			
	5:4	rw	0x0	Wideband Tuner 0 Polyphase (Decimate by 2) Gain in units of 6dB. 00: 0 dB Gain 01: 6 dB Gain 10: 12 dB Gain 11: 18 dB Gain
	3:2			
	1:0	rw	0x0	Wideband Tuner 0 Polyphase (Decimate by 8) Gain in units of 6dB. 00: 0 dB Gain 01: 6 dB Gain 10: 12 dB Gain 11: 18 dB Gain
0x131 Wideband Tuner 0 Phase Increment	7:0	rw	0x0	Wideband Tuner 0 NCO Phase Increment Value. Phase increment for the NCO within Wide Band tuner 0. If 10-bit value is N then the phase-increment corresponds to 2*pi/N. The output frequency = (Wideband Tuner 0 NCO Phase Increment Value * Fs) / 1024

Register Address (hex) and Name	Bit Location	Field Access	Field Default (hex)	Field Description
Least Significant Bits				
0x132 Wideband Tuner 0 Phase Increment Most Significant Bits	7:2			
	1:0	rw	0x0	Wideband Tuner 0 NCO Phase Increment Value. Phase increment for the NCO within Wide Band Tuner 0. If 10-bit value is N then the phase-increment corresponds to 2*pi/N. The output frequency = (Wideband Tuner 0 NCO Phase Increment Value * Fs) / 1024
0x138 Wideband Tuner 1 Gain Control Register	7:6			
	5:4	rw	0x0	Wideband Tuner 1 Polyphase (Decimate by 2) Gain in units of 6dB. 00: 0 dB Gain01: 6 dB Gain10: 12 dB Gain11: 18 dB GainNote:
	3:2			
	1:0	rw	0x0	Wideband Tuner 1 Polyphase (Decimate by 8) Gain in units of 6dB. 00: 0 dB Gain 01: 6 dB Gain 10: 12 dB Gain 11: 18 dB Gain
0x139 Wideband Tuner 1 Phase Increment Least Significant Bits	7:0	rw	0x0	Wideband Tuner 1 NCO Phase Increment Value. Phase increment for the NCO within Wide Band Tuner 1. If 10-bit value is N then the phase-increment corresponds to 2*pi/N. The output frequency = (Wideband Tuner 1 NCO Phase Increment Value * Fs) / 1024
0x13A Wideband Tuner 1 Phase Increment Most Significant Bits	7:2			
	1:0	rw	0x0	Wideband Tuner 1 NCO Phase Increment Value. Phase increment for the NCO within Wide Band tuner 0. If 10-bit value is N then the phase-increment corresponds to 2*pi/N. The output frequency = (Wideband Tuner 1 NCO Phase Increment Value * Fs) / 1024

MEMORY MAP REGISTER DESCRIPTION

For more information on functions controlled in Register 0x00 to Register 0x25, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

THEORY OF OPERATION

ADC ARCHITECTURE

AD9625 is a 12-bit pipeline ADC.

TEMPERATURE SENSOR (VMON)

The VMON circuitry on AD9625 can be used to monitor AD9625 die temperature. Figure.xx below shows VMON pin voltage output versus AD9625 Case Temperature. VMON output is not calibrated at factory and can vary from part to part.

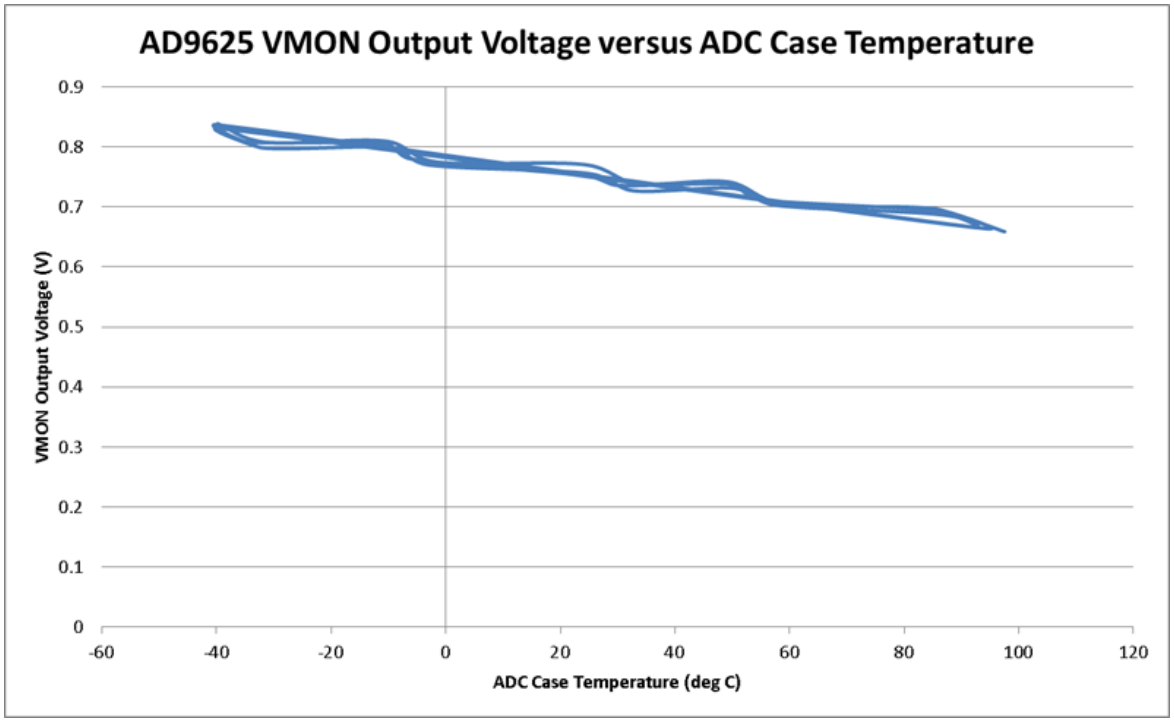


Figure XX: VMON Voltage Output versus AD9625 Case Temperature

FAST DETECT

The fast detect block within the AD9625 is used to generate a fast detection bit (FD) which can be used with variable gain amplifier front end blocks to reduce the gain and prevent the ADC input signal levels from exceeding the converter range.

Figure below shows the how the fast detection bit is programmable using an upper threshold, lower threshold, and dwell time.

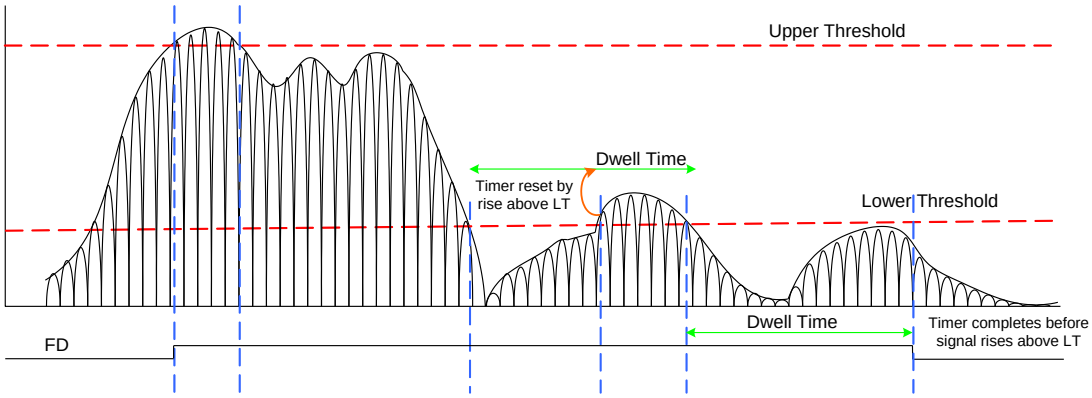


Figure XX: Fast Detection Bit

The FD bit is immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit is cleared only when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This provides hysteresis and prevents the FD bit from excessively toggling.

THRESHOLD OPERATION

The threshold is used to prohibit background calibration updates for small signal amplitudes.

Data Set Threshold Operation

For data set threshold, every sample is used for calibration. In addition, the absolute value of every sample is accumulated to produce an average voltage estimate. Once the calibration has run for its pre-determined number of samples, the voltage estimate is compared to the data set threshold. If the voltage estimate is greater than the threshold, the calibration coefficients will be updated, if not, no update will take place.

Threshold Format

The threshold registers are all 16-bit registers loaded via the SPI a byte at a time. The threshold values range from 0 to 16384 corresponding to a voltage range of 0.0V to 1.0V (full scale).

Threshold Examples

Threshold value	Corresponding voltage level
0x0000 (0)	0.00V
0x1000 (4096)	0.25V
0x2000 (8192)	0.50V
0x4000 (16384)	1.00V (full scale)

Table X. Threshold Examples

Threshold Register Set

Background Gain Sample Threshold High Byte	Must be a value from 0x0000 to 0x4000
Background Gain Sample Threshold Low Byte	
Background Gain Sample Threshold Timeout count	Bits[2:0] = 0, 2^27 discarded samples Bits[2:0] = 1, 2^28 discarded samples Bits[2:0] = 2, 2^29 discarded samples Bits[2:0] = 3, 2^30 discarded samples Bits[2:0] = 4, 2^31 discarded samples Bits[2:0] = 5, 2^32 discarded samples Bits[2:0] = 6, 2^33 discarded samples Bits[2:0] = 7, not used
Background Gain Data Set Threshold High Byte	Must be a value from 0x0000 to 0x4000

Background Gain Data Set Threshold Low Byte	

Table X. Threshold Register Set

Note: there's a corresponding registers set for foreground gain calibration and background gain calibration.

SYSREF SETUP AND HOLD GUARDBAND

The AD9625 includes a Setup/Hold detector that allows a system integrator to calibrate the SYSREF signals. This is useful in situations where the delay differences (due to components or trace length mismatches) of the CLK and the SYSREF inputs are different. For example, a customer may wish to filter the input CLK signal, but not the SYSREF signal. This Setup/Hold detector allows a system designer the flexibility to calibrate the SYSREF signals relative to the CLK inputs in the system by allowing a fixed amount of setup/hold guard band beyond the normal setup/hold requirements of the Flip-Flop (see figure below for a timing diagram of the SYSREF signal relative to the clock). If the SYSREF signal changes inside the guard band, error bits are set. These error bits are cleared only when a valid SYSREF signal is captured. With this mechanism, as long as the skew between the input SYSREF signals to multiple AD9625 devices is smaller than the setup/hold guard band settings, then it is possible to detect when a setup/hold requirement has been violated or whether AD9625 devices are sampling on different clock edges. If an error is detected, then it would be the responsibility of the system integrator to change the phase of the SYSREF signals to a position that would not produce an error.

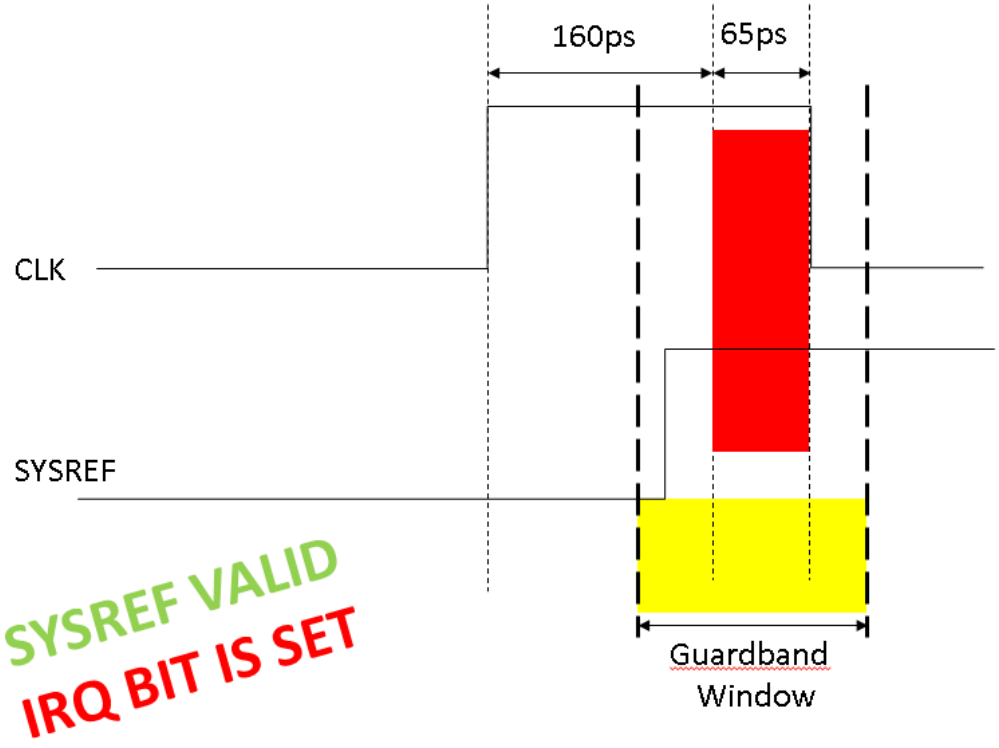
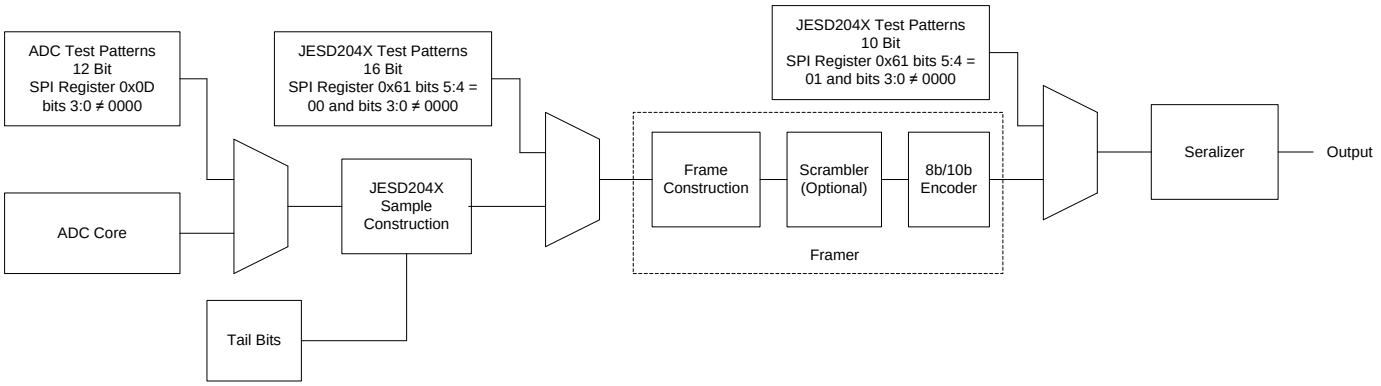


Figure xx. SYSREF Guardband

TEST MODES

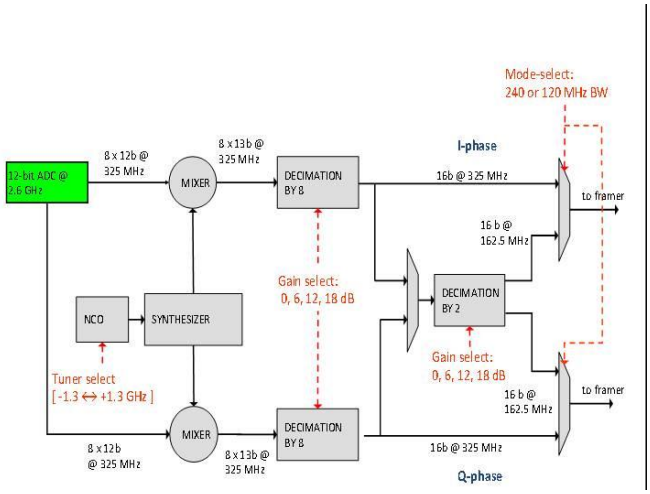


Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1 (Default Twos Complement Format)	Digital Output Word 2 (Default Twos Complement Format)	Subject to Data Format Select
0000	Off (default)	Not applicable	Not applicable	Yes
0001	Midscale short	0000 0000 0000	= Word1	Yes
0010	+Full-scale short	0111 1111 1111	= Word1	Yes
0011	–Full-scale short	1000 0000 0000	= Word1	Yes
0100	Checkerboard	1010 1010 1010	0101 0101 0101	No
0101	PN sequence long	Not applicable	Not applicable	Yes
0110	PN sequence short	Not applicable	Not applicable	Yes
0111	One-/zero-word toggle	1111 1111 1111	0000 0000 0000	No
1000	User test mode	User data from Register 0x19 to Register 0x20	User data from Register 0x19 to Register 0x20	Yes
1001 to 1110	Not used	Not applicable	Not applicable	
1111	Ramp output	N	N + 1	No

Table XX. Flexible Output Test Modes from SPI Register 0x0D

DIGITAL DOWNCONVERTERS (WIDE BAND TUNERS)

The architecture includes two (2) wide-band tuners, each designed to extract a portion of the full digital spectrum captured by the ADC. Each tuner consists of an independent frequency-synthesizer and quadrature mixer. These are followed by a chain of low-pass filters for rate-conversion.



Assuming a sampling frequency of 2.600 GHz, the frequency synthesizer (10-bit NCO) allows for 1024 discrete tuning frequencies, ranging from - 1.299 GHz to +1.300 GHz, in steps of 2500/1024 = 2.441 MHz. The low-pass filters allow for two modes of decimation:

- A high-bandwidth mode 240 MHz wide (from -120 MHz to +120 MHz), sampled at 2.5 GHz /8 = 312.5 MHz for I and Q separately. The 16-bit samples from the I and Q branches are transmitted through dedicated JESD204B interface
- A low-bandwidth mode 120 MHz wide (from -60 MHz to +60 MHz), sampled at 2.5 GHz / 16 = 156.2 MHz for I and Q separately. The 16-bit samples from the I and Q branches *can* be transmitted through dedicated JESD204B interface

All the blocks are designed to operate at a single clock frequency of 2.5 GHz / 8 = 325 MHz.

Each filter stage includes a gain-control block that can be programmed by the user. The gain varies from 0 to 18 dB, in steps of 6 dB and is applied before final scaling and rounding. This may be useful in cases where the tuner filters out a strong out-of-band interferer, leaving a weak in-band signal.

Frequency Synthesizer and Mixer

For a sampling rate of 2.500 GHz, the synthesizer (10-bit NCO) outputs one of 1024 possible complex frequencies from -1.249 GHz to +1.25 GHz. The synthesizer employs the direct-digital synthesis technique, utilizing look-up *sine* tables and a phase-accumulator. The user specifies the tuner frequency by writing to a 10-bit phase-increment register.

High-Bandwidth Decimator

The first filter stage is designed for a rate-reduction-factor of 8, yielding a sample rate of 2.600 GHz / 8 = 325 MHz. To achieve a combination of low complexity and low clock-rate, the wide-band tuner employs a decimate-by-8 filter that takes in eight 13-bit samples from the mixer block at every clock cycle.

The block has been designed to provide user-specified gain control, from 0 to 18 dB in steps of 6 dB. The gain is applied before final scaling and rounding to 16-bits.

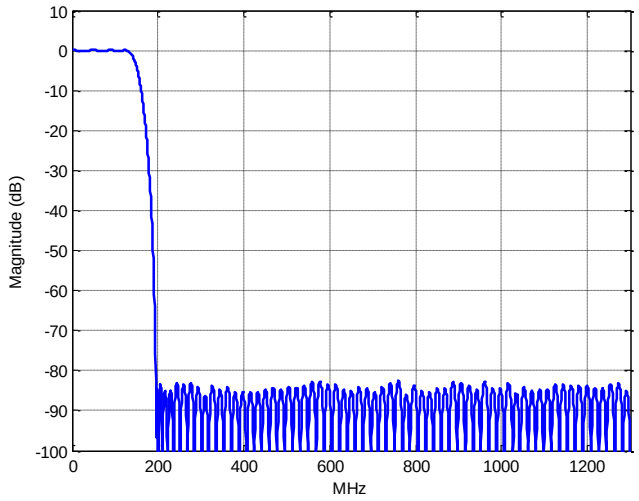


Figure 2: Magnitude response of the decimate-by-8 polyphase fuse filter.

The performance of the filter is shown in Figure 2 and Figure 3. The filter yields an effective bandwidth of 120 MHz, with a transition band of 162.5 – 120 = 42.5 MHz. Hence, the two-sided complex bandwidth of the filter is 240 MHz. A rejection ratio of 85 dB ensures that the 7 aliases that fold back into the pass-band yield an SNR of 85 – 10log10(7) = 76.5 dB, which ensures that the aliases lie sufficiently below the noise floor of the input signal. The pass-band ripple is +/- 0.05 dB, as can be seen from Figure 3.

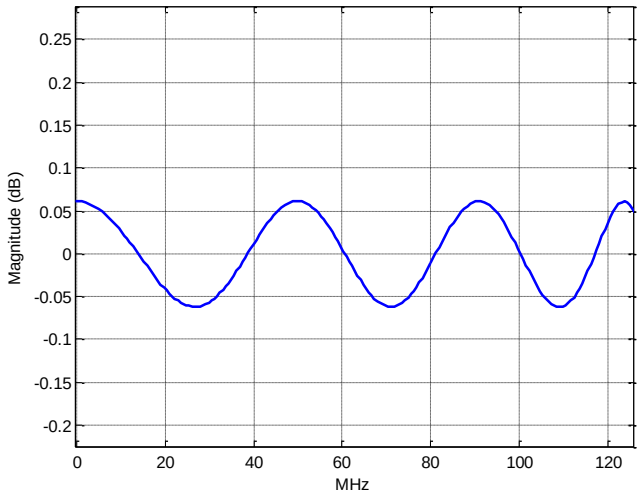


Figure 3: Magnitude ripple in the pass-band.

Low-Bandwidth Decimator

The second filter stage is employed only in the optional low-bandwidth mode. It achieves an additional rate-reduction-factor of 2, yielding a final sample rate of 2.500 GHz / 16 = 156.2 MHz. The internal architecture of the filter is similar to that of high-bandwidth decimator. Moreover, for ease of physical design, the block operates at 312.5 MHz, as result of which both the I- and Q-phases can "time-share" the filter engine.

The performance of the filter is shown in Figure 4 and Figure 5. The filter yields an effective bandwidth of 60 MHz, with a transition band of 81.25 – 60 = 21.25 MHz. Hence, the two-sided complex bandwidth of the filter is 120 MHz. A rejection ratio of 85 dB ensures that the alias region folds back well below the noise floor of the input signal.

As with the high-bandwidth filter, this block provides user-specified gain control, from 0 to 18 dB, in steps of 6 dB. The gain is applied before final quantization at the output of the filter to 16-bits.

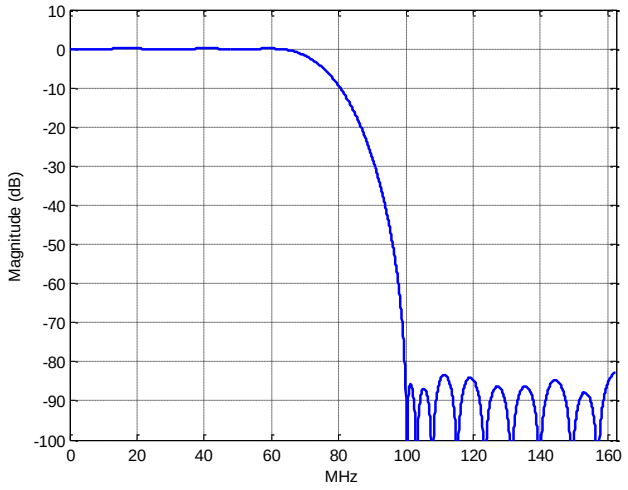


Figure 4: Magnitude response of decimate-by-2 filter.

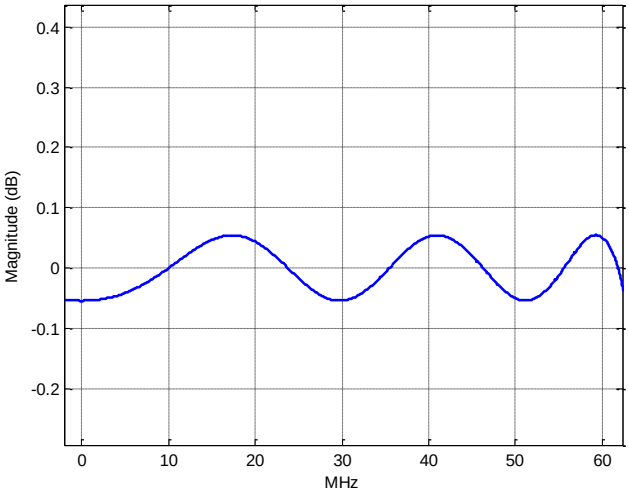


Figure 5: Magnitude ripple in the pass-band.

ANALOG INPUT CONSIDERATIONS

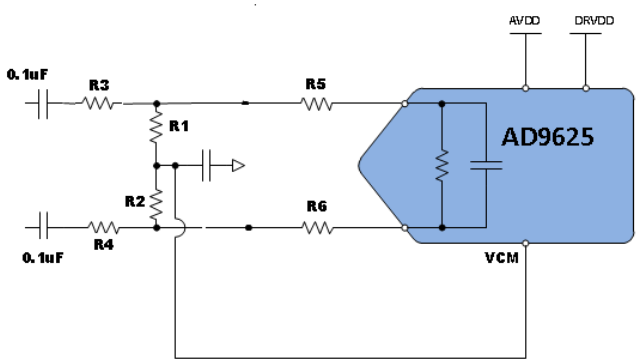


Figure xx: AD9625 Frontend Minimum Requirement

De-Q resistors (R5 and R6) are recommended to reduce bandwidth peaking and minimize kickbacks from the ADC. External termination (R1 and R2) are not required in AD9625 Rev3 silicon. Small series resistors (R3 and R4) limits bandwidth, but can be installed to further improve performance. Table xx below shows minimum front end requirements.

Components	Rev1 and Rev2 Silicon	Rev3 Silicon
R1	Impedance Matching	DNI
R2	Impedance Matching	DNI
R3	0-33 ohm	
R4	0 -33 ohm	
R5	0-33 ohm	
R6	0-33 ohm	

Table xx: Recommended AD9625 Frontend Components

In addition to the minimum front end requirements, AD9625 bandwidth and performance may be improved by the topologies below.

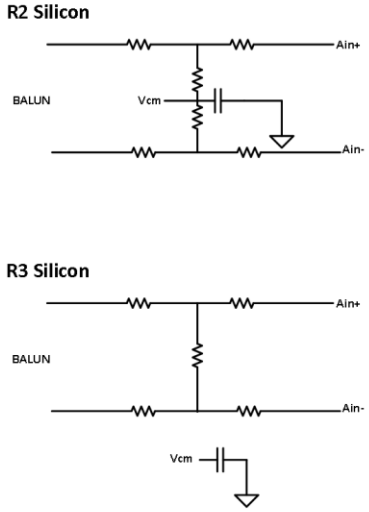


Figure xx: Recommended AD9625 Frontend

DIGITAL OUTPUTS

The JESD204B interface is described according to the following nomenclature (the term "converter device" and "link" can be used interchangeably in the specification):

- S=Samples transmitted/single converter/frame cycle
- M= Number of converters/converter device (link)
- L=Number of lanes/converter device (link)
- N=Converter Resolution
- N'=Total number of bits per sample
- CF=Number of control words/frame clock cycle/converter device (link)
- CS=Number of control bits/conversion sample
- K=Number of frames per multi-frame
- HD=High Density Mode
- F=Octets/Frame
- C=Control Bit (Over-Range, Overflow, Underflow, Timestamp)
- T=Tail Bit

The AD9625 adheres to the JESD204B draft specification which provides a high speed serial, embedded clock interface standard for Data Converters and Logic Devices. It is designed as a MCDA-ML, Subclass 1 Device which utilizes the "SYSREF" input signal for multi-chip synchronization and deterministic latency using the following basic JESD204B Link Configuration Parameters:

- M=1 (single converter)
- L=1-8 (eight lanes)
- S=4 (four samples per JESD204B frame)
- F=1 (one octet per frame)
- N'=12,16 (twelve or sixteen bit JESD204B word size)
- HD=0,1 (high density mode – sample span multiple lanes)

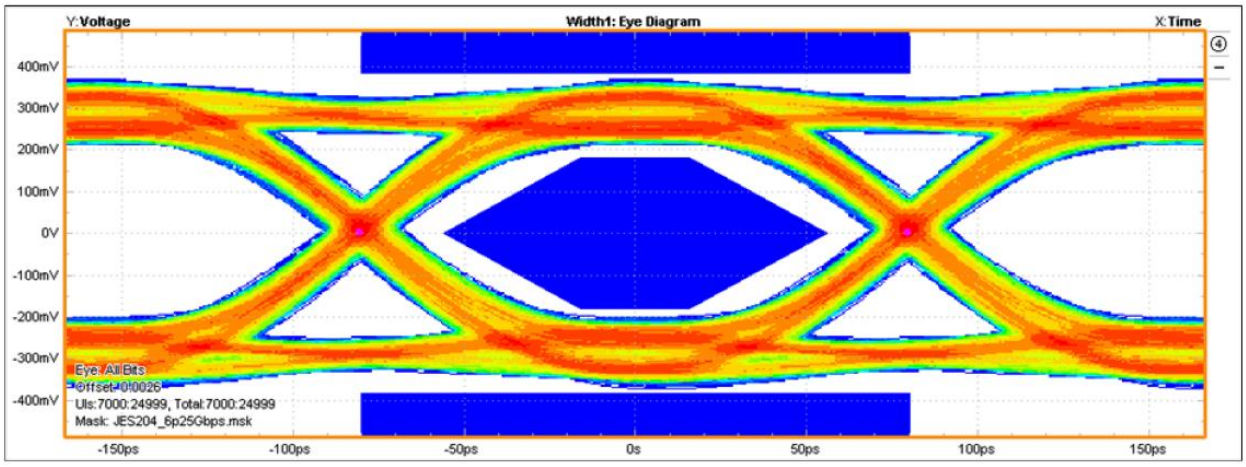
JESD Modes of Operation

Mode #	Configuration (add columns for L and F) Quick Config Value	Sample Clock (Min MSPS)	Sample Clock (Max MSPS)	Sample Clock Multiplier	JESD204B Output Rate per Lane (Min Mbps)	JESD204B Output Rate per Lane (Max Mbps)
1	Generic - 2 Lanes	325	650	10	3250	6500
2	Generic - 4 Lanes	650	1300	5	3250	6500
3	Generic - 6 Lanes (N' = 12)	1300	2600	2.5	3250	6500
4	Generic - 8 Lanes	1300	2600	2.5	3250	6500
5	FSX8 - 2 Lanes	406	813	8	3250	6500
6	FSX4 - 4 Lanes	813	1625	4	3250	6500
7	FSX2 - 8 Lanes	1625	2600	2	3250	5200
8	Single WBT High BW - 1 Lane	650	1300	5	3250	6500
9	Single WBT High BW - 2 Lanes	1300	2600	2.5	3250	6500
10	Single WBT Low BW - 1 Lane	1300	2600	2.5	3250	6500
11	Dual WBT High BW - 1 Lane	325	650	10	3250	6500
12	Dual WBT High BW - 2 Lanes	650	1300	5	3250	6500
13	Dual WBT High BW - 4 Lanes	1300	2600	2.5	3250	6500

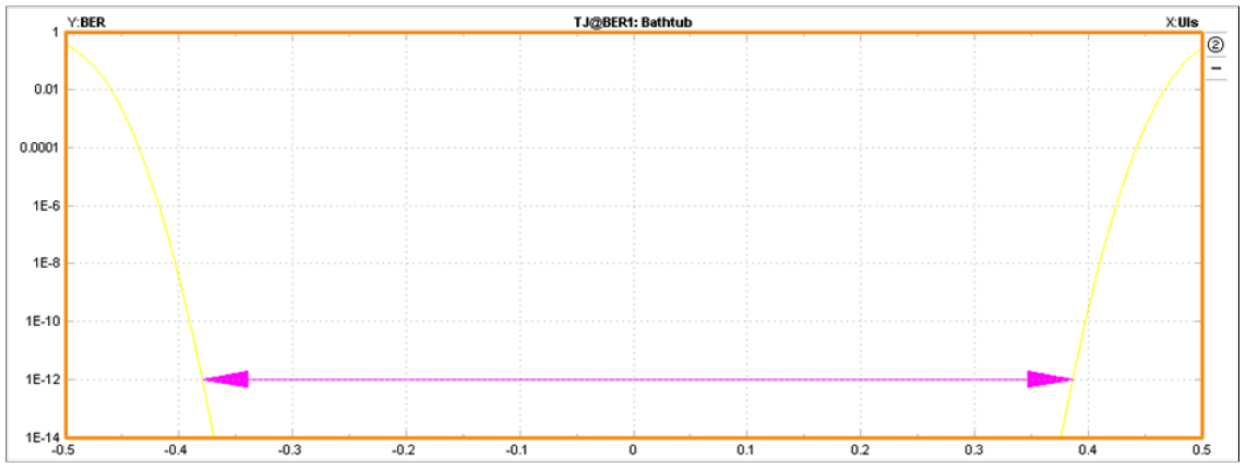
14	Dual WBT Mixed BW - 1 Lane	325	650	10	3250	6500
15	Dual WBT Mixed BW - 2 Lanes	650	1300	5	3250	6500
16	Dual WBT Mixed BW - 4 Lanes	1300	2600	2.5	3250	6500
17	Dual WBT Low BW - 1 Lane	650	1300	5	3250	6500
18	Dual WBT Low BW - 2 Lane	1300	2600	2.5	3250	6500

Mode #	Configuration	Typical Latency (CLK Cycles)
1	Generic - 2 Lanes	181
2	Generic - 4 Lanes	191
3	Generic - 6 Lanes	222
4	Generic - 8 Lanes	232
5	FSX8 Mode - 2 Lanes	187
6	FSX4 Mode - 4 Lanes	131
7	FSX2 Mode - 8 Lanes	219
8	Single WBT High BW - 1 Lane	624
9	Single WBT High BW - 2 Lanes	444
10	Single WBT Low BW - 1 Lane	524
11	Dual WBT High BW - 1 Lane	148
12	Dual WBT High BW - 2 Lanes	347
13	Dual WBT High BW - 4 Lanes	374
14	Dual WBT Mixed BW - 1 Lane	333
15	Dual WBT Mixed BW - 2 Lanes	338
16	Dual WBT Mixed BW - 4 Lanes	378
17	Dual WBT Low BW - 1 Lane	502
18	Dual WBT Low BW - 2 Lane	558

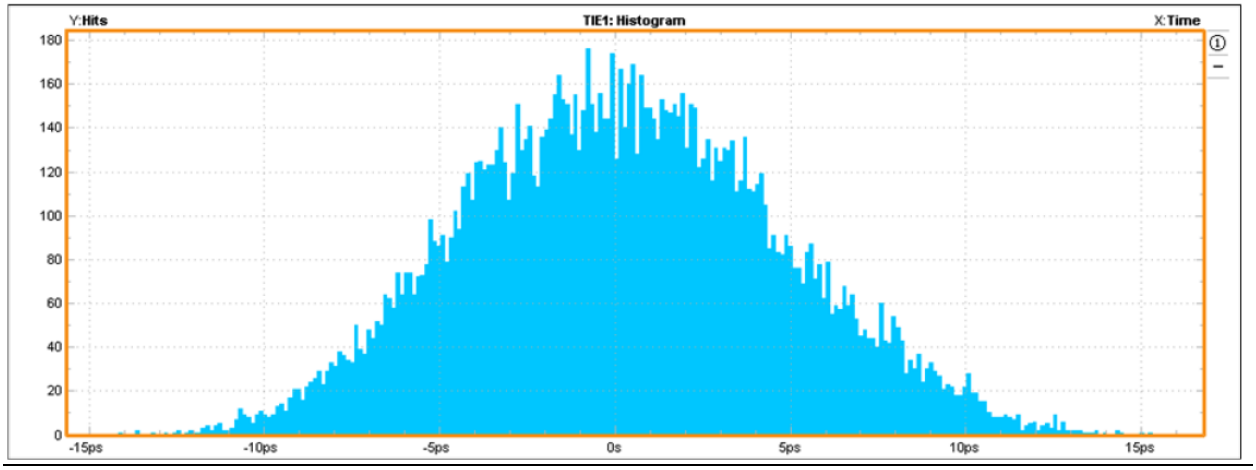
PHY



Recovered Data eye of JESD204B lane at 6.25Gbps



Bathtub plot of JESD204B output at 6.25Gbps



Time Interval Histogram Error of JESD204B output at 6.25Gbps

Scrambler

The scrambler polynomial is 1+x^14+x^15.

The scrambler enable bit is located in register 0x6E[7].

- 0: Disabled
- 1: Enabled

Tail Bits

The tail bit PN generator bit is located in register 0x5F[6].

- 0: Disabled
- 1: Enabled

Wide Band Tuner Modes (Single and Dual)

The AD9625 contains two separate Wide Band Tuners which can be used to digitally down convert the real ADC output data into I/Q decimated data at a reduced bandwidth. This feature is useful when customers do not need the full 1.3 GHz bandwidth supplied by the 2.6 MSPS converter. The figure below shows a simplified block diagram of the Wideband Tuner blocks as they traverse through the AD9625.

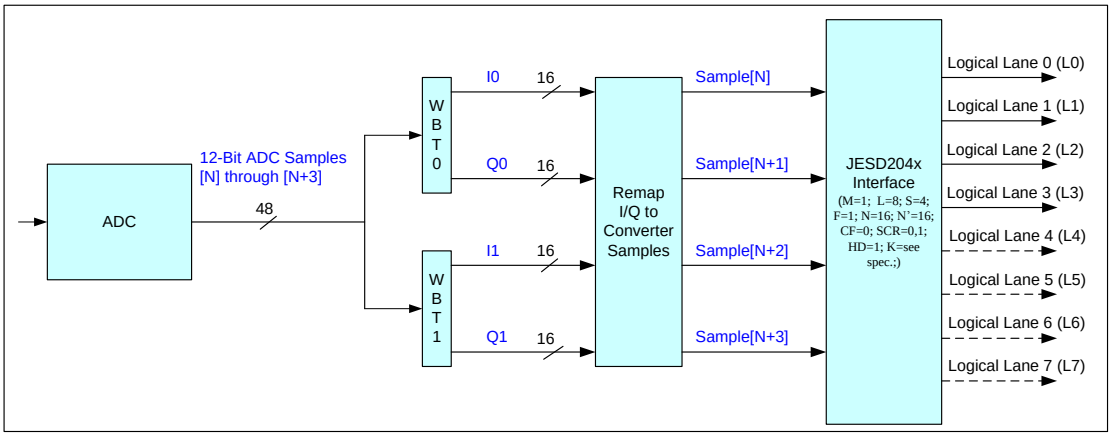


Figure 6 Wideband Tuner Mapping

Since all JESD204x frames contain 4 samples (S=4), the output from the wideband tuners must also output 4 samples. Table XX shows the remapping of I/Q samples to converter samples for the JESD204x interface, specific to AD9625

TableXX: Wideband Tuner Remap I/Q to Converter Samples

App Mode	Sample[N]	Sample[N+1]	Sample[N+2]	Sample[N+3]
Single Wideband Tuner	I_0[N]	Q_0[N]	I_0[N+1]	Q_0[N+1]
Dual (2) Wideband Tuners	I_0[N]	Q_0[N]	I_1[N]	Q_1[N]

When only one wideband tuner is enabled, the samples must be buffered in order to write the correct number of samples to the JESD204x interface.

When two wideband tuners are enabled and both tuners are in either low or high bandwidth mode, no buffering is required. While in "Mixed bandwidth mode", wideband tuner 0 is always in high bandwidth mode and wideband tuner 1 is always in low bandwidth mode. In order to match the data throughput of the high bandwidth mode, the low bandwidth samples are repeated twice in "Mixed bandwidth mode". Table XX below shows 4 frames of data for both wideband tuner 0 (high bandwidth mode) and 1 (low bandwidth mode).

TableXX: Wideband Tuner "Mixed Bandwidth Mode"

JESD204x Frame Number	Sample[N]	Sample[N+1]	Sample[N+2]	Sample[N+3]
Frame 0	I_0[N]	Q_0[N]	I_1[N]	Q_1[N]
Frame 1	I_0[N+1]	Q_0[N+1]	I_1[N]	Q_1[N]
Frame 2	I_0[N+2]	Q_0[N+2]	I_1[N+1]	Q_1[N+1]
Frame 3	I_0[N+3]	Q_0[N+3]	I_1[N+1]	Q_1[N+1]

CHECKSUM

The JESD204x checksum value is sent along with the configuration parameters during the initial lane alignment sequence. Disabling the checksum is primarily for debug purposes only.

8B/10B CONTROL

The 8b/10b encoder must be controlled in the following ways:

- Bypass 8b/10b controlled by the register 0x60 [2] bit (0=8b/10b enabled; 1=8b/10b bypassed) in the register map
- Invert 10b controlled by the 0x60 [1] bit (0=Normal; 1=Invert) in the register map.
- Mirror 10b controlled by the 0x60 [0] bit (0=Normal; 1= Mirrored) in the register map.

The inversion of the 10b values allows the user to effectively swap the true/complement differential pins when swapped on the boards.

Figure XX below shows a diagram of the 10bit symbols normally and when mirrored.

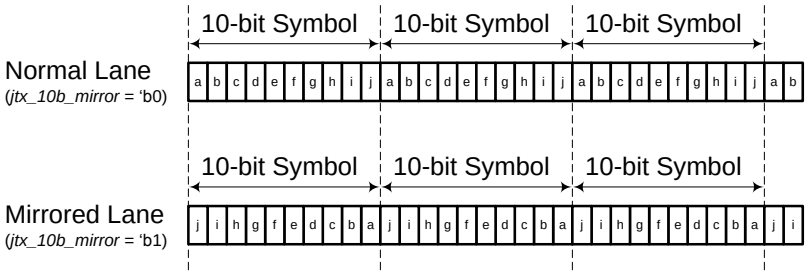


Figure 7: JESD204B 10b Mirror Feature

INITIAL LANE ALIGNMENT SEQUENCE (ILAS)

The AD9625 must support 3 different ILAS Modes controlled using the 0x05F [3:2] bits in the register map:

- 00: Disabled
- 01: Enabled
- 11: Always On Test Mode
- 10: Reserved

When enabled, it must also support the capability to repeat the ILAS using 0x062 [7:0] bits in the register map to determine the number of times ILAS is repeated (0=repeat 0 times, ILAS will run once, 1=repeat 1 times, ILAS will run twice, etc). Since the number of frames per multiframe is determined by the value of K, the total number of frames transmitted during the Initial Lane Alignment Sequence = 4 * (K+1) * (ILAS_COUNT + 1). The value of K is defined in register 0x070 [4:0]. Only values divisible by 4 can be used.

LANE SYNCHRONIZATION

Lane Synchronization is defined by register 0x05F bit [4] (0=disabled, 1=enabled) in the register map.

JESD204X INTERFACE TEST MODES

Figure XX below shows the 4 different test injection points for the AD9625. Three of the injection points are contained in the JESD204B Interface and affect all lanes at once.

ADC Output Control Bits on JESD204B samples

When N'=16 and the ADC resolution is 12, there are 4 spare bits available per sample. 3 of these can be used as control bits in locations [3:1] of the sample based on the configuration options. The control bits are set in register 0x072 [7:6].

- 00: No control bits sent per sample (CS=0)
- 01: One control bits sent per sample - Over-Range Bit Enabled. (CS=1)
- 11: Two control bits sent per sample - Over-Range + Timestamp SYSREF Bit (CS=2)
- 10: Three control bits sent per sample - Over-Range + Timestamp SYSREF Bit + Data Valid (CS=3) - Debug Only

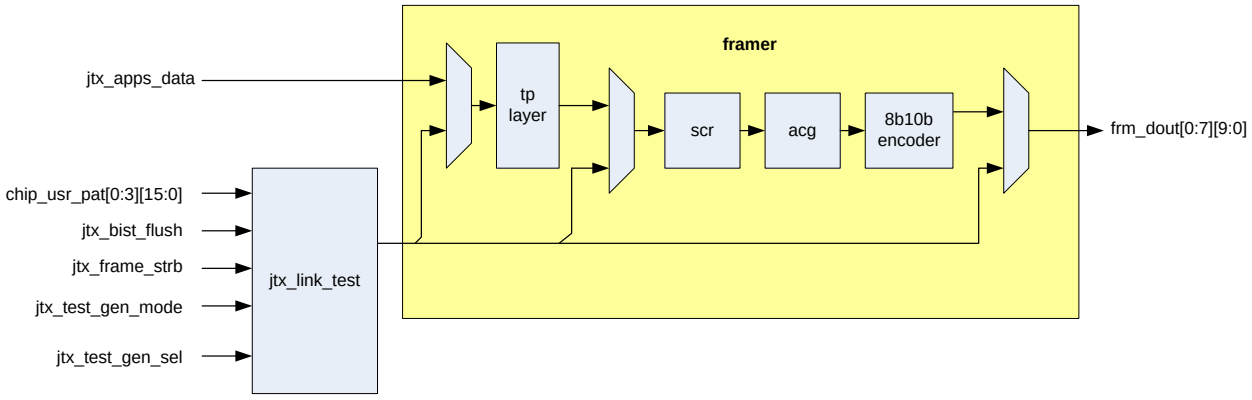


Figure 8: JESD204x Test Injection Points

The JESD204B interface test injection points are controlled by the register 0x061 [5:4] bits in the register map:

- 10: 8-bit input into Scrambler
- 01: 10-bit output of JESD204B framer (PHY)
- 00: 12 or 16 (depending on the value of N') input to JESD204B framer.
- 11: Reserved

The test patterns injected, depend on register 0x061 [3:0] bits in the register map:

- 0000: Normal Operation (test mode disabled)
- 0001: Alternating Checker Board
- 0010: 1/0 Word Toggle
- 0011: PN Sequence – Long (X^23 + X^18 + 1)
- 0100: PN Sequence – Short (X^9 + X^5 + 1)
- 0101: Continuous/Repeat User Test Mode - Most significant bits from 16-bit User Pattern (1,2,3,4) placed on the output for 1 clock cycle and then repeat. (Output User Pattern 1, 2, 3, 4, 1, 2, 3, 4, 1, 2, 3, 4, ...etc.) 0110: Single User Test Mode - Most significant bits from 16-bit User Pattern (1,2,3,4) placed on the output for 1 clock cycle and then output all zeros. (Output User Pattern 1, 2, 3, 4, then output all zeros)
- 0111: Ramp Output (dependent on Test Injection Point and number of bits - N)
- 1000: Modified RPAT Test Sequence
- 1001: Unused
- 1010: JSPAT Test Sequence
- 1011: JTSPAT Test Sequence

- 1100-1111: Unused

JESD204B APPLICATION LAYERS

The AD9625 supports the following application layer modes: 0x63[3:0]

1) 0110: Fsx2 Mode which supports line rates at integer multiples of the sample rates
2) Dual Wideband Tuner Mode which can be used to down convert the ADC
   1000: Single Wide Band Tuner Mode - High Bandwidth Mode (only WBT0 used)
   1001: Single Wide Band Tuner Mode - Low Bandwidth Mode (only WBT0 used)
   1010-1011: Unused
   1100: Dual (2) Wide Band Tuner Mode - High Bandwidth Mode (both WBT0 and WBT1 used)
   1101: Dual (2) Wide Band Tuner Mode - Low Bandwidth Mode (both WBT0 and WBT1 used)
   1110: Dual (2) Wide Band Tuner Mode - Mixed Bandwidth Mode (WBT0 High Bandwidth Mode, WBT1 Low Bandwidth Mode - samples repeated)

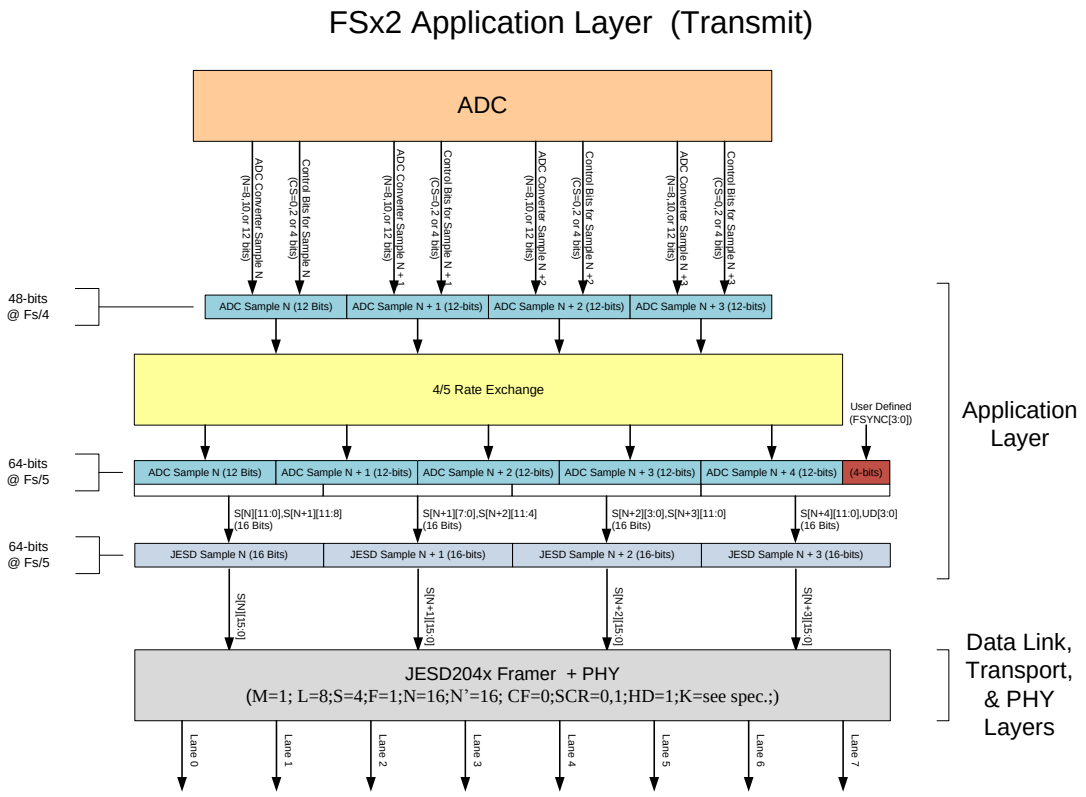
FSX2, FSX4, FSX8 Modes

The JESD204B Low Multiplier Mode Application Layer adds a rate conversion on top of a JESD204B transmitter/receiver with the following configuration parameters:

M=1; L=8;S=4;F=1;N=16;N'=16;CS=0;CF=0; SCR=0,1;HD=1;K=see spec.;

The actual number of samples per frame is 5 in this mode and scrambling can be optionally enabled in the JESD204B interface.

The transmit portion of the Low Multiplier Mode JESD204B Application Layer is shown in Figure XX.

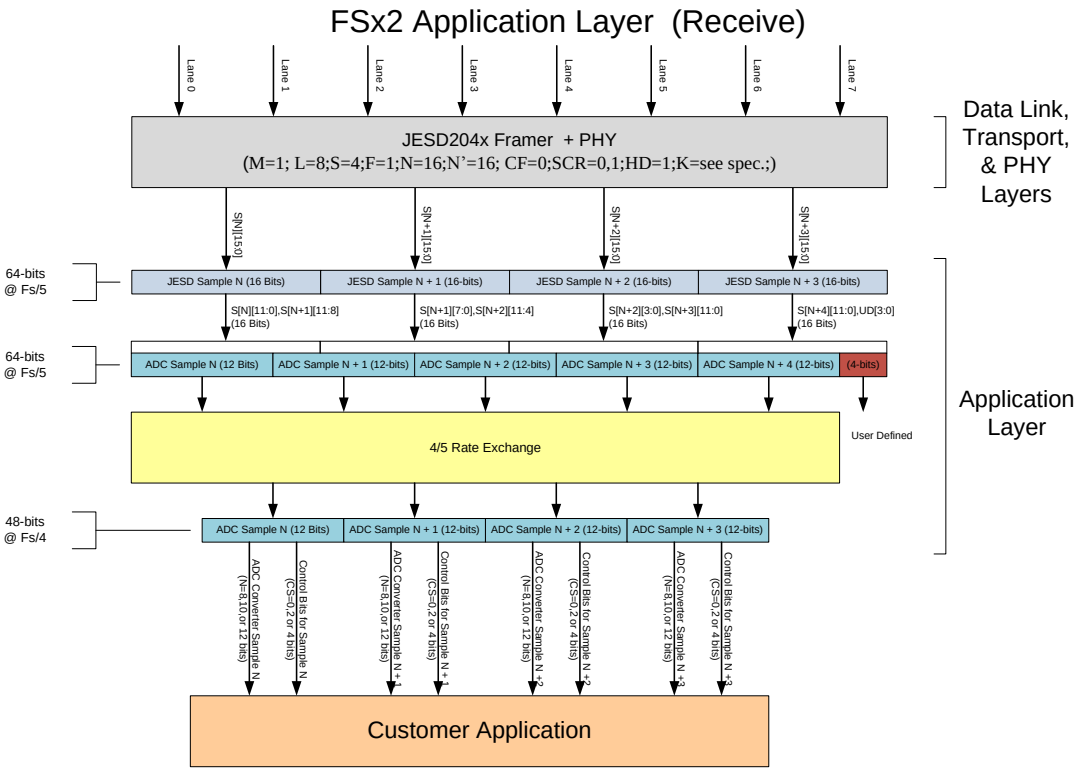


Fsx2 Mode Application Layer (Transmit)

The first step in this application layer is where 12-bit ADC Samples are broken into six bytes.

In order to allow the line rate of the JESD204B interface to map directly into an integer of the converter sample rate, a 4 to 5 rate conversion takes place to group the 12-bit ADC Samples into blocks of five samples. During this rate conversion, for every five 12-bit ADC Samples, an extra User Defined 4-bit Nibble is appended to create a 64-bit frame (0x88 bits [3:0]) in the register map). The 64-bit Low Multiplier frame is then mapped into the four 16-bit JESD Samples. The most significant 16-bits of the 64-bit Low Multiplier frame is mapped to the oldest 16-bit JESD Sample and the least significant 16-bits of the 64-bit Low Multiplier frame is mapped to the newest 16-bit JESD Sample.

The receive portion of the FSx2 JESD204x Application Layer is shown in **Error! Reference source not found.**.



Fsx2 Application Layer (Receive)

FRAME ALIGNMENT CHARACTER INSERTION

Frame alignment character insertion is defined in the register map. It should only be disabled as a test feature.

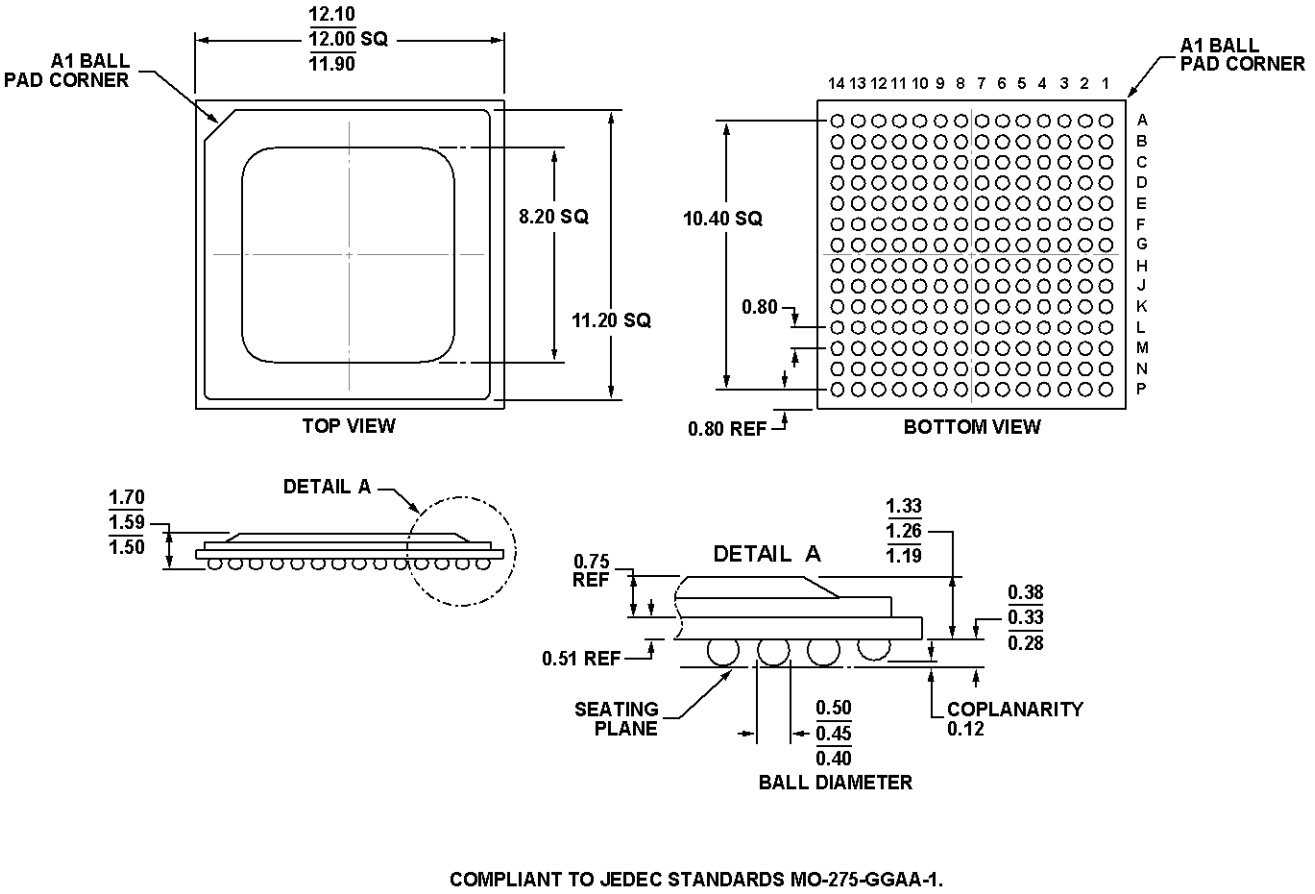
The frame alignment character insertion disable bit is located in register 0x5F[1].

- 0: FACI Enabled
- 1: FACI Disabled

THERMAL CONSIDERATIONS

Due to the high power nature of the part, it is critical to provide airflow and/or install heat sink when operating at high temperature. This ensures that the maximum junction temperature (125°C) is not exceeded.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-GGAA-1.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9625XBPZ-2.5	–40°C to +85°C	196-ball 12x12 BGA	196 12x12 BGA_ED
AD9625EBZ		Evaluation Board with AD9625	

[1] Z = RoHS Compliant Part.