Data Sheet

ACPL-M61M

2.5V/3.3V Low-Power 10 MBd Digital Optocoupler

Description

The Broadcom ACPL-M61M is an optocoupler that combines a light emitting diode and an integrated high gain photo detector to address a low power supply need. It supports 2.5V/3.3V supply voltage with guaranteed AC and DC operational parameters at full industrial temperature range –40°C to +125°C. The optocoupler consumes low power across temperature with the LED driving current operating from as low as 1.6 mA.

The output of the detector IC is a CMOS output. The internal Faraday shield provides a guaranteed common mode transient immunity specification of 20 kV/µs.

CAUTION! It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this datasheet are not to be used in military or aerospace applications or environments.

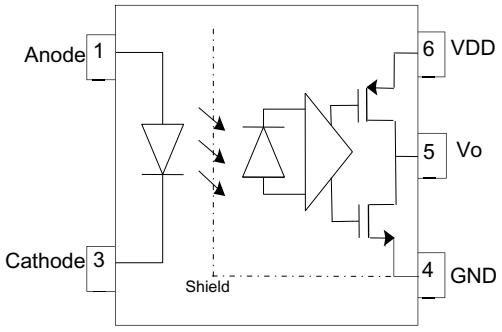
Features

- Supply voltage: 2.5V/3.3V
- Guaranteed AC and DC performance over wide industrial temperature: –40°C to +125°C
- Low supply current I_{DD}: 1.5 mA max
- Low LED input driving current I_F: 1.6 mA min
- Package: SO-5
- High data rate: 10 MBd min
- Common Mode Rejection (CMR): 20 kV/µs minimum at V_{CM} = 1000V
- Safety Approval:
  - UL 1577 - 3750 V_{rms} for 1 minute
  - CSA
  - IEC/EN/DIN EN 60747-5-5 for Reinforced Insulation

Applications

- Communication interface: RS485, CANBus
- ASIC system interface
- Digital isolation for A/D, D/A conversion

Functional Diagram



Truth Table

LED	Output
ON	L
OFF	H

NOTE: A 0.1-µF bypass capacitor must be connected as close as possible between pins V_{DD} and GND.

Ordering Information

ACPL-M61M is UL Recognized with 3750 V_{rms} for 1 minute per UL1577.

Part Number	Option	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant					
ACPL-M61M	-000E	SO-5	X			100 per tube
	-060E		X		X	100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel

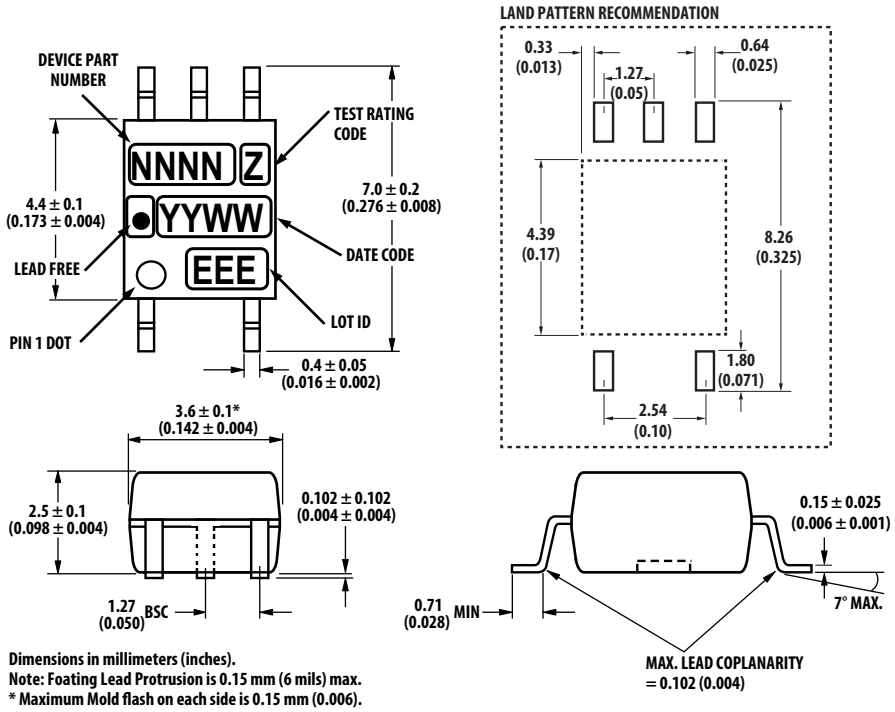
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-M61M-560E to order product of Small Outline SO-5 package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Package Outline Drawing

ACPL-M61M SO-5 Package



Dimensions in millimeters (inches).
Note: Foating Lead Protrusion is 0.15 mm (6 mils) max.
* Maximum Mold flash on each side is 0.15 mm (0.006).

Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

- IEC/EN/DIN EN 60747-5-5 (Option 060E only)
- UL - Approval under UL 1577, component recognition program up to V_{ISO} = 3750 V_{rms}.
- CSA - Approval under CSA Component Acceptance Notice #5, File CA 88324.

Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-M61M	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	5	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	5	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1).

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060E)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/39, Table 1			
For Rated Mains Voltage ≤ 150 V_{rms}		I – IV	
For Rated Mains Voltage ≤ 300 V_{rms}		I – IV	
For Rated Mains Voltage ≤ 450 V_{rms}		I – III	
Climatic Classification		55/125/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	567	V_{PEAK}
Input to Output Test Voltage, Method b[a] V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1063	V_{PEAK}
Input to Output Test Voltage, Method a[a] V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	907	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	V_{PEAK}
Safety-Limiting Values – maximum values allowed in the event of a failure			
Case Temperature	T_S	150	°C
Input Current	$I_{S, INPUT}$	150	mA
Output Power	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$	Ω

a. Refer to the optocoupler section of the *Isolation and Control Components Designer's Catalog*, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for detailed description of Method a and Method b partial discharge test profiles.

NOTE: These optocouplers are suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition
Storage Temperature	T_S	–55	150	°C	
Operating Temperature	T_A	–40	125	°C	
Reverse Input Voltage	V_R	—	5	V	
Supply Voltage	V_{DD}	—	4	V	
Average Forward Input Current	I_F	—	8	mA	
Peak Forward Input Current	$I_{F(TRAN)}$	—	1	A	≤1 µs pulse width, ≤100 pulses per second
		—	80	mA	≤1 µs pulse width, <10% duty cycle
Output Current	I_O		10	mA	
Output Voltage	V_O	–0.5	V_{DD} + 0.4	V	
Input Power Dissipation	P_I	—	14	mW	
Output Power Dissipation	P_O	—	8	mW	
Lead Solder Temperature	T_{LS}	—	260°C for 10 sec, 1.6 mm below seating plane		
Solder Reflow Temperature Profile	See Package Outline Drawing section.				

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	–40	125	°C
Input Current, Low Level	I_{FL}	0	250	µA
Input Current, High Level	I_{FH}	1.6	3.2	mA
Power Supply Voltage	V_{DD}	2.25	3.6	V
Forward Input Voltage	$V_{F(OFF)}$	—	0.8	V

Electrical Specifications (DC)

Over recommended temperature (T_A = –40°C to +125°C) and supply voltage (2.25V ≤ V_{DD} ≤ 2.75V) and (3.0V ≤ V_{DD} ≤ 3.6V). All typical specifications at V_{DD} = 2.5V, T_A = 25°C, unless stated otherwise.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions	Figure
Input Forward Voltage	V_F	0.95	1.33	1.7	V	I_F = 2 mA	1, 2
Input Reverse Breakdown Voltage	BV_R	3	—	—	V	I_R = 10 µA	
Logic High Output Voltage	V_{OH}	V_{DD} – 0.1	V_{DD}	—	V	I_F = 0 mA, I_O = –20 µA	
		V_{DD} – 0.4	V_{DD} – 0.1	—	V	I_F = 0 mA, I_O = –3.2 mA	
Logic Low Output Voltage	V_{OL}	—	0.01	0.1	V	I_F = 2 mA, I_O = 20 µA	
		—	0.11	0.4	V	I_F = 2 mA, I_O = 3.2 mA	
Input Threshold Current	I_{TH}	—	0.7	1.3	mA		3
Logic Low Output Supply Current	I_{DDL}	—	0.77	1.5	mA		4
Logic High Output Supply Current	I_{DDH}	—	0.72	1.5	mA		5
Input Capacitance	C_{IN}	—	21	—	pF	f = 1 MHz, V_F = 0V	
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	—	–1.76	—	mV/°C	I_F = 2 mA	2

Switching Specifications (AC)

Over recommended temperature (T_A = –40°C to +125°C) and supply voltage (2.25V ≤ V_{DD} ≤ 2.75V) and (3.0V ≤ V_{DD} ≤ 3.6V). All typical specifications at V_{DD} = 2.5V, T_A = 25°C, unless stated otherwise.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output	t_{PHL}	—	47	90	ns	I_F = 2 mA, C_L= 15 pF, CMOS signal levels.	6, 7, 8, 9, 10, 11, 12	a, b
Propagation Delay Time to Logic High Output	t_{PLH}	—	49	90	ns		6, 7, 8, 9, 10, 11, 12	a, b
Pulse Width Distortion	PWD	—	2	45	ns		6, 7, 8, 9, 10, 11, 12	a, c
Propagation Delay Skew	t_{PSK}	—	—	50	ns			a, d
Output Rise Time (10% to 90%)	t_R	—	6	—	ns			
Output Fall Time (90% to 10%)	t_F	—	7	—	ns			
Static Common Mode Transient Immunity at Logic High Output	$\lvert CM_H \rvert$	20	—	—	kV/µs	V_{CM} = 1000V, T_A = 25 °C, I_F = 0 mA, C_L= 15 pF, CMOS signal levels.	13	a, e
Static Common Mode Transient Immunity at Logic Low Output	$\lvert CM_L \rvert$	20	—	—	kV/µs	V_{CM} = 1000V, T_A = 25 °C, I_F = 2 mA, C_L= 15 pF, CMOS signal levels.	13	a, f

a. Bypass capacitor places at no more than 3 mm from optocoupler's power pins (V_{DD}, GND).

b. t_{PHL} propagation delay is measured from the 50% (V_{in} or I_F) on the rising edge of the input pulse to the 50% V_{DD} of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{in} or I_F) on the falling edge of the input pulse to the 50% level of the rising edge of the V_O signal.

c. PWD is defined as $|t_{PHL} - t_{PLH}|$.

d. t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.

e. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.

f. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.

Package Characteristics

All typical at T_A = 25°C.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input-Output Insulation	V_{ISO}	3750	—	—	V_{rms}	RH < 50% for 1 min. T_A = 25°C
Input-Output Resistance	R_{I-O}	—	10^{14}	—	Ω	V_{I-O} = 500V
Input-Output Capacitance	C_{I-O}	—	0.5	—	pF	f = 1 MHz, T_A = 25°C

Figure 1: Typical Input Diode Forward Characteristic

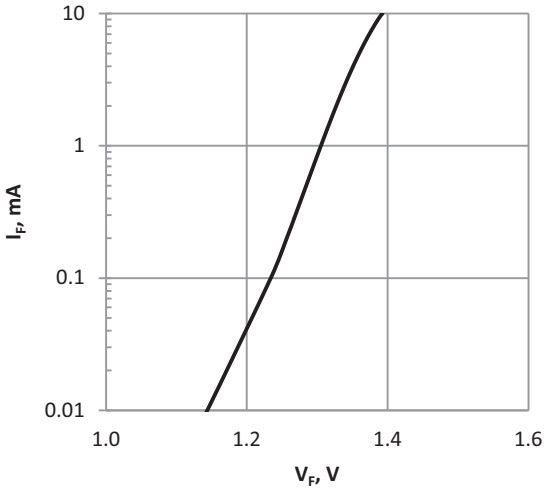


Figure 2: Typical V_F vs. Temperature

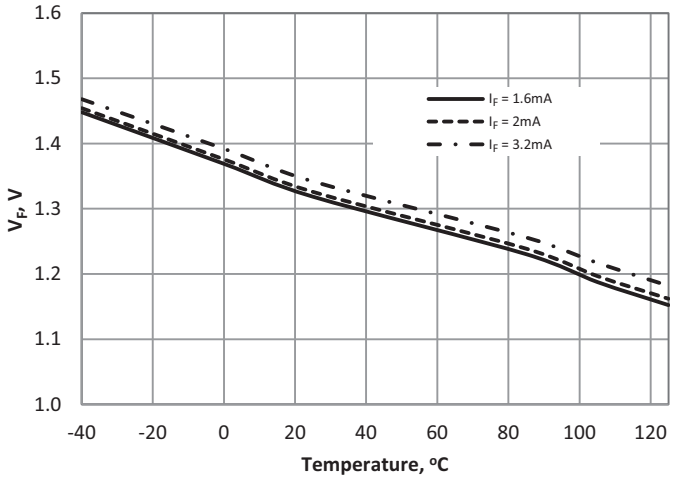


Figure 3: Typical Input Threshold Current I_{TH} vs. Temperature

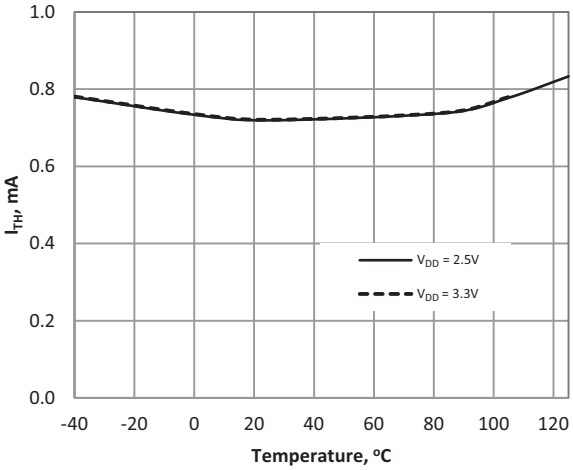


Figure 4: Typical Logic Low Output Supply Current I_{DDL} vs. Temperature

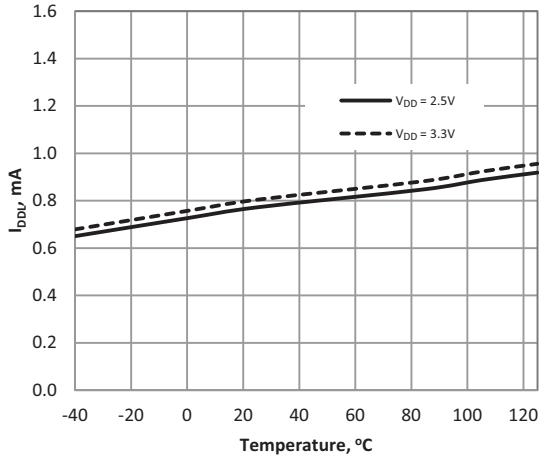


Figure 5: Typical Logic High Output Supply Current I_{DDH} vs. Temperature

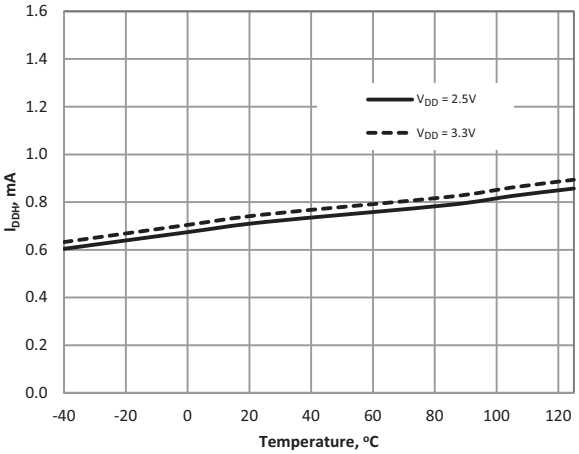


Figure 6: Typical Switching Timing (Propagation Delay, PWD) vs. LED Input Forward Current at 2.5V Supply

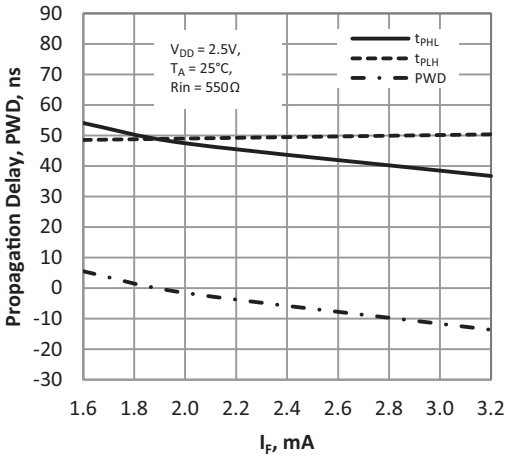


Figure 7: Typical Switching Timing (Propagation Delay, PWD) vs LED Input Forward Current at 3.3V Supply

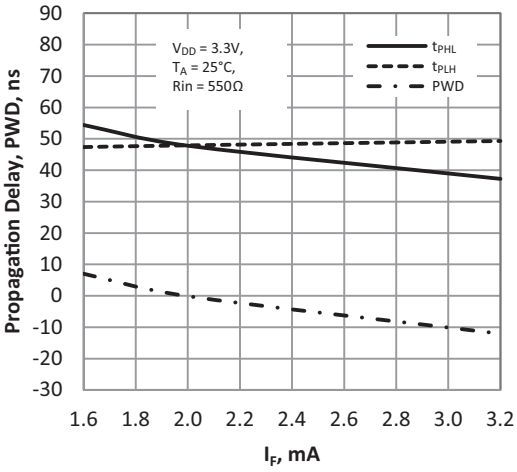


Figure 8: Typical Switching Timing (Propagation Delay, PWD) vs Temperature at 2-mA LED Driving Current, 2.5V Supply

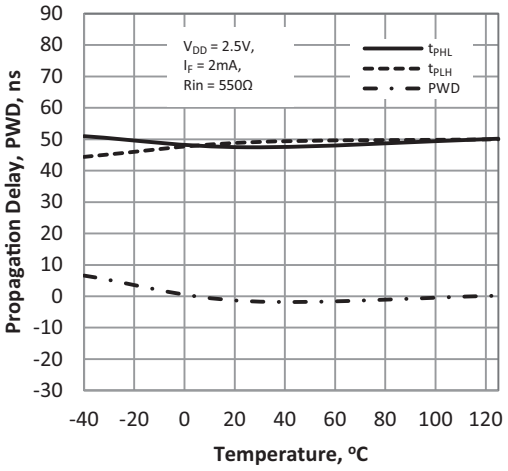


Figure 9: Typical Switching Timing (Propagation Delay, PWD) vs Temperature at 3.2-mA LED Driving Current, 2.5V Supply

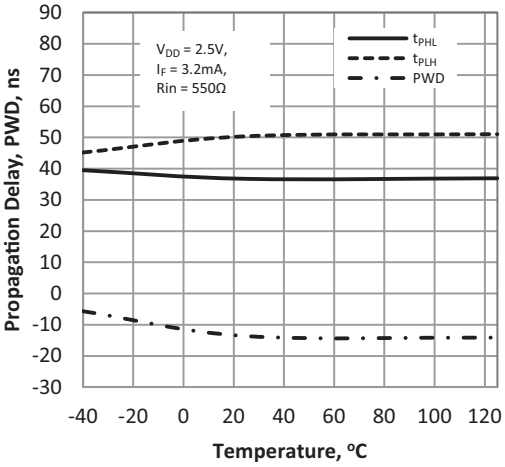


Figure 10: Typical Switching Timing (Propagation Delay, PWD) vs Temperature at 2-mA LED Driving Current, 3.3V Supply

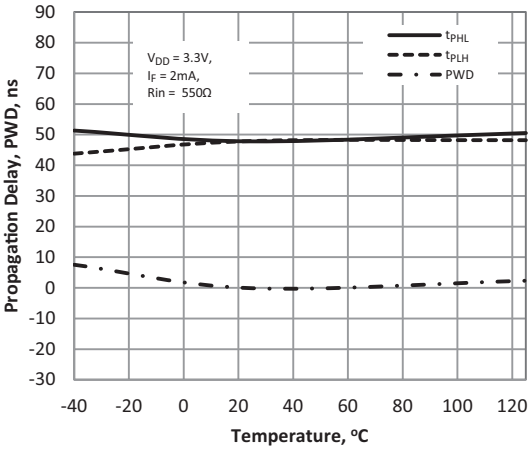


Figure 11: Typical Switching Timing (Propagation Delay, PWD) vs Temperature at 3.2-mA LED Driving Current, 3.3V Supply

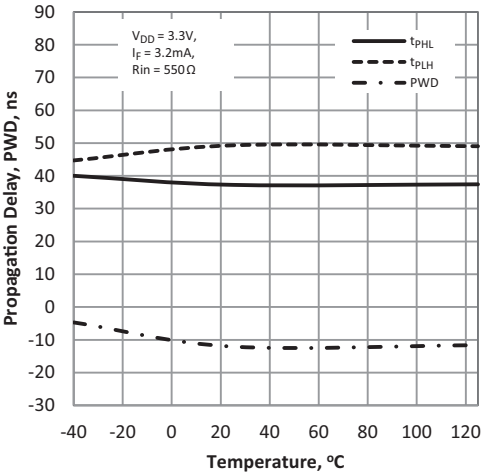
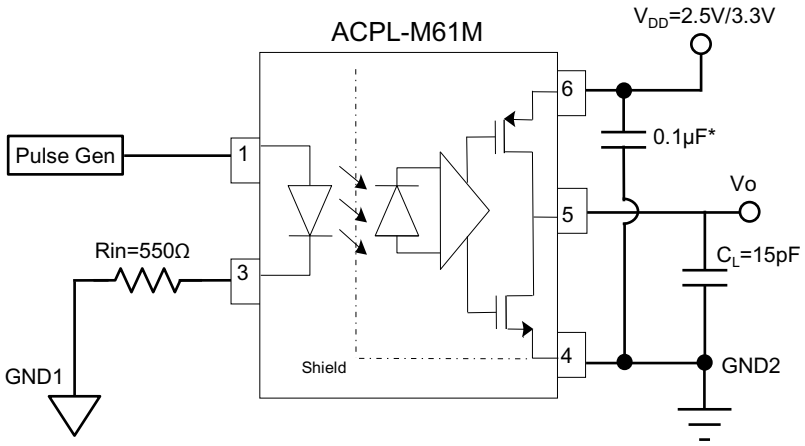
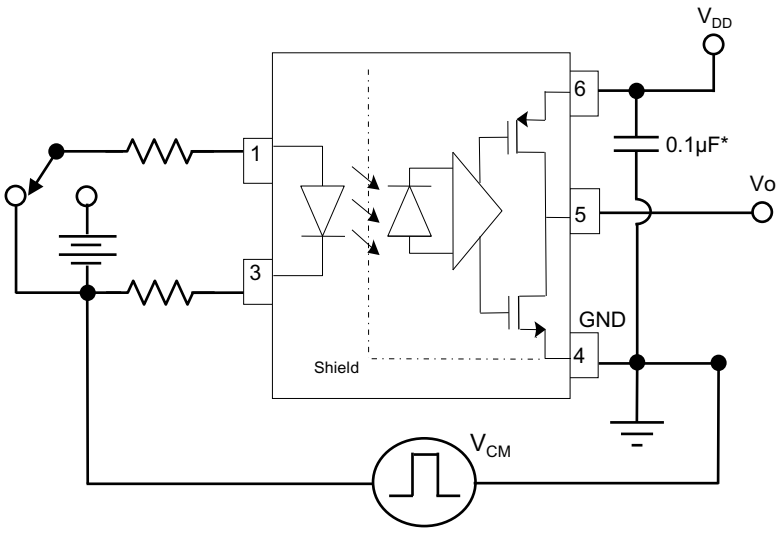


Figure 12: Switching Timing Test Circuit



* Bypass capacitor at no more than 3 mm from optocoupler's power pins (V_{DD}, GND).

Figure 13: Common Mode Transient Immunity Test Circuit



* Bypass capacitor at no more than 3 mm from optocoupler's power pins (V_{DD}, GND).

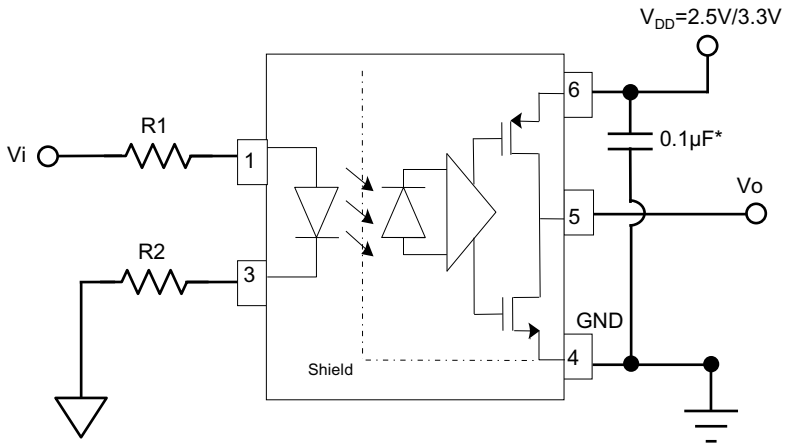
Bypassing and PC Board Layout

The ACPL-M61M provides CMOS logic output due to the high-speed CMOS IC technology used.

The external components required for proper operation are the input limiting resistors and the output's power supply bypass capacitor. It should be placed as close as possible to the power-supply pins, and the recommended value is 0.1 µF.

$R_T = R_1 + R_2$, $R_1/R_2 \approx 1.5$

Figure 14: Recommended Application Circuit



* Bypass capacitor at no more than 3 mm from optocoupler's power pins (V_{DD}, GND).

Mouser Electronics

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