Description

The 9ZXL1951D is a second-generation, enhanced performance DB1900ZL derivative buffer. The part is a pin-compatible upgrade to the 9ZXL1951A, offering a much improved phase jitter performance. It has 8 OE# pins that can be configured via SMBus to control up to 16 of the device's 19 outputs, and is packaged in a 6 x 6 mm QFN package for maximum space savings. A fixed external feedback maintains low drift for critical QPI/UPI applications.

PCIe Clocking Architectures Supported

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Recommended Applications

- Servers, Storage, Networking, SSDs

Key Specifications

- Cycle-to-cycle jitter: < 50ps
- Output-to-output skew: < 50ps
- Input-to-output delay: Fixed at 0ps
- Input-to-output delay variation: < 50ps
- Phase jitter: PCIe Gen4 < 0.5ps rms
- Phase jitter: QPI/UPI > = 9.6GB/s < 0.2ps rms
- Phase jitter: IF-UPI < 1.0ps rms

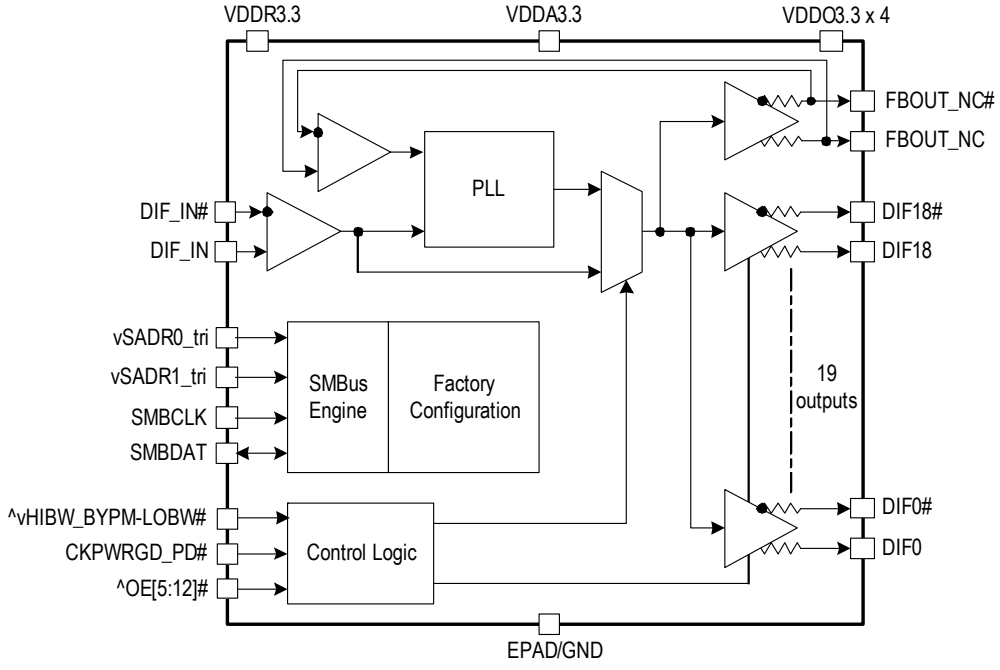
Features

- LP-HCSL outputs with 85Ω Zout; eliminates 76 termination resistors, saves 130mm^2 area
- 8 OE# pins configurable to control up to 16 outputs; easy power management
- 9 selectable SMBus addresses; multiple devices can share same SMBus segment
- Selectable PLL BW; minimizes jitter peaking in cascaded PLL topologies
- Hardware/SMBus control of PLL bandwidth and bypass; change mode without power cycle
- Spread spectrum compatible; tracks spreading input clock for EMI reduction
- 100MHz PLL mode; UPI support
- DIF input and DIF outputs on outer row of pins; easy board routing
- 6 x 6 mm dual-row 80-GQFN; smallest 19-output Z-buffer

Output Features

19 Low-Power (LP) HCSL output pairs with 85Ω Zout

Block Diagram



Pin Assignments

Figure 1. Pin Assignments for 6 × 6 mm 80-GQFN Package – Top View

Pin Descriptions

Table 1. Pin Descriptions

Number		Name	Type	Description
A	1	DIF16#	Output	Differential complementary clock output.
A	2	DIF16	Output	Differential true clock output.
A	3	DIF15#	Output	Differential complementary clock output.
A	4	DIF15	Output	Differential true clock output.
A	5	DIF14#	Output	Differential complementary clock output.
A	6	DIF14	Output	Differential true clock output.
A	7	NC	—	No connection.
A	8	DIF13#	Output	Differential complementary clock output.
A	9	DIF13	Output	Differential true clock output.
A	10	DIF12#	Output	Differential complementary clock output.
A	11	DIF12	Output	Differential true clock output.
A	12	DIF11#	Output	Differential complementary clock output.
B	1	DIF17	Output	Differential true clock output.
B	2	VDDO3.3	Power	Power supply for outputs, nominal 3.3V.
B	3	NC	—	No connection.
B	4	NC	—	No connection.
B	5	VDDA3.3	Power	3.3V power for the PLL core.
B	6	NC	—	No connection.
B	7	vSADR0_tri	Input	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins to decode SMBus addresses. It has an internal 120kΩ pull-down resistor. See the *SMBus Addressing* table.
B	8	vSADR1_tri	Input	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins to decode SMBus addresses. It has an internal 120kΩ pull-down resistor. See the *SMBus Addressing* table.
B	9	^vHIBW_BYPM_LOBW#	Latched In	Tri-level input to select High BW, Bypass or Low BW Mode. This pin is biased to $V_{DD}/2$ (Bypass Mode) with internal pull-up/pull-down resistors. See *PLL Operating Mode* table for details.
B	10	^OE12#	Input	Active low input for enabling output 12. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
B	11	VDDO3.3	Power	Power supply for outputs, nominal 3.3V.
B	12	DIF11	Output	Differential true clock output.
C	1	DIF17#	Output	Differential complementary clock output.
C	2	NC	—	No connection.
C	11	^OE11#	Input	Active low input for enabling output 11. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.

Table 1. Pin Descriptions (Cont.)

Number		Name	Type	Description
C	12	DIF10#	Output	Differential complementary clock output.
D	1	DIF18	Output	Differential true clock output.
D	2	NC	—	No connection.
D	11	NC	—	No connection.
D	12	DIF10	Output	Differential true clock output.
E	1	DIF18#	Output	Differential complementary clock output.
E	2	NC	—	No connection.
E	11	^OE10#	Input	Active low input for enabling output 10. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
E	12	NC	—	No connection.
F	1	NC	—	No connection.
F	2	FBOUT_NC#	Output	Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
F	11	NC	—	No connection.
F	12	DIF9#	Output	Differential complementary clock output.
G	1	DIF_IN	Input	HCSL true input.
G	2	FBOUT_NC	Output	True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
G	11	^OE9#	Input	Active low input for enabling output 9. This pin has an internal pull-up resistor. 1 =disable outputs, 0 = enable outputs.
G	12	DIF9	Output	Differential true clock output.
H	1	DIF_IN#	Input	HCSL complementary input.
H	2	VDDR3.3	Power	3.3V power for differential input clock (receiver). This V_{DD} should be treated as an analog power rail and filtered appropriately.
H	11	CKPWRGD_PD#	Input	3.3V input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.
H	12	DIF8#	Output	Differential complementary clock output.
J	1	DIF0	Output	Differential true clock output.
J	2	NC	—	No connection.
J	11	^OE8#	Input	Active low input for enabling output 8. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
J	12	DIF8	Output	Differential true clock output.
K	1	DIF0#	Output	Differential complementary clock output.
K	2	NC	—	No connection.

Table 1. Pin Descriptions (Cont.)

Number		Name	Type	Description
K	11	^OE7#	Input	Active low input for enabling output 7. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
K	12	DIF7#	Output	Differential complementary clock output.
L	1	DIF1	Output	Differential true clock output.
L	2	VDDO3.3	Power	Power supply for outputs, nominal 3.3V.
L	3	NC	—	No connection.
L	4	SMBDAT	I/O	Data pin of SMBUS circuitry.
L	5	SMBCLK	Input	Clock pin of SMBUS circuitry.
L	6	NC	—	No connection.
L	7	NC	—	No connection.
L	8	^OE5#	Input	Active low input for enabling output 5. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
L	9	NC	—	No connection.
L	10	^OE6#	Input	Active low input for enabling output 6. This pin has an internal pull-up resistor. 1 = disable outputs, 0 = enable outputs.
L	11	VDDO3.3	Power	Power supply for outputs, nominal 3.3V.
L	12	DIF7	Output	Differential true clock output.
M	1	DIF1#	Output	Differential complementary clock output.
M	2	DIF2	Output	Differential true clock output.
M	3	DIF2#	Output	Differential complementary clock output.
M	4	DIF3	Output	Differential true clock output.
M	5	DIF3#	Output	Differential complementary clock output.
M	6	NC	—	No connection.
M	7	DIF4	Output	Differential true clock output.
M	8	DIF4#	Output	Differential complementary clock output.
M	9	DIF5	Output	Differential true clock output.
M	10	DIF5#	Output	Differential complementary clock output.
M	11	DIF6	Output	Differential true clock output.
M	12	DIF6#	Output	Differential complementary clock output.
—		EPAD	GND	Connect EPAD to ground.

Power Management

Table 2. Power Management and Output Control Truth Table

Inputs					Outputs		PLL State
CKPWRGD_PD#	DIF_IN	OEx bit Byte[2:0]	OE Pin CFG bit Byte[4,8]	OEx# Pin	DIFx	FBOUT_NC	
0	X	X	X	X	Low/Low	Low/Low	Off
1	Running	0	X	X	Low/Low	Running	On
		1	0	X	Running	Running	On
1	Running	1	1	0	Running	Running	On
		1	1	1	Low/Low	Running	On

Table 3. Power Connections

Pin Number		Description
V_{DD}	GND	
B5	EPAD	Analog PLL
H2		Analog input
B2, B11, L2, L11		DIF clocks

Table 4. PLL Operating Mode Table

HIBW_BYPM_LOBW#	Byte0, bits (7:6)
Low (PLL Low BW)	00
Mid (Bypassed and Off)	01
High (PLL High BW)	11

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9ZXL1951D at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	
SMBus Output Low Voltage	V_{OLSMB}	At I_{PULLUP}.			0.4	V	
SMBus Sink Current	I_{PULLUP}	At V_{OL}.	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max V_{IL} - 0.15V) to (Min V_{IH} + 0.15V).			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min V_{IH} + 0.15V) to (Max V_{IL} - 0.1V).			300	ns	1
SMBus Operating Frequency	f_{SMB}	SMBus operating frequency.			400	kHz	5

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

[5] The differential input clock must be running for the SMBus to be active.

Electrical Characteristics

$T_A = T_{AMB}$. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Table 6. DIF_IN Clock Input Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Crossover Voltage – DIF_IN	V_{CROSS}	Cross over voltage.	150		900	mV	1
Input Swing – DIF_IN	V_{SWING}	Differential value.	300			mV	1
Input Slew Rate – DIF_IN	dv/dt	Measured differentially.	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND.	-5		5	µA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform.	45		55	%	1
Input Jitter – Cycle to Cycle	J_{DIFIn}	Differential measurement.	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through ±75mV window centered around differential zero.

Table 7. Input/Supply/Common Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	$V_{DD}x$	Supply voltage for core and analog.	3.135	3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range.	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, tri-level inputs.	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, tri-level inputs.	GND - 0.3		0.8	V	
Input High Voltage	V_{IH}	Tri-level inputs.	2.2		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IM}	Tri-level inputs.	1.2	$V_{DD}/2$	1.8	V	
Input Low Voltage	V_{IL}	Tri-level inputs.	GND - 0.3		0.8	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DD}.	-5		5	µA	
	I_{INP}	Single-ended inputs. V_{IN} = 0 V; inputs with internal pull-up resistors. V_{IN} = V_{DD}; inputs with internal pull-down resistors.	-100		100	µA	
Input Frequency	F_{ibyp}	V_{DD} = 3.3V, Bypass Mode.	1		400	MHz	
	F_{ipll}	V_{DD} = 3.3V, 100MHz PLL Mode.	98.5	100.00	102	MHz	
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic inputs, except DIF_IN.	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs.	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance.			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} power-up and after input clock stabilization or de-assertion of PD# to 1st clock.		1.0	1.8	ms	1,2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable frequency for PCIe applications (Triangular modulation).	30	31.500	33	kHz	
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion. DIF stop after OE# deassertion.	4	5	10	clocks	1,2,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion.		49	300	µs	1,3
Tfall	t_F	Fall time of control inputs.			5	ns	2
Trise	t_R	Rise time of control inputs.			5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

Table 8. HCSL/LP-HCSL Outputs

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limit	Units	Notes
Slew Rate	dV/dt	Scope averaging on, fast setting.	2	2.6	4	1 – 4	V/ns	1,2,3
	dV/dt	Scope averaging on, slow setting.	1	1.8	3	1 – 4	V/ns	1,2,3
Slew Rate Matching	ΔdV/dt	Single-ended measurement.		4.3	20	20	%	1,4,7
Maximum Voltage	Vmax	Measurement on single ended signal using absolute value. (scope averaging off).	660	751	850	1150	mV	7
Minimum Voltage	Vmin		-150	-1.9	150	-300		7
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.	250	381	550	250 – 550	mV	1,5,7
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.		15	140	140	mV	1,6,7

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

Table 9. Current Consumption

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	I_{DDVDD}	All outputs 100MHz, C_L = 2pF; Zo = 85Ω.		171	200	mA	
	$I_{DDVDDA/R}$	PLL Mode, all outputs 100MHz, C_L = 2pF; Zo = 85Ω.		45	55	mA	1
Powerdown Current	$I_{DDVDDPD}$	All differential pairs low-low		1	2	mA	
	$I_{DDVDDA/RPD}$	All differential pairs low-low		4	6	mA	

[1] In Bypass Mode (PLL off), $I_{DDVDDA/R}$ is 12mA.

Table 10. Skew and Differential Jitter Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
CLK_IN, DIF[x:0]	t_{SPO_PLL}	Input-to-output skew in PLL Mode nominal value at 25°C, 3.3V.	-100	-14	100	ps	1,2,4, 5,8
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-output skew in Bypass Mode nominal value at 25°C, 3.3V.	2.3	2.9	3.5	ns	1,2,3, 5,8
CLK_IN, DIF[x:0]	t_{DSPO_PLL}	Input-to-output skew variation in PLL Mode across voltage and temperature.	-50	0	50	ps	1,2,3, 5,8
CLK_IN, DIF[x:0]	t_{DSPO_BYPIND}	Input-to-output skew variation in Bypass Mode across **commercial** voltage and temperature.	-250	0	250	ps	1,2,3, 5,8
CLK_IN, DIF[x:0]	t_{DSPO_BYPCOM}	Input-to-output skew variation in Bypass Mode across **industrial** voltage and temperature.	-300	0	300	ps	1,2,3, 5,8
CLK_IN, DIF[x:0]	t_{DTE}	Random differential tracking error between two 9ZX devices in Hi BW Mode.			5	ps (rms)	1,2,3, 5,8
CLK_IN, DIF[x:0]	t_{DSSTE}	Random differential spread spectrum tracking error between two 9ZX devices in Hi BW Mode.			75	ps	1,2,3, 5,8
DIF[x:0]	t_{SKEW_ALL}	Output-to-output skew across all outputs (common to Bypass and PLL Mode).		39	50	ps	1,2,3, 8
PLL Jitter Peaking	$j_{peak-hibw}$	LOBW#_BYPASS_HIBW = 1.	0	1.3	2.5	dB	7,8
PLL Jitter Peaking	$j_{peak-lobw}$	LOBW#_BYPASS_HIBW = 0.	0	1.3	2	dB	7,8
PLL Bandwidth	pll_{HIBW}	LOBW#_BYPASS_HIBW = 1.	2	2.6	4	MHz	8,9
PLL Bandwidth	pll_{LOBW}	LOBW#_BYPASS_HIBW = 0.	0.7	1.0	1.4	MHz	8,9
Duty Cycle	t_{DC}	Measured differentially, PLL Mode.	45	50	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode at 100MHz.	-0.5	0.0	0.5	%	1,10
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	PLL Mode.		14	50	ps	1,11
		Additive Jitter in Bypass Mode.		0.1	50	ps	1,11

[1] Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

[3] All Bypass Mode input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

[4] This parameter is deterministic for a given device.

[5] Measured with scope averaging on to find mean value.

[6] 't' is the period of the input clock.

[7] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

[8] Guaranteed by design and characterization, not 100% tested in production.

[9] Measured at 3db down or half power point.

[10] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[11] Measured from differential waveform.

Table 11. Filtered Phase Jitter Parameters – PCIe Common Clocked (CC) Architectures

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1-CC}$	PCIe Gen 1		14	30	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz)		0.24	0.7	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz)		1.1	1.5	3.1	ps (rms)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)		0.26	0.4	1	ps (rms)	1,2
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)		0.26	0.4	0.5	ps (rms)	1,2
Additive Phase Jitter, Bypass Mode	$t_{jphPCIeG1-CC}$	PCIe Gen 1		0	0.05	Not applicable	ps (p-p)	1,2,3, 4
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz)		0	0.05		ps (rms)	1,2,3, 4
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz)		0	0.05		ps (rms)	1,2,3, 4
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)		0	0.05		ps (rms)	1,2,3, 4
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)		0	0.05		ps (rms)	1,2,3, 4

[1] Applies to all differential outputs, when driven by 9SQL495x or equivalent, guaranteed by design and characterization.

[2] According to the PCIe Base Specification Rev 4.0 version 0.7 draft.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] For RMS values additive jitter is calculated by solving the following equation for b [$b = sqrt(c^2 - a^2)$] where “a” is rms input jitter and “c” is rms total jitter.

Table 12. Filtered Phase Jitter Parameters – PCIe Independent Reference (IR) Architectures

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG2-SRIS}$	PCIe Gen 2 (PLL BW of 16MHz, CDR = 5MHz)		0.9	1	2	ps (rms)	1,2,5
	$t_{jphPCIeG3-SRIS}$	PCIe Gen 3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)		0.6	0.65	0.7	ps (rms)	1,2,5
Additive Phase Jitter, Bypass Mode	$t_{jphPCIeG2-SRIS}$	PCIe Gen 2 (PLL BW of 16MHz, CDR = 5MHz)		0	0.15	Not applicable	ps (rms)	1,4,5
	$t_{jphPCIeG3-SRIS}$	PCIe Gen 3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)		0.0	0.03		ps (rms)	1,4,5

[1] Applies to all differential outputs, when driven by 9SQL495x or equivalent, guaranteed by design and characterization.

[2] According to the PCIe Base Specification Rev 4.0 version 0.7 draft.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] For RMS values additive jitter is calculated by solving the following equation for b [$b = sqrt(c^2 - a^2)$] where "a" is rms input jitter and "c" is rms total jitter.

[5] IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures. According to the PCIe Base Specification Rev 4.0 version 0.7 draft, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted industry limits using widely accepted industry filters are used to populate this table. There are no accepted filters or limits for IR clock architectures at PCIe Gen1 or Gen4 data rates.

Table 13. Filtered Phase Jitter Parameters – QPI/UPI

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, PLL Mode	t_{jphQPI_UPI}	QPI & UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.16	0.4	0.5	ps (rms)	1,2
		QPI & UPI (100MHz, 8.0Gb/s, 12UI)		0.08	0.15	0.3		1,2
		QPI & UPI (100MHz, ≥ 9.6Gb/s, 12UI)		0.07	0.03	0.2		1,2
	$t_{jphIF-UPI}$	IF-UPI		0.1 0.17	0.14 0.2	1		1,4,5
Additive Phase Jitter, Bypass Mode	t_{jphQPI_UPI}	QPI & UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.00	0.01	Not applicable	ps (rms)	1,2,3
		QPI & UPI (100MHz, 8.0Gb/s, 12UI)		0.00	0.01			1,2,3
		QPI & UPI (100MHz, ≥ 9.6Gb/s, 12UI)		0.00	0.01			1,2,3
	$t_{jphIF-UPI}$	IF-UPI		0.06	0.08			1,4

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Calculated from Intel-supplied clock jitter tool, when driven by 9SQL495x or equivalent.

[3] For RMS values, additive jitter is calculated by solving for b where [$b = sqrt(c^2 - a^2)$] where "a"' is rms input jitter and "c" is rms total jitter.

[4] Calculated from phase noise analyzer when driven by Wenzel Associates source with Intel-specified brick-wall filter applied.

[5] Top number is when the buffer is in Low BW mode, bottom number is when the buffer is in High BW mode.

Table 14. Unfiltered Phase Jitter Parameters – 12kHz to 20MHz

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, PLL Mode	$t_{jph12k-20MHi}$	PLL High BW, SSC Off, 100MHz		181	250	Not applicable	fs (rms)	1,2
Phase Jitter, PLL Mode	$t_{jph12k-20MLo}$	PLL Low BW, SSC Off, 100MHz		199	250		fs (rms)	1,2
Additive Phase Jitter, Bypass Mode	$t_{jph12k-20MByp}$	Bypass Mode, SSC Off, 100MHz		106	150		fs (rms)	1,2,3

[1] Applies to all outputs when driven by Wenzel clock source.

[2] 12kHz to 20MHz brick wall filter.

[3] Additive jitter for RMS values is calculated by solving for b [$b = sqrt(c^2 - a^2)$] where "a" is rms input jitter and "c" is rms total jitter.

Test Loads

Low-Power HCSL Output Test Load
(standard PCIe source-terminated test load)

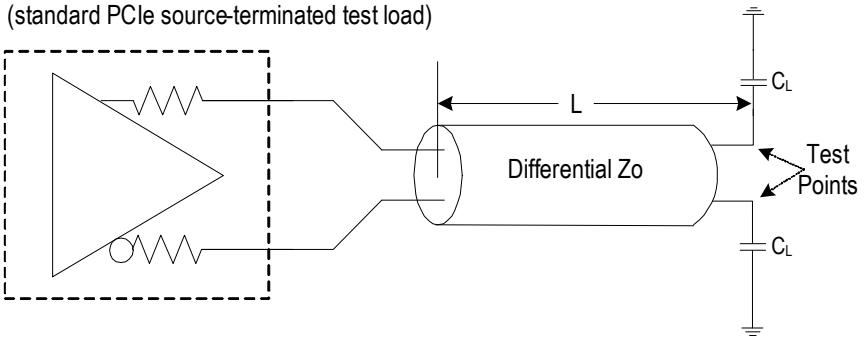


Table 15. Parameters for Low-Power HCSL Output Test Load

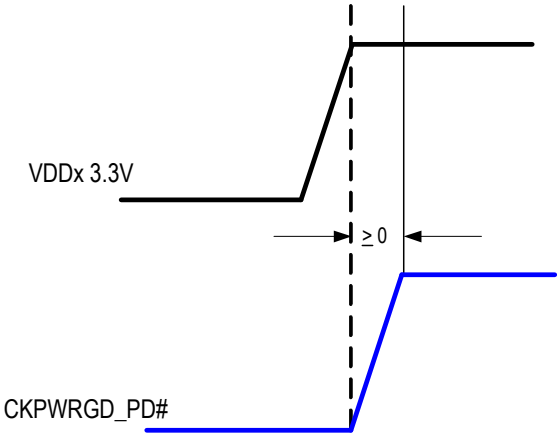
Rs (Ω)	Zo (Ω)	L (Inches)	C_L (pF)
Internal	85	12	2

Alternate Terminations

The LP-HCSL output can easily drive other logic families. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for termination schemes for LVPECL, LVDS, CML and SSTL.

Power-up Timing

Figure 2. Power-up Timing Diagram



SMBus Addressing

Table 16. 9ZXL1951 SMBus Addressing

SADR(1:0)_tri	SMBus Address (Read/Write bit = 0)
00	D8
0M	DA
01	DE
M0	C2
MM	C4
M1	C6
10	CA
1M	CC
11	CE

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: PLL Mode and Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	B9	PLL Mode 1	PLL Operating Mode Rd back 1	R	See PLL Operating Mode Readback table		Latch
Bit 6	B9	PLL Mode 0	PLL Operating Mode Rd back 0	R			Latch
Bit 5	D1/E1	DIF18_En	Output Enable	RW	Low/Low	Enable	1
Bit 4	B1/C1	DIF17_En	Output Enable	RW	Low/Low	Enable	1
Bit 3	A2/A1	DIF16_En	Output Enable	RW	Low/Low	Enable	1
Bit 2	Reserved						0
Bit 1	Reserved						0
Bit 0	Reserved						0

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	L12/K12	DIF7_En	Output Enable	RW	Low/Low	Enabled or Pin Control (see Byte 4 or Byte 8)	1
Bit 6	M11/M12	DIF6_En	Output Enable	RW			1
Bit 5	M9/M10	DIF5_En	Output Enable	RW			1
Bit 4	M7/M8	DIF4_En	Output Enable	RW			1
Bit 3	M4/M5	DIF3_En	Output Enable	RW			1
Bit 2	M2/M3	DIF2_En	Output Enable	RW			1
Bit 1	L1/M1	DIF1_En	Output Enable	RW			1
Bit 0	J1/K1	DIF0_En	Output Enable	RW			1

SMBus Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	A4/A3	DIF15_En	Output Enable	RW	Low/Low	Enabled or Pin Control (see Byte 4 or Byte 8)	1
Bit 6	A6/A5	DIF14_En	Output Enable	RW			1
Bit 5	A9/A8	DIF13_En	Output Enable	RW			1
Bit 4	A11/A10	DIF12_En	Output Enable	RW			1
Bit 3	B12/A12	DIF11_En	Output Enable	RW			1
Bit 2	D12/C12	DIF10_En	Output Enable	RW			1
Bit 1	G12/F12	DIF9_En	Output Enable	RW			1
Bit 0	J12/H12	DIF8_En	Output Enable	RW			1

SMBus Table: PLL SW Override Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	Reserved						0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	Reserved						0
Bit 3	—	PLL_SW_EN	Enable S/W control of PLL BW	RW	HW Latch	SMBus Control	0
Bit 2	—	PLL Mode 1	PLL Operating Mode 1	RW	See PLL Operating Mode Readback table		1
Bit 1	—	PLL Mode 0	PLL Operating Mode 1	RW			1
Bit 0	Reserved						0

Note: Setting bit 3 to '1' allows the user to override the Latch value from pin 4 via use of bits 2 and 1. Use the values from the PLL Operating Mode Readback table. Note that Byte 0, Bits 7:6 will keep the value originally latched on pin 4. If the user changes these bits, a warm reset of the system will have to accomplished.

SMBus Table: OE Pin Configuration A Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	B10	OE12#_CFGA	Controls DIF12	RW	Does not Control	Controls	1
Bit 6	C11	OE11#_CFGA	Controls DIF11	RW			1
Bit 5	E11	OE10#_CFGA	Controls DIF10	RW			1
Bit 4	G11	OE09#_CFGA	Controls DIF9	RW			1
Bit 3	J11	OE08#_CFGA	Controls DIF8	RW			1
Bit 2	K11	OE07#_CFGA	Controls DIF7	RW			1
Bit 1	L10	OE06#_CFGA	Controls DIF6	RW			1
Bit 0	L8	OE05#_CFGA	Controls DIF5	RW			1

SMBus Table: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	—	RID3	REVISION ID	R	D rev = 0011		0
Bit 6	—	RID2		R			0
Bit 5	—	RID1		R			1
Bit 4	—	RID0		R			1
Bit 3	—	VID3	VENDOR ID	R	—	—	0
Bit 2	—	VID2		R	—	—	0
Bit 1	—	VID1		R	—	—	0
Bit 0	—	VID0		R	—	—	1

SMBus Table: Device ID

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	—	Device ID 7 (MSB)		R	1951 is C4 Hex		1
Bit 6	—	Device ID 6		R			1
Bit 5	—	Device ID 5		R			0
Bit 4	—	Device ID 4		R			0
Bit 3	—	Device ID 3		R			0
Bit 2	—	Device ID 2		R			1
Bit 1	—	Device ID 1		R			0
Bit 0	—	Device ID 0		R			x

SMBus Table: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	Reserved						0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	—	BC4	Writing to this register configures how many bytes will be read back.	RW	Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default.		0
Bit 3	—	BC3		RW			1
Bit 2	—	BC2		RW			0
Bit 1	—	BC1		RW			0
Bit 0	—	BC0		RW			0

SMBus Table: OE Pin Configuration B Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	B10	OE12#_CFGB	Controls DIF13	RW	Does not Control	Controls	0
Bit 6	C11	OE11#_CFGB	Controls DIF14	RW			0
Bit 5	E11	OE10#_CFGB	Controls DIF15	RW			0
Bit 4	G11	OE09#_CFGB	Controls DIF0	RW			0
Bit 3	J11	OE08#_CFGB	Controls DIF1	RW			0
Bit 2	K11	OE07#_CFGB	Controls DIF2	RW			0
Bit 1	L10	OE06#_CFGB	Controls DIF3	RW			0
Bit 0	L8	OE05#_CFGB	Controls DIF4	RW			0

Package Drawings

Figure 3. 80-GQFN Package Drawings– page 1

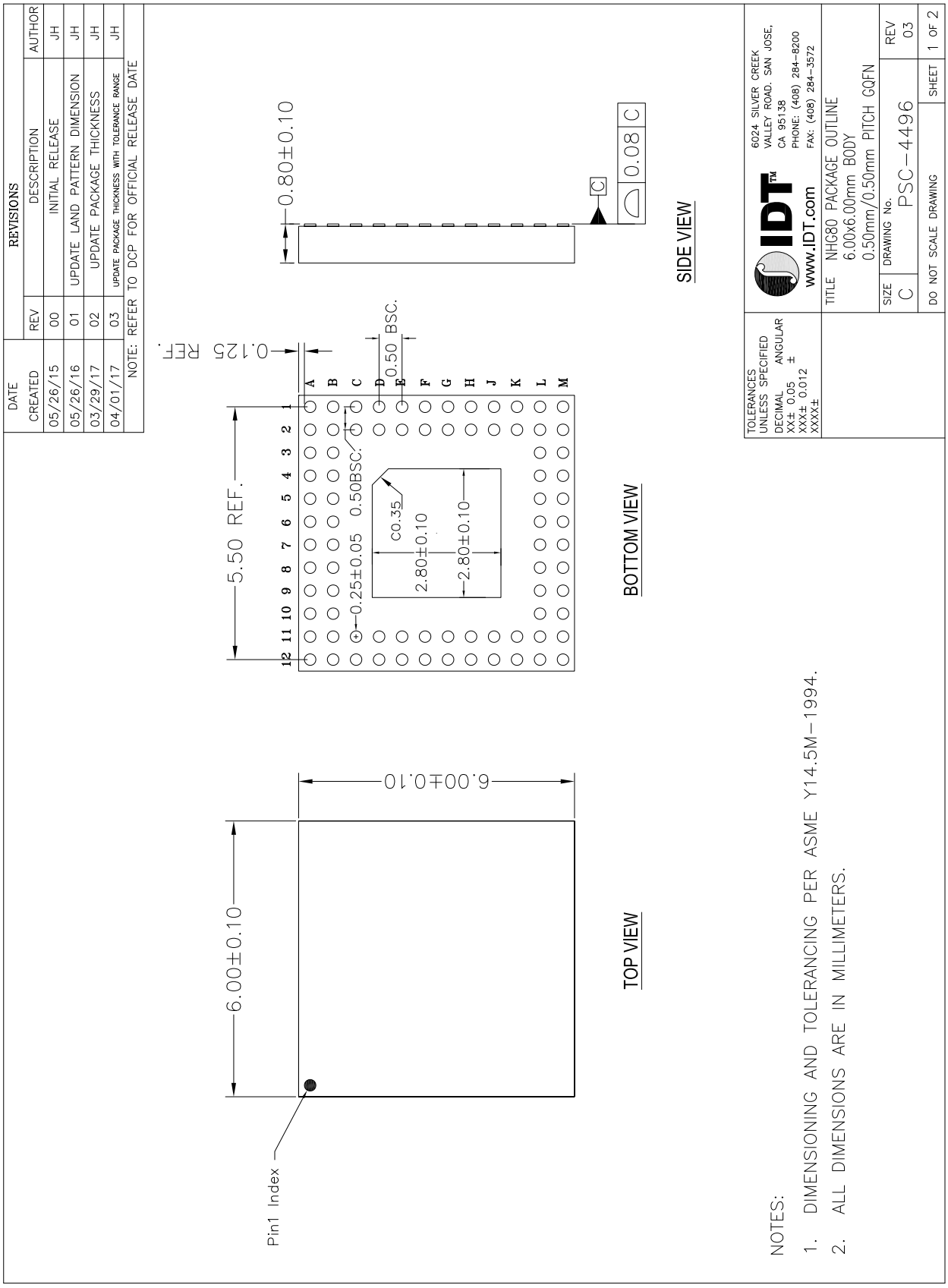
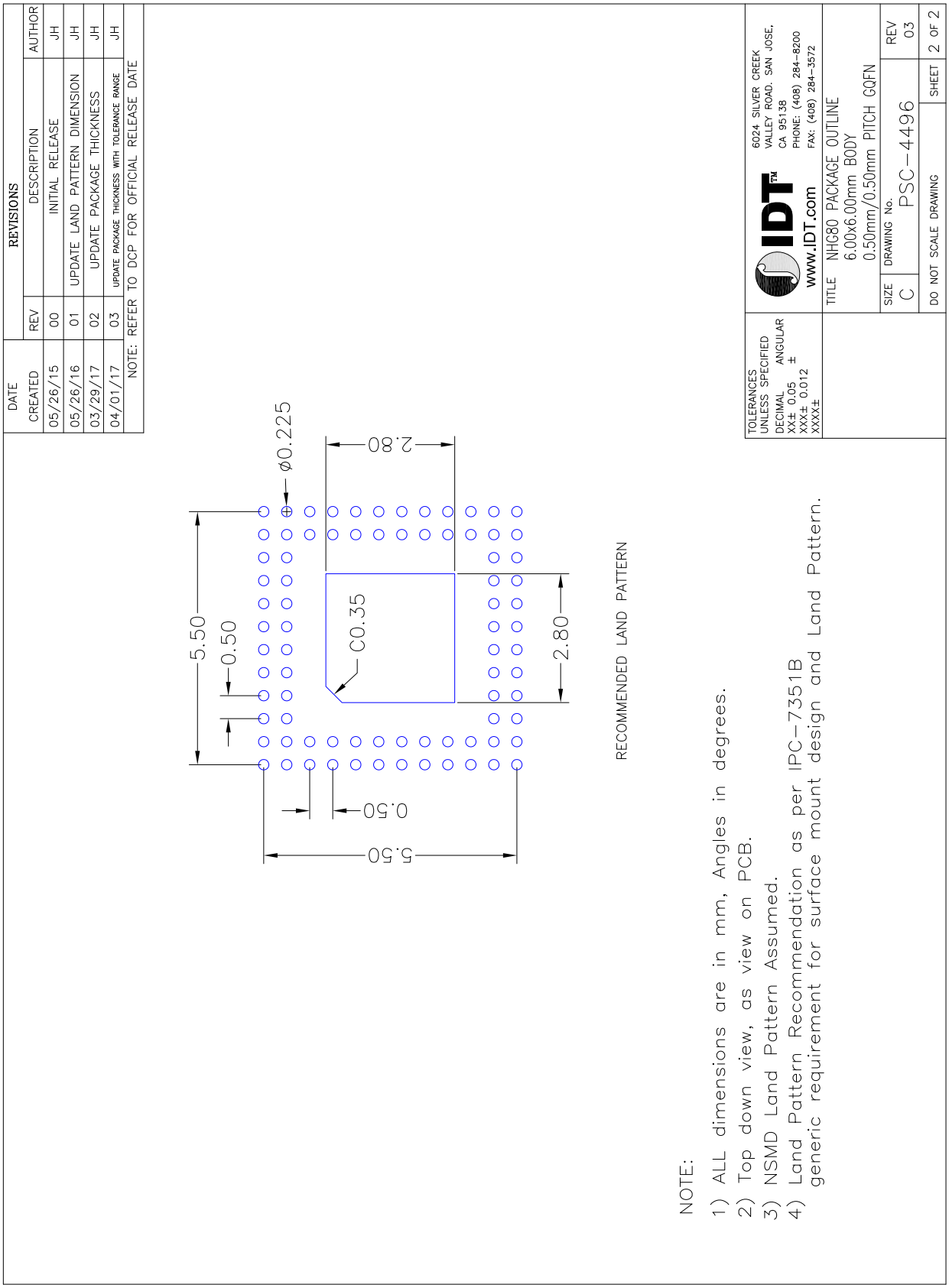


Figure 4. 80-GQFN Package Drawings– page 2



Marking Diagram

1. “YYWW” is the last digits of the year and week that the part was assembled.
2. “$” denotes mark code.
3. “I” denotes industrial temperature.
4. “LOT” denotes the lot sequence code.

Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature
9ZXL1951DNHGI	6 × 6 × 0.5 mm 80-GQFN	Tray	-40° to +85°C
9ZXL1951DNHGI8	6 × 6 × 0.5 mm 80-GQFN	Tape and Reel	-40° to +85°C

“G” designates PB-free configuration, RoHS compliant.

“D” is the device revision designator (will not correlate with the datasheet revision).

Revision History

Revision Date	Description of Change
December 1, 2017	Removed “5V tolerant” reference in pins L4 and L5 descriptions.
September 29, 2017	▪ Updated Slew Rate Matching conditions.
May 1, 2017	▪ Updated front page text for family consistency. ▪ Updated Filtered Phase Jitter Parameters - QPI/UPI table to add IF-UPI. ▪ Test load updated to standard test load drawing for family.
April 3, 2017	▪ Updated package outline drawings to latest version (revision 03).
March 31, 2017	▪ Updated package outline drawings to latest version (revision 02).
March 27, 2017	Initial release.

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