CrCM PFC Boost Converter Design

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1   Introduction

Power Factor Correction (PFC) shapes the input current of the power supply to be in synchronization with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, load should look like a pure resistance load. The input current is a clean sine wave and in phase with the voltage, with no input current harmonics. This document is intended to discuss the topology and operational mode for low power (<300W) PFC applications, and provide detailed design equations through an example.

2   Boost topology

Active PFC can be achieved by any basic topology, the boost converter (Figure 2.1) is the most popular topology used in PFC applications.

<u>The advantages of boost topology are:</u>

☺ Voltage gain >1 works for AC input
☺ Only one MOSFET
☺ Control Voltage referred to ground
☺ capable of high efficiency
☺ simple choke, no problems with magnetic coupling
☺ CCM provides continuous input current
☺ CCM mode with favorable waveform   factor for conduction loss

<u>The disadvantages of boost topology are:</u>

☹ MOSFET: $V_{DS} \approx V_O > V_I$
☹ no galvanic isolation - short circuit protection a problem
☹ Medium ripple current loading of   output capacitor
☹ CCM Mode requires hard switching   of boost diode- SiC required for high efficiency

<u>Comments on other topologies:</u>

☹ Buck:

          Lacks voltage gain; pulsating input current

☹Buck/Boost:

           Complex, output voltage has opposite polarity, pulsating input current

☹ Flyback:

           Easily resistive, but pulsating input current (can be solved with interleaved),

           but 2x copper losses for given magnetic

☹ SEPIC:

         Step down/step up with continuous input current, but having two inductors,

          two capacitors, more complex control, only one inductor can be made sinusoidal, more distortion.

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Boost Key Waveforms

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \quad \text{(CCM operation)} \sim \text{(CrCM Operation)}$$
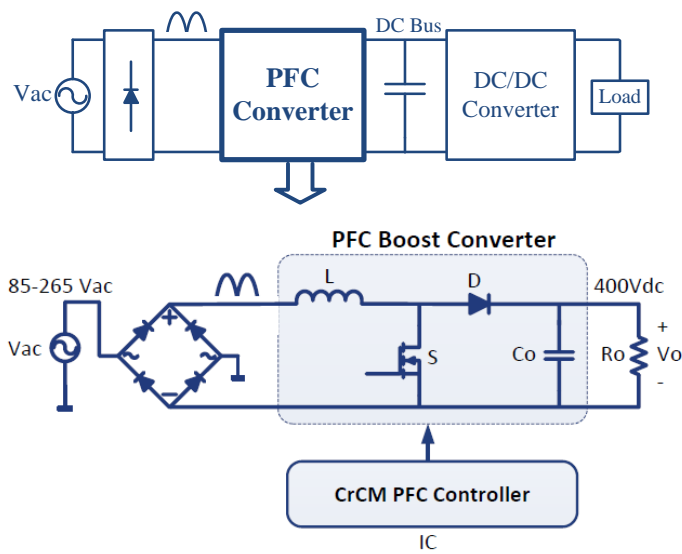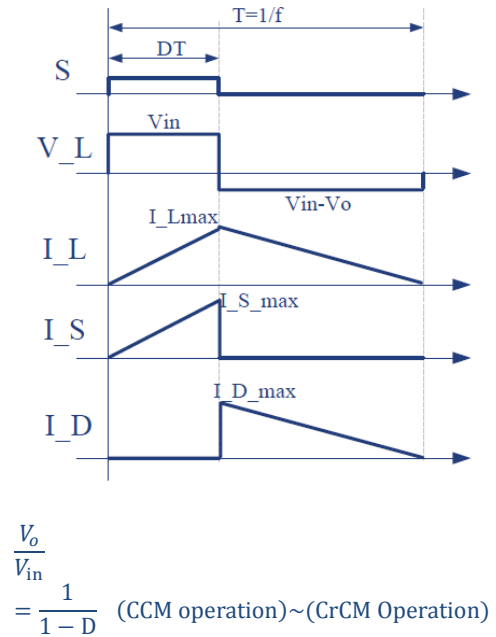
Figure 2.1

3   PFC Modes of Operation

The boost converter can operate in three modes; continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CrCM). Fig. 3.1 shows modeled waveforms to illustrate the inductor and input currents in the three operating modes, for the same exact voltage and power conditions.

Continuous Conduction Mode (CCM)   Critical Conduction Mode (CrM)   Discontinuous Conduction Mode (DCM)

Figure 3.1

Quick comparison between operting modes is given in the table below:

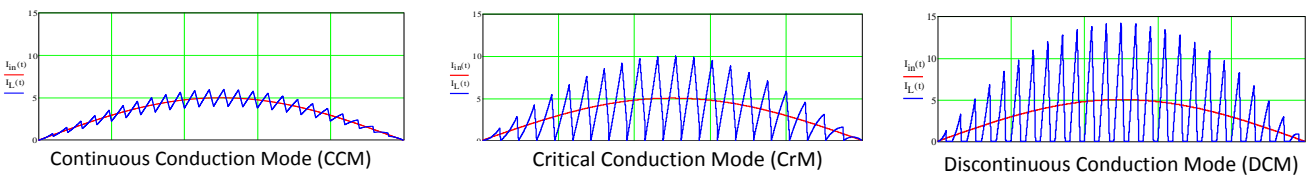| Part / Characteristic	CrCM Variable Frequency	Fixed Frequency CCM	Variable Frequency CCM
Input Current	High Ripple current - large EMI filter	Lower Ripple Current- smaller EMI	Lower Ripple Current - smaller EMI
$I^2 XR$ MOSFET loss	High conduction loss: 9-12% penalty	Trapezoidal waveform- lower loss	Trapezoidal waveform- lower loss
MOSFET t_{ON}	Quasi resonant Ton possible	High- dependent on Boost diode	High- dependent on boost diode
MOSFET t_{OFF}	Toff at 2x input current- high loss High f_{SW} = higher losses	Lower - Toff dependent on design	Lower- Toff dependent on design
Boost Diode	Slow, cheap type OK- select for QR	Best performance with SiC or GaN	Best performance with SiC or GaN
Inductor	Design for high ripple- gapped soft ferrite usually best choice; combine with Litz wire; lower temp range	Design for high average LF current and lower ripple current; powdered core: Kool Mu, High Flux	Design for high average LF current and lower ripple current; powdered core: Kool Mu, High Flux
Output Capacitor	Sized for f_{AC} input current, very HF RMS ripple current	Sized for f_{AC} input current, HF RMS ripple current	Sized for f_{AC} input current, HF RMS ripple current
PF/Distortion	Controller and design dependent; can be quite good	Controller and design dependent; fixed CCM inherently higher distortion due to current loop	Controller and design dependent; very low distortion possible; few off the shelf controller solutions
Power Density	Design dependent on inductor and semiconductors	Design dependent on inductor and semiconductors	Design dependent on inductor and semiconductors
Cost	Low for lower power levels; EMI filter a limit	Better at higher power levels	Better at higher power levels

4   CrCM PFC Boost Design Equations

The following are design equations for the CrCM operated boost, also a design example is integrated to further clarify the usage of all equations. The boost converter encounters the maximum current stress and

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power losses at the minimum line voltage condition (V_{inmin}), hence, all design equations and power losses will be using the low line voltage condition.

Table 1 Specifications

Input voltage	90-270 Vac 60 Hz
Output voltage	420 V
Maximum power	150 W
Minimum frequency	25 kHz
Output voltage ripple	10 Vp-p
Hold-up time	16.6 ms @ V$_{o.min}$=350 V
Estimated efficiency η	0.9

4.1 Rectifier Bridge

The bridge total power loss is calculated using the average input current flowing through two of the bridge rectifying diodes.

$$P_{bridge} = \frac{4 \cdot \sqrt{2}}{\pi} \cdot \frac{P_o}{V_{inmin*\eta}} \cdot V_{f.bridge}$$

$$= \frac{4 \cdot \sqrt{2}}{\pi} \cdot \frac{150}{90*0.9} \cdot V_{f.bridge} = 3.17 \cdot V_{f.bridge} \quad W.$$

$$P_{bridge} = 3.33 * 1.5 = 5W$$

4.2 Input Capacitor

The input high frequency filter Cin has to attenuate the switching noise due to the high frequency inductor current ripple (twice of average line current). The worst conditions will occur on the peak of the minimum input voltage.

The maximum high frequency voltage ripple is usually imposed between 1% and 10% of the minimum rated input voltage. This is expresses by a coefficient r (typically, r = 0.01 to 0.1).

$$C_{in} = \frac{I_{rms}}{2\pi * f_{sw} * r * V_{inmin}}$$

High values of Cin helps EMI filter but causes lower power factor to decrease (higher displacemet component), especially at high input voltage and low load. Low values of Cin improve power factor (lower displacement component) but require larger EMI filter.

4.3 Input Inductor

Lets define following parameters:

a - ratio between peak input voltage and output voltage (DC bus voltage)

$$a\_max := 1.41 \cdot \frac{Vinmax}{Vo}$$

$$a\_max = 9.064 \times 10^{-1}$$

$$a\_min := 1.41 \cdot \frac{Vinmin}{Vo}$$

Ro - equivalent output load (resistance)
$$a\_min = 3.021 \times 10^{-1}$$

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$$Ro := \frac{Vo^2}{Pin}$$

$$Ro = 1.058 \times 10^3$$

Switching frequency is changing with input voltage amplitude and angle. Amplitude varies from minimum (90V*1.41) to maximum (270*1.41) value. Angle is changing from o to π during each half grid cycle. Switching frequency as function of these two variable is represented on graph below:

$$f(x,y) := \frac{1}{2} \cdot \frac{1}{2} y^2 \cdot (1 - y \cdot \sin(x))$$


normalized operating frequency

f
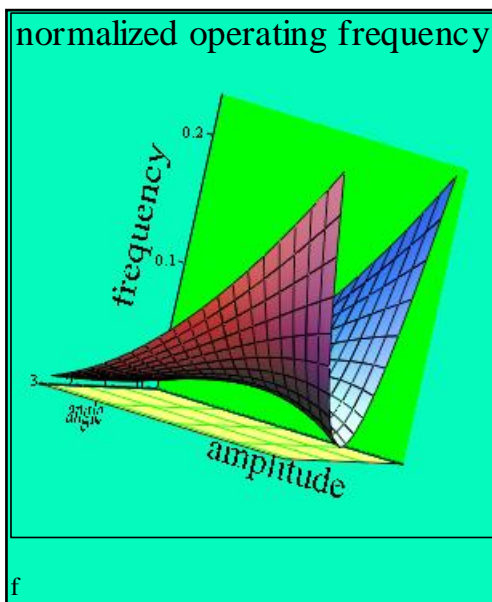
One can notice that during each cycle (angle axis) switching frequency start with maximum value travels through minimum value at peak voltage (angle = π/2) and goes back to maximum. See details below:

operating frequency versus line voltage angle

$f(x, a\_max)$
$f(x, 0.5)$
$f(x, a\_min)$
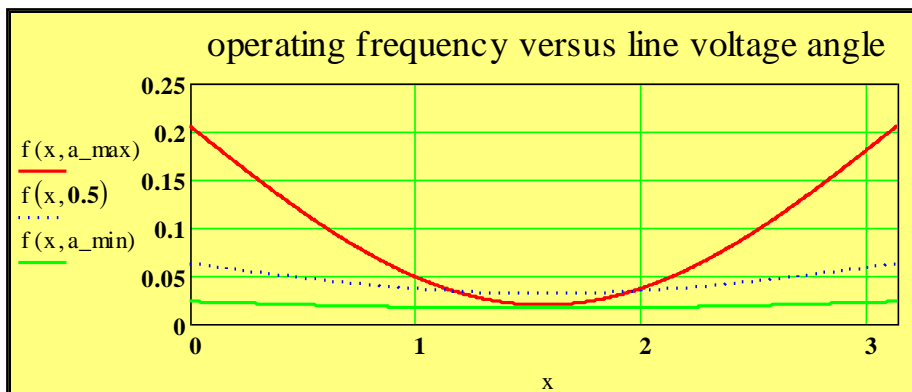
Also, when amplitude changes from minimum value (90*1.41) to the maximum value (270*1.41) frequency travel from one minimum through maximum to another minimum value. One needs to choose smaller of these two and use to calculate inductance value. Details are given below:

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operating frequency versus peak input voltage

$$f\left(\frac{\pi}{2}, \text{a\_max}\right) = 1.922 \times 10^{-2}$$
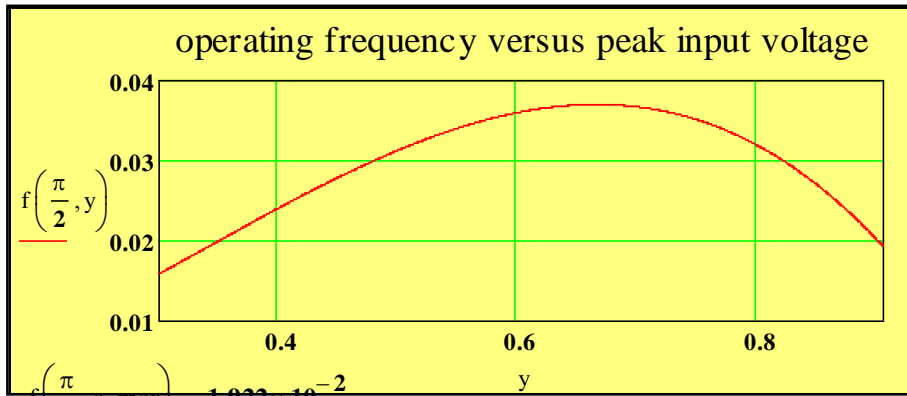
Frequency multiplier at max input voltage.

$$f\left(\frac{\pi}{2}, \text{a\_min}\right) = 1.593 \times 10^{-2}$$

Frequency multiplier at max input voltage

One needs to select condiotion at overall minimum frequency, so:

boost inductor value is:

$$\text{Lin} := \frac{\text{Ro}}{\text{fswmin}} \cdot \min\left(f\left(\frac{\pi}{2}, \text{a\_min}\right), f\left(\frac{\pi}{2}, \text{a\_max}\right)\right)$$

$$\text{Lin} = 6.743 \times 10^{-4}$$

Design criteria comment:

Calculated L_P was to obtain operating frequencies higher than 25 kHz at peak input voltage (min or max) and twice of nominal output power (to cover start up and load transients).

Let's calculate other inductor parameters like peak current and RMS current. Peak current is responsible for inductor saturation and RMS current together with inductor resistance produces heat. These three parameters (Lin, IPKin and IRMSin) determine inductor and a vendor can design and provide inductor based on them.

Peak Input current

$$IPKin := 4 \cdot \frac{Pin}{\sqrt{2} \cdot VminVo}$$

$$IPKin = 5.253$$

RMS Input current

$$IRMSin := \frac{IPKin}{\sqrt{3} \cdot \sqrt{2}}$$

$$IRMSin = 2.145$$

4.4 MOSFET

In order to select the the optimum MOSFET, one must understand the MOSFET requirements in a CrCM boost converter. High voltage MOSFETS have several families based on different technologies, which each target a specific application, topology or operation. For a boost converter, the following are some major MOSFET selection considerations:

- Low FOMs - $R_{on}*Q_g$ and $R_{on}*Q_{oss}$

- Fast Turn-on/off switching, gate plateau near middle of gate drive range

- Low Output capacitance C_{oss} for low switching energy, to increase light load efficiency.

- Switching and conduction losses must be balanced for minimum total loss- this is typically optimized at the low line condition, where worse case losses and temperature rise occur.

- VDS rating to handle spikes/overshoots

- Low thermal resistance $R_{thJC.}$

- Package selection must consider the resulting total thermal resistance from junction to ambient.

- Body diode speed and reverse recovery charge are not important, since body diode never conducts in a boost converter.
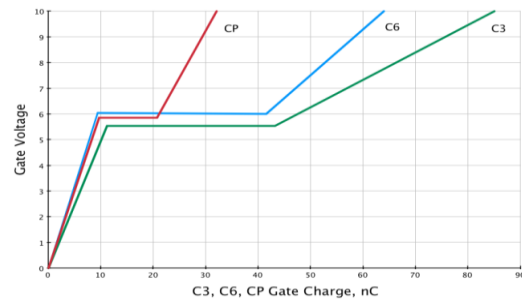

Fig 4.1 Gate voltage versus charge

The recommended CoolMOS MOSFET series for boost applications are the CP series and the C6/E6 series.

CP CoolMOS provides fastest switching (**Error! Reference source not found.**), hence, best performance, but requires careful design in terms of gate driving circuit and PCB layout. While C6/E6 series provides cost advantage, easier design, but less performance compare to CP series.

MOSFET **IPW60R199CP** is selected, and its parameters will be used for the following calculations.

The MOSFET rms current across the 60Hz line cycle can be calculated by the following equation, and consequently the MOSFET conduction loss is obtained.

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MOSFET RMS current:

$$RMSsw := \sqrt{\frac{1}{6} - \frac{4 \cdot a\_min}{9 \cdot \pi}}$$

$RMSsw = \mathbf{0.352}$

$IRMSsw := IPKin \cdot RMSsw$

IRMSsw = **1.849**

$P_{cond} = 0.68W$

MOSFET conduction losses are:

$$P_{cond} = IRMSsw^2 \cdot R_{on(100°C)}$$

The switching losses ,due to current – voltage cross,   occur only at turn-off because of the Critical Conduction Mode operation.

$$P_{cross} = V_0 * IPKav * t_{fall} * f_{pav}$$

Average input peak current is:

$$IPKav = IPKin * \frac{2}{\pi} = 3.34\ A$$

Where t_{fall} is crossover time at turn off. Estimate value is around $t_{fall} = 10nS$.

Average switching frequency needs to be calculated at minimum input voltage as well.

Let's first calculate MOSFET on time.

MOSFET on time at minimum input voltage:

$$Ton := \frac{IPKin \cdot Lin}{a\_minVo}$$

$Ton = \mathbf{2.791 \times 10^{-5}}$

as function of input voltage
angle is given on Fig 4.2:

$$fsw(x) := \frac{1}{Ton} \cdot (1 - a\_min\sin(x))$$

Switching   frequency $\underline{fsw(x)}$
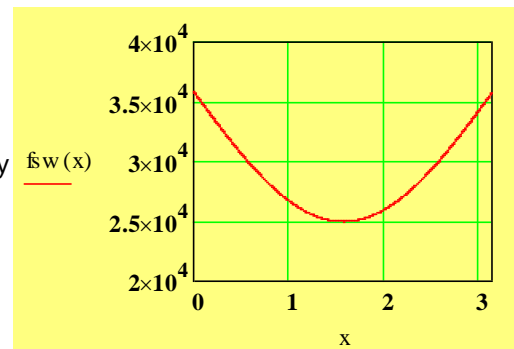

Fig 4.2 Switching frequency as function of angle

The average switching frequency is:

$$fswav := \frac{1}{\pi} \cdot \int_0^\pi fsw(x)\, dx$$

$fswav = \mathbf{2.893 \times 10^4}$

Now, one can calculate switching losses as:

$$P_{cross} = 420 * 3.34 * 10nS * 29kHz$$

$$P_{cross} = 0.4W$$

Turn-on the losses are due to the discharge of the total drain-source capacitance inside the MOSFET.

$$P_{cap} = E_{oss} * f_{swav}$$

Where $Eoss$ is energy contained in the MOSFET output capacitance.

$P_{cap} = 6uJ * 40kHz = 0.24\,W$

This is the worst case scenario, if MOSFET turns on at max voltage. Because MOSFET operates in QR mode

This value is much smaller, an estimate says that is usually half of this value. So,

$P_{cap} = 0.12W$

<u>MOSFET total losses are:</u>

$P_{tot} = P_{cond} + P_{cros} + P_{cap}$

$P_{tot} = 1.2W$

4.5 Boost Diode

The boost freewheeling diode will be a fast recovery one. The value of its DC and RMS current, useful for losses computation, are respectively:

Diode RMS current:

$$RMSd := \frac{1}{3} \cdot \sqrt{\frac{4 \cdot a}{\pi}}$$

$RMSd = \mathbf{0.207}$

$IRMSd := IPKin \cdot RMSc$

$IRMSd = \mathbf{1.086}$

The conduction losses can be estimated as follows:

$P_{Don} = V_{to} * I_{Do} + R_d * I^2_{Drms}$

Where V_{to} (threshold voltage) and Rd (differential resistance) are parameters of the diode.

The breakdown voltage is fixed with the same criteria as the MOSFET.

4.6 Output Capacitor:

The output bulk capacitor (Co) selection depends on the DC output voltage, the output power and the desired voltage ripple.The 100 to 120Hz (twice the mains frequency) voltage ripple is a function of the capacitor impedance and the peak capacitor current :

Output capacitor value based on ripple:

$$Cor := \frac{Po}{4 \cdot \pi \cdot fl \cdot Vo \cdot \Delta Vo}$$

$Cor = \mathbf{2.707 \times 10^{-5}}$ ΔVo is usually selected in the range of less than 5% of the output voltage.

Although ESR usually does not affect the output ripple, it has to be taken into account for power losses calculation. The total RMS capacitor ripple current, including mains frequency and switching frequency components, is:

Output capacitor RMS current:

$$IRMSc := \sqrt{IRMSd^2 - \left(\frac{Po}{Vo}\right)^2}$$

$IRMSc = \mathbf{1.026}$

If the application has to guarantee a specified hold-up time, the selection criterion of the capacitance will change: Co has to deliver the output power for a certain time (tHold) with a specified maximum dropout voltage:

Output capacitor based on hold up time:

$$Coh := \frac{2 \cdot Po \cdot thold}{Vo^2 - Vomin^2}$$

$Coh = \mathbf{2.268 \times 10^{-5}}$ where Vomin is the minimum output voltage value (which takes load regulation and output ripple into (account) and Vopmin is the minimum output operating voltage before the 'power fail' detection from the downstream system supplied by the PFC.

Final selection is larger out of these two:

$$Co := \max(Cor, Coh)$$

$Co = \mathbf{2.707 \times 10^{-5}}$

4.7 Heatsink

The MOSFET and diode can have separate heatsinks or share the same one, however, the selection of the heatsink is based on its required thermal resistivity.

In case of separate heatsinks for the diode and MOSFET, thermal resistors are modeled as in Figure 4.1.

$$R_{thSA.FET} = \frac{T_{J.FET} - T_A}{P_{FET}} - R_{thCS.FET} - R_{thJC.FET}$$

$$R_{thSA.diode} = \frac{T_{J.FET} - T_A}{P_{diode}} - R_{thCS.diode} - R_{thJC.diode}$$
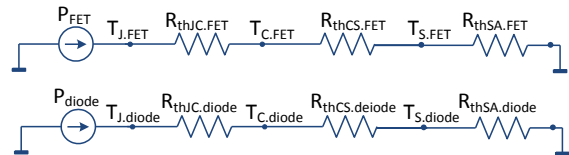

Figure 4.1

In case of a single heatsink for both the diode and the MOSFET, thermal resistors are modeled as in Figure 4.2.

The maximum heatsink temperature T_S is the minimum outcome of the two equations below

$$T_S = T_{J.diode} - P_{diode} \cdot (R_{thCS.diode} + R_{thJC.diode})$$

$$T_S = T_{J.FET} - P_{FET} \cdot (R_{thCS.FET} + R_{thJC.FET})$$

Once T_S is specified, then the heatsink thermal resistance can be calculated.
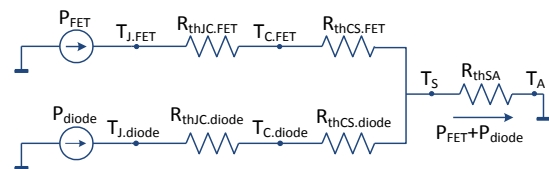
$$R_{thSA} = \frac{T_S - T_A}{P_{FET} + P_{diode}}$$

Figure 4.2

R_{thJC} is the thermal resistance from junction to case, this is specified in the MOSFET and Diode datasheets.

R_{thCS} is the thermal resistace from case to heatsink, typically low compared to the overall thermal resistance, its value depends on the the interface material, for example, thermal grease and thermal pad.

R_{thSA} is the thermal resistance from heatsink to ambient, this is specified in the heatsink datasheets, it depends on the heatsink size and design, and is a function of the surroundings, for example, a heatsink could have difference values for R_{thSA} for different airflow conditions.

T_S is the heatsink temperature, T_C is the case temperature , T_A is the ambient temperature.

P_{FET} is FET's total power loss , P_{diode} is diode's total power loss.

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5 References

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[5] Infineon Technologies Application Note: "CCM Boost converter design" by Abdel-Rahman Sam, Infineon Technologies; January 2013

[6] "PFC topologies and control fundamentals" by Jon Hancock and Mladen Ivankovic, Infineon technologies Detroit PFC training; September 2011.

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Symbols used in formulas

V_{inmin}: Minimum input voltage
V_o: Output voltage
V_{inmax}: Maxmum input voltage
V_o: Output voltage
P_o: Output power
fsw: Switching frequency
Tsw: Switching time period
f_{line}: line frequency

Lin: Input Inductor
IAV_{in}: Inductor average current across the line cycle
IPK_{in}: Inductor peak current

$V_{f.bridge}$: Bridge diode forward voltage drop
P_{bridge}: Bridge power loss

$R_{on(100C)}$: MOSFET on resistance at 100^oC
Q_{gs}: MOSFET gate-source charge
Q_{gd}: MOSFET gate-drain charge
Q_g: MOSFET total gate charge
R_g: MOSFET gate resistance
V_{pl}: MOSFET gate plateau voltage
V_{th}: MOSFET gate threshold voltage
t_{on}: MOSFET switching on time
t_{off}: MOSFET switching off time
E_{oss}: MOSFET output capacitance switching energy
IRMSsw: MOSFET rms current across the line cycle
P_{cond}: MOSFET conduction loss
P_{cross}: MOSFET switching off power loss
P_{cap}: MOSFET output capacitance switching loss

I_{Do}: Boost diode average current
I_{RMSd}: Boost diode average current
V_{to}: Boost diode threshold forward voltage drop
P_{Don}: Boost diode conduction loss

C_o: Output capacitor
ESR: Output capacitor resistance
t_{hold}: Hold-up time
V_{omin}: Hold up minimum output voltage
ΔV_o: Output voltage ripple
$IRMS_C$: Output capacitor rms current