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CrCM Flyback PFC Converter Design

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Subjects: CrCM Flyback PFC Converter Design

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1 Introduction

Power Factor Correction (PFC) shapes the input current of the power supply to be in synchronization with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage as would an equivalent resistor, with no added input current harmonics. This document is intended to discuss the topology and operational mode for low power (<100W) PFC applications, and provide detailed design equations with examples.

2 Flyback topology

Active PFC can be achieved by any basic topology, the boost converter is the most popular topology used in PFC applications. In an application such as LED lighting, where a different output voltage is required from the typical 390-400V bulk bus, the major drawback of boost converter comes to light. Boost converter has voltage gain with the output greater than the input, so the output voltage is always higher than maximum input voltage. Also, there is no galvanic isolation between primary and secondary, an undesirable situation for some applications like LED lighting, with their secondary side heatsinks often exposed to touch. Keeping in mind these two requirements, the flyback (Figure 2.1) emerges as the best solution for this application. The flyback converter can be understood as operating like a boost with split windings. The primary side winding is used for charging energy into the core, and secondary side is used to discharge/transfer it to the output. During the MOSFET ON time, current in the primary winding "charges" the magnetic flux density, as the current ramps up at a rate controlled by the primary inductance. When MOSFET turns OFF current flow moves from primary to the secondary side, and discharges energy stored in the core to the output (magnetic flux density drops to zero, in the case of DCM or CrCM mode operation.)

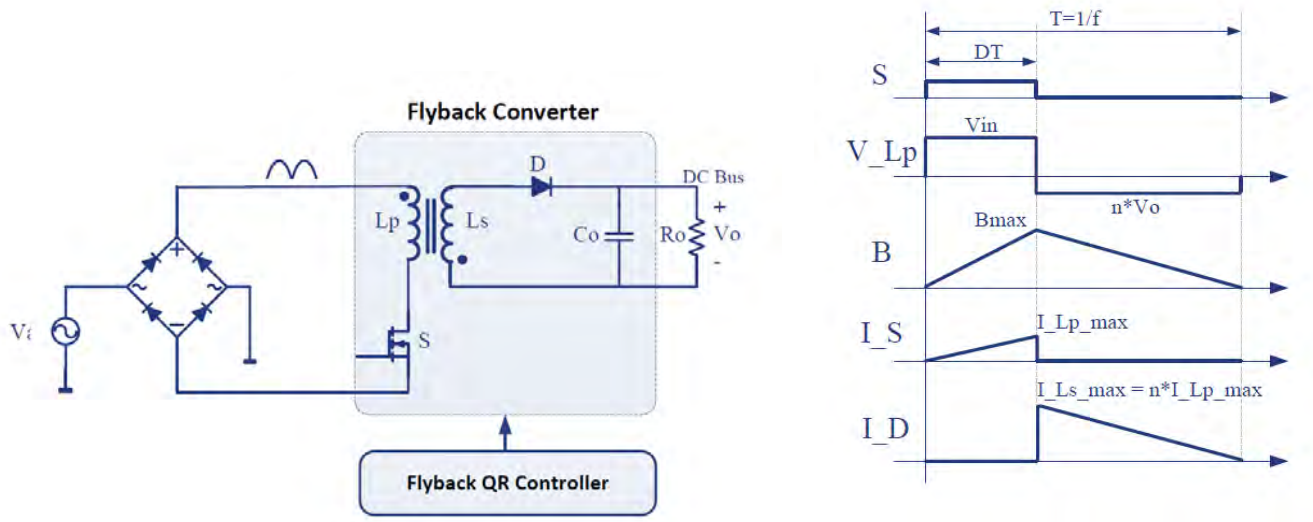


Figure 2.1

3 Flyback Equations

The flyback converter can operate in three modes; continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CrCM). The modes are defined based on transformer current. Critical Conduction Mode is the most popular one for PFC application.

The primary current has sinewave envelope of triangular-shaped units and flows during the switch ON-time, as illustrated by the shaded triangles shown in figure 2.2 below. When MOSFET turns off, the voltage reverses on the primary and secondary, and conducts current through the Flyback rectifier diode D on the secondary side until it dropes to zero (energy completely discharged to zero). At the end of the core reset period, both windings are "open" and this starts an oscillation between transformer magnetizing inductance and parasitic capacitance present at this node (MOSFET, transformer and diode). When the voltage across MOSFET reaches the minimum, (achieving partial ZVS turn-on), the MOSFET is turned on and new switching cycle begins.

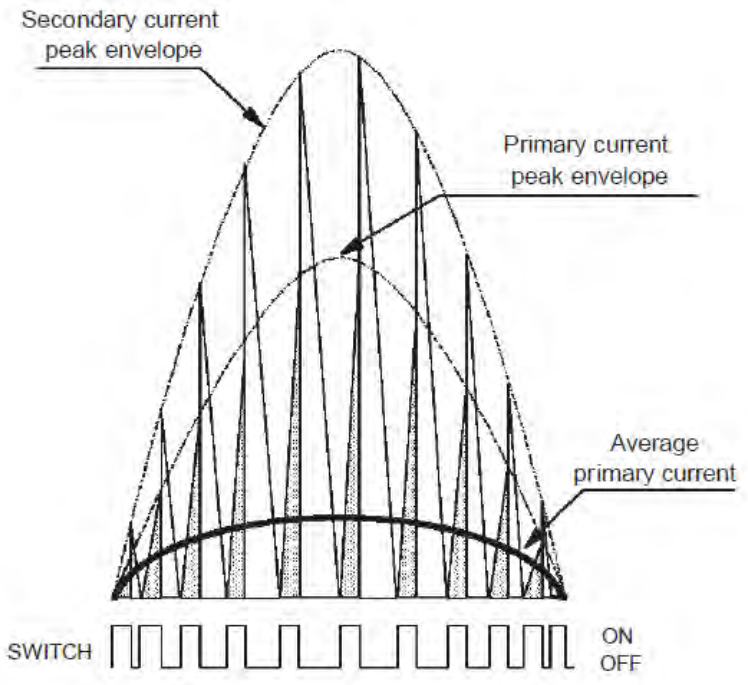


Fig 2.2 PFC Flyback Input current

3.1 Timing equations:

The primary current Ip(t) is triangular-shaped and flows only during the switch ON-time, as illustrated by the shaded triangles shown in above. During each half-cycle the height of these triangles varies with the instantaneous line voltage:

$$V_{in}(\theta) = V_{PK} * |\sin(2 * \pi * fl * t)| \quad (1)$$

$$I_{pkp}(\theta) = I_{PKp} * |\sin(2 * \pi * fl * t)| \quad (2)$$

their width is constant T_{on}:

$$T_{on} = \frac{L_p * I_{pkp}(\theta)}{V_{in}(\theta)} = \frac{L_p * I_{PKp}}{V_{PK}} \quad (3)$$

but they are spaced out by a variable amount T_{off}:

$$T_{off} = \frac{L_p * I_{PKp} * |\sin(\theta)|}{n * (V_{out} + V_f)} \quad (4)$$

L_p - Flyback transformer primary side inductance

n - Flyback transformer transfer ratio

V_f - voltage drop on secondary side rectifier

The converter operates in CrCM, so the switching period is the sum of T_{on} and T_{off}:

$$T_{on} + T_{off} = \frac{L_p * I_{PKp}}{V_{PK}} * [1 + \frac{V_{PK}}{V_R} * |\sin(\theta)|] \quad (5)$$

where Vr = n*(Vo +Vf) is the reflected voltage.

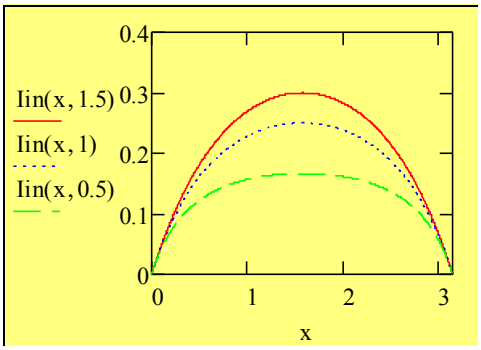
The ratio between the reflected voltage and the input peak voltage is **b = V_r/V_{PKmin}**.

3.2 Power transfer:

Looking at the primary on a "f_l- line frequency" time scale, the current Iin(θ) downstream of the bridge rectifier is the average value of each triangle over a switching cycle (the thick black curve of fig. 3):

$$I_{in}(\theta) = = \frac{1}{2} * I_{pkp} * D = \frac{1}{2} I_{PKp} * \frac{|\sin(\theta)|}{1 + |\sin(\theta)|/b} \quad (6)$$

$$Iin(x, b) := \frac{1}{2} \cdot \frac{\sin(x)}{1 + \frac{\sin(x)}{b}}$$



Note that the reflected voltage ratio b affects envelope of the input current, as seen for values of b from 0.5 to 1.5. A larger b means that the current envelope is closer to the sinewave, i.e better power factor.

Input power Pin is average product of input voltage and input current:

$$P_{in} = P_o/\eta \quad (7)$$

$$P_{in} = \frac{1}{\pi} * \int_0^{\pi} V_{in}(\theta) * I_{in}(\theta) * d\theta = \frac{1}{2} * V_{PK} * I_{PK} * \frac{1}{\pi} * \int_0^{\pi} \frac{\sin^2(\theta)}{1 + \sin(\theta)/b} d\theta \quad (8)$$

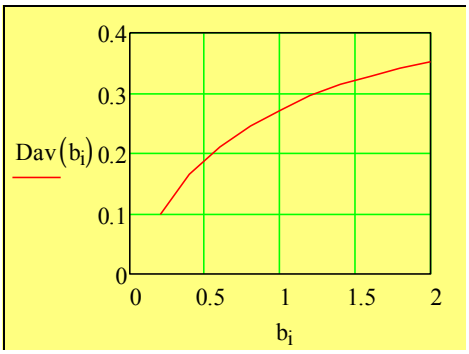
$$P_{in} = \frac{1}{2} * V_{PK} * I_{PK} * Dav(b) \quad (9)$$

Let's introduce function **Dav(b)** – the average power integral as a function of the reflected voltage ratio **b** as:

$$Dav(b) = \frac{1}{\pi} * \int_0^{\pi} \frac{\sin^2(\theta)}{1+\sin(\theta)/b} d\theta \quad (10)$$

b_i =	$Dav(b_i)$ =
0.2	0.099
0.4	0.164
0.6	0.211
0.8	0.246
1	0.273
1.2	0.295
1.4	0.313
1.6	0.329
1.8	0.341
2	0.352

$Dav(b_i)$ - Average duty cycle related to input power:



Reflected voltage ratio **b** is the designers choice. Higher **b** results in higher peak voltage on the main switch (MOSFET) with lower Input RMS current. MOSFET resources should be used wisely, so select a reflected voltage that basic voltage criteria for MOSFET is satisfied with good margin:

$V_{ds} \geq V_{PK} + V_r + V_{sp} + V_m$

Vds is the MOSFET drain to source breakdown voltage; V_r is the transformer reflected voltage; V_{sp} is the spike voltage caused by transformer leakage inductance; V_m is the desired voltage margin.

In order to design the converter and properly dimension the components, we need to calculate the key parameters. This is the list of parameters together with the main reasons why they are needed:

Parameter	**Reason:**
Transformer inductance	Transfer power at given minimum frequency
Input peak current	Transformer saturation point should be above this value
Input average current	Rectifier bridge losses
Input RMS current	MOSFET conduction losses
Output average current	Diode conduction losses
Output capacitor RMS current	Output capacitor losses
The second harmonic of output current	Output capacitor low frequency ripple voltage

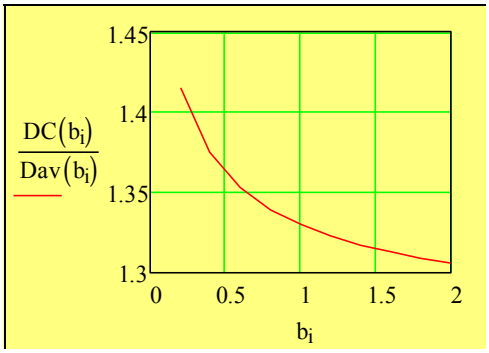
4 Component selection

4.1 Input rectifier bridge:

The average input current can be calculated from:

b_i =	$\frac{DC(b_i)}{Dav(b_i)}$ =
0.2	1.415
0.4	1.375
0.6	1.353
0.8	1.339
1	1.33
1.2	1.323
1.4	1.317
1.6	1.313
1.8	1.309
2	1.306

DC input current: $I_{DCp} = \frac{Pin}{V_{PK}} \cdot \frac{DC(b)}{Dav(b)}$



$$A_{ic} = DC(b)/Dav(b)$$

Note that larger reflected voltage results in lower average input current. This will lower conduction losses on input rectifier bridge. The losses on input rectifier bridge are given as:

$$P_{bridge} = 2 * Vf * I_{DCp} \quad (11)$$

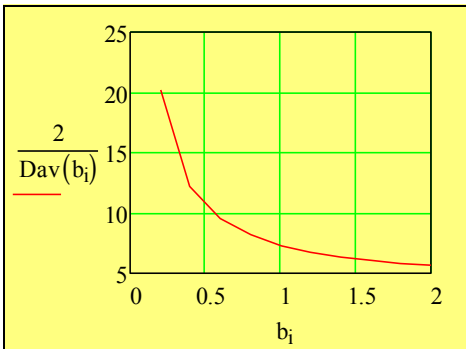
There is 2 multiplied in the formula, because two diode in the rectifier bridge are conducting simultaneously in series.

4.2 Transformer:

The peak input current depends on the reflected voltage ratio b.

b_i =	$\frac{2}{Dav(b_i)}$ =
0.2	20.153
0.4	12.173
0.6	9.487
0.8	8.135
1	7.32
1.2	6.774
1.4	6.382
1.6	6.088
1.8	5.859
2	5.675

Peak primary current: $I_{PKp} = \frac{Pin}{V_{PK}} \cdot \frac{2}{Dav(b_i)}$



When b is selected, we can calculate Input peak current as

$$I_{PKp}(b) = \frac{2*P_{in}}{V_{Pk}*Dav(b)} \quad (12)$$

The minimum frequency occurs when converter operates at V_{PKmin} value of minimum input voltage. That frequency needs to be selected above $f_{swmin} \geq 20kHz$ to prevent audio noise. The transformer primary side inductance can be calculated by:

$$Lp = \frac{V_{PKmin}}{f_{swmin}*I_{PKp}(b)} * \frac{1}{1+1/b} \quad (13)$$

The transformer transfer ratio n can be calculated from:

$$n = \frac{b*V_{PKmin}}{V_o+V_f} \quad (14)$$

Now the transformer parameters are complete:

Input power Pi; Primary inductance Lp; Primary peak current I_{PKp}; and turns ratio n.

Also, the type of isolation and space restriction are important parameters for core selection.

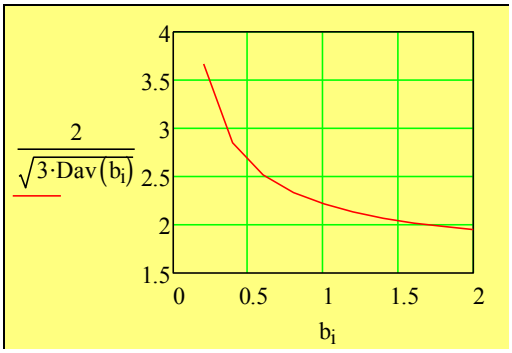
The best approach may be to calculate key parameters and contact transformer manufacturer for a design meeting all safety and isolation parameters.

4.3 MOSFET:

MOSFET rms current determines MOSFET conduction losses.

b_i =	$\frac{2}{\sqrt{3 \cdot Dav(b_i)}}$
0.2	3.665
0.4	2.849
0.6	2.515
0.8	2.329
1	2.209
1.2	2.125
1.4	2.063
1.6	2.015
1.8	1.976
2	1.945

RMS primary current: $I_{RMSp} = \frac{Pin}{V_{PK}} \cdot \frac{2}{\sqrt{3 \cdot Dav(b_i)}}$



$$RMS_{pc} = 2/\sqrt{3 * Dav(b)}$$

The graph shows the key performance trade-off. By selecting larger b, rms current for given power becomes smaller and lowers not only MOSFET losses but also lowers conduction losses in the input EMI filter (resistance of EMI choke). The trade-off involves VDS rating, which for wide range input may become rather high. For applications with standard household or office lines voltage, a larger b is practical with medium voltage CoolMOS™.

4.4 Output Diode:

Conduction losses dominate the performance consideration for the output diode as well. Because of mode of operation, the diode current at the end of each cycle is zero, and there are no diode recovery losses.

Average Diode current is:

$$I_o = \frac{P_o}{V_o} \quad (15)$$

Peak Diode current is:

$$I_{PKs} = n * I_{PKp} \quad (16)$$

The input current peak is multiplied by transformer the ratio n. The output diode conduction losses can be calculated as:

$$P_{Dcl} = V_f * I_o \quad (17)$$

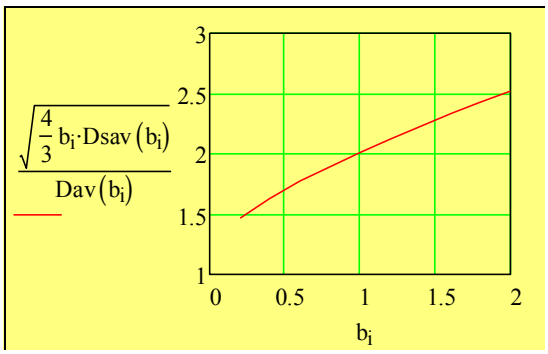
4.5 Output capacitor:

The output capacitor's primary function is to filter the output voltage, but we need to keep in mind that the capacitor ESR together with RMS current produce power dissipation in the capacitor. When one selects a capactior for the LED driver, a

primary criteria is that the capacitor rated RMS current is larger than capacitor current in the converter. The larger this difference is, the longer the capacitor life. The preferred capacitor type for this application is a low ESR capacitor designed for high ripple current.
In the next calculation for the RMS secondary current, we see where the advantages on the primary side brought by a higher "b" have a secondary side cost in higher RMS current.

RMS secondary current: $I_{RMSs}(b) = \left(\frac{Pin}{Vo + Vf}\right) * \frac{\sqrt{\frac{4}{3} b_i \cdot Dsav(b_i)}}{Dav(b_i)}$

b_i =	$\frac{\sqrt{\frac{4}{3} b_i \cdot Dsav(b_i)}}{Dav(b_i)}$
0.2	1.473
0.4	1.629
0.6	1.767
0.8	1.894
1	2.012
1.2	2.123
1.4	2.229
1.6	2.329
1.8	2.425
2	2.517



$$RMS_{sc} = \frac{\sqrt{\frac{4}{3} * b * Dsav(b)}}{Dav(b)}$$

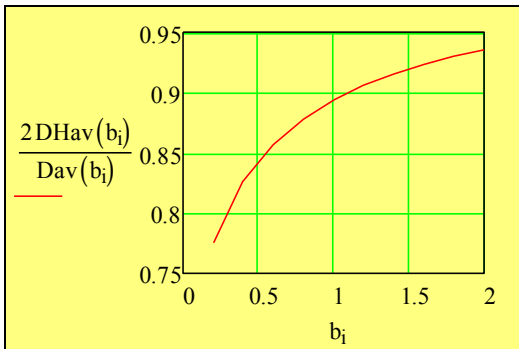
Capacitor RMS current can be calculated from:

$$I_{RMSc} = \sqrt{I_{RMSs}{}^2 - I_o{}^2} \qquad (18)$$

LED drivers use a control loop closed on the primary side, so the capacitor voltage ripple is not important to the loop behavior. However, if the application requires an output voltage control loop, output voltage double line frequency ripple becomes important, so one need to select a capacitor to filter 2x line frequency components to a low value, as the necessary low loop crossover for PFC means there will be no reduction of the ripple voltage by the feedback loop. When the capacitor is selected it needs to checked for RMS current criteria. It must fulfill both criterias: one for voltage ripple and the second for RMS current.
The low frequency component of the ripple is related to the twice line frequency envelope, and depends on the capcitance value. The ESR contribution can be neglected for this calculation. To calculate the amplitude we will use Fourier analysis. The *peak amplitude of the second harmonic* is:

b_i =	$2\frac{DHav(b_i)}{Dav(b_i)}$
0.2	0.775
0.4	0.825
0.6	0.856
0.8	0.878
1	0.893
1.2	0.906
1.4	0.915
1.6	0.923
1.8	0.929
2	0.935

Second harmonic amplitude $I_{o2} = Io \cdot 2\frac{DHav(b_i)}{Dav(b_i)}$



$$OC_{sh} = 2 * \frac{DHav(b)}{Dav(b)}$$

So the capacitor value can be calculated based on the requirement for output ripple ΔV_o, as:

$$Co = \frac{I_o * OC_{sh}}{\pi * \Delta V_o * f_l} \quad (19)$$

4.6 Heatsink

The MOSFET and diode can have separate heatsinks or share the same one; however, the selection of the heatsink is based on its required thermal resistance to ambient under worst case conditions.

In case of separate heatsinks for the diode and MOSFET, thermal resistors are modeled as in Figure 4.1.

$$R_{thSA.FET} = \frac{T_{J.FET} - T_A}{P_{FET}} - R_{thCS.FET} - R_{thJC.FET}$$

$$R_{thSA.diode} = \frac{T_{J.FET} - T_A}{P_{diode}} - R_{thCS.diode} - R_{thJC.diode}$$

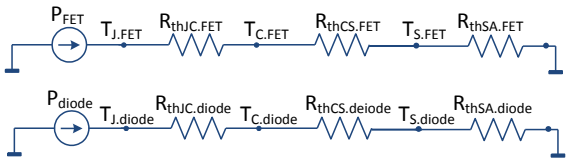


Figure 4.1

In the case of a single heatsink for both the diode and the MOSFET, thermal resistors are modeled as in Figure 4.2.

The maximum heatsink temperature T_S is the minimum outcome of the two equations below:

$$T_S = T_{J.diode} - P_{diode} \cdot (R_{thCS.diode} + R_{thJC.diode})$$

$$T_S = T_{J.FET} - P_{FET} \cdot (R_{thCS.FET} + R_{thJC.FET})$$

Once T_S is specified, then the heatsink thermal resistance can be calculated.

$$R_{thSA} = \frac{T_S - T_A}{P_{FET} + P_{diode}}$$

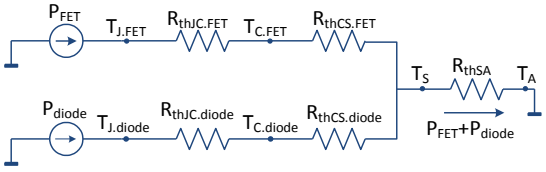


Figure 4.2

R_{thJC} is the thermal resistance from junction to case, which is specified in the MOSFET and Diode datasheets.

R_{thCS} is the thermal resistace from case to heatsink, which is typically low compared to the overall thermal resistance; its value depends on the the interface material, for example, thermal grease and thermal pad.

R_{thSA} is the thermal resistance from heatsink to ambient, this is specified in the heatsink datasheets; this depends on the heatsink size and design, and is a function of the surroundings. For example, a heatsink could have different values for R_{thSA} for different airflow conditions. Worst case performance is usually used.

T_S is the heatsink temperature, T_C is the case temperature , T_A is the ambient temperature.

P_{FET} is FET's total power loss , P_{diode} is diode's total power loss.

5 CrCM Flyback example

The basic design equations for the CrCM operated Flyback are given below. This design example is included to further clarify the usage of all equations. The flyback converter encounters the maximum current stress and power losses at the minimum line voltage condition (V_{PKmin}), hence, all design equations and power losses will be calculated using the low line voltage condition.

Design Specifications:

Input voltage V_{in}	85-270 Vac 60 Hz
Output voltage V_o	50 V
Output power P_o	50 W
Epected efficiency n	0.85
Output voltage ripple $\Delta V_o = 0.05 * V_o$	2.5V
Hold-up time	It is not required by LED drivers.

Preliminary choices

Minimum frequency f_{swmin}	25 kHz
Reflected voltage ratio **b**	1
Spike voltage caused by leakage inductance V_{sp}	80V

Preliminary calculations:

Minimum Input Peak Voltage	V_{Pkmin}=85*V2=	120V
Maximum Input Peak Voltage (V)	V_{PKmax} = 265*V2	374
Input Power	P_{in}= 50/0.85	59
Output Current Io	Io=50/50	1

Output voltage ripple ΔV_o	$0.05*V_o$	2.5

Characteristic functions:

Average duty cycle function	$Dav(b)$	0.273
Input average current function A_{ic}	$A_{ic} = DC(b)/Dav(b)$	1.33
Primary RMS current function RMS_{pc}	$RMS_{pc} = 2/\sqrt{3 * Dav(b)}$	2.2
Secondary RMS current function RMS_{sc}	$RMS_{sc} = \sqrt{\frac{4}{3} * Dsav(b)/Dav(b)}$	2.012
Output current second harmonic function	$OC_{sh} = 2 * DHav(b)/Dav(b)$	0.893

Operating Conditions:

Input average current I_{DCp}	$\frac{P_{in}}{V_{PKmin}} * A_{ic}$	0.65
Peak Primary Current I_{PKp}	$\frac{P_{in}}{V_{PKmin}} * \frac{2}{Dav(b)}$	3.60
RMS Primary Current I_{RMSp}	$\frac{P_{in}}{V_{PKmin}} * RMS_{pc}$	1.08
RMS secondary Current I_{RMSs}	$\frac{P_o}{V_o} * RMS_{sc}$	2.01
Capacitor RMS current I_{RMSc}	$\sqrt{I^2_{RMSs} - I^2_o}$	1.73

Transformer design

Primary Inductance L_p	$\frac{V_{PKmin}}{f_{swmin} * I_{PKp}(b)} * \frac{1}{1 + 1/b}$	879uH
Primary to secondary turns ratio n	$V_r/(V_o + V_f)$	2.35
Primary side peak current = I_{PKp}		2.73

Transformer core selection:

Transformer key parameters: Input power Pi; Primary inductance Lp; Primary peak current I_{PKp}; turns ratio n; Type of isolation and space restriction are important parameters for core selection.

The best approach is to calculate key parameters and contact transformer manufacturer.

Core size	Le (cm)	Ae (cm²)	**Wattage range**	Bobbin type	Insulation	Notes
EE13/7/4 (EF12.6)	2.96	0.124	**1-10**	Horizontal 8 pin	Functional US, Functional Europe	Smallest, lowest cost only 4 pins on one side so should not split PRI. 10W is a stretch
EE13/7/4 (EF12.6)	2.96	0.124	**1-10**	Horizontal 9 pin	Reinforced US, Reinforced Europe	5 pin side for PRI and AUX, 4 pin extended rail side for TIW SEC. 10W is a stretch.
EE16/8/5 (EF16)	3.76	0.201	**5-15**	Horizontal 8 pin	Functional US, Functional Europe	Small, low cost only 4 pins on one side so should not split PRI.
EE16/8/5 (EF16)	3.76	0.201	**5-15**	Horizontal 9 pin	Reinforced US, Reinforced Europe	5 pin side for PRI and AUX, 4 pin extended rail side for TIW SEC (Great package for manufacturing).
EE16/7/4	3.55	0.184	**5-12**	Vertical 10 pin	Functional or Reinforced US and Europe	Small PCB area, 4 pin side normally used for SEC. Reinforced insulation consumes copper area so wattage is lower.
EE20/10/6 (EF20)	4.6	0.32	**15-30**	Horizontal 10 pin	Functional or Reinforced US and Europe	Bobbin designed for functional insulation. Need to add 2 x margin tape or margin tape + TIW to meet reinforced insulation. US working voltage is okay but more of a problem with European working voltage. See extended rail version for more efficiency
EE20/10/6 (EF20)	4.6	0.32	**15-30**	Horizontal 14 pin	Reinforced US, Reinforced Europe	Larger PCB area - bobbin has creepage distance built into bobbin rail. Can achieve higher power levels and better efficiency because winding area is copper instead of insulation.
EE25/13/7 (EF25)	5.78	0.514	**20-50**	Horizontal 10 pin	Functional or Reinforced US and Europe	Bobbin designed for functional insulation. Need TIW for US reinforced. Need to add 2 x margin tape or margin tape + TIW to meet European reinforced insulation. See extended rail version for more efficiency.
EE25/13/7 (EF25)	5.78	0.514	**20-50**	Vertical 10 pin	Functional or Reinforced US and Europe	Small PCB area. Bobbin designed for functional insulation. Need TIW for US reinforced. Need to add 2 x margin tape or margin tape + TIW to meet European reinforced insulation. See extended rail version for more efficiency.

Input bridge rectifier:

The voltage rating is determined based on the maximum input voltage:

Vbr ≥ V_{PKmax} = 374 V, at least to have 400V rectifier diode.

A good choice is a 600V rectifier to cover spikes from the grid; the cost impact for higher VBR rating is small.

I_{DCp} = 0.65 .

1A rectifier bridge is a good choice.

Estimated losses on rectifier bridge:

$$P_{bridge} = 2 * Vf * I_{DCp}$$

$$P_{bridge} = 2 * 1 * 0.65 = 1.3W$$

MOSFET

Voltage class:

MOSFET is exposed to:

V_{ds} = V_{PKmax}+V_r+V_{sp} = 374 +120 +80 = 574V

So, a 650V MOSFET is good choice.

The MOSFET rms current across the 60Hz line cycle is equal to Primary side RMS current. MOSFET conduction loss could be calculated as:

$$P_{Q.cond} = {I_{RMSp}}^2 \cdot R_{on(100℃)}$$

Because of CrCM conduction losses dominate, so we will estimate conduction losses only.

IPD65R600E6 is good choice for this case, so:

$$P_{Q.cond} = 1.08^2 * 1.1 = 1.28W$$

Rectifier Diode

The rectifier diode will be a fast recovery one.

The maximum voltage that diode is exposed:

V_{Dmax} = (V_{PKmax}+V_{sp})/n + V_o = 243V, so we will need at least 300V diode.

The value of its DC and RMS current, useful for losses computation, are respectively:

$I_{Do} = Io$ = 1 A

$I_{Drms} = I_{RMSs}$= 2.01A

The conduction losses can be estimated as follows:

Using DC current and average voltage drop V_f across the diode:

$P_{Don} = I_{Do} * V_f$

Estimate for conduction losses:

$P_{Don} = 1 * 1 = 1W$

Or more accurate formula (when a particular diode is selected):

$P_{Don} = V_{to} * I_{Do} + R_d * I^2{}_{Drms}$

Where V_{to} (threshold voltage) and Rd (differential resistance) are parameters of the diode.

The good choice is 2A ; 300V diode.

This is not socket for Silicon Carbide diode because diode recovery losses are not primary criteria. For the lower voltage range (**≤ 100V**) Schotkey rectifier diodes are a good choice.

Output Capacitor:

The key criteria to select the output capcacitor for the LED driver are:

- Output voltage

  Output voltage is 50V, but we need to take into account variation on LED voltage drop, a good choice is 63V

- Capacitor RMS current

  $I_{RMSc} = \sqrt{I^2{}_{Drms} - I^2{}_{Do}} = \sqrt{2.01^2 - 1^2} = 1.73A$

The best choice is to select low ESR capacitors.

The selection criteria are: Vdc = 63 V and $\boldsymbol{I_{RMSc} \geq 1.73A}$

Output capacitor conduction losses are:

$PCo = I^2{}_{RMSc} * \boldsymbol{ESR}$

If there is requirement for double line frequency ripple, it could be solved from:
Output capacitor value based on the second harmonic voltage ripple:

$$Co = \frac{I_0 * OC_{sh}}{\pi * \Delta V_o * f_l}$$

$$Co = \frac{1 * 0.89}{3.14 * 2.5 * 60} = 1890uF \sim 2000uF$$

One needs to select low ESR capacitor with RMS current larger than $\boldsymbol{I_{RMSc} \geq 1.73A}$.

6 References

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[3] ST Application Note:"AN-1059 Design Equations of high power factor Flyback converters based on TLE6561"

[4] Infineon Technologies Application Note: "CCM Boost converter design" by Abdel-Rahman Sam, Infineon Technologies; January 2013

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Symbols used in formulas

P_{in}: Input power

V_{in}: Input voltage

V_{PK}: Peak input voltage

$V_{PK.min}$: Minimum Peak input voltage

$V_{PK.max}$: Maximum Peak input voltage

I_{pkp}: Peak current at switching cycle

I_{PKp}: Maximum Peak current at line frequency cycle

I_{DCp}: Input average current

I_{RMSp}: RMS Primary side current

I_{RMSs}: RMS Secondary side current

I_{RMSc}: Capacitor RMS current

V_o: Output voltage

P_o: Output power

fsw: Switching frequency

T: Switching time period

f_l: line frequency

$R_{on(100C)}$: MOSFET on resistance at 100°C

$V_{f.bridge}$: Bridge diode forward voltage drop

P_{bridge}: Bridge power loss

P_{Dcl}: output diode conduction loss

Q_{gs}: MOSFET gate-source charge

Q_{gd}: MOSFET gate-drain charge

Q_g: MOSFET total gate charge

R_g: MOSFET gate resistance

V_{pl}: MOSFET gate plateau voltage

V_{th}: MOSFET gate threshold voltage

T_{on}: MOSFET switching on time

T_{off}: MOSFET switching off time

E_{oss}: MOSFET output capacitance switching energy

$P_{Q.cond}$: MOSFET conduction loss

C_o: Output capacitor

ESR: Output capacitor resistance

ΔV_o: Output voltage ripple

I_{RMSc}: Output capacitor rms current

P_{Co}: Output capacitor conduction loss