Hardware User Guide

Zipcores FMC-DSP Mezzanine Card

ZIP-FMC-DSP Rev. C.1
August 2025

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Overview

Introduction

The Zipcores FMC-DSP Mezzanine card is a high-performance digital signal processing platform featuring 2 x ADC (125 MSPS) inputs and 2 x DAC (500 MSPS) outputs. The card conforms to the ANSI/VITA 57.1 FMC™ mezzanine standard, allowing connection to a wide range of base-boards and FMC-compliant systems. Examples include development boards from AMD/Xilinx®, Intel/Altera®, Avnet® and Digilent®.

Designed for use with both IF and baseband signals, the FMC-DSP card is ideal for applications that require high-speed data acquisition and logging, Software Defined Radio (SDR), Digital Signal Processing (DSP) and Digital Signal Synthesis (DSS). In addition, the inclusion of dual, symmetrical and balanced ADC and DAC channels, means that the card is suitable for the processing of complex I/Q signals such as those required in baseband I/Q modulation and de-modulation schemes. Figures (1) and (2) show the general board layout and the distribution of main board components.

Board layout

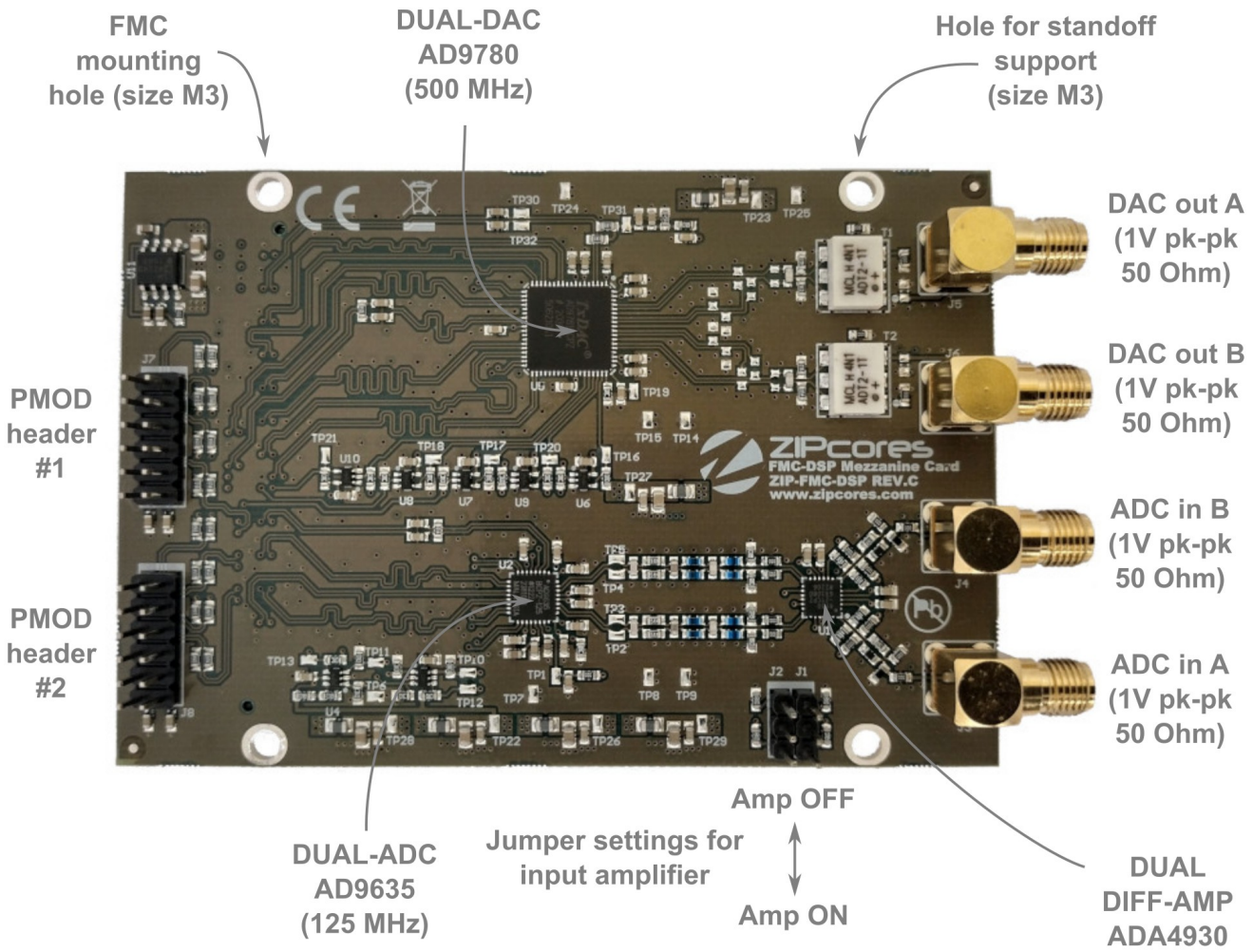

Figure 1: ZIP-FMC-DSP Rev. C board (top view)

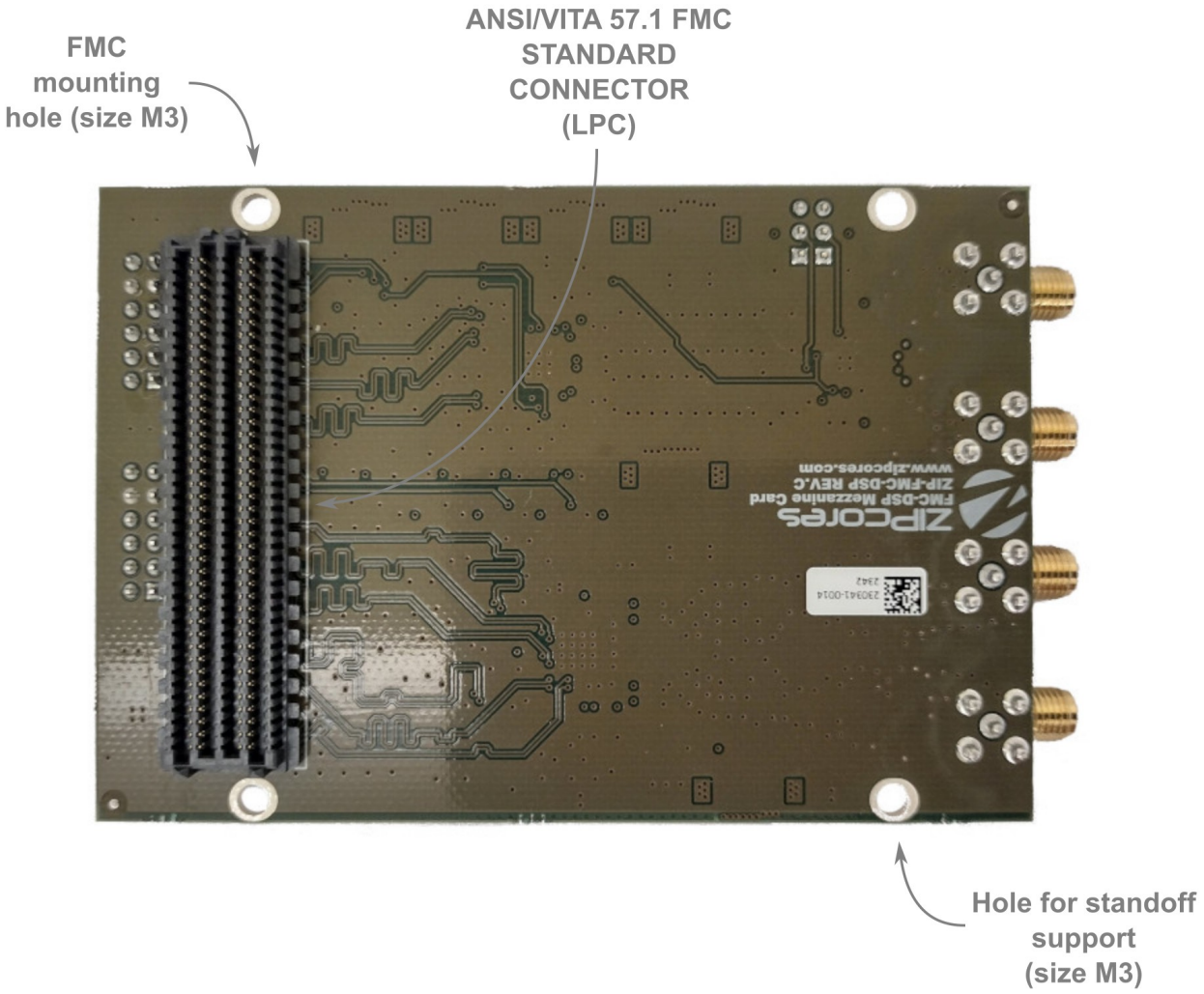

Figure 2: ZIP-FMC-DSP Rev. C board (bottom view)

Key features

- 2 x ADC Analogue inputs (1V pk-pk) 50Ω nominal
- 2 x DAC Analogue outputs (1V pk-pk) 50Ω nominal
- DC-coupled inputs with anti-aliasing filter (~100 MHz B/W)
- Transformer-coupled outputs (~20 kHz to 450 MHz)
- Standard SMA (right-angle) female connectors x 4
- Standard ANSI/VITA 57.1 FMC™ LPC connector
- Also compatible with FMC-HPC or FMC+
- Dual 125 MSPS ADC from Analog Devices® (AD9635)
- Dual 500 MSPS DAC from Analog Devices® (AD9780)
- Dual input amplifier with selectable setting (ADA4930)
- Electrically symmetrical/balanced input and output channels
- Flexible clocking provided via LVDS I/O on FMC connector
- All digital ADC and DAC I/O provided as LVDS on FMC
- Flexible VADJ voltage setting from 1.5V to 2.5V
- Main power drawn from the 3.3V pin on the FMC connector
- Full access to the ADC and DAC registers via SPI bus
- 2 x general-purpose PMOD™ headers for debug and GPIO
- 2 x M3 mounting holes for securing the FMC connector
- 2 x M3 mounting holes for supporting standoff ‘legs’
- Compatible with a wide range of evaluation boards

Block diagram

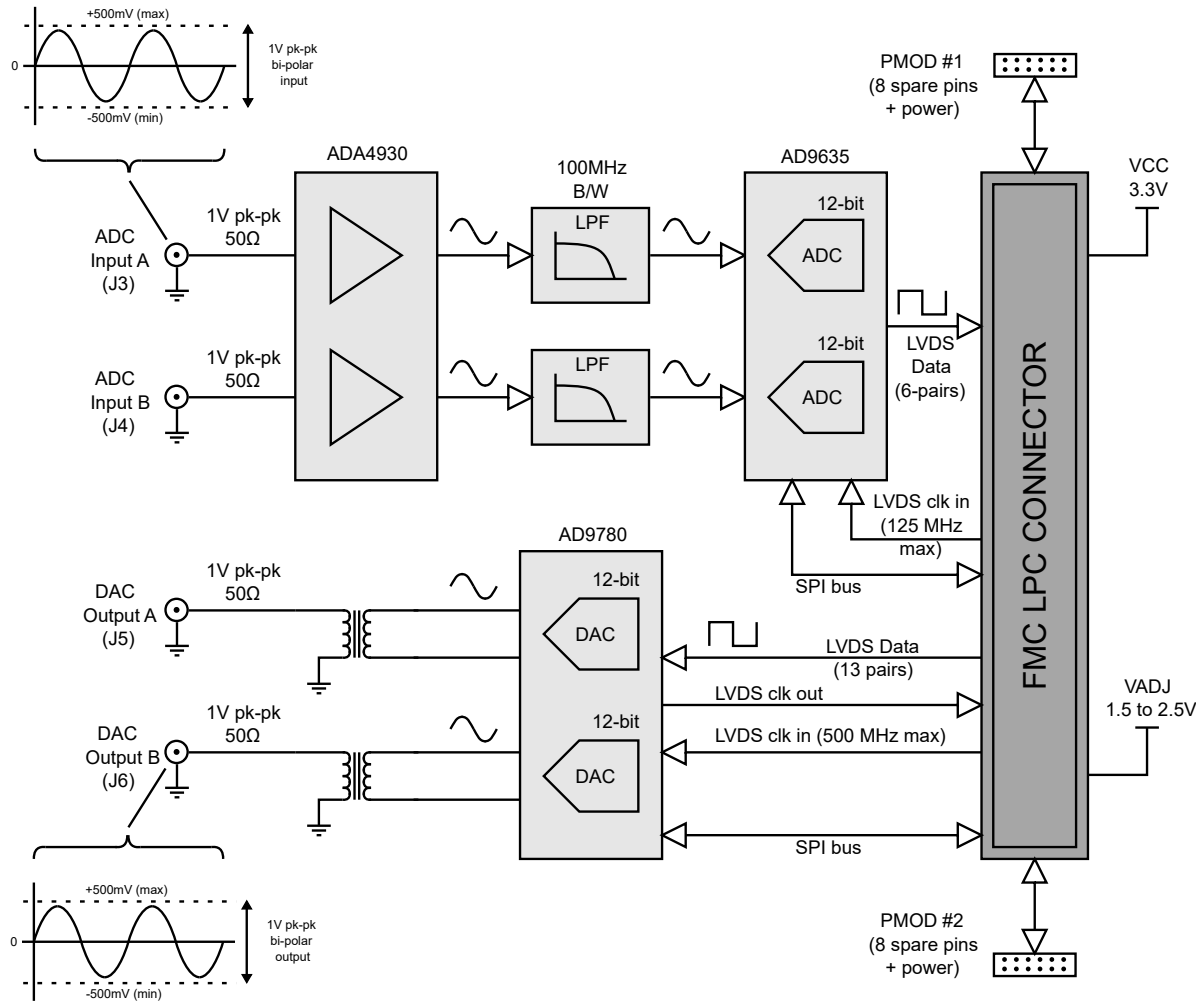

Figure 3: Block diagram of the core functions showing main connectivity with the FMC LPC

Detailed description

Dual input-amplifier stage

Analogue inputs to the mezzanine card are provided by single-ended signals into standard 50Ω SMA female connectors. The analogue front-end circuit converts the single-ended inputs into balanced, differential signals for amplification by the ADA4930 low-voltage driver. In the case where the input amplifier stage is not required, then the board provides two separate jumper settings (J1 & J2) for enabling or disabling the input drivers.

Setting the jumper in the lower position (or removing the jumper completely) will *enable* the driver. In the upper position, the driver is *disabled* as described by figure (1). Note that if one of the analogue inputs is not used, then it is recommended that the corresponding driver is disabled in order to prevent the ADC being driven by an amplified noisy signal. Jumper 'J1' controls analogue input 'A'. Jumper 'J2' controls analogue input 'B'.

Both analogue inputs are designed to have a 50Ω input impedance. The inputs are bi-polar DC-coupled inputs with a min/max voltage swing from -500mV to +500mV (1V pk-pk) when the input drivers are enabled. A voltage swing greater than +/-500mV will cause clipping of the input waveform. It is recommended that voltages *exceeding* 4V peak-to-peak are not applied to the inputs as this may cause damage to the FMC card.

Anti-aliasing input filters

The amplified, differential signals from the ADA4930 are passed into a pair of passive RLC anti-aliasing filters. The filters have a -3dB cut-off frequency of ~100 MHz. Figures (4) & (5) below show the calculated magnitude and phase responses of the filter.

Depending on the application (and for the best possible results) it is recommended that the user implement further *digital* filtering using the resources available on the FPGA or SoC base-board. For instance, FIR or IIR digital filters may be used to further clean-up the channel. Other options such as low-pass filters, decimation filters, interpolation filters or pulse shaping filters may also be employed on the sampled signal[1].

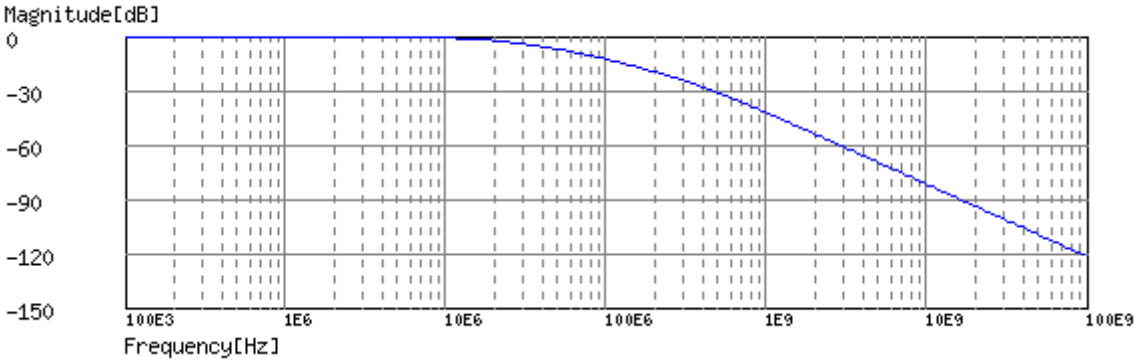

Figure 4: Input filter magnitude response

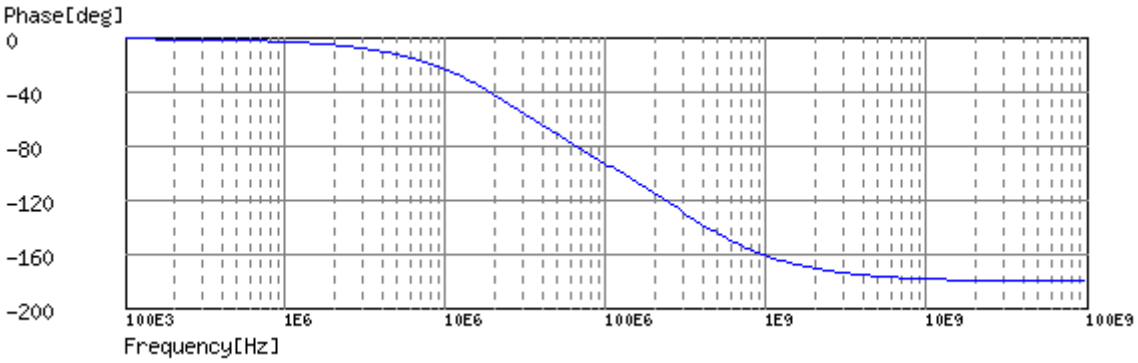

Figure 5: Input filter phase response

1 Please contact Zipcores for more information regarding our range of IP cores for digital filtering and DSP applications. All FPGAs, ASICs and SoCs are supported.

Dual ADC inputs

The dual ADC is a high-performance 12-bit, low-power component from Analog Devices® part number: AD9635. The ADC is designed for a wide range of applications including: data acquisition, digital signal processing, software radio and I/Q demodulation. The sampling frequency can be set to anything from 20 MSPS to 125 MSPS.

Note that the ADC channels are fully independent and they may both be operated at the full 125 MSPS if required. All data ports and clocks into and out of the ADC are differential LVDS signals. Full timing diagrams may be found in the relevant Analog Devices datasheets. For the most robust operation it is recommended that the default DDR, two-lane, 'bytewise' mode of operation is used. Figure (6) shows an excerpt from the AD9635 datasheet with the relevant timing diagrams.

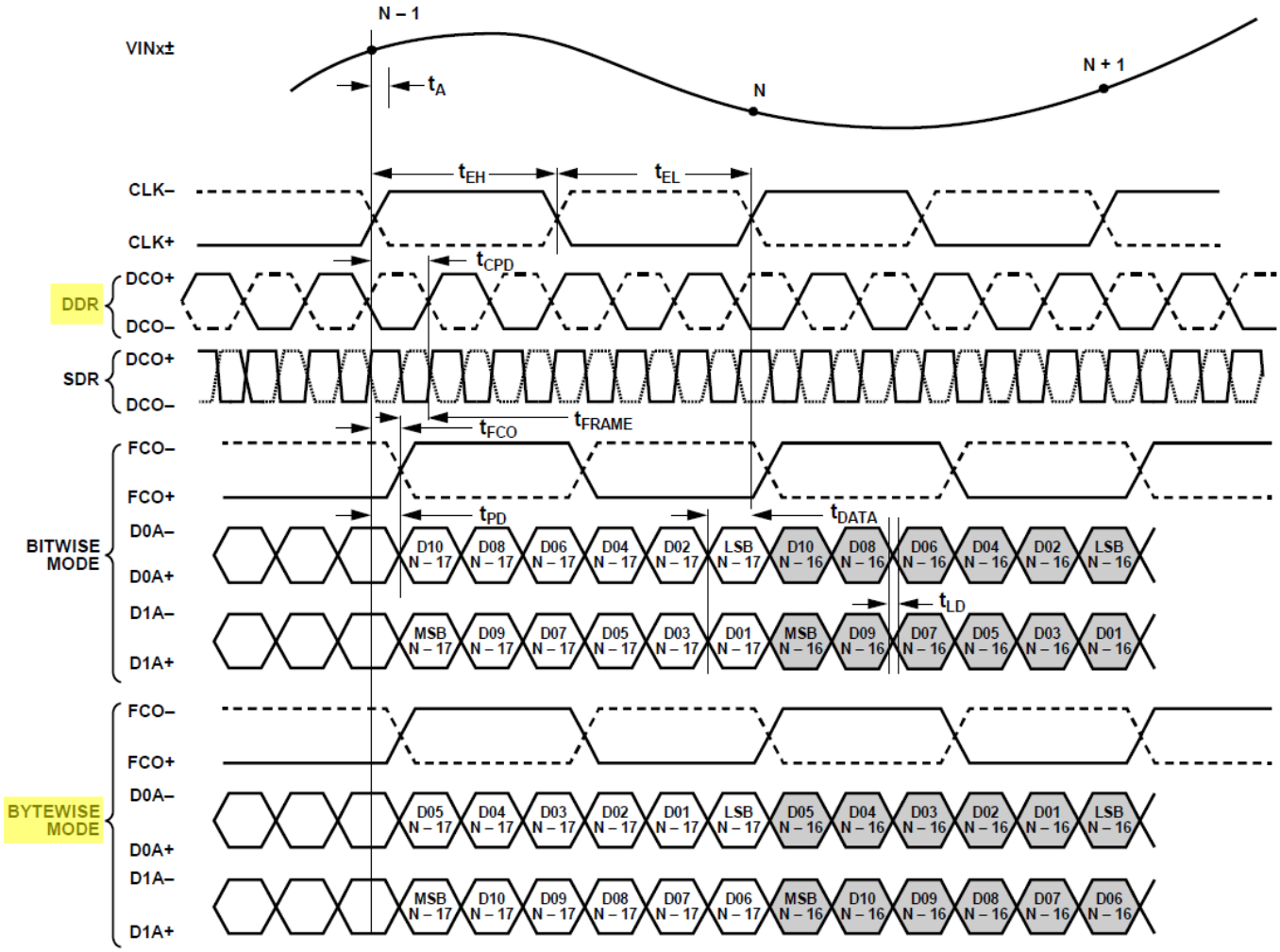

Figure 6: 12-bit DDR, two-lane, 1 x frame mode (default highlighted yellow)

Important: on power-up, and once the inputs are stable, the ADC should be *fully* reset to ensure correct operation of the device. A full device reset is performed via the SPI port. Details of how to do this are given in Appendix A at the end of the document.

Dual DAC outputs

The dual DAC outputs are provided by a high sample-rate, 12-bit, low-power component from Analog Devices® part number: AD9780. The sampling frequency can be set to anything up to 500 MSPS. The input data is multiplexed at double the sampling rate into a single 12-bit data bus. As with the ADC, all data ports and clocks in and out of the DAC are differential LVDS signals.

Note that due to the high sample-rate of the DAC, careful attention must be given to the generation of the sampling clock and data lanes to ensure that the data is captured cleanly in the centre of the data 'eye'. For this reason, the DAC has a programmable sample delay register which may be used to adjust the sample-clock edge relative to the data. Alternatively, the clock-edge may be skewed using the clocking resources on the base-board. For example, most FPGAs have PLL resources that allow different phase-shifted clocks to be generated. Figure (7) shows an excerpt from the AD9780 datasheet with the relevant timing diagrams.

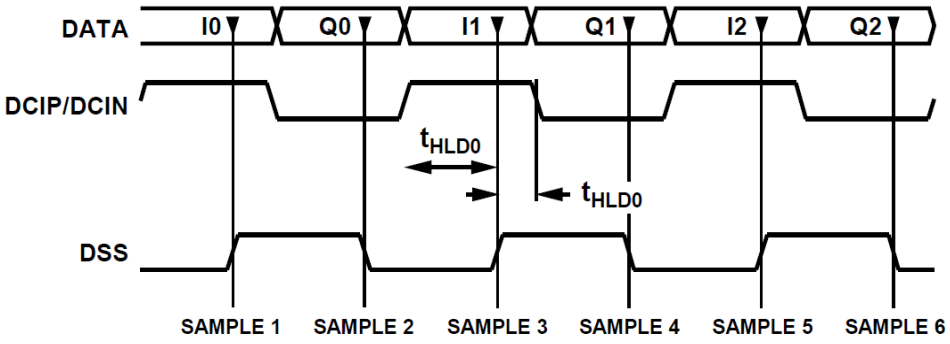

Figure 7: Timing diagram of the DAC parallel interface

The output signals from the DAC are converted to single-ended via the transformer. These analogue output signals are then connected to standard 50Ω female SMA connectors. Under default conditions, the outputs have a swing of around 1V pk-pk maximum into a 50Ω load when the full 12-bit dynamic range is used. In addition, the DAC has various programmable current and gain settings which may be used to adjust the output current and therefore adjust the pk-pk voltage into the output load accordingly.

It is important to note that on power-up, the hardware 'DAC_RESET' pin must be asserted (active low) for at least 10 ms. Without a reset, then the DAC will initialize into an unknown state and the outputs will be erroneous. In addition, it's also good practice to perform a software reset via the SPI port. Additional information is provided in Appendix B.

Clock generation and clocking considerations

The mezzanine card features a flexible clocking arrangement whereby all clocks into and out of the card are provided by the differential I/O pins on the FMC connector. Figure (8) shows the general clocking architecture. All differential LVDS pins are at the VADJ voltage level which can be anything from 1.5V to 2.5V.

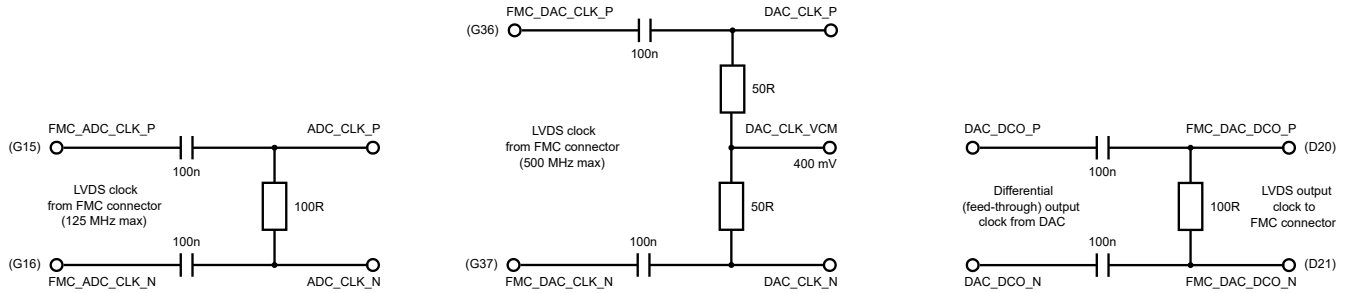

Figure 8: Clocking circuits for the ADC and DAC clocks. (Pins in brackets are the FMC pin numbers)

All FMC base-boards provide oscillators that may be used as source clocks for the ADC and DAC components. Together with the flexible PLL and clock-manager resources on most modern FPGAs, a wide range of sample-clock frequencies can be provided via the FMC pins.

General purpose PMOD™ headers

The board features two separate 12-pin male headers (J7 & J8) that conform to the PMOD standard for a general purpose bi-directional GPIO interface. The PMOD pins are connected to the spare pins on the FMC connector and are useful for general debug and additional board connectivity.

Note that the VCC pin is connected to the VADJ voltage on the FMC connector which is a slight deviation from the normal PMOD specification (normally 3.3V fixed). The VADJ voltage is adjustable according to the setting on the base-board. Each PMOD pin also has a 100Ω resistor in series to limit potential damage to the I/O of the source or sink device. Figure (9) below describes the pinout of the PMOD headers.

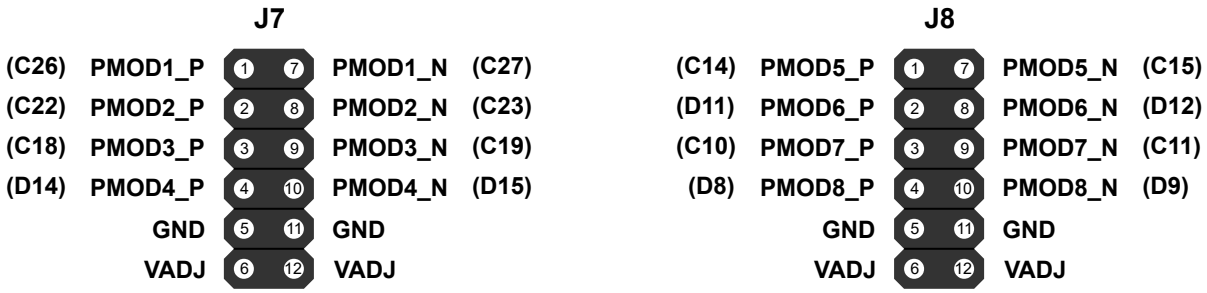

Figure 9: General purpose PMOD headers. (Pins in brackets are the FMC connector pin numbers)

ANSI/VITA 57.1 FMC™ connector

The mezzanine card uses a standard ANSI/VITA 57.1 FMC connector. The pinouts of the connector are configured with the Low-Pin-Count (LPC) option occupying sub-sets of rows D/C and G/H. Although the pinouts are designed for the LPC connector, the mezzanine card is also compatible with the High-Pin-Count connector (HPC) and latest FMC+ connectors from Samtec. Note that in the case of HPC then rows A/B, E/F and K/J will be left unconnected. A detailed specification of the FMC connector may be found on the Samtec® website here:

https://www.samtec.com/standards/vita/fmc

The FMC standard connector is used in a wide selection of FPGA development boards from vendors such as AMD/Xilinx®, Intel/Altera®, Avnet® and Digilent®. AMD in particular have adopted the FMC standard in all their FPGA and SoC development boards. Appendix C gives some examples of FMC compatible base-boards. More information can be found on the Xilinx website just here:

https://www.xilinx.com/products/boards-and-kits/fmc-cards.html

A full description of the FMC connector pinout with the mezzanine card is given in Appendix D.

Board power supplies

Main power on the board is derived from the fixed 3.3V supply on the FMC connector corresponding to pins D36, D38, D40 & C39. A linear regulator (ADP7158) is used to generate the 1.8V supply from the 3.3V input. This in turn is used as the core voltage for the ADC and DAC components. In addition, the 3.3V supply is used for the input drivers and some of the DAC digital I/O.

The adjustable voltage setting (VADJ) is used for the FMC differential LVDS pins and control pins for the SPI buses. The VADJ supply corresponds to pins G39 and H40 on the FMC. Normally, the VADJ voltage will be the same as the voltage as the FPGA bank(s) on the base-board. Most base-boards have a jumper setting that permits the VADJ voltage to be set from 1.2V to 2.5V. Setting VADJ to the highest possible value (e.g. 2.5V) is recommended to achieve the best possible performance and noise immunity. However, values as low as 1.5V have been tested on various AMD/Xilinx evaluation boards with correct results.

During normal operation with both the ADC and DAC being driven and the ADC input drivers enabled, the maximum power dissipation of the mezzanine card is 1W with a total current draw of 80 mA.

Appendices

Appendix A: Example SPI register configuration (AD9635)

This shows an example (minimum) register configuration for the default setup of the ADC in 12-bit mode. The registers should be written in the order given in the table below. (Note: the test mode option is not for normal operation, but is useful when performing initial board bring-up and debug when the mezzanine card is attached to the base-board for the first time).

Reg address	Value	Reg name	Description
0x00	0x3C	SPI port configuration	Performs a reset of the SPI port. Reset bits are automatically cleared after the register is written and defaults back to the value 0x18
0x08	0x03	Global power mode	Performs a full hardware reset of the ADC
0x08	0x00	Global power mode	Brings the ADC out of hardware reset and chip resumes normal operation

Test mode option:

0x0D	0x07	Test mode	This is register may be written to put the ADC in test mode. This is useful to verify that the ADC inputs are being sampled correctly and the ADC sample clock is good. Writing the value 0x7 generates an alternating one/zero word toggle on the ADC outputs.

In addition, please refer to the AD9635 datasheet for a full description of the SPI registers. Information can be downloaded from the Analog Devices website at: https://www.analog.com/en/products/ad9635.html

Appendix B: Example SPI register configuration (AD9780)

The DAC requires very little register setup save for a software reset of the SPI interface and controllers. The registers should be written in the following order:

Reg address	Value	Reg name	Description
0x00	0x20	SPI control	Reset the SPI controller
0x00	0x00	SPI control	Release SPI controller reset

Please refer to the AD9780 datasheet for a full description of the SPI registers. Information can be downloaded from the Analog Devices website at: https://www.analog.com/en/products/ad9780.html

Appendix C: Examples of supported FMC base-boards

ZYNQ-BASED SYSTEMS

Base-board name	***Supplier***	***No. of FMCs***	***VADJ options***
ZedBoard www.zedboard.org/product/zedboard	Digilent/Avnet	1 x LPC	1.8V, 2.5V, 3.3V
MicroZed FMC Carrier Card www.zedboard.org/product/microzed-fmc-carrier	Avnet	1 x LPC	1.8V, 2.5V, 3.3V
PicoZed FMC Carrier Card V2 www.zedboard.org/product/picozed-fmc-carrier-card-v2	Avnet	1 x LPC	1.8V, 2.5V, 3.3V
Xilinx Zynq UltraScale+ MPSoC ZCU104 Evaluation Kit www.xilinx.com/products/boards-and-kits/zcu104.html	Xilinx/Avnet	1 x LPC	1.2V, 1.5V, 1.8V
Xilinx Zynq-7000 SoC ZC702 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-z7-zc702-g.html	Xilinx/Avnet	2 x LPC	2.5V fixed
Xilinx Zynq-7000 SoC ZC706 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-z7-zc706-g.html	Xilinx/Avnet	1 x LPC + 1 x HPC	2.5V fixed

GENERAL FPGA-BASED SYSTEMS

Base-board name	***Supplier***	***No. of FMCs***	***VADJ options***
Spartan-7 FPGA SP701 Evaluation Kit www.xilinx.com/products/boards-and-kits/sp701.html	Xilinx/Avnet	1 x LPC	2.5V fixed
Nexys Video Artix-7 FPGA store.digilentinc.com/nexys-video-artix-7-fpga-trainer-board-for-multimedia-applications/	Digilent	1 x LPC	1.2V, 1.8V, 2.5V, 3.3V
Xilinx Artix-7 FPGA AC701 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-a7-ac701-g.html	Xilinx/Avnet	1 x HPC	1.8V, 2.5V, 3.3V
Xilinx Kintex-7 FPGA KC705 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-k7-kc705-g.html	Xilinx/Avnet	1 x LPC + 1 x HPC	1.8V, 2.5V, 3.3V
Genesys 2 Kintex-7 FPGA Development Board store.digilentinc.com/genesys-2-kintex-7-fpga-development-board/	Digilent	1 x HPC	1.2V, 1.8V, 2.5V, 3.3V
NetFPGA-1G-CML Kintex-7 FPGA Development Board store.digilentinc.com/netfpga-1g-cml-kintex-7-fpga-development-board/	Digilent	1 x HPC	1.2V, 1.8V, 2.5V, 3.3V
Xilinx Virtex-7 FPGA VC707 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-v7-vc707-g.html	Xilinx/Avnet	2 x HPC	1.2V, 1.5V, 1.8V
Xilinx Virtex-7 FPGA VC709 Connectivity Kit www.xilinx.com/products/boards-and-kits/dk-v7-vc709-g.html	Xilinx/Avnet	2 x HPC	1.8V fixed
NetFPGA-SUME Virtex-7 FPGA Development Board store.digilentinc.com/netfpga-sume-virtex-7-fpga-development-board/	Digilent	1 x HPC	1.2V, 1.8V, 2.5V, 3.3V

ULTRASCALE-BASED SYSTEMS

Base-board name	***Supplier***	***No. of FMCs***	***VADJ options***
Xilinx Kintex UltraScale FPGA KCU105 Evaluation Kit www.xilinx.com/products/boards-and-kits/kcu105.html	Xilinx/Avnet	1 x LPC + 1 x HPC	1.2V, 1.5V, 1.8V
Xilinx Kintex UltraScale FPGA KCU1250 Characterization Kit www.xilinx.com/products/boards-and-kits/ck-u1-kcu1250-g.html	Xilinx/Avnet	3 x HPC	1.8V fixed
Xilinx Virtex UltraScale FPGA VCU108 Evaluation Kit www.xilinx.com/products/boards-and-kits/ek-u1-vcu108-g.html	Xilinx/Avnet	2 x HPC	1.2V, 1.5V, 1.8V
Xilinx Virtex UltraScale+ FPGA VCU118 Evaluation Kit www.xilinx.com/products/boards-and-kits/vcu118.html	Xilinx/Avnet	1 x HPC	1.2V, 1.5V, 1.8V

Appendix D: FMC Connector pinout (rows H/G)

FMC pin	*VITA net name*	*FMC-DSP net name*	*FMC pin*	*VITA net name*	*FMC-DSP net name*
H1	VREF_A_M2C	N/C	G1	GND	GND
H2	PRSNT_M2C_L	N/C	G2	CLK1_M2C_P	FMC_ADC_SPI_SCLK
H3	GND	GND	G3	CLK1_M2C_N	FMC_ADC_SPI_CSB
H4	CLK0_M2C_P	FMC_ADC_SPI_SDI	G4	GND	GND
H5	CLK0_M2C_N	FMC_ADC_SPI_SDO	G5	GND	GND
H6	GND	GND	G6	LA00_P_CC	FMC_ADC_DCO_P
H7	LA02_P	FMC_ADC_D0A_P	G7	LA00_N_CC	FMC_ADC_DCO_N
H8	LA02_N	FMC_ADC_D0A_N	G8	GND	GND
H9	GND	GND	G9	LA03_P	FMC_ADC_FCO_P
H10	LA04_P	FMC_ADC_D1A_P	G10	LA03_N	FMC_ADC_FCO_N
H11	LA04_N	FMC_ADC_D1A_N	G11	GND	GND
H12	GND	GND	G12	LA08_P	FMC_ADC_D0B_P
H13	LA07_P	FMC_ADC_D1B_P	G13	LA08_N	FMC_ADC_D0B_N
H14	LA07_N	FMC_ADC_D1B_N	G14	GND	GND
H15	GND	GND	G15	LA12_P	FMC_ADC_CLK_P
H16	LA11_P	N/C	G16	LA12_N	FMC_ADC_CLK_N
H17	LA11_N	N/C	G17	GND	GND
H18	GND	GND	G18	LA16_P	FMC_DAC_SPI_SDI
H19	LA15_P	FMC_DAC_D0_P	G19	LA16_N	FMC_DAC_SPI_SDO
H20	LA15_N	FMC_DAC_D0_N	G20	GND	GND
H21	GND	GND	G21	LA20_P	FMC_DAC_D2_P
H22	LA19_P	FMC_DAC_D1_P	G22	LA20_N	FMC_DAC_D2_N
H23	LA19_N	FMC_DAC_D1_N	G23	GND	GND
H24	GND	GND	G24	LA22_P	FMC_DAC_D3_P
H25	LA21_P	FMC_DAC_DCI_P	G25	LA22_N	FMC_DAC_D3_N
H26	LA21_N	FMC_DAC_DCI_N	G26	GND	GND
H27	GND	GND	G27	LA25_P	FMC_DAC_D5_P
H28	LA24_P	FMC_DAC_D4_P	G28	LA25_N	FMC_DAC_D5_N
H29	LA24_N	FMC_DAC_D4_N	G29	GND	GND
H30	GND	GND	G30	LA29_P	FMC_DAC_D8_P
H31	LA28_P	FMC_DAC_D6_P	G31	LA29_N	FMC_DAC_D8_N
H32	LA28_N	FMC_DAC_D6_N	G32	GND	GND
H33	GND	GND	G33	LA31_P	FMC_DAC_D10_P
H34	LA30_P	FMC_DAC_D9_P	G34	LA31_N	FMC_DAC_D10_N
H35	LA30_N	FMC_DAC_D9_N	G35	GND	GND
H36	GND	GND	G36	LA33_P	FMC_DAC_CLK_P
H37	LA32_P	FMC_DAC_D11_P	G37	LA33_N	FMC_DAC_CLK_N
H38	LA32_N	FMC_DAC_D11_N	G38	GND	GND
H39	GND	GND	G39	VADJ	VADJ
H40	VADJ	VADJ	G40	GND	GND

Appendix E: FMC Connector pinout (rows D/C)

FMC pin	*VITA net name*	*FMC-DSP net name*	*FMC pin*	*VITA net name*	*FMC-DSP net name*
D1	PG_C2M	N/C	C1	GND	GND
D2	GND	GND	C2	DP0_C2M_P	N/C
D3	GND	GND	C3	DP0_C2M_N	N/C
D4	GBTCLK0_M2C_P	N/C	C4	GND	GND
D5	GBTCLK0_M2C_N	N/C	C5	GND	GND
D6	GND	GND	C6	DP0_M2C_P	N/C
D7	GND	GND	C7	DP0_M2C_N	N/C
D8	LA01_P_CC	FMC_PMOD8_P	C8	GND	GND
D9	LA01_N_CC	FMC_PMOD8_N	C9	GND	GND
D10	GND	GND	C10	LA06_P	FMC_PMOD7_P
D11	LA05_P	FMC_PMOD6_P	C11	LA06_N	FMC_PMOD7_N
D12	LA05_N	FMC_PMOD6_N	C12	GND	GND
D13	GND	GND	C13	GND	GND
D14	LA09_P	FMC_PMOD4_P	C14	LA10_P	FMC_PMOD5_P
D15	LA09_N	FMC_PMOD4_N	C15	LA10_N	FMC_PMOD5_N
D16	GND	GND	C16	GND	GND
D17	LA13_P	N/C	C17	GND	GND
D18	LA13_N	FMC_DAC_SPI_SCLK	C18	LA14_P	FMC_PMOD3_P
D19	GND	GND	C19	LA14_N	FMC_PMOD3_N
D20	LA17_P_CC	FMC_DAC_DCO_P	C20	GND	GND
D21	LA17_N_CC	FMC_DAC_DCO_N	C21	GND	GND
D22	GND	GND	C22	LA18_P_CC	FMC_PMOD2_P
D23	LA23_P	FMC_DAC_D7_P	C23	LA18_N_CC	FMC_PMOD2_N
D24	LA23_N	FMC_DAC_D7_N	C24	GND	GND
D25	GND	GND	C25	GND	GND
D26	LA26_P	FMC_DAC_RESET	C26	LA27_P	FMC_PMOD1_P
D27	LA26_N	FMC_DAC_SPI_CSB	C27	LA27_N	FMC_PMOD1_N
D28	GND	GND	C28	GND	GND
D29	TCK	N/C	C29	GND	GND
D30	TDI	N/C	C30	SCL	N/C
D31	TDO	N/C	C31	SDA	N/C
D32	3P3VAUX	N/C	C32	GND	GND
D33	TMS	N/C	C33	GND	GND
D34	TRST_L	N/C	C34	GA0	N/C
D35	GA1	N/C	C35	12P0V	N/C
D36	3P3V	VFIX_33	C36	GND	GND
D37	GND	GND	C37	12P0V	N/C
D38	3P3V	VFIX_33	C38	GND	GND
D39	GND	GND	C39	3P3V	VFIX_33
D40	3P3V	VFIX_33	C40	GND	GND

Appendix F: List of supporting design files

The FMC-DSP card has a number of supporting design files and documents that may be downloaded from the Zipcores website at: www.zipcores.com/downloads.html. Most of the design files are source-code files that are required for building and running the example demo as described in Appendix G. A list of these files and a brief description is given below:

Folders and important files	***Description***
docs/ zip_fmc_dsp_user_guide.pdf zip_fmc_dsp_safety_info.pdf zip_fmc_dsp_schematic.pdf zip_fmc_dsp_assembly.pdf zip_fmc_dsp_gerber.pdf zip_fmc_dsp_bom.pdf	Folder containing various design documents. FMC-DSP hardware user guide (this document). FMC-DSP regulatory compliance and safety information. FMC-DSP design schematics. FMC-DSP assembly drawings. FMC-DSP gerber summary. FMC-DSP bill of materials.
const/ fmc_dsp_top.xdc	Folder containing the physical constraints for the Xilinx Vivado project. Example master 'XDC' file that defines all the top-level pinouts and design constrains for the FMC-DSP card when connected to the ZedBoard base-board. This file may be adapted for use with all Xilinx FPGAs.
vivado/ FMC_DSP_TOP.xpr	This folder contains the Vivado project environment for the demo. Vivado project setup file (double click to invoke project).
verilog/	This folder contains all the source-code for the Xilinx 7-series hard IP such as the ISERDES, OSERDES and PLL components. (*Note: this IP ships for free with Vivado but is Xilinx proprietary*)
vhdl/ fmc_dsp_top.vhd fmc_dsp_top_bench.vhd	This folder contains the top-level VHDL source-code files for the example demo. The main top-level files are: The top-level component. The top-level testbench for the VHDL simulation.
modelsim/ FMC_DSP_TOP.mpf	This folder contains the Modelsim® simulation environment in order to run a VHDL hardware simulation of the demo. You will need to obtain a copy of Mentor Graphics Modelsim in order to use these files. Modelsim project setup file (double click to invoke project).
misc/	This folder contains various data sheets, schematics and design notes for the components on the FMC-DSP card.

Zipcores offers a wide range of IP Cores and custom solutions for the FMC-DSP development board. As well as Xilinx FPGAs, we can provide IP for other FPGAs or SoCs on request. If you have a specific requirement or simply want to discuss a potential solution then please get in touch. Further details may be found by visiting our website or contacting us at: www.zipcores.com/help.php.

Appendix G: Running the example demo

A simple demo is provided to get started with the FMC-DSP card. The demo provides a basic pass-through of the dual ADC input channels to the dual DAC output channels. The example demo uses a sample rate of 75 MHz throughout the design. In order to run the demo, the following basic lab setup is recommended:

- Waveform generator capable of generating a sine wave with a frequency of 1 MHz or greater. The output impedance should be 50Ω with a bi-polar input signal of +/-500 mV maximum (with input drivers enabled). This will provide the ADC input signals for channels A and B. (e.g. Teledyne LeCroy Wavestation 2022).
- Oscilloscope for measuring the output DAC waveforms. Ideally, it should have an option to set the load impedance to 50Ω with a bandwidth of 50 MHz or better. (e.g. Tektronix MDO3014).
- 4 x coaxial cables (50Ω) with suitable SMA + BNC connectors and/or adapters.
- Digilent/Avnet Zedboard (https://www.avnet.com/americas/products/avnet-boards/avnet-board-families/zedboard). This will be used as the base board on which the FMC-DSP mezzanine card will be mounted. (Note: other base boards may be supported on request. Please contact us for more details).
- Standoff legs and screws (size M3) in order to secure the FMC-DSP card to the base-board and provide structural support for the card on the bench.
- Xilinx Vivado Software (rev. 2018.3 or later) together with the ZedBoard board definition files.
- USB cable for programming the ZedBoard.

Once the equipment is set up then the user should invoke the Vivado software and load the project environment 'FMC_DSP_TOP.xpr' which is in the 'vivado' folder as described in Appendix F above. The same directory structure should be maintained so that the links and dependencies are correctly resolved. If the project loads correctly, the initial project layout should look something like Figure (10) below:

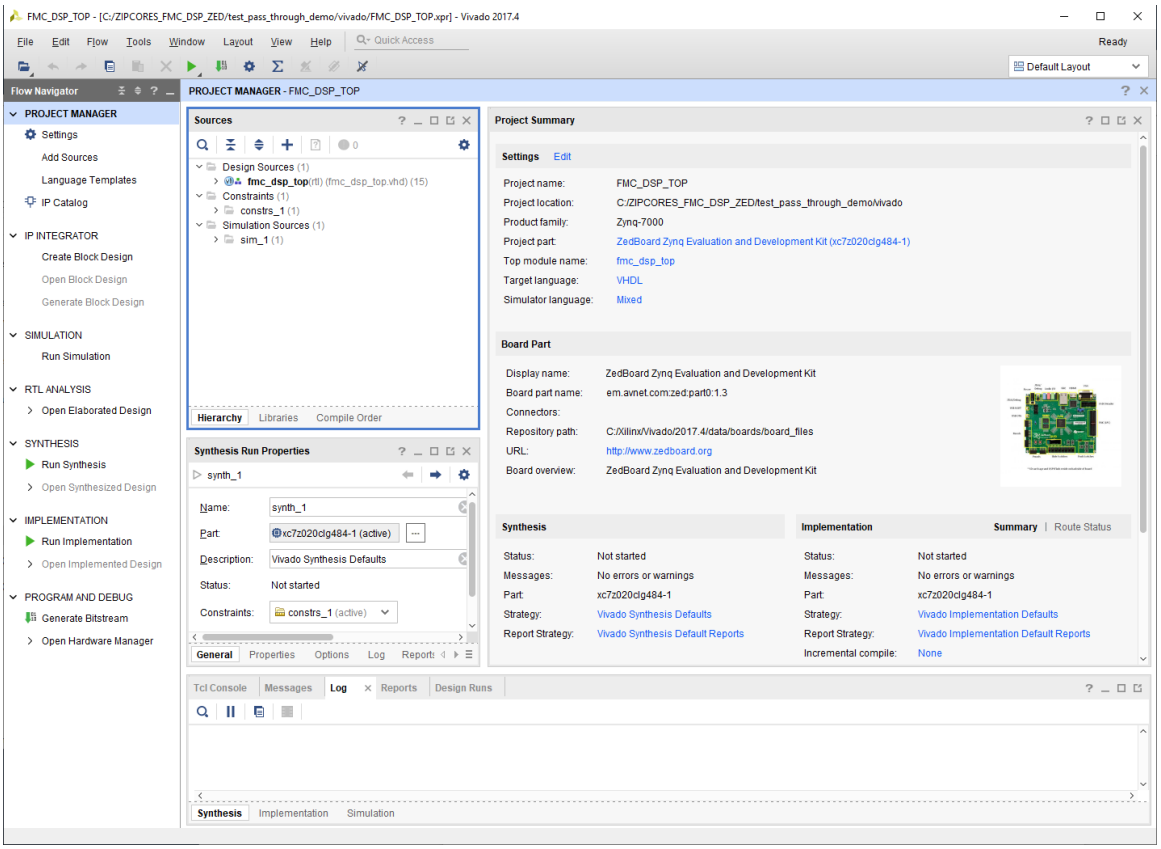

Figure 10: Initial Vivado project startup for demo

Once the project is loaded then the next step is to build the bitstream for programming the FPGA. Click on 'Generate Bitstream' in the project manager window and wait for the compile process to complete. After the bitstream is generated then open the hardware manager and program the ZedBoard. Figure (11) below shows an example bench setup with the FMC-DSP card being driven by separate 1 MHz sine waves and the input drivers enabled.

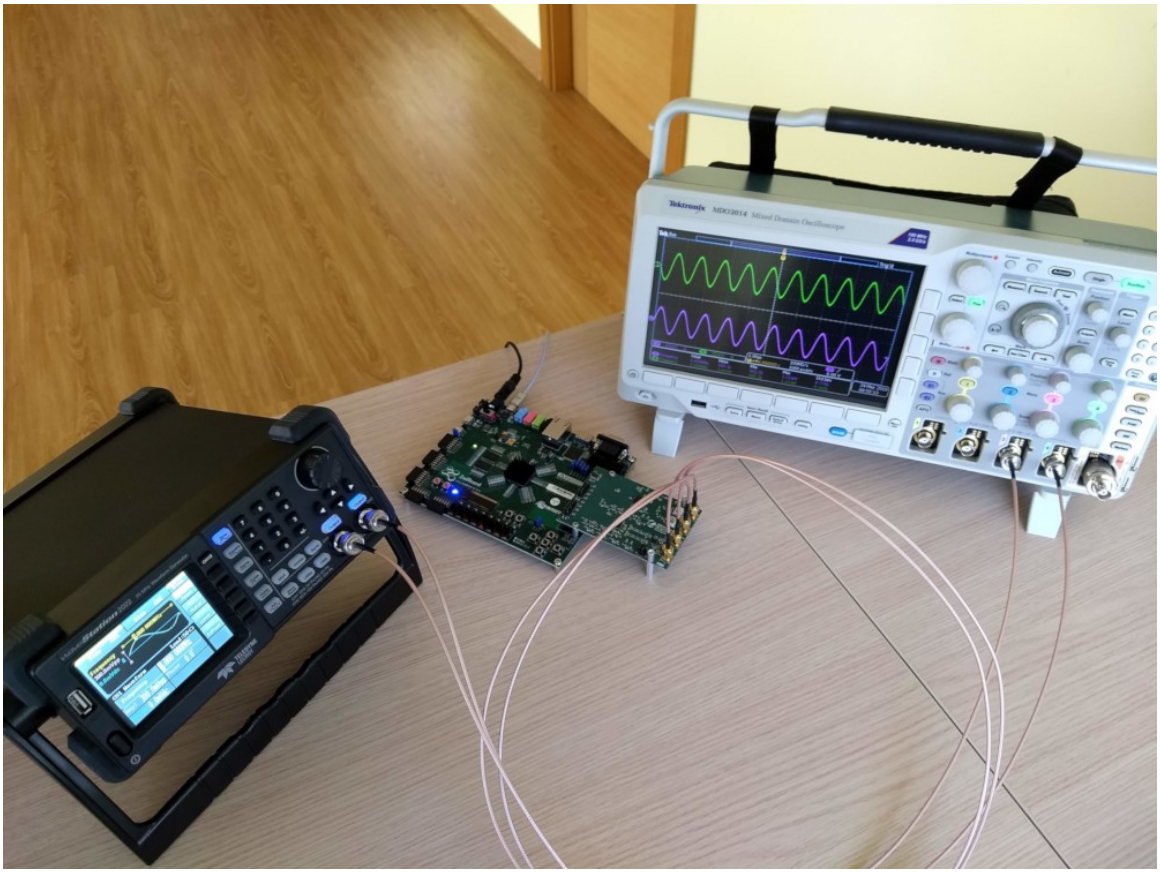

Figure 11: Bench setup showing FMC-DSP card connected to the Digilent ZedBoard

[*** IMPORTANT *** After powering-up and programming the ZedBoard then the user must initialize the DAC and ADC components on the FMC-DSP card. This is done by pressing the centre user button 'BTNC' followed by any one of the other user buttons e.g. 'BTND'].

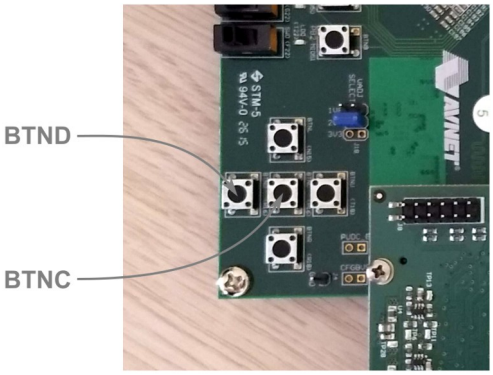

Figure 12: Button positions on the ZedBoard

Revision history

Revision	*Change description*	*Date*
C.0	Initial revision	25/11/2021
C.1	Updated board layout photos to show right-angled SMA connectors. Updated block diagram to fix number of LVDS lanes between FMC connector. Fixed typo in description of pins on PMOD7 connector which were incorrectly labelled (Figure 9). Fixed incorrect URL for the AD9780 component in Appendix B. Added gerber file description in Appendix F. Updated ZedBoard URL in Appendix G.	01/08/2025