

## 36V Operation 600mA Synchronous Step-Down DC/DC Converters with a Built-in Driver FET

### ■ GENERAL DESCRIPTION

The XC9704/XC9705 series are 36V operation synchronous step-down DC/DC converter ICs with a built-in High side driver FET and Low side driver FET. The XC9704/XC9705 series has an operating voltage range of 3.0V to 36.0V, a switching frequency can be selected from 1.2MHz and 2.2MHz, and the circuit scheme of synchronous rectification to be a highly efficient and stable power supply. The output voltage can be changed from 2.8V to 18.0V(XC9704), 2.8V to 15.0V(XC9705) using an external resistor, so the same part number can be used for multiple power lines.

By connecting a resistor and capacitor to the EN/SS pin, the soft start time can be externally adjusted to be longer than the internal soft start. The power good function also monitors the state of the output voltage. This soft-start external adjustment and power good functions make it easy to configure the power supply sequence.

Over-current protection and thermal shutdown are built in as protection function, and it can be used safely.

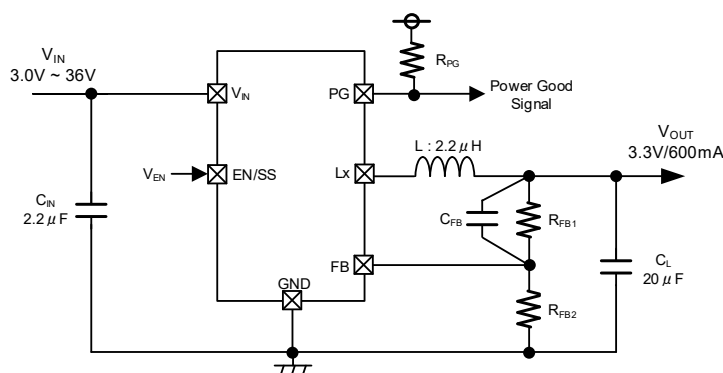
### ■ APPLICATIONS

- Industrial Automation
- Industrial Sensors
- Security Systems
- Home Appliances
- 4~20mA Current Loop
- High-Voltage LDO Replacement
- General-Purpose Power-circuit / Point-of-load

### ■ FEATURES

Input Voltage Range	: 3.0V ~ 36.0V (Absolute Max 40.0V)
Surge Voltage	: 46.0V (Applied Time $\leq$ 400ms)
Output Voltage Range	: 2.8V ~ 18.0V (XC9704) 2.8V ~ 15.0V (XC9705)
FB Voltage	: 0.75V $\pm$ 1.5%
Maximum Output Current	: 600mA
Oscillation Frequency	: 1.2MHz, 2.2MHz
Quiescent Current	: 11 $\mu$ A (XC9705)
Control Methods	: F-PWM Control (XC9704) PWM/PFM Control (XC9705)
Efficiency	: 90%@12V $\rightarrow$ 5V, 300mA
Protection functions	: Current Limit (Automatic Recovery) Thermal Shutdown
Functions	: Soft Start (external adjustment) Power Good (USP-6C only)
Output Capacitor	: Ceramic Capacitor
Operating Junction Temperature	: -40°C ~ 150°C
Packages	: SOT-89-5 (4.5 x 4.6 x 1.6mm) (Without Power Good) USP-6C (1.8 x 2.0 x 0.6mm) (With Power Good)
Environmentally Friendly	: EU RoHS Compliant, Pb Free

### ■ TYPICAL APPLICATION CIRCUIT



### ■ TYPICAL PERFORMANCE CHARACTERISTICS

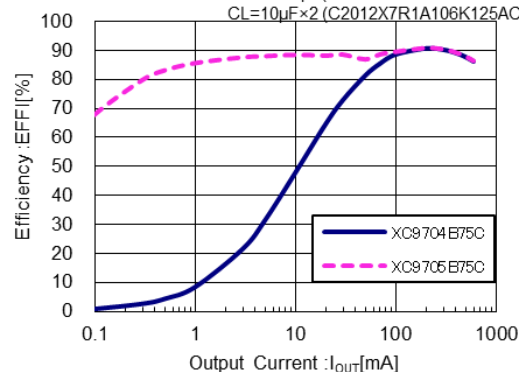
XC9704B75C/XC9705B75C

V<sub>IN</sub>=12V, V<sub>OUT</sub>=5.0V

L=6.8 $\mu$ H (CLF5030NIT-6R8N)

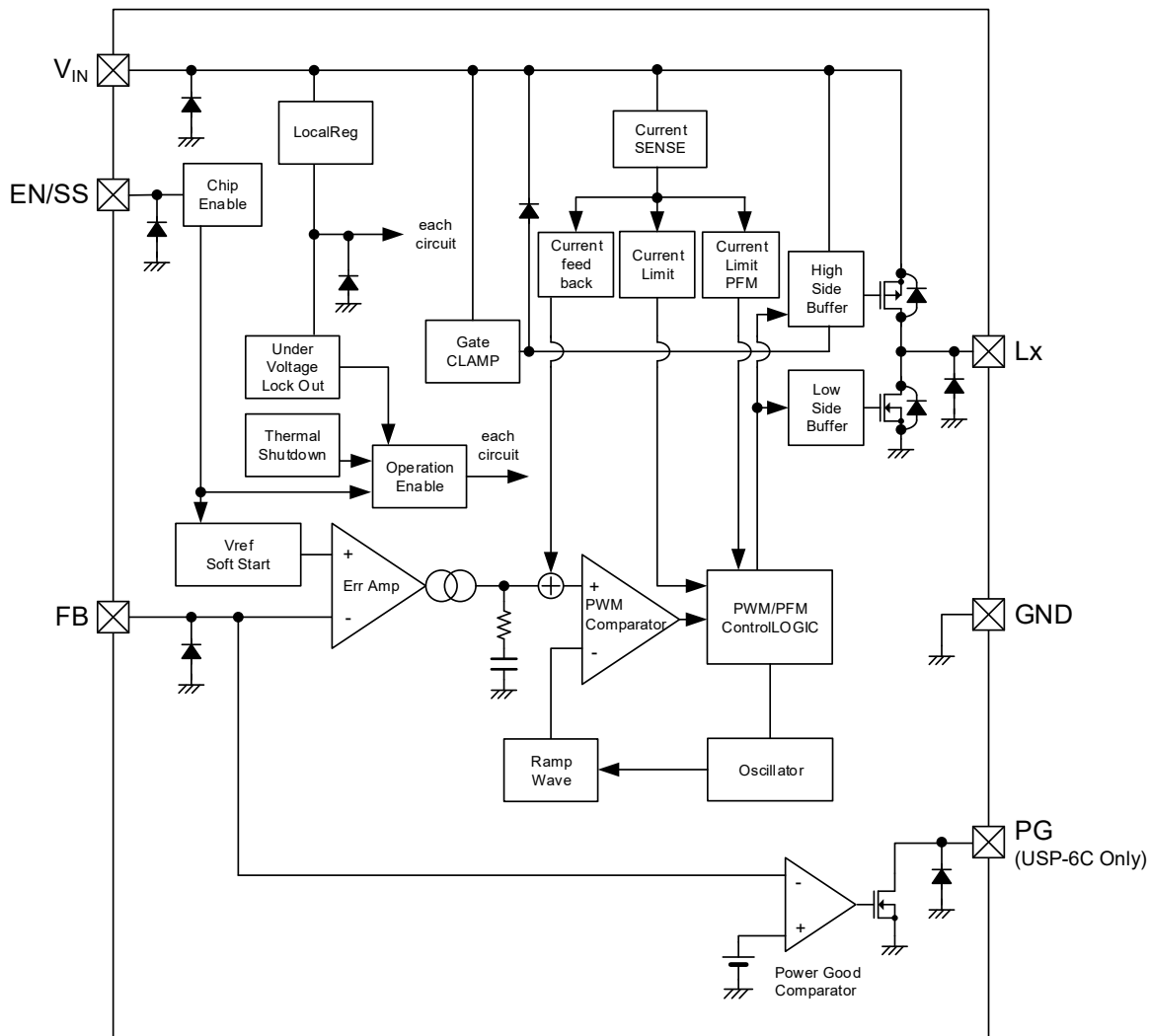
C<sub>IN</sub>=2.2 $\mu$ F (C2012X7R1H225K125AC)

C<sub>L</sub>=10 $\mu$ F $\times$ 2 (C2012X7R1A106K125AC)



# XC9704/XC9705 Series

## BLOCK DIAGRAM



\* Diodes inside the circuit are ESD protection diodes and parasitic diodes.

## ■PRODUCT CLASSIFICATION

### ●Ordering Information

XC9704①②③④⑤⑥-⑦<sup>(\*)</sup> : F-PWM Control

XC9705①②③④⑤⑥-⑦<sup>(\*)</sup> : PWM/PFM Control

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	B	-
②③	FB Voltage	75	0.75V
④	Oscillation Frequency	C	1.2MHz
		D	2.2MHz
⑤⑥-⑦	Packages	PR-G <sup>(*)</sup>	SOT-89-5 (1,000pcs/Reel)
		ER-G <sup>(*)</sup>	USP-6C (3,000pcs/Reel)

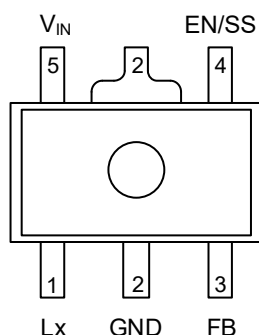
<sup>(\*)</sup> "Halogen and Antimony free" as well as being fully EU RoHS compliant.

### ●Selection Guide

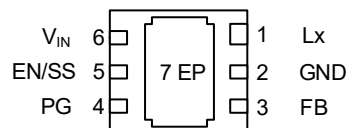
FUNCTION	SOT-89-5	USP-6C
Enable	Yes	Yes
UVLO	Yes	Yes
Thermal Shutdown	Yes	Yes
Soft Start	Yes	Yes
Power-Good	-	Yes
Current Limiter (Automatic Recovery)	Yes	Yes

# XC9704/XC9705 Series

## PIN CONFIGURATION



SOT-89-5  
(TOP VIEW)



USP-6C  
(BOTTOM VIEW)

## PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-89-5	USP-6C		
1	1	Lx	Switching Output
2	2	GND	Ground
3	3	FB	Output Voltage Sense
-	4	PG	Power-good Output
4	5	EN/SS	Enable, Soft-start
5	6	V <sub>IN</sub>	Power Input
-	7	EP	Exposed thermal pad. The Exposed pad is recommended to be connected to GND (Pin2)

## FUNCTION CHART

PIN NAME	SIGNAL	STATUS
EN/SS	H	Active
	L	Stand-by
	OPEN	Stand-by

PIN NAME	CONDITION		SIGNAL
PG	EN/SS = H	$V_{FB} > V_{PGDET}$	H (High impedance)
		$V_{FB} \leq V_{PGDET}$	L (Low impedance)
		Thermal Shutdown	L (Low impedance)
		UVLO ( $V_{IN} < V_{UVLOD}$ )	Undefined State
	EN/SS = L	Stand-by	L (Low impedance)

## ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
V <sub>IN</sub> Pin Voltage		V <sub>IN</sub>	-0.3 ~ 40.0	V
EN/SS Pin Voltage		V <sub>EN/SS</sub>	-0.3 ~ 40.0	V
FB Pin Voltage		V <sub>FB</sub>	-0.3 ~ 6.2	V
PG Pin Voltage <sup>(*)4</sup>		V <sub>PG</sub>	-0.3 ~ 6.2	V
PG Pin Current <sup>(*)4</sup>		I <sub>PG</sub>	8	mA
Lx Pin Voltage		V <sub>Lx</sub>	-0.3 ~ V <sub>IN</sub> + 0.3 or 40.0 <sup>(*)1</sup>	V
Power Dissipation (Ta=25°C)	SOT-89-5	P <sub>d</sub>	2150 (JESD51-7 Board) <sup>(*)2</sup>	mW
	USP-6C		1550 (JESD51-7 Board) <sup>(*)2</sup>	
V <sub>IN</sub> Pin Surge Voltage		V <sub>IN_SURGE</sub>	46.0 <sup>(*)3</sup>	V
EN/SS Pin Surge Voltage		V <sub>EN/SS_SURGE</sub>	46.0 <sup>(*)3</sup>	V
Junction Temperature		T <sub>j</sub>	-40 ~ 150	°C
Storage Temperature		T <sub>stg</sub>	-55 ~ 150	°C

All voltages are described based on the GND pin.

<sup>(\*)1</sup> The maximum value should be either V<sub>IN</sub>+0.3V or 40.0V in the lowest.

<sup>(\*)2</sup> The power dissipation figure shown is PCB mounted and is for reference only.

Please refer to PACKAGING INFORMATION for the mounting condition.

<sup>(\*)3</sup> Applied Time ≤ 400ms

<sup>(\*)4</sup> For the USP-6C only.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER			SYMBOL	MIN.	TYP.	MAX.	UNIT					
Setting Output Voltage Range		XC9704	V <sub>OUTSET</sub>	2.8	-	18.0	V					
		XC9705				15.0						
Input Voltage			V <sub>IN</sub>	3.0	-	36.0	V					
Output Current			I <sub>OUT</sub>	0.0	-	600	mA					
EN/SS Pin Voltage			V <sub>EN/SS</sub>	0.0	-	36.0	V					
PG Pull-up Voltage			V <sub>PG</sub>	0.0	-	5.5	V					
PG Pull-up Resistor			R <sub>PG</sub>	5	100	-	kΩ					
Operating Ambient Temperature			T <sub>opr</sub>	-40	-	125	°C					
Input Capacitor (Effective Value) <sup>(*)</sup>			C <sub>IN</sub>	0.5	-	1000 <sup>(*)</sup>	μF					
Output Capacitor (Effective Value) <sup>(*)</sup>	V <sub>IN</sub> <20V, f <sub>OSCSET</sub> 1.2MHz	V <sub>OUTSET</sub> ≤3.3V	C <sub>L</sub>	13.2	-	1000 <sup>(*)</sup>	μF					
		3.3V<V <sub>OUTSET</sub> ≤6V		10.4								
		6V<V <sub>OUTSET</sub>		12.0								
	20V≤V <sub>IN</sub> , f <sub>OSCSET</sub> 1.2MHz	V <sub>OUTSET</sub> ≤3.3V		24.6								
		3.3V<V <sub>OUTSET</sub> ≤6V		29.6								
		6V<V <sub>OUTSET</sub>		15.0								
	f <sub>OSCSET</sub> 2.2MHz	V <sub>OUTSET</sub> ≤3.3V		13.2								
		3.3V<V <sub>OUTSET</sub> ≤6V		10.4								
		6V<V <sub>OUTSET</sub>		12.0								
	Inductor	f <sub>OSCSET</sub> 1.2MHz		V <sub>OUTSET</sub> ≤3.3V				L	4.7 x 0.7	4.7	4.7 x 1.3	μH
				3.3V<V <sub>OUTSET</sub> ≤6V					6.8 x 0.7	6.8	6.8 x 1.3	
				6V<V <sub>OUTSET</sub>					10 x 0.7	10	10 x 1.3	
f <sub>OSCSET</sub> 2.2MHz		V <sub>OUTSET</sub> ≤3.3V	2.2 x 0.7	2.2	2.2 x 1.3							
		3.3V<V <sub>OUTSET</sub> ≤6V	3.3 x 0.7	3.3	3.3 x 1.3							
		6V<V <sub>OUTSET</sub>	4.7 x 0.7	4.7	4.7 x 1.3							

All voltages are described based on the GND pin.

<sup>(\*)</sup> Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

<sup>(\*)</sup> If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitance, place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase and the IC may malfunction.

<sup>(\*)</sup> If a large-capacity capacitor is used as output capacitor, the output stability may be reduced, and the ripple voltage may increase. Even if a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor is used as output capacitor, please place a low-ESR ceramic capacitor in parallel. Even if the capacitance is within the recommended range, the output stability may be reduced depending on the type and ESR etc. of the capacitor used, so please thoroughly test it on the actual equipment before use.

## ■ ELECTRICAL CHARACTERISTICS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
Operating Input Voltage Range	V <sub>IN</sub>	-		3.0	-	36.0	V	-
Setting Output Voltage Range	V <sub>OUTSET</sub>	-	XC9704	2.8	-	18.0	V	-
			XC9705	2.8	-	15.0		
FB Voltage	V <sub>FBE</sub>	V <sub>FB</sub> =0.739V→0.761V, V <sub>FB</sub> Voltage when Lx pin voltage changes from "H" level to "L" level		0.739	0.750	0.761	V	②
Over Voltage Protection	V <sub>OVP</sub>	-		-	0.81	-	V	-
UVLO Detect Voltage	V <sub>UVLOD</sub>	V <sub>EN/SS</sub> =12V, V <sub>IN</sub> :2.80V→2.60V, V <sub>FB</sub> =0V V <sub>IN</sub> Voltage when Lx pin changes "L" to "H" level		2.60	2.70	2.80	V	②
UVLO Release Voltage	V <sub>UVLOR</sub>	V <sub>EN/SS</sub> =12V, V <sub>IN</sub> : 2.70V→2.90V, V <sub>FB</sub> =0V V <sub>IN</sub> Voltage when Lx pin changes "H" to "L" level		2.70	2.80	2.90	V	②
Quiescent Current	I <sub>q</sub>	V <sub>FB</sub> =0.765V	XC9704B75C	-	270	540	μA	④
			XC9704B75D	-	320	640		
			XC9705	-	11	19		
Stand-by Current	I <sub>STB</sub>	V <sub>IN</sub> =12V, V <sub>EN/SS</sub> =0V		-	0.6	1.2	μA	④
Oscillation Frequency	f <sub>OSC</sub>	Connected to external components	XC970xB75C	1.098	1.200	1.302	MHz	①
			XC970xB75D	2.013	2.200	2.387		
Minimum Duty Cycle	D <sub>MIN</sub>	V <sub>FB</sub> =0.825V		-	-	0	%	②
Maximum Duty Cycle	D <sub>MAX</sub>	V <sub>FB</sub> =0.675V		100	-	-	%	②
Lx SW "H" On Resistance	R <sub>LxH</sub>	V <sub>FB</sub> =0.6V, I <sub>Lx</sub> =200mA		-	1.20	1.38	Ω	⑤
Lx SW "L" On Resistance	R <sub>LxL</sub>	I <sub>Lx</sub> =200mA		-	0.60	0.70	Ω	-
High side Current Limit	I <sub>LIMH</sub>	V <sub>FB</sub> =V <sub>FBE</sub> ×0.98		1.1	1.4	1.7	A	⑤
Internal Soft-Start Time	t <sub>SS1</sub>	V <sub>FB</sub> =0.71V		1.0	2.2	4.5	ms	②
External Soft-Start Time	t <sub>SS2</sub>	V <sub>FB</sub> =0.71V, R <sub>SS</sub> =430kΩ, C <sub>SS</sub> =0.47μF		14	21	32	ms	③

Test Condition : Unless otherwise stated, V<sub>IN</sub>=12V, V<sub>EN/SS</sub>=12V, V<sub>PG</sub>: OPEN (\*1)

(\*1) For the USP-6C only.

## ELECTRICAL CHARACTERISTICS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
PG Detect Voltage <sup>(*)</sup>	V <sub>PGDET</sub>	V <sub>FB</sub> =0.712V→0.638V, R <sub>PG</sub> :100kΩ pull-up to 5V V <sub>FB</sub> Voltage when PG pin voltage changes from "H" level to "L" level		0.638	0.675	0.712	V	⑤
PG Output Voltage <sup>(*)</sup>	V <sub>PG</sub>	V <sub>FB</sub> =0.6V, I <sub>PG</sub> =1mA		-	-	0.3	V	②
PFM Switch Current (XC9705)	I <sub>PFM</sub>	Connected to external components, I <sub>OUT</sub> =0mA	XC9705B75C	-	300	-	mA	①
			XC9705B75D	-	450	-		
FB Voltage Temperature Characteristics	$\Delta V_{FB}/(\Delta T_{opr} \cdot V_{FBE})$	-40°C≤T <sub>opr</sub> ≤125°C		-	±100	-	ppm/°C	②
FB "H" Current	I <sub>FBH</sub>	V <sub>IN</sub> =V <sub>EN/SS</sub> =36V, V <sub>FB</sub> =3.0V		-	0.0	0.1	μA	④
FB "L" Current	I <sub>FBL</sub>	V <sub>IN</sub> =V <sub>EN/SS</sub> =36V, V <sub>FB</sub> =0V		-	0.0	0.1	μA	④
EN/SS "H" Voltage	V <sub>ENSSH</sub>	V <sub>EN/SS</sub> =0.3V→2.5V, V <sub>FB</sub> =0.71V V <sub>EN/SS</sub> Voltage when Lx pin voltage changes from "L" level to "H" level		2.5	-	36.0	V	④
EN/SS "L" Voltage	V <sub>ENSSL</sub>	V <sub>EN/SS</sub> =2.5V→0.3V, V <sub>FB</sub> =0.71V V <sub>EN/SS</sub> Voltage when Lx pin voltage changes from "H" level to "L" level		GND	-	0.3	V	④
EN/SS "H" Current	I <sub>ENSSH</sub>	V <sub>IN</sub> =V <sub>EN/SS</sub> =36V, V <sub>FB</sub> =0.825V		-	0.1	0.3	μA	④
EN/SS "L" Current	I <sub>ENSSL</sub>	V <sub>IN</sub> =36V, V <sub>EN/SS</sub> =0V, V <sub>FB</sub> =0.825V		-	0.0	0.1	μA	④
Thermal Shutdown Temperature	T <sub>TSD</sub>	Junction Temperature		-	160	-	°C	—
Hysteresis Width	T <sub>HYS</sub>	Junction Temperature		-	25	-	°C	—

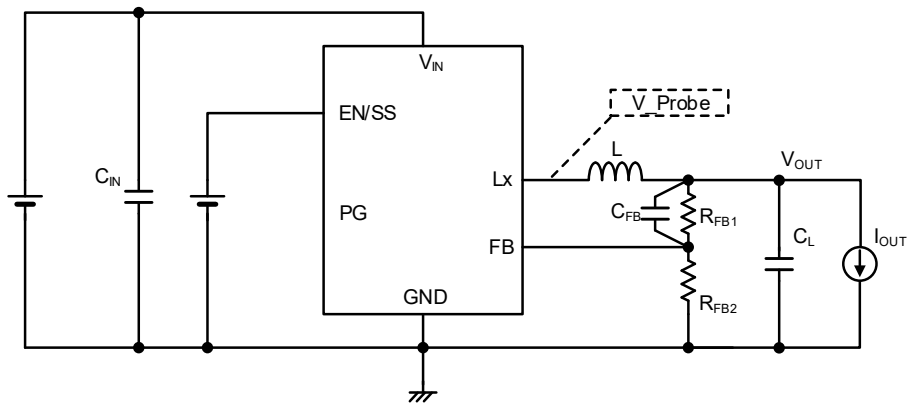
Test Condition : Unless otherwise stated, V<sub>IN</sub>=12V, V<sub>EN/SS</sub>=12V, V<sub>PG</sub>: OPEN <sup>(\*)</sup>

<sup>(\*)</sup> For the USP-6C only.



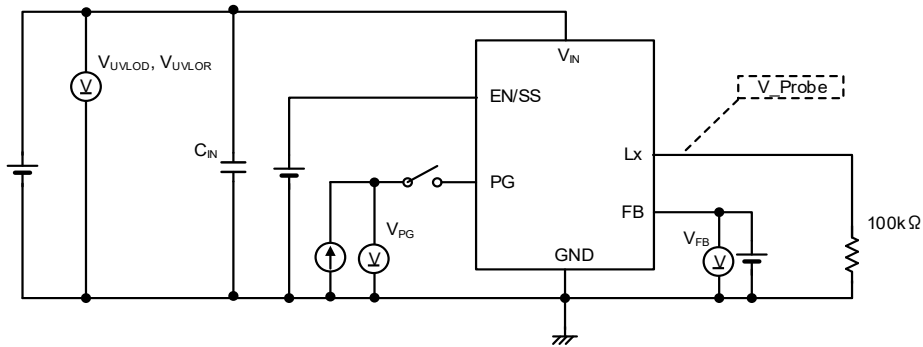
## ■ TEST CIRCUITS

CIRCUIT①

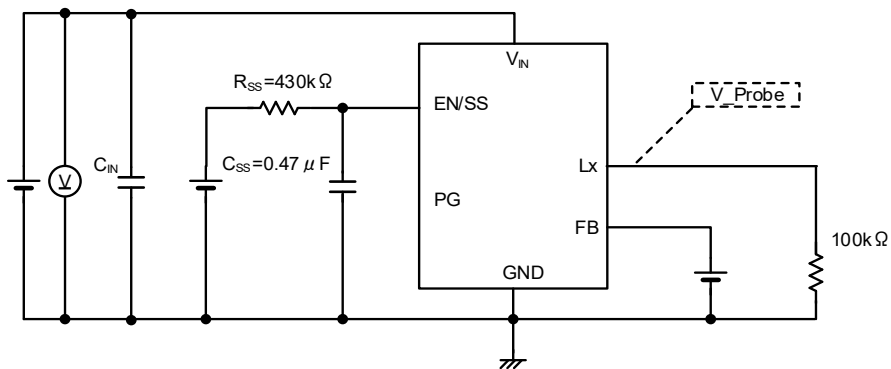


$f_{osc}=1.2\text{MHz}$ :  $L=6.8\mu\text{H}$ ,  $R_{FB1}=680\text{k}\Omega$ ,  $R_{FB2}=120\text{k}\Omega$ ,  $C_{FB}=18\text{pF}$ ,  $C_L=10\mu\text{F}\times 2\text{parallel}$ ,  $C_{IN}=2.2\mu\text{F}$   
 $f_{osc}=2.2\text{MHz}$ :  $L=3.3\mu\text{H}$ ,  $R_{FB1}=680\text{k}\Omega$ ,  $R_{FB2}=120\text{k}\Omega$ ,  $C_{FB}=12\text{pF}$ ,  $C_L=10\mu\text{F}\times 2\text{parallel}$ ,  $C_{IN}=2.2\mu\text{F}$

CIRCUIT②



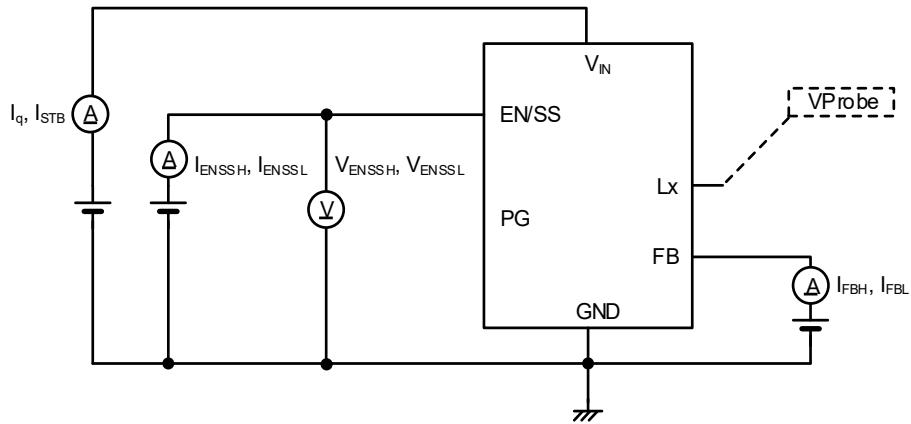
CIRCUIT③



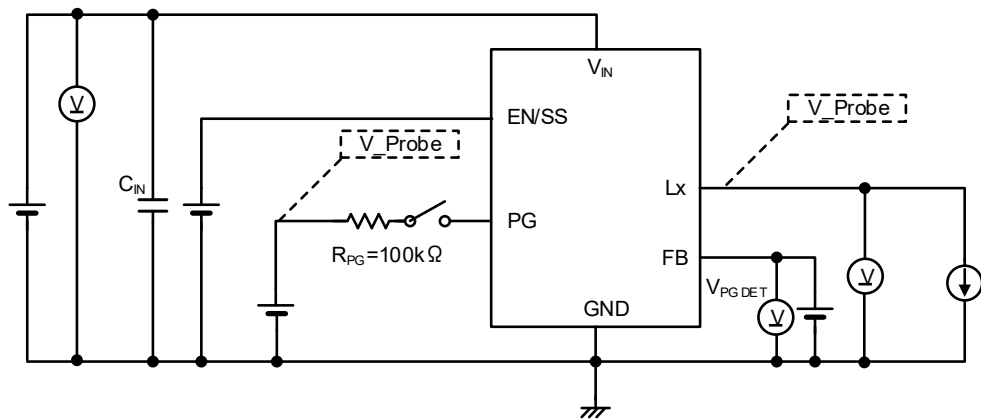
\* PG Pin is USP-6C Package only.

## TEST CIRCUITS

CIRCUIT④

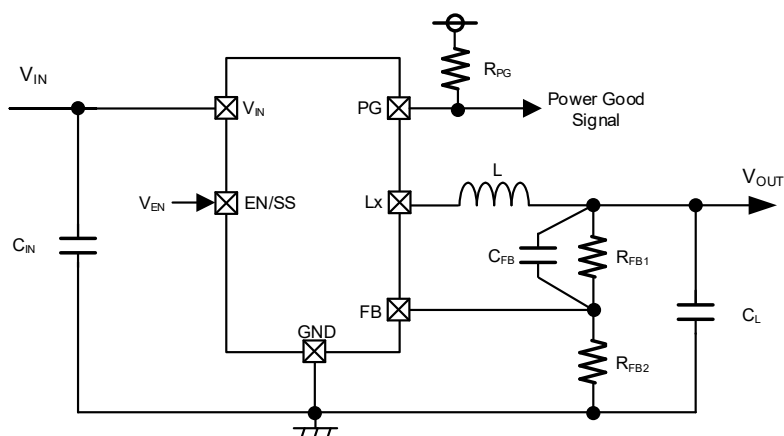


CIRCUIT⑤



\* PG Pin is USP-6C Package only.

# TYPICAL APPLICATION CIRCUIT / Parts Selection Method



	f <sub>OSCSET</sub>	V <sub>OUTSET</sub>	MANUFACTURER	PRODUCT NUMBER	VALUE
L	1.2MHz	$V_{OUTSET} \leq 3.3V$	TDK	CLF5030NIT-4R7N	4.7μH
			Coilcraft	XGL3530-472ME	
				XGL4030-472ME	
			Taiyo Yuden	LSXND5050WDL4R7MMG	
		$3.3V < V_{OUTSET} \leq 6V$	Tokyo Coil	SHP0530P-F4R7AP	6.8μH
			TDK	CLF5030NIT-6R8N	
			Coilcraft	XGL3530-682ME	
				XGL4030-682ME	
			Taiyo Yuden	LSXND5050WDL6R8MMG	
			Tokyo Coil	SHP0530P-F6R8AP	
		$6V < V_{OUTSET}$	TDK	CLF5030NIT-100N	10μH
			Taiyo Yuden	LSXND5050YAL100MMG	
			Coilcraft	XGL4030-103ME	
			Tokyo Coil	SHP0530P-F100AP	
	2.2MHz	$V_{OUTSET} \leq 3.3V$	TDK	VLS252012CX-2R2M-1	2.2μH
				CLF5030NIT-2R2N-D	
			Coilcraft	XGL3530-222ME	
				XGL4030-222ME	
			Taiyo Yuden	LCXND4040TKL2R2MDG	
			Tokyo Coil	SHP0420P-F2R2NAP	
		$3.3V < V_{OUTSET} \leq 6V$	TDK	CLF5030NIT-3R3N-D	3.3μH
			Coilcraft	XGL3530-332ME	
				XGL4030-332ME	
			Taiyo Yuden	LCXND4040TKL3R3MDG	
			Tokyo Coil	SHP0420P-F3R3NAP	
		$6V < V_{OUTSET}$	TDK	CLF5030NIT-4R7N	4.7μH
			Coilcraft	XGL3530-472ME	
				XGL4030-472ME	
			Taiyo Yuden	LSXND5050WDL4R7MMG	
			Tokyo Coil	SHP0530P-F4R7AP	

## TYPICAL APPLICATION CIRCUIT / Parts Selection Method

	$f_{OSCSET}$	$V_{IN}$	$V_{OUTSET}$	MANUFACTURER	PRODUCT NUMBER	VALUE
$C_{IN}$	-	-	-	TDK	C2012X7R1H225K125AC	2.2 $\mu$ F/50V
$C_L$	1.2MHz	$V_{IN} < 20V$	$V_{OUTSET} \leq 6V$	TDK	C2012X7R1A106K125AC	10 $\mu$ F/10V 2parallel
			$6V < V_{OUTSET} \leq 12V$	TDK	C3216X7R1E106K160AB	10 $\mu$ F/25V 2parallel
			$12V < V_{OUTSET}$	TDK	C3225X7R1H106M250AC	10 $\mu$ F/50V 2parallel
		$20V \leq V_{IN}$	$V_{OUTSET} \leq 6V$	Murata	GRM21BR61A476ME15	47 $\mu$ F/10V 2parallel
				Murata	GRM21BC81C226ME44	22 $\mu$ F/16V 3parallel
				TDK	C3225X7R1C226M250AC	22 $\mu$ F/16V 2parallel
			$6V < V_{OUTSET} \leq 12V$	TDK	C3225X7R1E226M250AB	22 $\mu$ F/25V 2parallel
			$12V < V_{OUTSET}$	TDK	C3225X7R1E226M250AB	22 $\mu$ F/25V 2parallel
	2.2MHz	-	$V_{OUTSET} \leq 6V$	TDK	C2012X7R1A106K125AC	10 $\mu$ F/10V 2parallel
			$6V < V_{OUTSET} \leq 12V$	TDK	C3216X7R1E106K160AB	10 $\mu$ F/25V 2parallel
			$12V < V_{OUTSET}$	TDK	C3225X7R1H106M250AC	10 $\mu$ F/50V 2parallel

(\*) Some ceramic capacitors have an effective capacitance that is significantly lower than the nominal value due to the applied DC bias and ambient temperature. For the input / output capacitance of this IC, use an appropriate ceramic capacitor according to the DC bias usage conditions (ambient temperature, input / output voltage) so that the effective capacitance value is equal to or higher than the recommended component.

(\*) If using a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor as the input capacitance, place a low ESR ceramic capacitor in parallel. If a ceramic capacitor is not placed, high-frequency voltage fluctuations will increase and the IC may malfunction.

(\*) If a large-capacity capacitor is used as output capacitor, the output stability may be reduced, and the ripple voltage may increase. Even if a large-capacity capacitor such as an electrolytic capacitor or tantalum capacitor is used as output capacitor, please place a low-ESR ceramic capacitor in parallel. Even if the capacitance is within the recommended range, the output stability may be reduced depending on the type and ESR etc. of the capacitor used, so please thoroughly test it on the actual equipment before use.

## ■ TYPICAL APPLICATION CIRCUIT / Parts Selection Method (Continued)

### <Output voltage setting>

The output voltage can be set by adding an external dividing resistor.

The output voltage setting is determined by the equation below based on the values of  $R_{FB1}$  and  $R_{FB2}$ .

$$V_{OUTSET} = V_{FBE} \times (R_{FB1} + R_{FB2}) / R_{FB2}$$

$$R_{FB2} \leq 200k\Omega \text{ and } R_{FB1} + R_{FB2} \leq 1M\Omega$$

If the IC does not operate properly due to external noise, noise resistance performance can be improved by using a combination of  $R_{FB1}$  and  $R_{FB2}$  that is smaller than the above conditional expression.

### < $C_{FB}$ setting>

Adjust the value of the phase compensation speed-up capacitor  $C_{FB}$  within  $\pm 20\%$  using the equation below.

$$C_{FB} = \frac{1}{2\pi \times f_{zfb} \times R_{FB1}}$$

$$f_{zfb} = \frac{1}{2\pi \sqrt{C_L \times L}}$$

### 【Calculation Example】

To set output voltage to 5.0V, ( $f_{osc}=2.2MHz$ ,  $C_L=10\mu F \times 2$ ,  $L=3.3\mu H$ )

$V_{OUTSET} = 0.75V \times (680k\Omega + 120k\Omega) / 120k\Omega = 5.0V$ , and  $f_{zfb}$  is set to a target of 19.6kHz using the above equation,

$C_{FB} = 1 / (2 \times \pi \times 19.6kHz \times 680k\Omega) = 11.95pF$ , which is 12pF for the E24 series.

### 【Typical example for 1.2MHz】

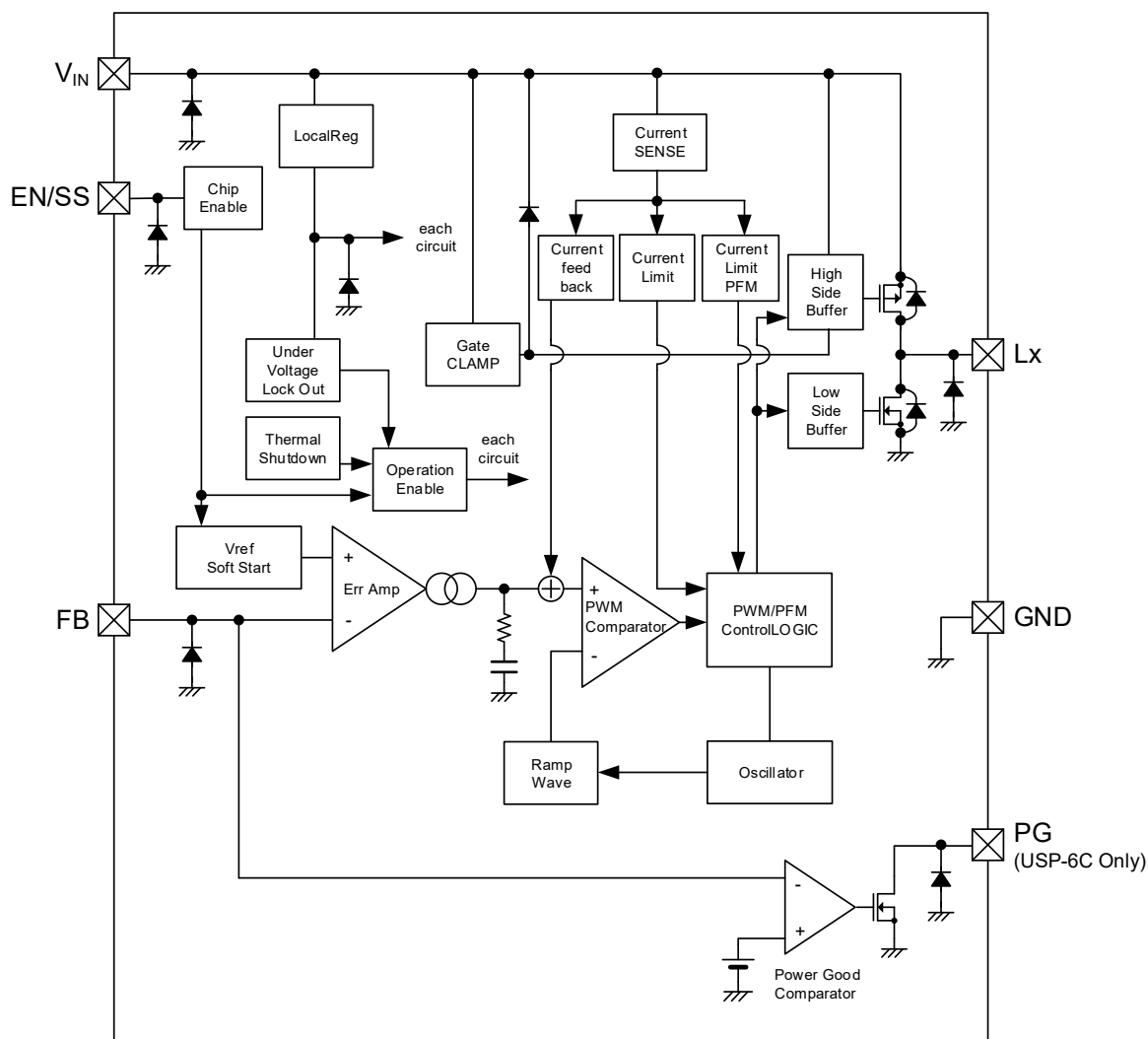
$V_{OUTSET}$	$R_{FB1}$	$R_{FB2}$	L	$C_L$	$C_{FB}$	$f_{zfb}$
3.3V	510k $\Omega$	150k $\Omega$	4.7 $\mu H$	10 $\mu F \times 2$	18pF	16.4kHz
				22 $\mu F \times 2$	27pF	11.1kHz
5.0V	680k $\Omega$	120k $\Omega$	6.8 $\mu H$	10 $\mu F \times 2$	18pF	13.7kHz
				22 $\mu F \times 2$	24pF	9.2kHz
12.0V	360k $\Omega$	24k $\Omega$	10 $\mu H$	10 $\mu F \times 2$	39pF	11.3kHz
				22 $\mu F \times 2$	56pF	7.6kHz

### 【Typical example for 2.2MHz】

$V_{OUTSET}$	$R_{FB1}$	$R_{FB2}$	L	$C_L$	$C_{FB}$	$f_{zfb}$
3.3V	510k $\Omega$	150k $\Omega$	2.2 $\mu H$	10 $\mu F \times 2$	13pF	24.0kHz
5.0V	680k $\Omega$	120k $\Omega$	3.3 $\mu H$	10 $\mu F \times 2$	12pF	19.6kHz
12.0V	360k $\Omega$	24k $\Omega$	4.7 $\mu H$	10 $\mu F \times 2$	27pF	16.4kHz

## ■ OPERATIONAL EXPLANATION

The XC9704/XC9705 series consists internally of a reference voltage supply with soft-start function, error amplifier, PWM comparator, ramp circuit, oscillator circuit, phase compensation (current feedback) circuit, current limit circuit, current limiting-PFM circuit, High-side driver FET, Low-side driver FET, buffer drive circuit, internal power supply (Local Reg) circuit, under voltage lockout (UVLO) circuit, gate clamp circuit, thermal shutdown circuit etc.



## ■ OPERATIONAL EXPLANATION

### <Normal operation>

The reference voltage  $V_{ref}$  and FB pin voltage are compared using an error amplifier, the output from the error amplifier is phase compensated, and the signal is input to the PWM comparator to determine the ON time of switching during PWM operation.

The output signal from the error amplifier is compared to the ramp wave by the PWM comparator, and the output is sent to the buffer drive circuit and output from the Lx pin as the duty width of switching. This operation is performed continuously to stabilize the output voltage.

The current sense circuit monitors the driver FET current at each switching, and the output signal from the error amplifier is modulated as a multi-feedback signal (current feedback circuit). This achieves a stable feedback system to be obtained even when a low ESR capacitor such as a ceramic capacitor is used, and this stabilizes the output voltage.

### XC9704 Series : F-PWM control

XC9704 series operates in forced PWM mode.

XC9704 series operates at a constant frequency  $f_{osc}$  regardless of the output current, making it easy to filter switching noise.

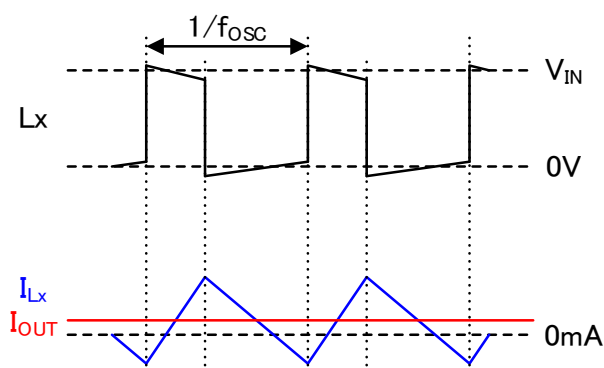
Also, if the FB pin voltage remains higher than  $V_{FB}$ , the switching operation will be stopped (High side driver FET turned off, Low side driver FET turned on) until the FB pin voltage drops.

### XC9705 Series : PWM/PFM Auto switching control

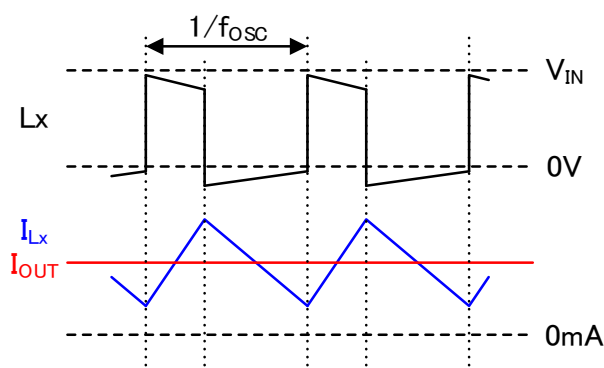
XC9705 series operates in PWM/PFM automatic switching mode.

PWM/PFM automatic switching control drops the switching frequency during light loads by turning on the High side driver FET when the coil current reaches the  $I_{PFM}$  (TYP. 300mA( $f_{osc}=1.2\text{MHz}$ ), 450mA( $f_{osc}=2.2\text{MHz}$ )).

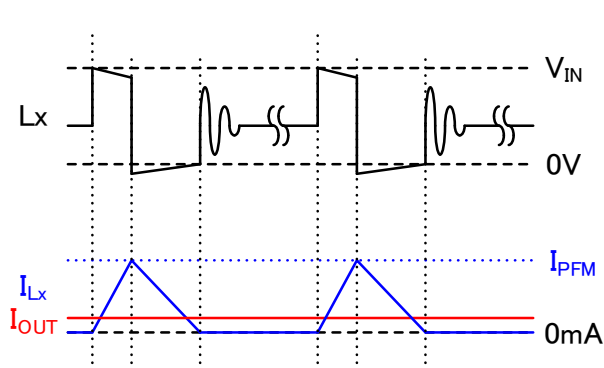
This operation reduces the loss during light loads and achieves high efficiency from light to heavy loads. As the output current increases, the switching frequency increases proportional to the output current, and when the switching frequency increases  $f_{osc}$ , the circuit switches from PFM control to PWM control and the switching frequency becomes fixed.



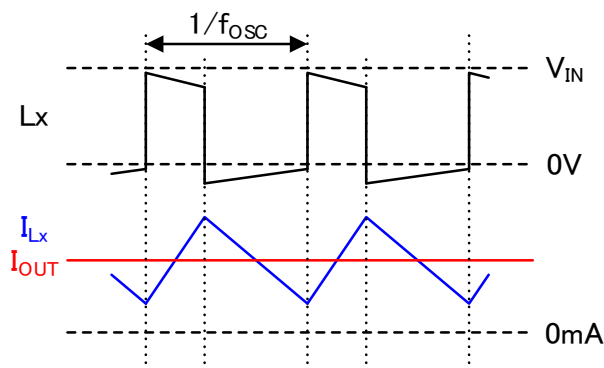
XC9704 Series(F-PWM Control) : Example of light load operation



XC9704 Series (F-PWM Control) : Example of heavy load operation



XC9705 Series(PWM/PFM Control) : Example of light load operation



XC9705 Series(PWM/PFM Control) : Example of heavy load operation

## ■ OPERATIONAL EXPLANATION

### <EN Function / Start Mode-Soft-start Function>

The state of the IC can be switched by applying voltage to the EN/SS pin.

SIGNAL	STATUS
H	Active
L	Stand-by
OPEN	Stand-by

#### EN/SS="L" : Stand-by mode

When the "L" voltage is input to the EN/SS pin, the IC enters the stand-by mode, and the current consumption is reduced to the stand-by current  $I_{STB}$  (TYP. 0.6μA). In the stand-by mode, no signal is output to the Lx pin and the output voltage does not rise.

In addition, various protection functions stop operating.

#### EN/SS="H" : Active mode

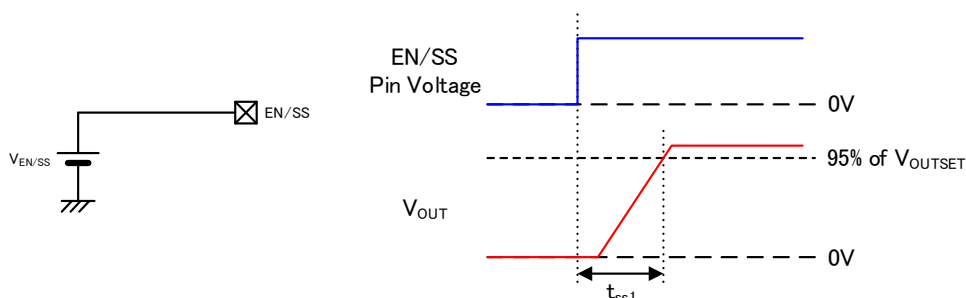
When the EN/SS pin voltage is "H", the IC becomes active. When the IC becomes active, it enters start-up mode and increases the output voltage to the set output voltage.

In start-up mode, a soft-start function is provided to gently raise the output voltage to suppress inrush current at start-up. The soft-start time can be adjusted by externally mounting a capacitor and resistor on the EN/SS pin.

During the start-up mode, the device operates in the same way as in normal operation, except that the reference voltage increases linearly.

##### (a) Internal soft-start time (without external RC)

When the EN/SS pin voltage rises steeply, the output voltage rises with an internally set soft-start time of  $t_{ss1}$  (TYP. 2.2ms) and shifts to normal mode.



##### (b) Soft-start time external adjustment (with external RC)

The soft-start time can be adjusted by externally mounting a capacitor and resistor on the EN/SS pin.

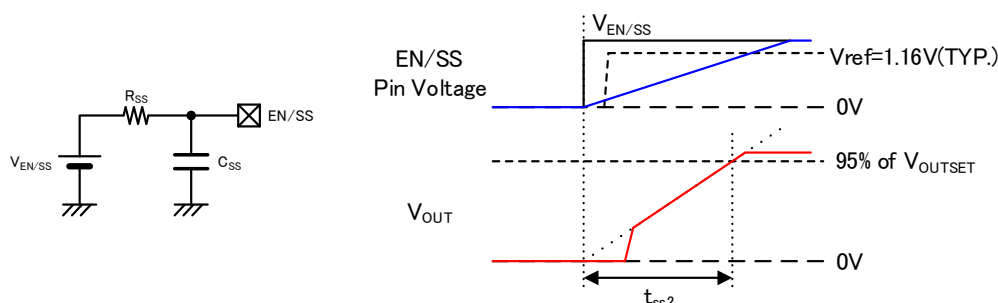
The externally set soft-start time ( $t_{ss2}$ ) is determined by the following formula, depending on the EN/SS pin voltage ( $V_{EN/SS}$ ),  $R_{SS}$ , and  $C_{SS}$  values.

$$t_{ss2} = C_{SS} \times R_{SS} \times \ln \frac{V_{EN/SS}}{V_{EN/SS} - 1.16V}$$

For example, When the soft-start time at  $C_{SS} = 0.47\mu F$ ,  $R_{SS} = 430k\Omega$ ,  $V_{EN/SS} = 12V$

$$t_{ss2} = 0.47 \times 10^{-6} \times 430 \times 10^3 \times \ln \frac{12}{12 - 1.16} = 21ms$$

However, it cannot start faster than the internally setting soft-start time  $t_{ss1}$ .



\* Definition of soft-start time : Time from  $V_{EN/SS}$  start-up until output voltage reaches 95% of set output voltage.



## ■ OPERATIONAL EXPLANATION

### <Current Limit>

The current limit circuit of this IC detects the current flowing through the driver FET connected to Lx pin and equivalently monitors the coil current. The current limit function operates when over current is detected. When the current limit function operates, the High side current limit function and Low side current limit function operate.

The current limit state continues until the overcurrent state is released, and the output voltage automatically recovers when the overcurrent state is released.

A current fold-back circuit is used for the current limit function.

The current foldback circuit reduces the current limit when the output voltage drops. This operation reduces the output current when the output voltage drops.

#### High side Current Limit

The High side current limit function detects when the coil current exceeds the High side current limit value  $I_{LIMH}$  (TYP. 1.4A) and turns off the High side driver FET. In other words, it controls the coil current so that it does not exceed a certain peak value. However, if the input voltage is high, the coil current peak value may exceed  $I_{LIMH}$  due to the operation delay of the internal circuit.

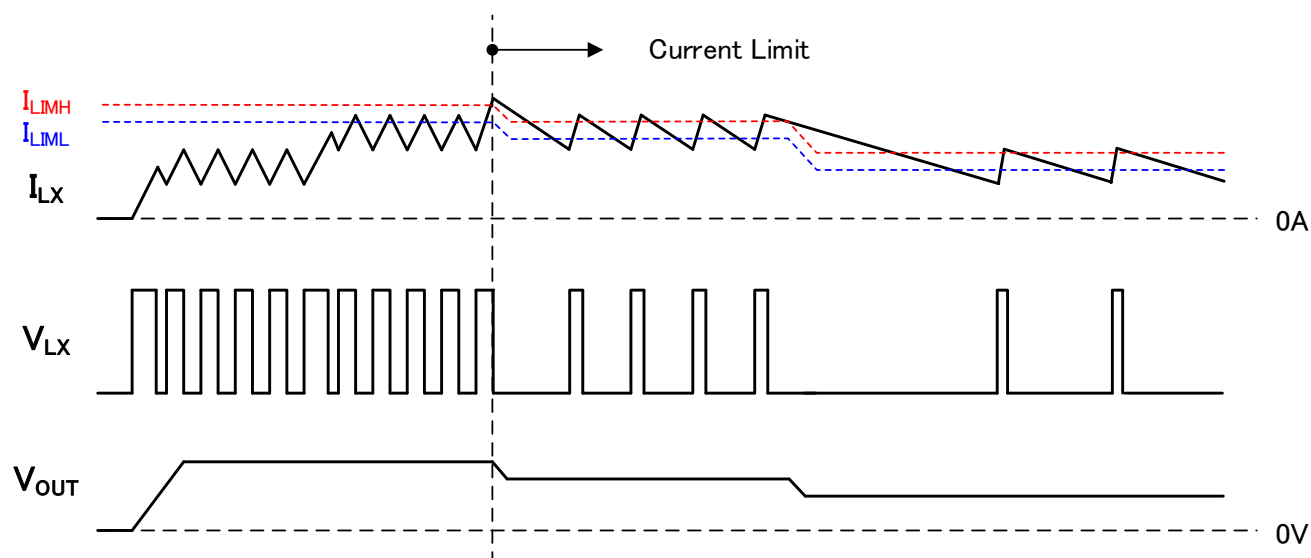
#### Low side Current Limit

The Low side current limit function turns on the Low side driver FET until the coil current becomes less than the Low side current limit value  $I_{LIML}$  (TYP. 1.0A). In other words, it controls the coil current to stay below a certain coil current bottom value.

The current limit function also operates during start-up mode.

During start-up mode, the output voltage is lower than the set output voltage, the current limit value is reduced, which speeds up overcurrent detection.

If an output capacitance with a higher effective capacitance value than the recommended component is used, the start-up will take place while the current limit function is operating, and the start-up time may be much longer than the soft-start time.



## ■ OPERATIONAL EXPLANATION

### <Thermal Shutdown>

The junction temperature is monitored to protect the IC from thermal destruction.

When the junction temperature reaches the thermal shutdown detection temperature  $T_{TSD}$  (TYP. 160°C), the thermal shutdown activated, the High side driver FET and Low side driver FET are turned off. When the junction temperature drops to the thermal shutdown release temperature  $T_{TSD-THYS}$  (TYP. 135°C) by stopping the current supply, the output voltage is turned on by the start-up mode, and then normal operation starts.

### <UVLO>

This function monitors the internal power supply of the IC and prevents false pulse output from the Lx pin due to unstable operation when the internal power supply is low. As the IC's internal power supply drops as the  $V_{IN}$  pin voltage drops, the UVLO function operates.

When the  $V_{IN}$  pin voltage falls below  $V_{UVLOD}$  (TYP. 2.7V), the UVLO function operates, and forcibly turns off the driver FETs.

When the  $V_{IN}$  pin voltage rises above  $V_{UVLOR}$  (TYP. 2.8V), the UVLO function is released, and the output voltage rises according to the start-up mode.

Moreover, during the UVLO operation, the internal circuit is operating because stopping by UVLO is not same to a stand-by mode and just switching operation is stopped.

### <Negative Current Limit>

When the output voltage becomes higher than the set voltage, the Low side driver FET turns on to reduce the output voltage. If the Low side driver FET continues to be turned on, the coil current reverses and a negative current continues to flow. This reverse current is limited to -900mA (TYP.) by the negative current limit function.

When the negative current limit function operates, the Low side driver FET turns off and remains until the next cycle. During this period, the reverse current flows through the parasitic diode of the High side driver FET into the power supply connected to the  $V_{IN}$  pin.

If the negative current limit function operates during start-up mode, the switching operation stops until the reference voltage becomes higher than the FB voltage.

### <Over Voltage Protection>

An output overvoltage protection function is built in to suppress output voltage overshoots after completion of start-up or transient response. When the FB pin voltage rises above  $V_{OVP}$  (TYP. 0.81V), the output overvoltage protection function operates and forcibly turns off the High side driver FET.

In forced PWM control (XC9704), the Low side driver FET is turned on immediately after the output overvoltage protection function operates and remains this state until the next cycle.

In PWM/PFM automatic switching control (XC9705), the driver FET is turned off by the output overvoltage protection function. When the output voltage drops to the set value due to the output current, switching operation resumes.

### <Power Good>

On USP-6C Package, the output state of IC can be monitored using the power good function.

CONDITIONS		SIGNAL
EN/SS = H	$V_{FB} > V_{PGDET}$	H (High impedance)
	$V_{FB} \leq V_{PGDET}$	L (Low impedance)
	Thermal Shutdown	L (Low impedance)
	UVLO ( $V_{IN} < V_{UVLOD}$ )	Undefined State
EN/SS = L	Stand-by	L (Low impedance)

The PG pin is an Nch open drain output, therefore a pull-up resistance (approx. 100kΩ) must be connected to the PG pin. When the power good function is not used, connect the PG pin to GND or leave it open.

A delay time of 400μs(TYP.) is provided from the moment, the FB pin voltage drops below  $V_{PGDET}$  to PG="L".

If the FB pin voltage returns to a voltage higher than  $V_{PGDET}$  during the delay time, PG remains "H".

This prevents PG="L" due to output undershoot during transient response.

In addition, there is no intentional delay for PG="L" due to the operation of the protection function or transition to the stand-by state.

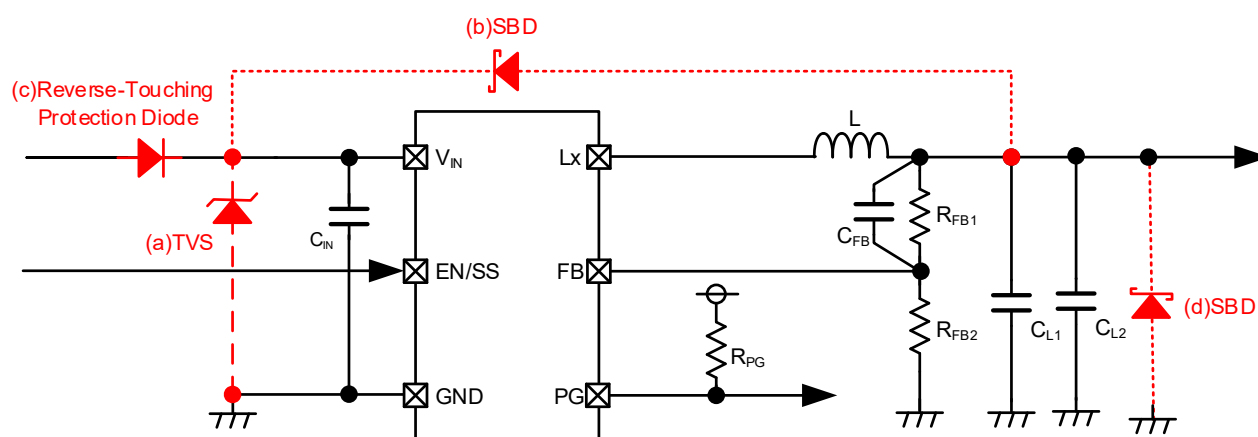
## ■NOTES ON USE

- 1) For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications. Also, if used under out of the recommended operating range, the IC may not operate normally or may cause deterioration.

If a voltage exceeding the absolute maximum voltage is applied to the IC due to chattering caused by a mechanical switch or an external surge voltage, please use a protection circuit as a countermeasure.

Please see the countermeasures from (a) to (d) shown below.

- (a) When voltage exceeding the absolute maximum ratings comes into the  $V_{IN}$  pin due to the transient change on the power line, there is a possibility that the IC breaks down in the end. To prevent such a failure, please add a TVS between  $V_{IN}$  and GND as a countermeasure.
- (b) When the input voltage decreases below the output voltage, there is a possibility that an overcurrent will flow in the IC's internal parasitic diode and exceed the absolute maximum rating of the  $Lx$  pin. If the current is pulled into the input side by the low impedance between  $V_{IN}$  and GND, then please add an SBD between  $V_{OUT}$  and  $V_{IN}$  as a countermeasure.
- (c) When a negative voltage is applied to the input voltage by a reverse connection or chattering, an overcurrent could flow in the IC's parasitic diode and damage the IC. Please add a reverse touching protection diode as a countermeasure.
- (d) When a sudden surge of electrical current travels along the  $V_{OUT}$  pin and GND due to a short-circuit, electrical resonance of circuit involving parasitic inductor of cable related to short circuit. An output capacitor ( $C_L$ ) and impedance such as  $V_{OUT}$  line generates a negative voltage exceeding the breakdown voltage and may damage the device. Please take measures such as adding an SBD between  $V_{OUT}$  and GND.



- 2) Switching regulators such as DC/DC converters generate spike noise and ripple voltage. The DC/DC converter characteristics depend greatly on the externally connected components such as coil inductance value, capacitor, board layout of peripheral components. Please refer to the specifications and standard circuit examples of each component when carefully considering which components to select.

## NOTES ON USE

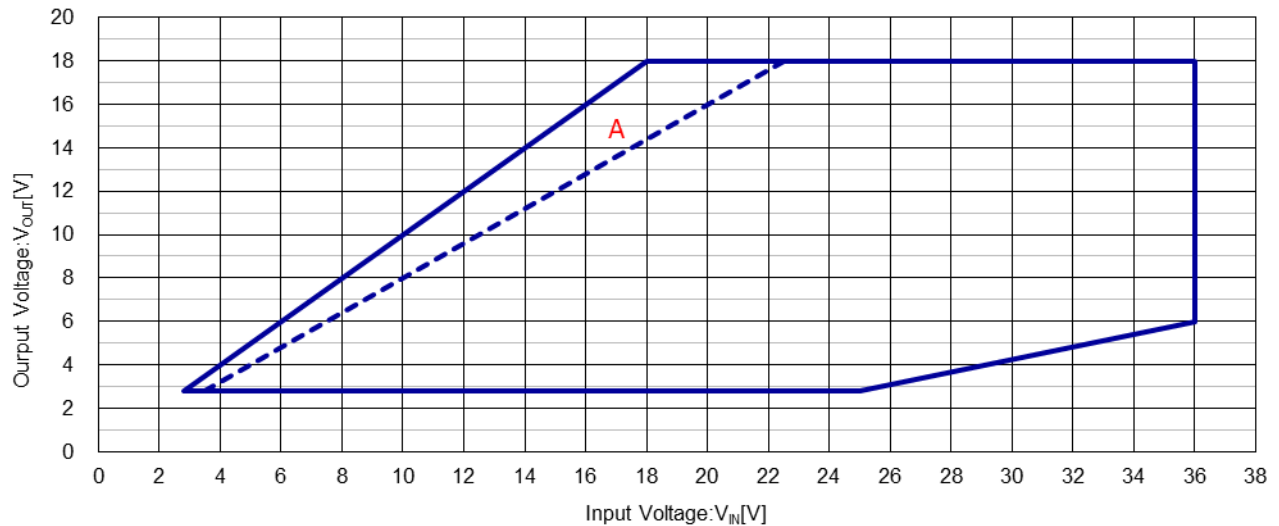
### 3) Stable operating range

The recommended operating range of this IC can operate normally varies depending on the product number.

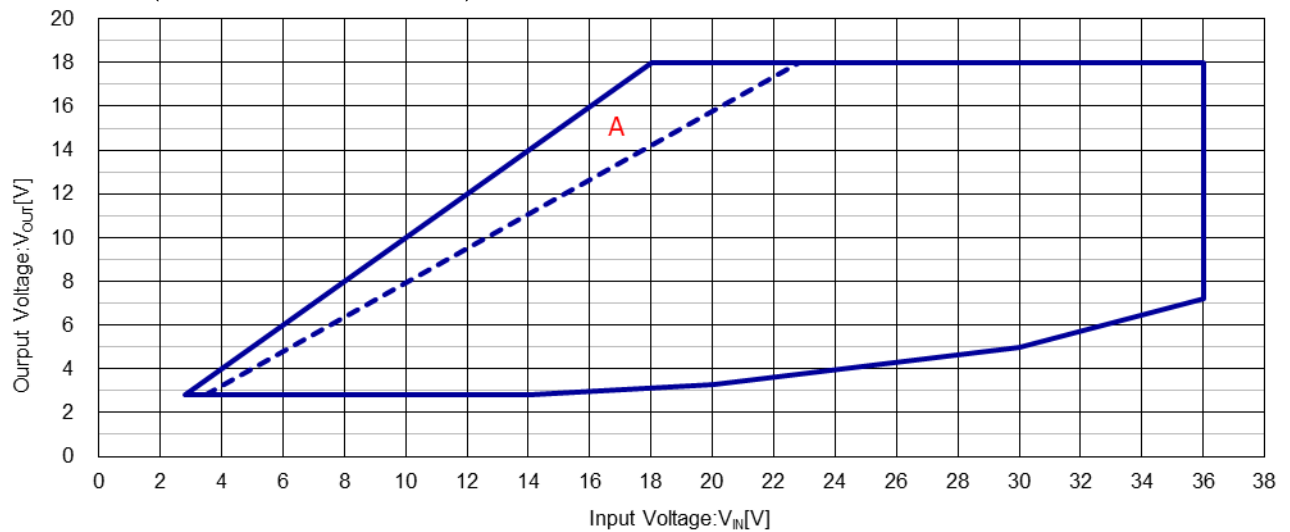
Please confirm that the power supply specifications you are using are within the recommended operating range before use.

#### $V_{OUTSET}-V_{IN}$ Stable operating range

XC9704B75C (F-PWM control,  $f_{osc}:1.2\text{MHz}$ )

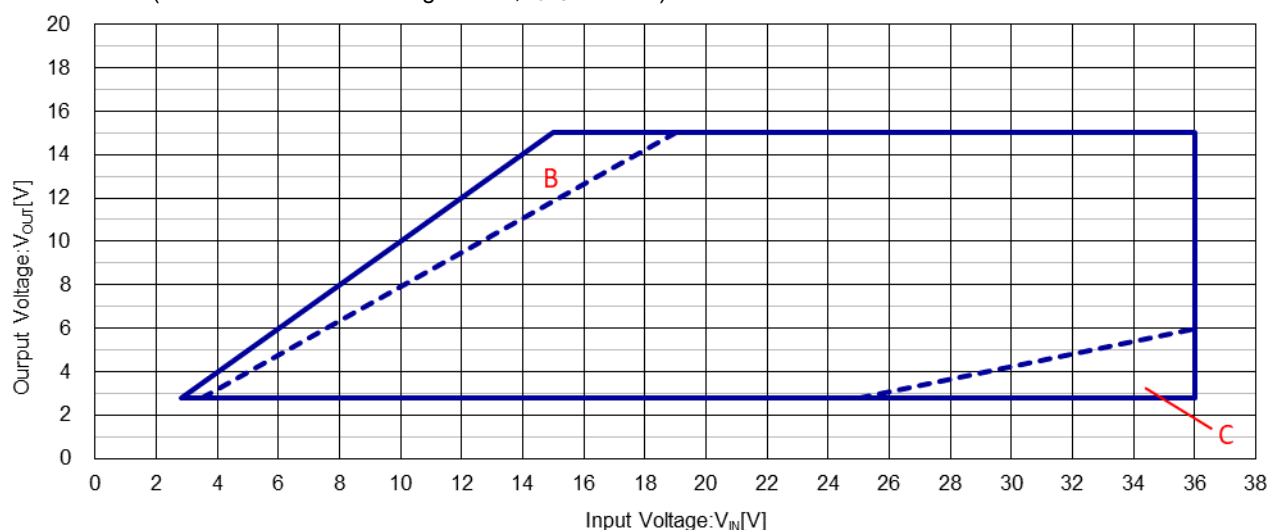


XC9704B75D (F-PWM control,  $f_{osc}:2.2\text{MHz}$ )

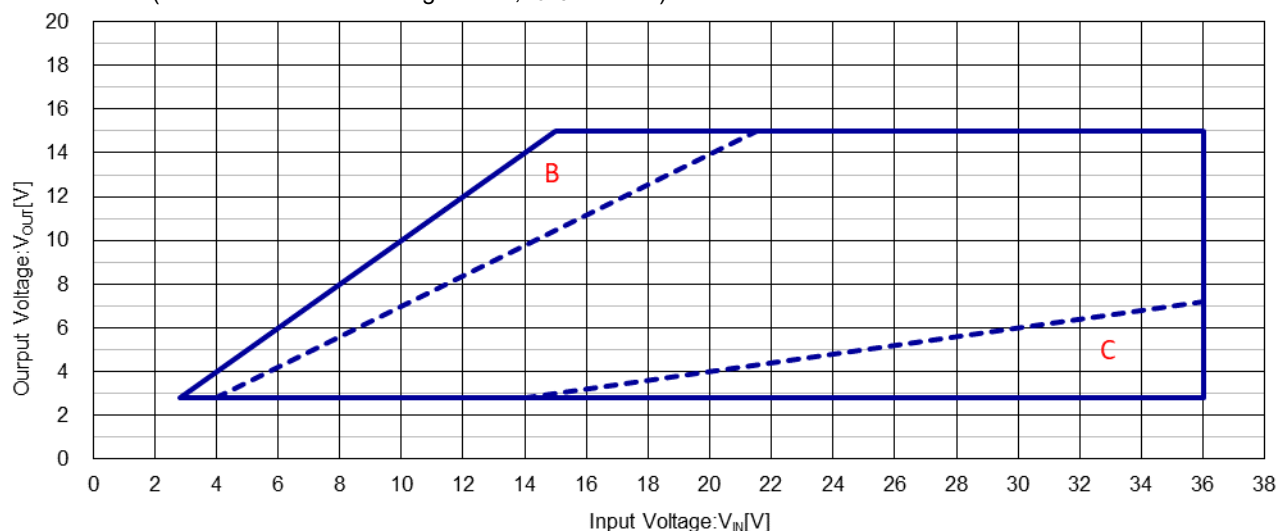


## ■NOTES ON USE

XC9705B75C (PWM/PFM Auto switching control,  $f_{osc}$ :1.2MHz)



XC9705B75D (PWM/PFM Auto switching control,  $f_{osc}$ :2.2MHz)



### 【Operation within the stable operating range】

Please note the following points when using in areas A to C within the stable operating range.

- (A) The switching frequency may drop or the  $V_{OUT}$  ripple voltage may increase near the switch to 100% Duty cycle.
- (B) The coil current may reserve, and the efficiency may drop significantly due to F-PWM operation instead of PFM operation at light loads. In addition, the switching frequency may drop and the  $V_{OUT}$  ripple voltage may increase near the switch to 100% Duty cycle.
- (C) Due to the Minimum On-time, the Lx oscillation may become unstable and the  $V_{OUT}$  ripple voltage may increase, or the IC may not switch to PWM operation up to the maximum output current.

### 【Operation over the stable operating range】

If the IC is used over the stable operating range, the following operations may occur, and the IC may not operate normally.

- (a) Under conditions where the step-down ratio is high, Lx oscillation may not be stable or pulse skipping may occur and the ripple voltage may increase, due to Minimum On-time.
- (b) Under conditions where the step-down ratio is low, the unit may operate at Maximum Duty Cycle and the output voltage may drop below the set output voltage.

## ■NOTES ON USE

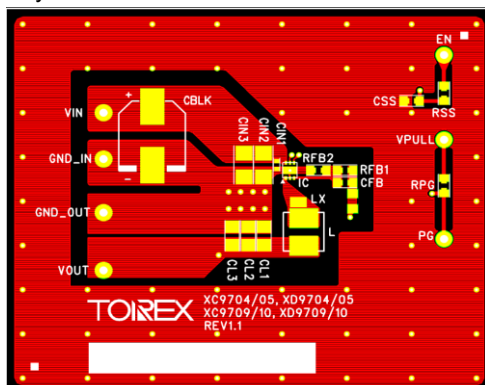
- 4) The ripple voltage could be increased when switching from discontinuous conduction mode to continuous conduction mode and when switching to 100% Duty cycle.
- 5) When using an external soft start using the EN/SS pin, if the EN/SS pin is at an intermediate voltage when the power is turned on, the external soft start will not work, and the inrush current will increase. etc.
- 6) The output overvoltage protection function suppresses output voltage overshoot, but on the other hand, it operates to suppress the operation of the error amplifier.  
Therefore, the output overvoltage protection function and the error amplifier may operate mutually, causing the output voltage to become unstable voltage. If the output overvoltage protection function operates and the output voltage is unstable due to sudden load fluctuations, etc., take measures such as increasing the output capacity.
- 7) Torex places an importance on improving our products and their reliability. We request that users incorporate fail safe designs and post aging protection treatment when using Torex products in their systems.
- 8) Instructions of pattern layouts  
Especially noted in the pattern layout are as follows.  
Please refer to the reference pattern layout on the next page.
  - (a) Wire the large current line using thick, short connecting traces.  
This makes it possible to reduce the wire impedance, which is expected to reduce noise and improve heat dissipation.  
If the wire impedance of the large current line is large, it may cause noise, or the IC cannot operate normally.
  - (b) Place the input capacitance  $C_{IN}$ , output capacitance  $C_L$ , inductor  $L$  and IC which the large current flows on the same surface.  
If they are placed on both sides, a large current will flow through Via which has high impedance, it may cause noise and the IC may not operate normally.
  - (c) Please mount each external component as close to the IC as possible.  
Especially place the input capacitance  $C_{IN}$  near the IC and connect it with as low impedance as possible.  
If the input capacity  $C_{IN}$  and IC are too far apart, it may cause noise, or the IC may not operate normally.
  - (d) The FB line connected to the FB pin is extremely sensitive to noise, so connect it with the shortest possible wire. If the FB line is long, the IC may not operate normally due to switching noise and external noise.  
If the IC does not operate normally due to external noise, etc., please review the board layout or adjust the value of FB resistance to low.  
If the FB resistance value is lowered, the efficiency during PFM operation may decrease. Please use it after confirming it with the actual machine.

## ■ NOTES ON USE

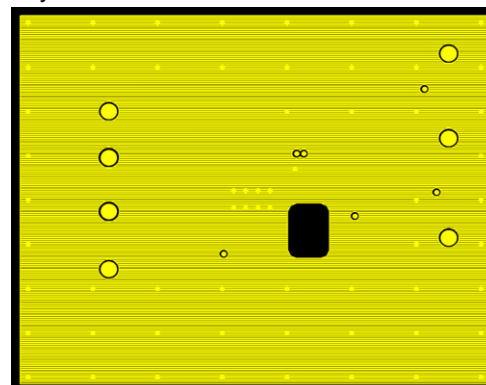
<Pattern layout>

### USP-6C

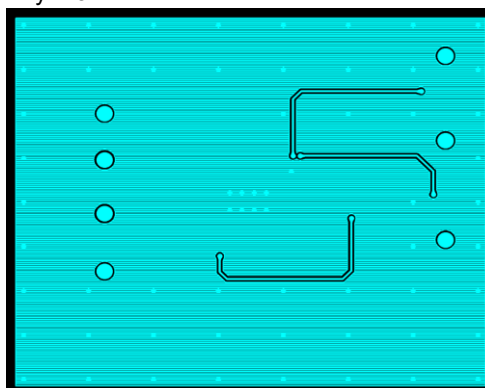
Layer 1



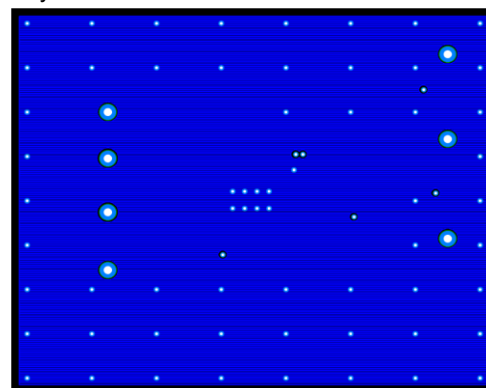
Layer 2



Layer 3

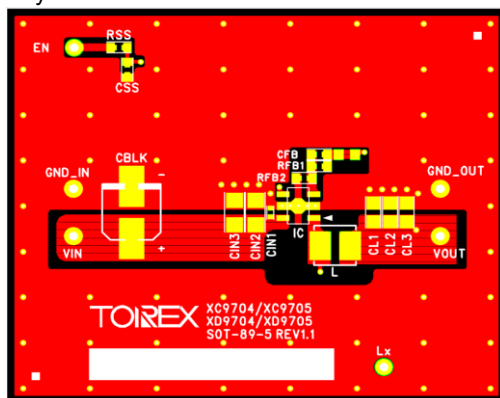


Layer 4

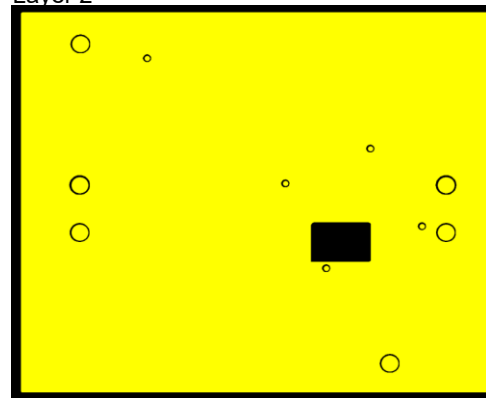


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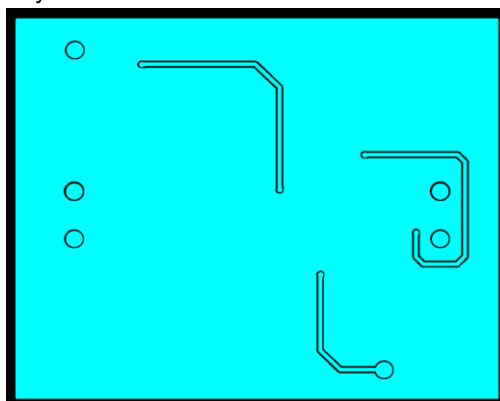
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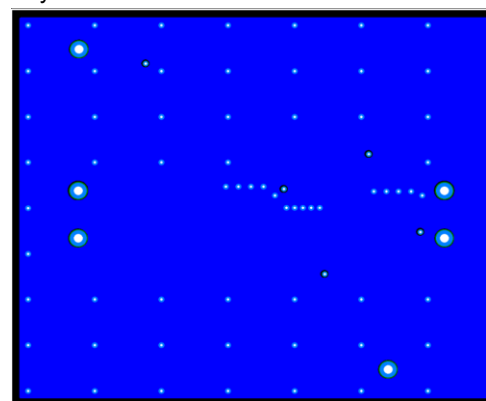
Layer 2



Layer 3



Layer 4



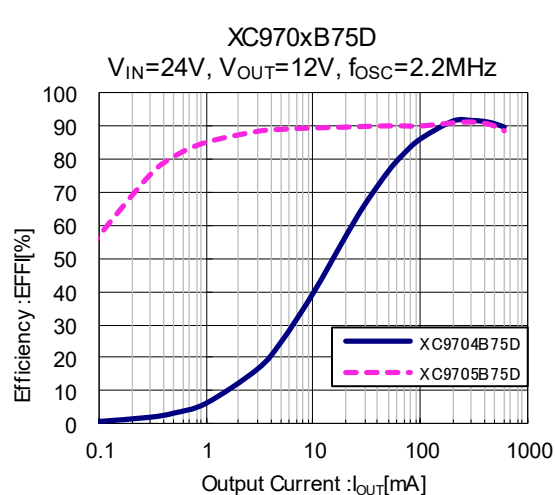
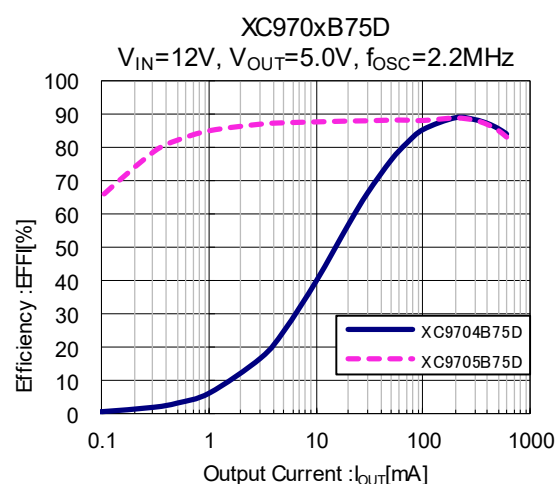
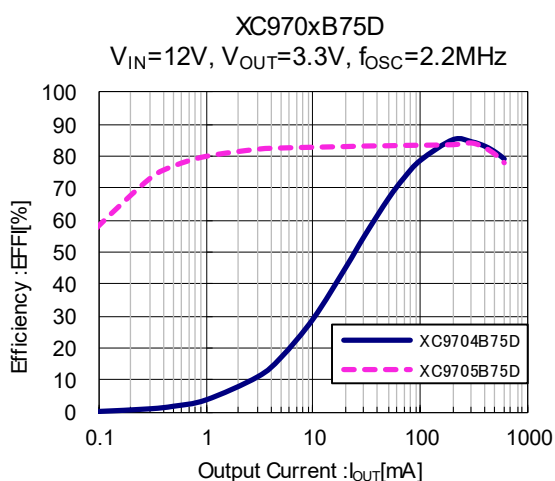
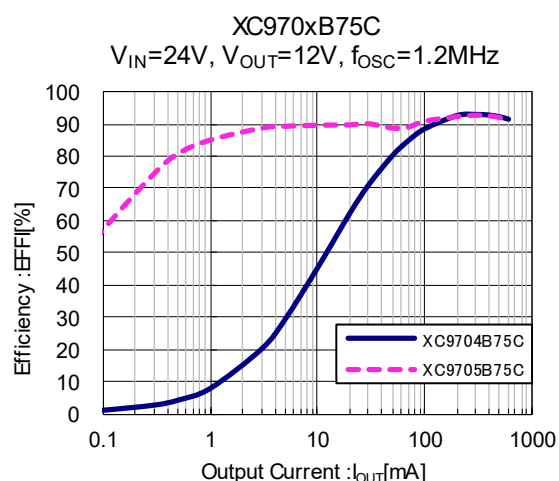
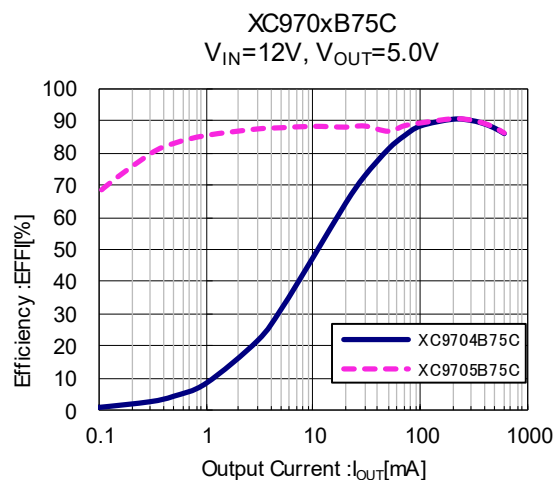
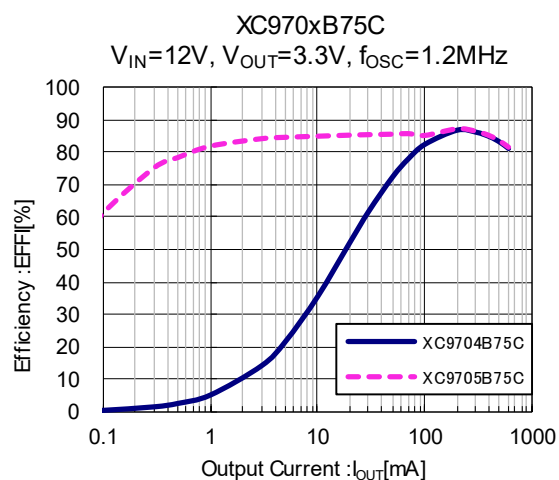
## TYPICAL PERFORMANCE CHARACTERISTICS

PRODUCTS	CONDITIONS	L	C <sub>IN</sub>	C <sub>L</sub>
XC9704B75C XC9705B75C (f <sub>osc</sub> =1.2MHz)	V <sub>IN</sub> =12V, V <sub>OUT</sub> =3.3V	4.7μH (CLF5030NIT-4R7N)	2.2μF (C2012X7R1H225K125AC)	10μF×2 (C2012X7R1A106K125AC)
	V <sub>IN</sub> =12V, V <sub>OUT</sub> =5.0V	6.8μH (CLF5030NIT-6R8N)	2.2μF (C2012X7R1H225K125AC)	10μF×2 (C2012X7R1A106K125AC)
	V <sub>IN</sub> =24V, V <sub>OUT</sub> =3.3V	4.7μH (CLF5030NIT-4R7N)	2.2μF (C2012X7R1H225K125AC)	22μF×2 (C3225X7R1C226M250AC)
	V <sub>IN</sub> =24V, V <sub>OUT</sub> =5.0V	6.8μH (CLF5030NIT-6R8N)	2.2μF (C2012X7R1H225K125AC)	22μF×2 (C3225X7R1C226M250AC)
	V <sub>IN</sub> =24V, V <sub>OUT</sub> =12V	10μH (CLF5030NIT-100N)	2.2μF (C2012X7R1H225K125AC)	22μF×2 (C3225X7R1C226M250AC)
XC9704B75D XC9705B75D (f <sub>osc</sub> =2.2MHz)	V <sub>IN</sub> =12V, V <sub>OUT</sub> =3.3V	2.2μH (CLF5030NIT-2R2N)	2.2μF (C2012X7R1H225K125AC)	10μF×2 (C2012X7R1A106K125AC)
	V <sub>IN</sub> =12V, V <sub>OUT</sub> =5.0V	3.3μH (CLF5030NIT-3R3N)	2.2μF (C2012X7R1H225K125AC)	10μF×2 (C2012X7R1A106K125AC)
	V <sub>IN</sub> =24V, V <sub>OUT</sub> =5.0V	3.3μH (CLF5030NIT-3R3N)	2.2μF (C2012X7R1H225K125AC)	10μF×2 (C2012X7R1A106K125AC)
	V <sub>IN</sub> =24V, V <sub>OUT</sub> =12V	4.7μH (CLF5030NIT-4R7N)	2.2μF (C2012X7R1H225K125AC)	10μF×2 (C3216X7R1E106K160AB)



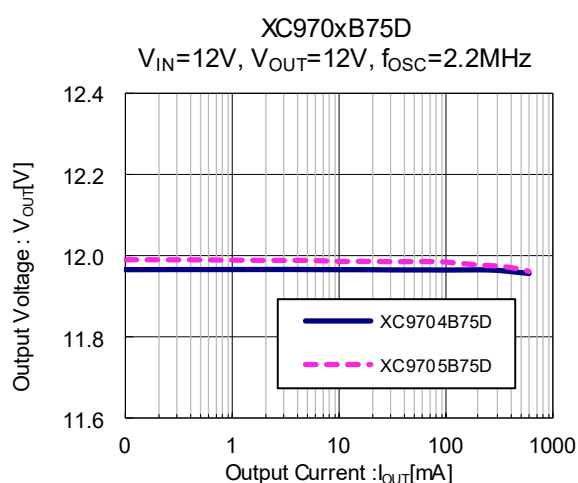
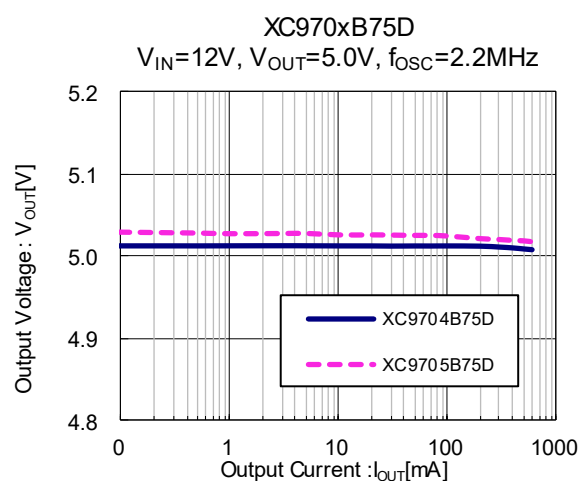
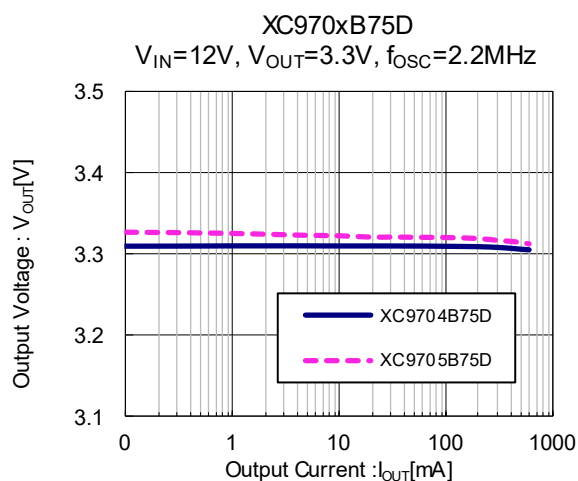
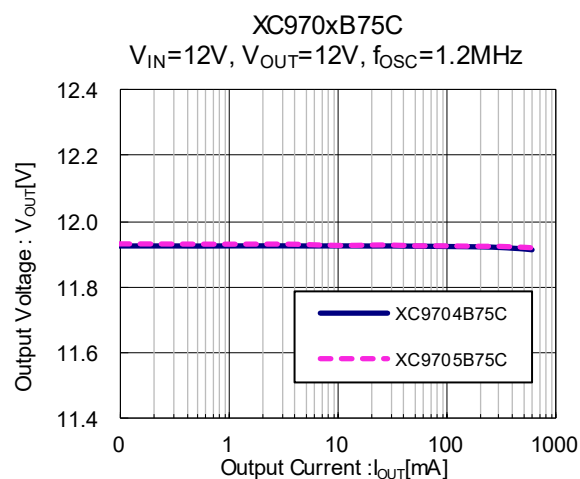
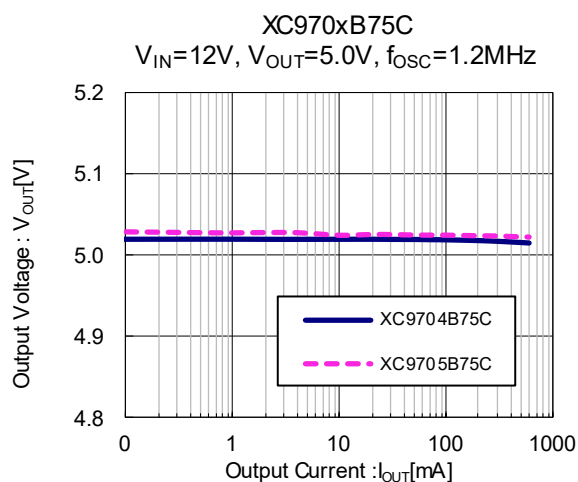
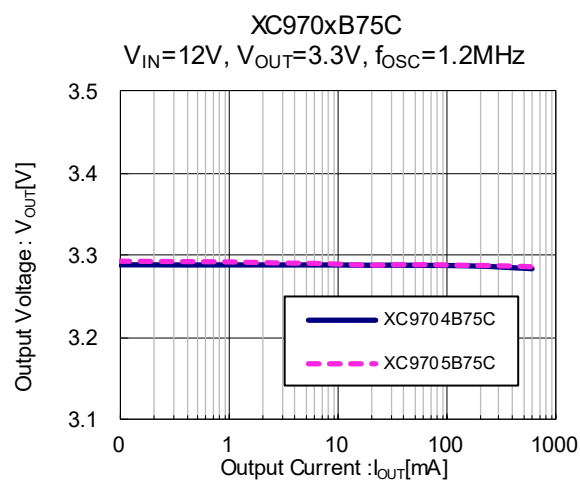
## ■ TYPICAL PERFORMANCE CHARACTERISTICS

### (1) Efficiency vs. Output current



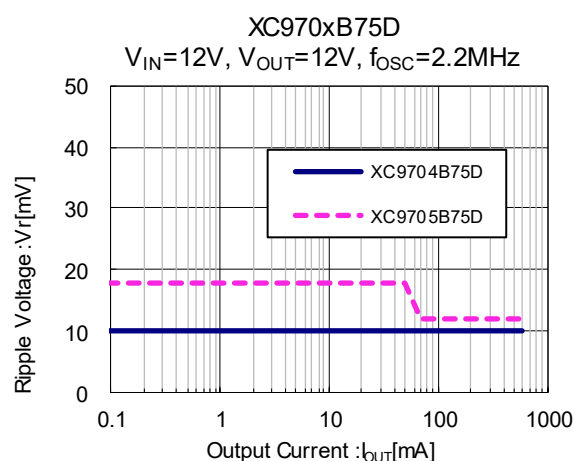
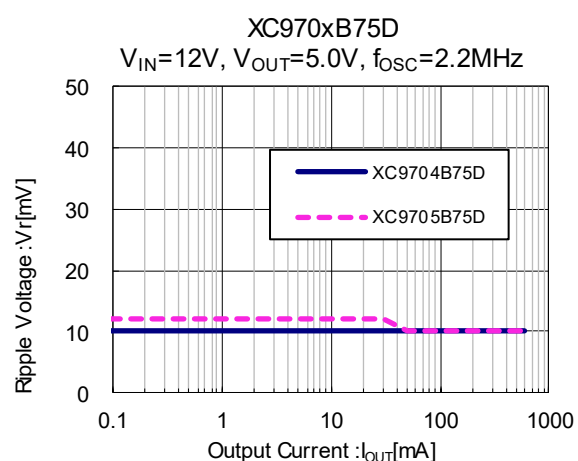
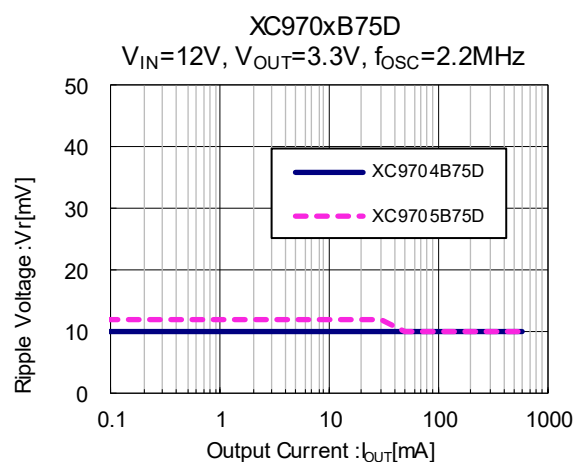
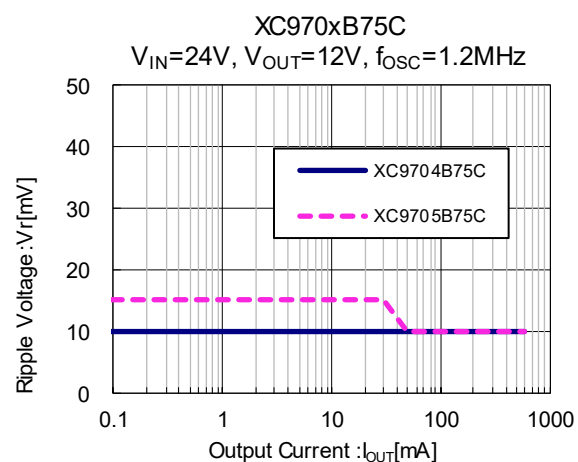
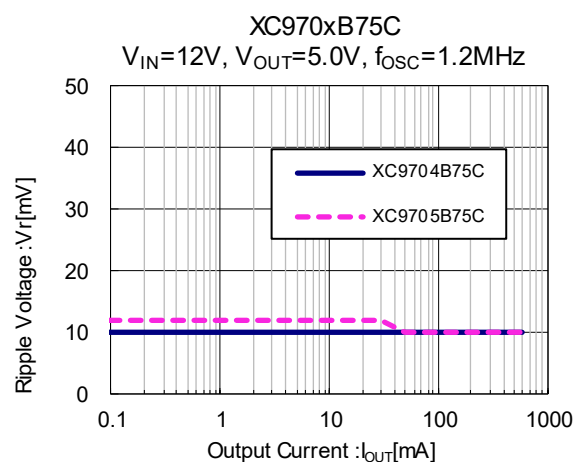
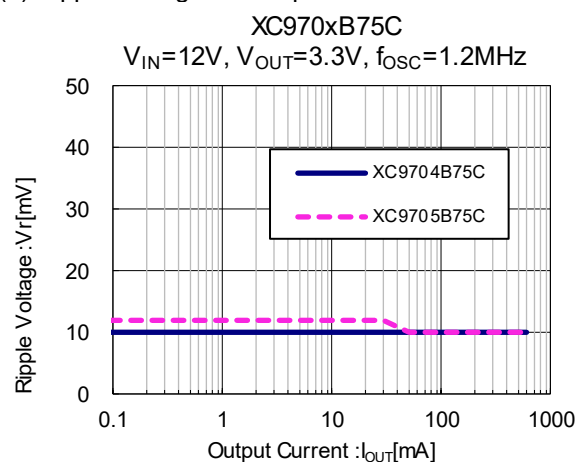
## TYPICAL PERFORMANCE CHARACTERISTICS

### (2) Output Voltage vs. Output Current



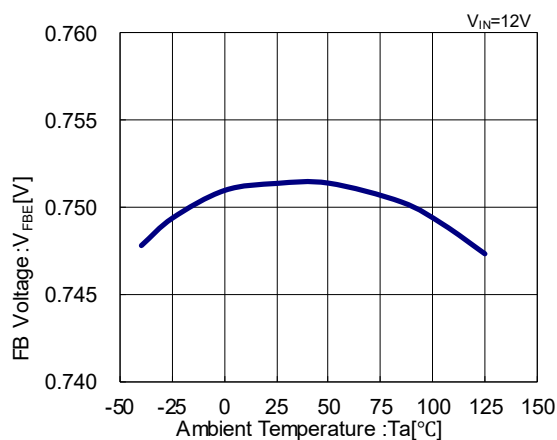
## ■ TYPICAL PERFORMANCE CHARACTERISTICS

### (3) Ripple Voltage vs. Output Current

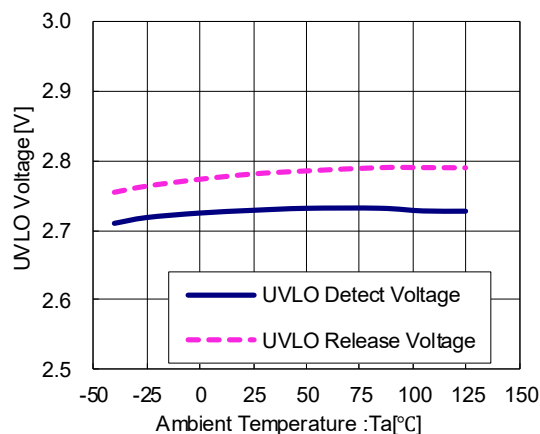


## TYPICAL PERFORMANCE CHARACTERISTICS

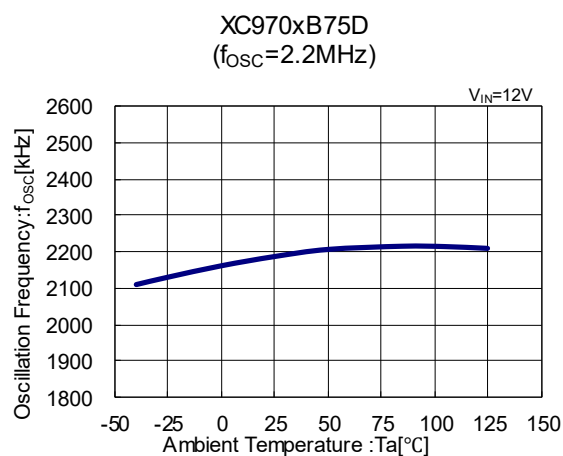
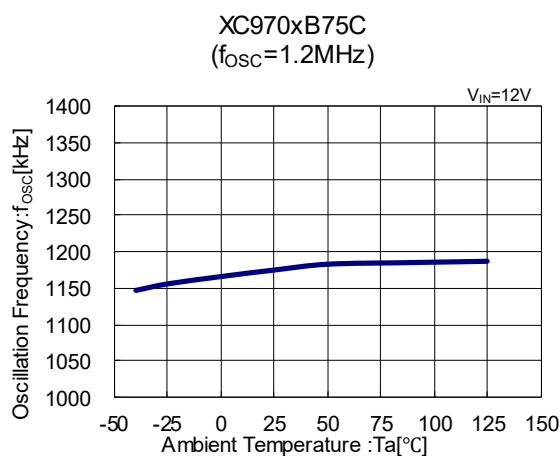
(4) FB Voltage vs. Ambient Temperature



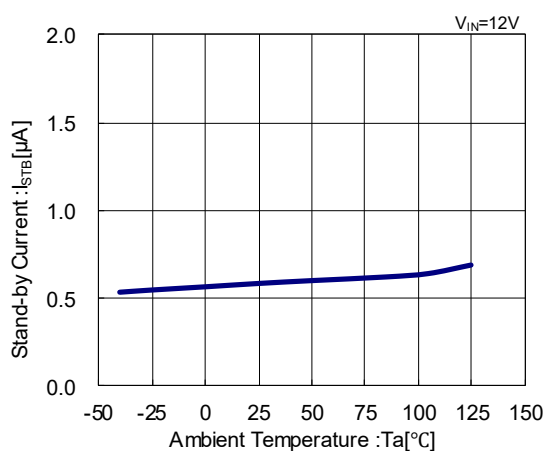
(5) UVLO Voltage vs. Ambient Temperature



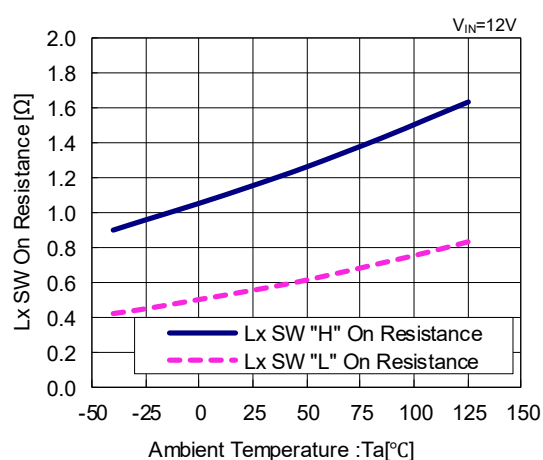
(6) Oscillation Frequency vs. Ambient Temperature



(7) Stand-by Current vs. Ambient Temperature

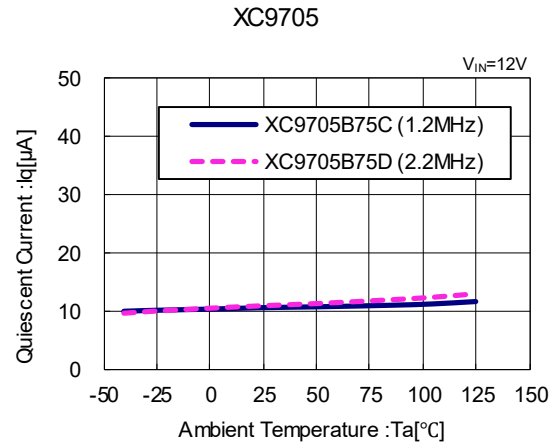
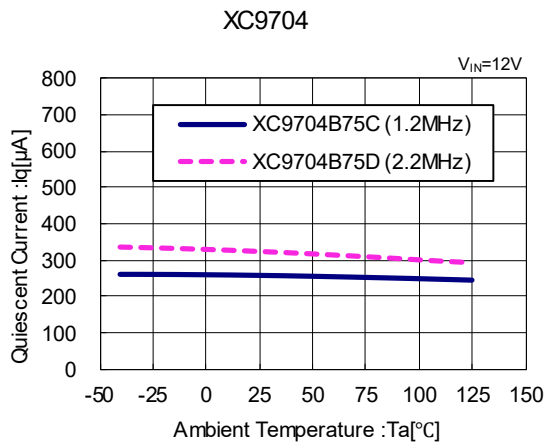


(8) Lx SW On Resistance vs. Ambient Temperature

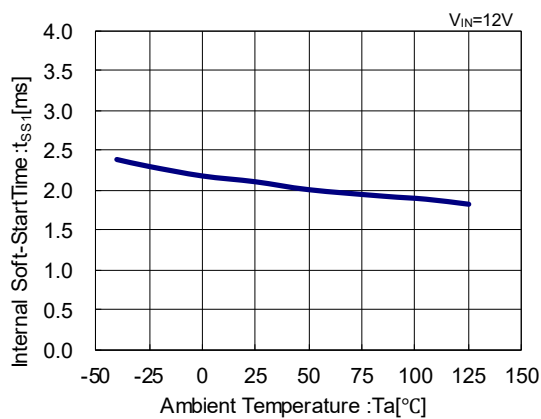


## ■ TYPICAL PERFORMANCE CHARACTERISTICS

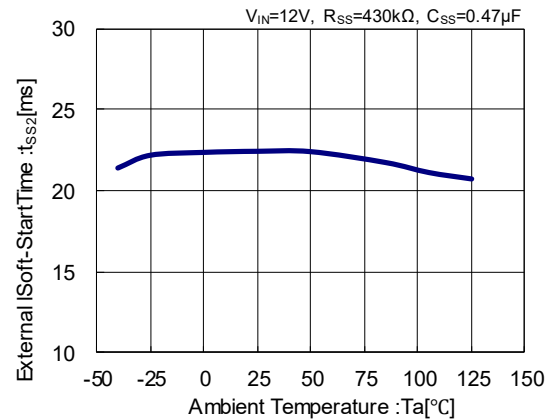
(9) Quiescent Current vs. Ambient Temperature



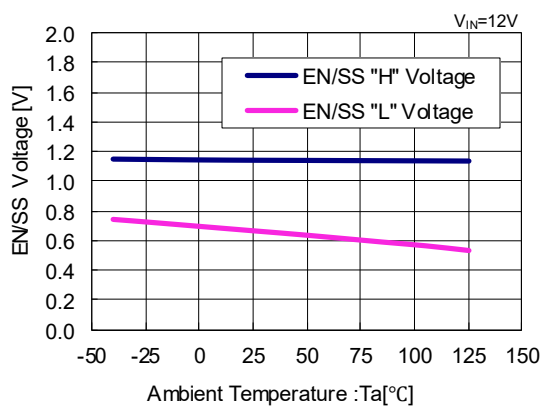
(10) Internal Soft-Start Time vs. Ambient Temperature



(11) External Soft-Start Time vs. Ambient Temperature

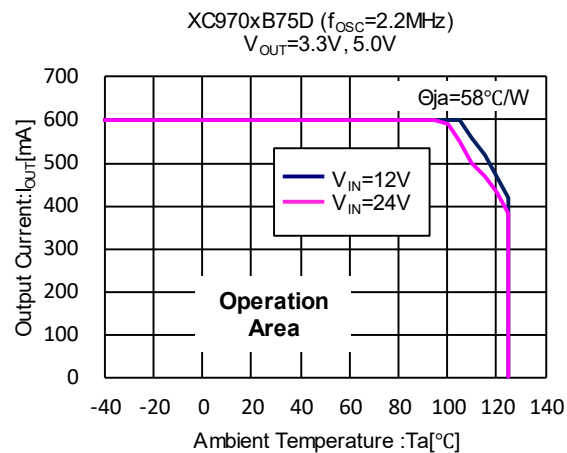
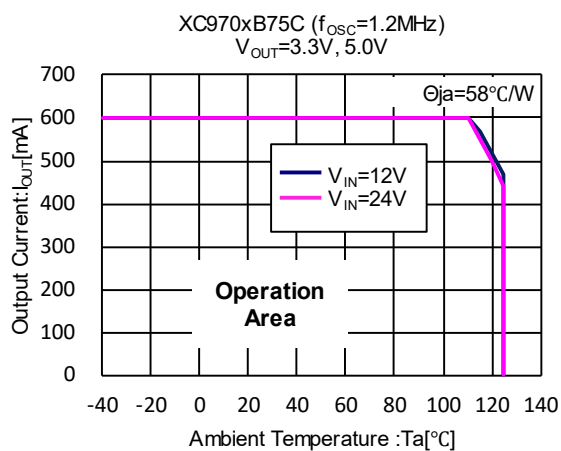


(12) EN/SS Voltage vs. Ambient Temperature

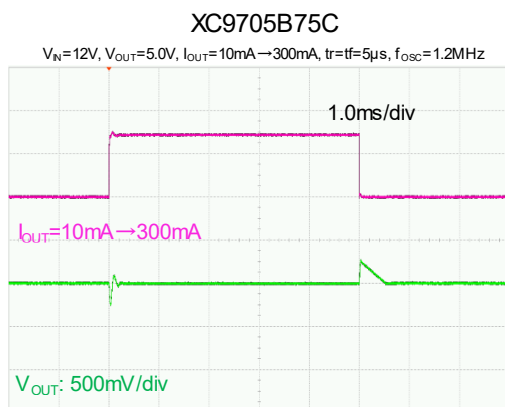
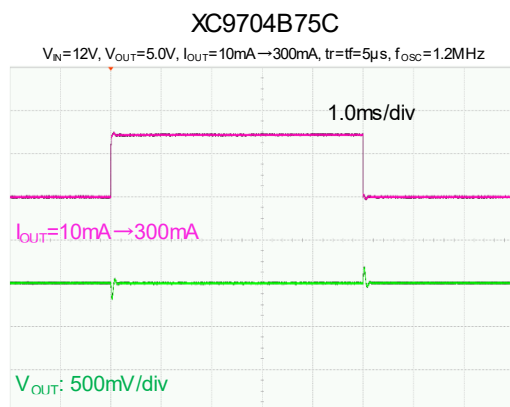
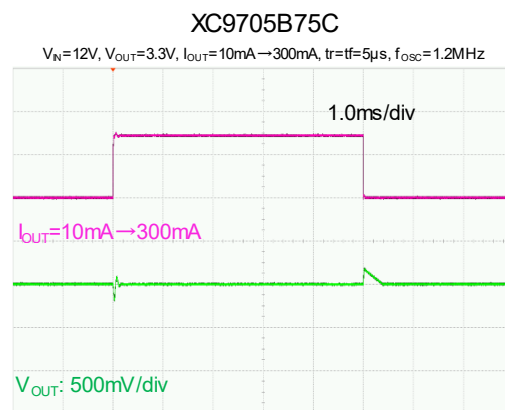
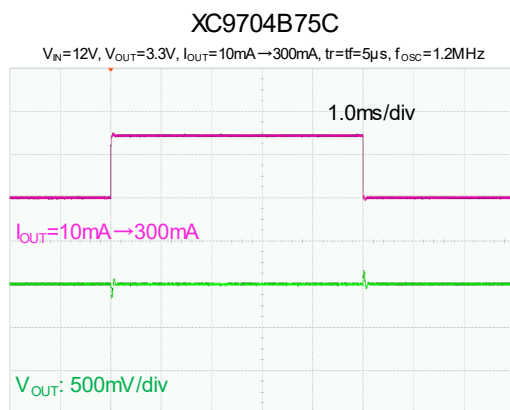


## TYPICAL PERFORMANCE CHARACTERISTICS

### (14) Output Current Operation Area



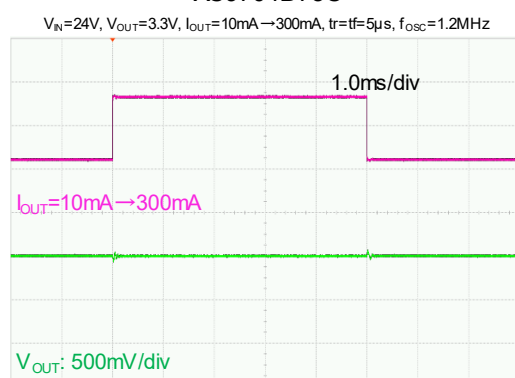
### (15) Load Transient Response



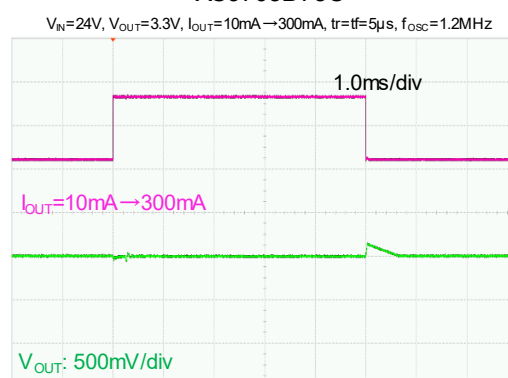
## ■ TYPICAL PERFORMANCE CHARACTERISTICS

### (15) Load Transient Response

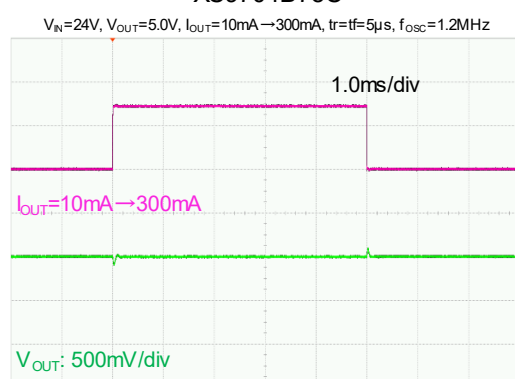
**XC9704B75C**



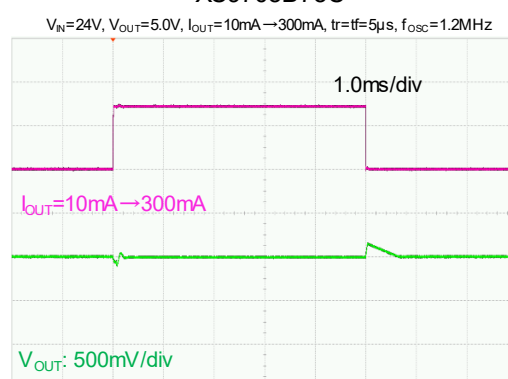
**XC9705B75C**



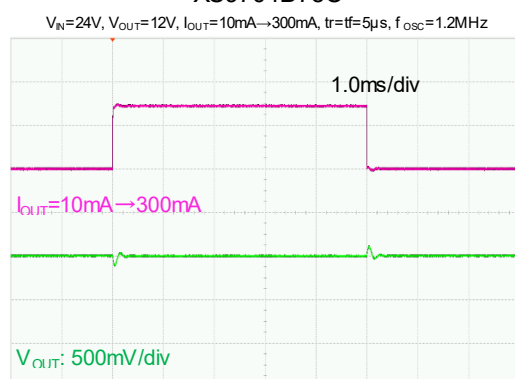
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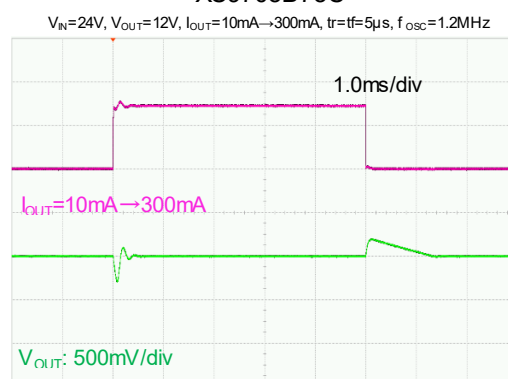
**XC9705B75C**



**XC9704B75C**



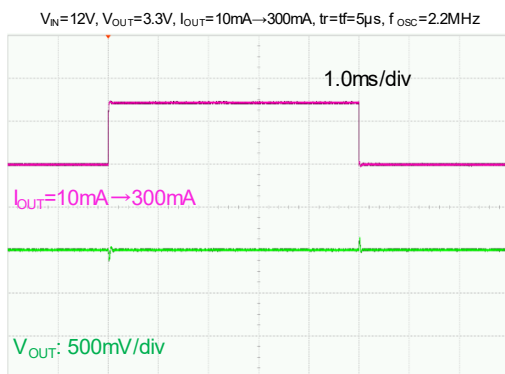
**XC9705B75C**



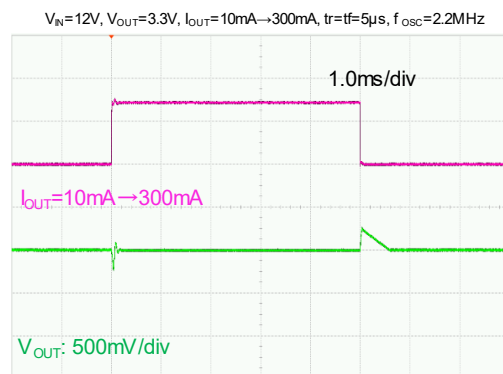
## TYPICAL PERFORMANCE CHARACTERISTICS

### (15) Load Transient Response

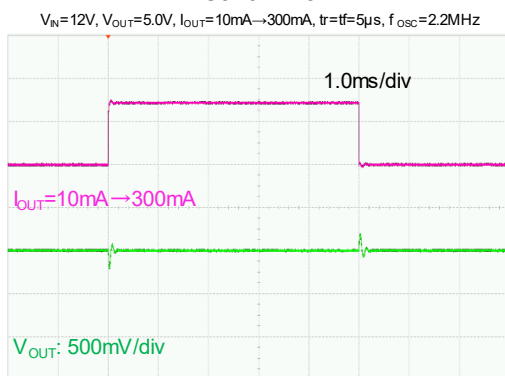
#### XC9704B75D



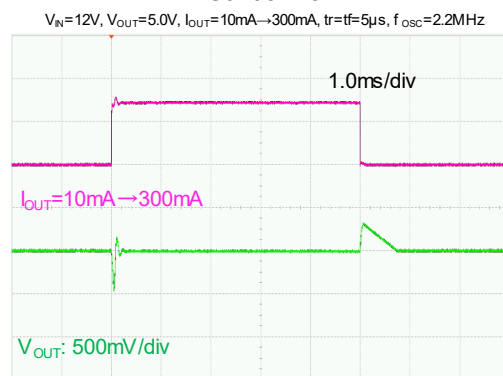
#### XC9705B75D



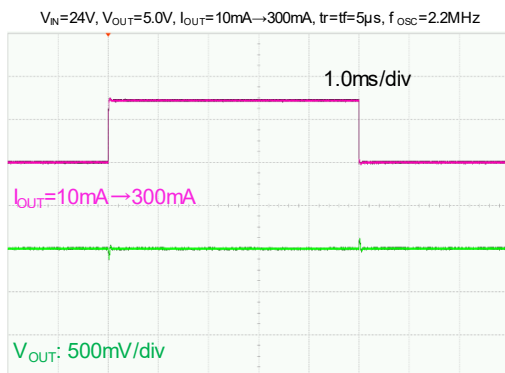
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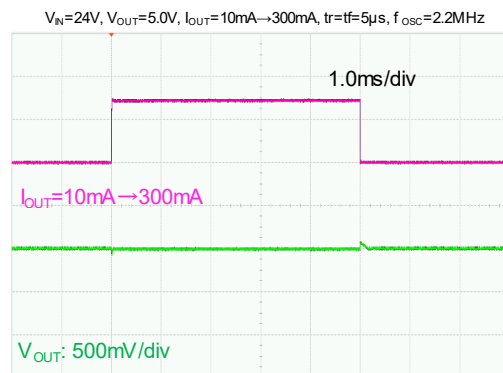
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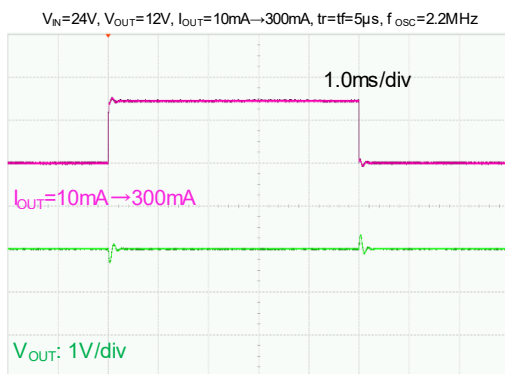
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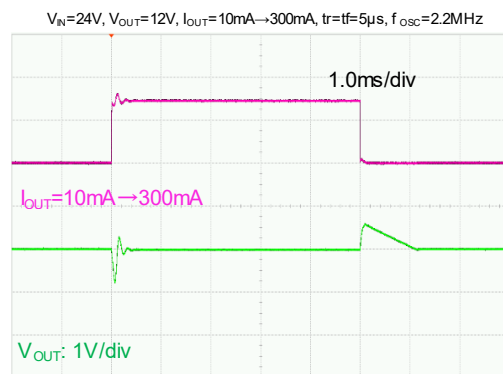
#### XC9705B75D



#### XC9704B75D



#### XC9705B75D



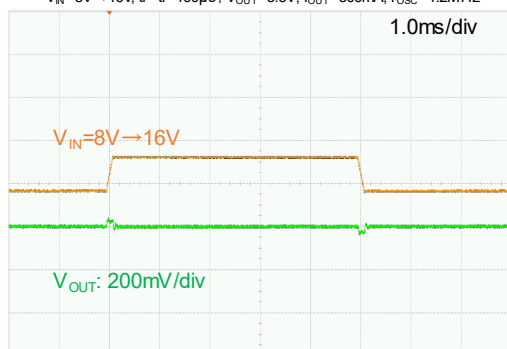


## ■ TYPICAL PERFORMANCE CHARACTERISTICS

### (16) Input Transient Response

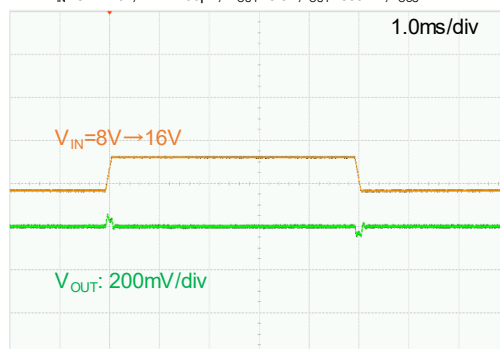
**XC9704B75C**

$V_{IN}=8V \rightarrow 16V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=3.3V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=1.2MHz$



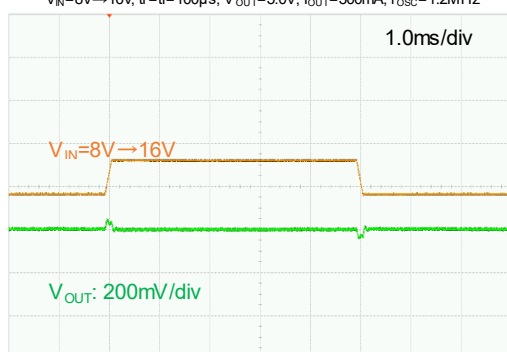
**XC9705B75C**

$V_{IN}=8V \rightarrow 16V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=3.3V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=1.2MHz$



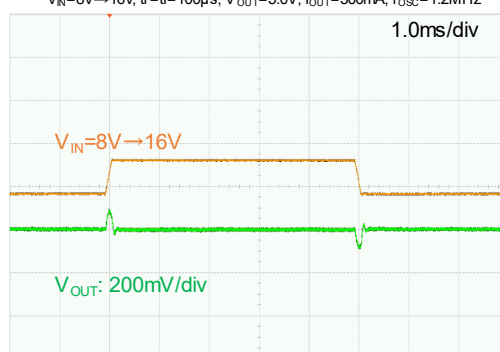
**XC9704B75C**

$V_{IN}=8V \rightarrow 16V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=5.0V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=1.2MHz$



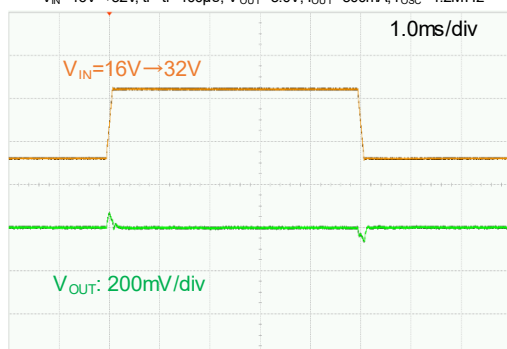
**XC9705B75C**

$V_{IN}=8V \rightarrow 16V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=5.0V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=1.2MHz$



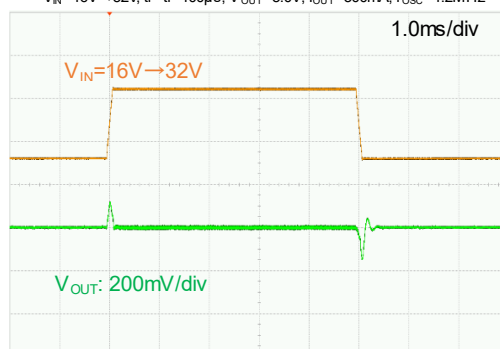
**XC9704B75C**

$V_{IN}=16V \rightarrow 32V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=5.0V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=1.2MHz$



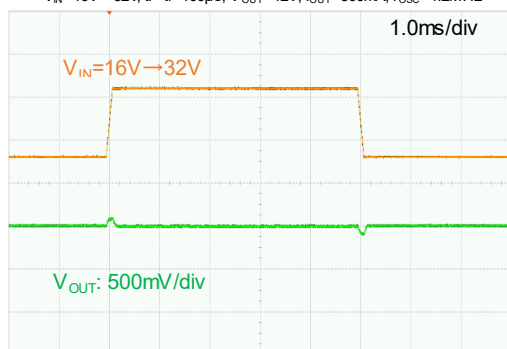
**XC9705B75C**

$V_{IN}=16V \rightarrow 32V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=5.0V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=1.2MHz$



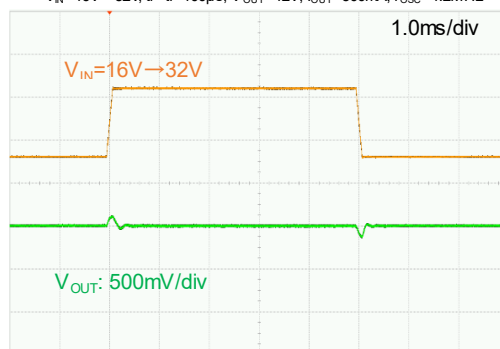
**XC9704B75C**

$V_{IN}=16V \rightarrow 32V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=12V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=1.2MHz$



**XC9705B75C**

$V_{IN}=16V \rightarrow 32V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=12V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=1.2MHz$

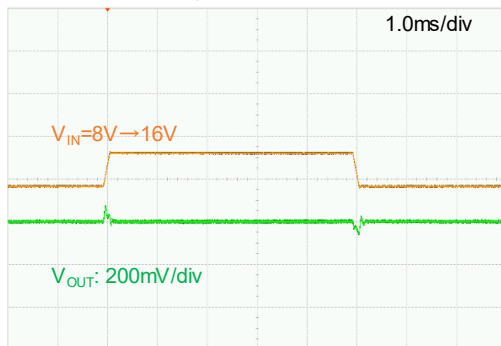


## TYPICAL PERFORMANCE CHARACTERISTICS

### (16) Input Transient Response

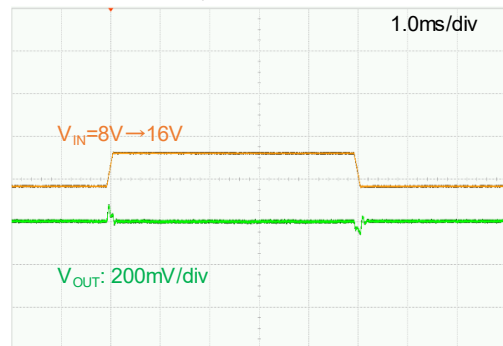
#### XC9704B75D

$V_{IN}=8V \rightarrow 16V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=3.3V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=2.2MHz$



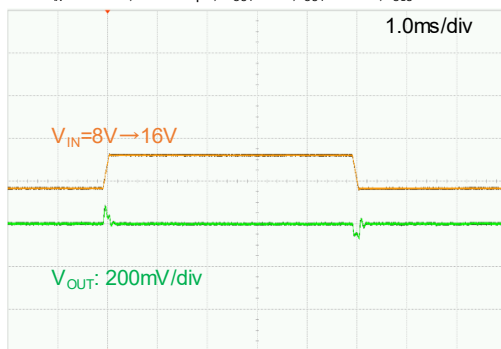
#### XC9705B75D

$V_{IN}=8V \rightarrow 16V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=3.3V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=2.2MHz$



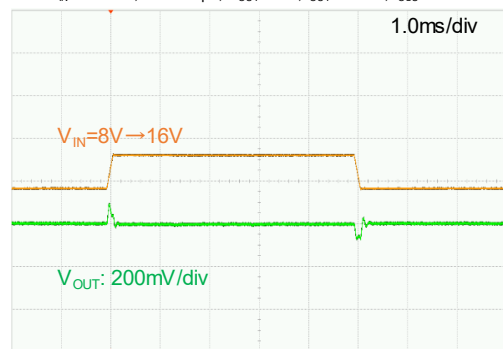
#### XC9704B75D

$V_{IN}=8V \rightarrow 16V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=5.0V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=2.2MHz$



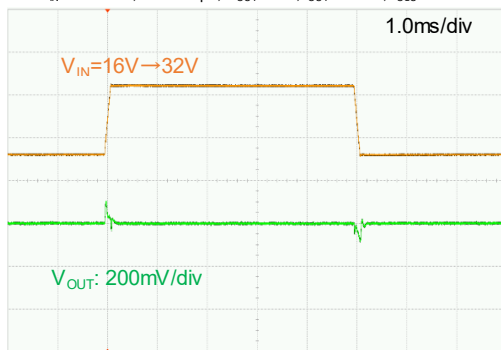
#### XC9705B75D

$V_{IN}=8V \rightarrow 16V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=5.0V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=2.2MHz$



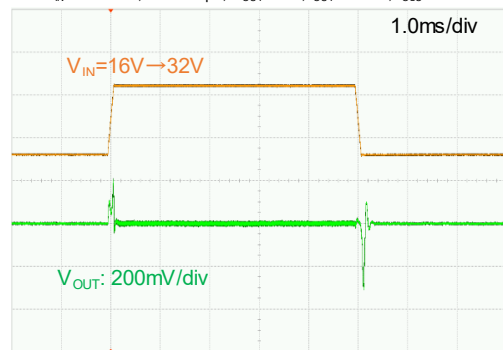
#### XC9704B75D

$V_{IN}=16V \rightarrow 32V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=5.0V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=2.2MHz$



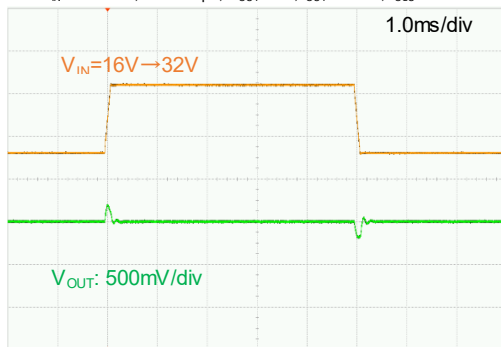
#### XC9705B75D

$V_{IN}=16V \rightarrow 32V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=5.0V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=2.2MHz$



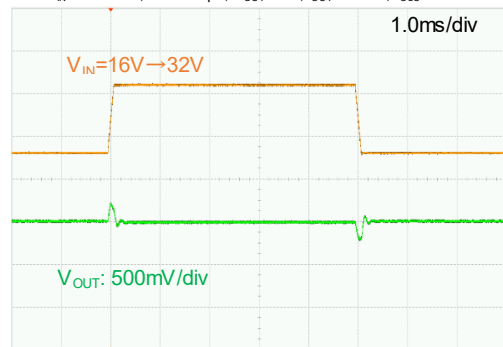
#### XC9704B75D

$V_{IN}=16V \rightarrow 32V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=12V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=2.2MHz$



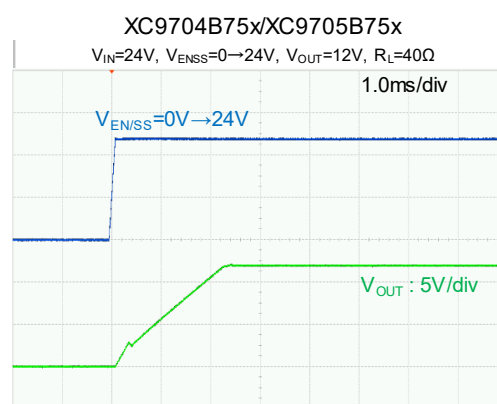
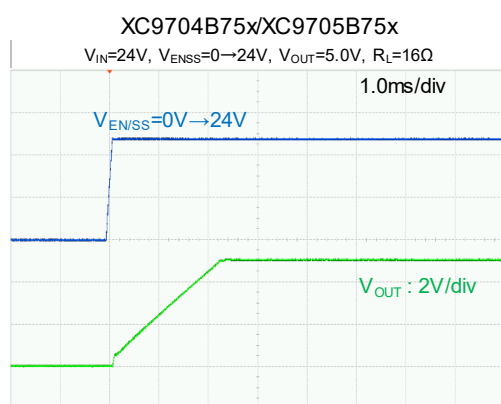
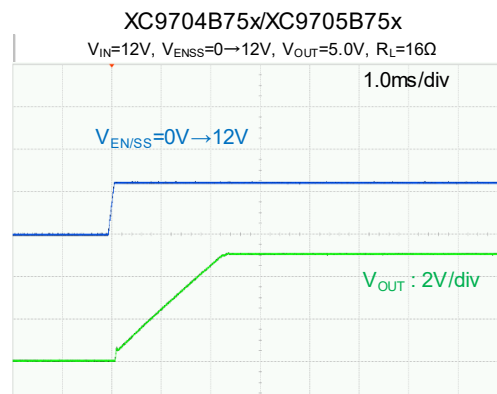
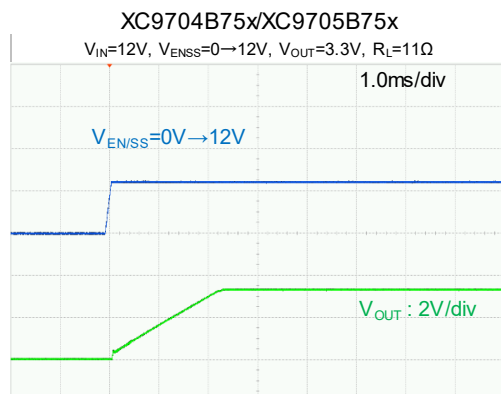
#### XC9705B75D

$V_{IN}=16V \rightarrow 32V$ ,  $t_r=t_f=100\mu s$ ,  $V_{OUT}=12V$ ,  $I_{OUT}=300mA$ ,  $f_{OSC}=2.2MHz$

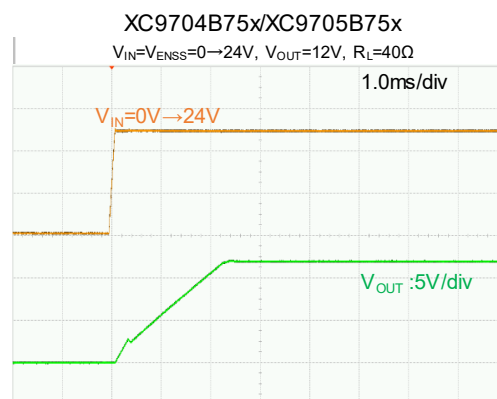
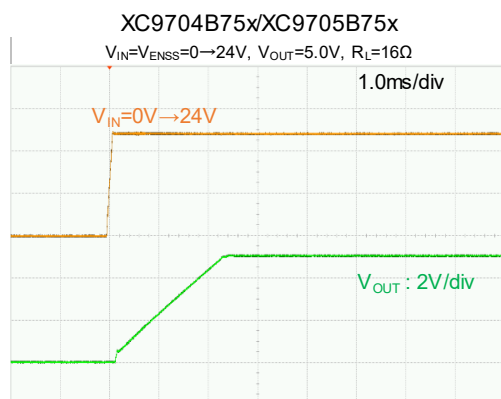
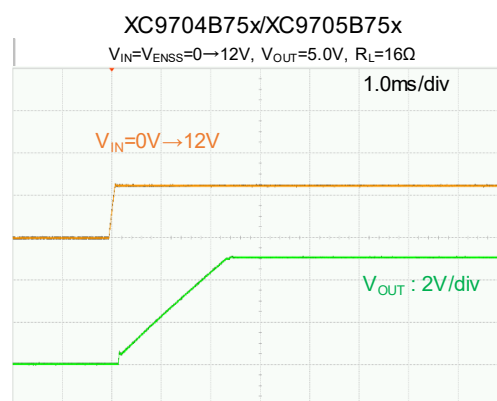
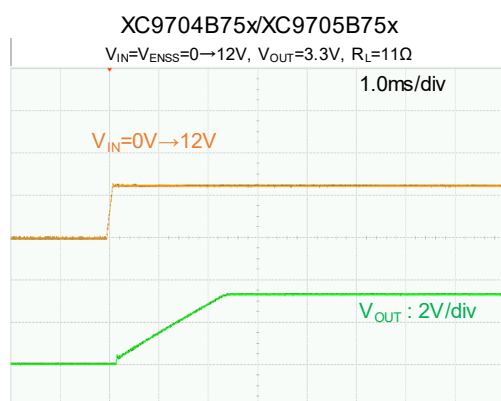


## ■ TYPICAL PERFORMANCE CHARACTERISTICS

### (17) Start-up Waveform (EN/SS Rising)



### (18) Start-up Waveform ( $V_{IN}$ Rising)



## ■ PACKAGING INFORMATION

For the latest package information go to, [www.torexsemi.com/technical-support/packages](http://www.torexsemi.com/technical-support/packages)

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
SOT-89-5	<a href="#">SOT-89-5 PKG</a>	<a href="#">SOT-89-5 Power Dissipation</a>
USP-6C	<a href="#">USP-6C PKG</a>	<a href="#">USP-6C Power Dissipation</a>

■

MARKING RULE

①,② represents products series

MARK		PRODUCT SERIES
①	②	
1	L	XC9704B75***-G
	M	XC9705B75***-G

③ represents type, Oscillation Frequency,

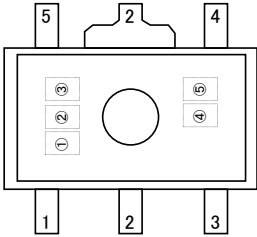
MARK	Oscillation Frequency	PRODUCT SERIES
A	1.2MHz	XC970*B75C**-G
B	2.2MHz	XC970*B75D**-G

④ ⑤ represents production lot number

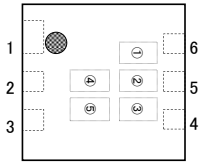
01~09, 0A~0Z, 11~9Z, A1~A9, AA~AZ, B1~ZZ in order. (G, I, J, O, Q, W excluded)

\* No character inversion used.

SOT-89-5



USP-6C



1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.
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