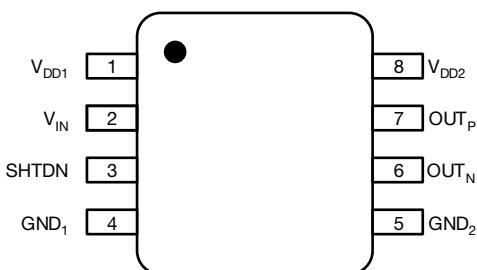


## High Reliability Reinforced Isolated Amplifier



### LINKS TO ADDITIONAL RESOURCES


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[Application Notes](#)

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[Design Tools](#)

### AGENCY APPROVALS

- UL
- cUL
- DIN EN 60747-5-5 (VDE 0884-5)
- CQC

### DESCRIPTION

VIA2000SD is a high performance differential output isolation amplifier suited for high precision isolated voltage sensing. The device is based on proprietary capacitive isolation technology and has a single-ended input signal range from 0.02 V to 2 V. The device has a high input impedance making it suitable for measurements across HV potential dividers. The devices unmatched CMTI of 100 kV/μs min. allows accurate measurements in the noisy environment.

### FEATURES

- Isolation test voltage: 5000 V<sub>RMS</sub>
- Fixed gain: 1
- Low offset error and drift: ± 1.5 mV (max.), -5 μV/°C to +30 μV/°C
- Low gain error and drift: ± 0.3 % (max.), ± 45 ppm/°C (max.)
- Low non-linearity and drift: ± 0.05 % (max.), ± 1 ppm/°C (typ.)
- SNR: 70 dB (typ., BW = 100 kHz)
- Wide bandwidth: 400 kHz (typ.)
- High CMTI: 150 kV/μs typ.
- Inbuilt V<sub>DD1</sub> monitoring
- Operating temperature: -40 °C to +125°C
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
**HALOGEN**  
**FREE**  
**GREEN**  
(5-2008)

### APPLICATIONS

- Bus voltage monitoring
- AC motor controls
- Power and solar inverters
- Uninterruptible power suppliers

#### Note

- For automotive qualification please contact our local sales.

DEVICE INFORMATION		
PART NUMBER	PACKAGE	BODY SIZE
VIA2000SD	SOP-8 (300 mil)	5.85 mm x 7.50 mm

ORDERING INFORMATION							
PART NUMBER	ISOLATION RATING (kV)	LINEAR INPUT RANGE (mV)	MOISTURE SENSITIVITY LEVEL	TEMPERATURE (°C)	AUTOMOTIVE	PACKAGE TYPE	SPQ
VIA2000SD	5	100 to 2000	Level 3	-40 to +125	No	SOP-8 (300 mil)	1000

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_{amb} = 25^{\circ}C$ , unless otherwise specified)			
PARAMETER	SYMBOL	VALUE	UNIT
Power supply voltage	$V_{DD1}, V_{DD2}$	-0.3 to 6.5	V
Input voltage	$V_{IN}$	GND <sub>1-6</sub> to $V_{DD1+0.5}$	V
	SHTDN	GND <sub>1-0.5</sub> to $V_{DD1+0.5}$	V
Output voltage	$OUT_P, OUT_N$	GND <sub>2-0.5</sub> to $V_{DD2+0.5}$	V
Output current per output pin	$I_O$	-10 to +10	mA
Operating temperature	$T_{amb}$	-40 to +125	$^{\circ}C$
Junction temperature	$T_j$	-40 to +150	$^{\circ}C$
Storage temperature	$T_{stg}$	-55 to +150	$^{\circ}C$
Electrostatic discharge	HBM <sup>(1)</sup>	$\pm 2000$	V
	CDM <sup>(2)</sup>	$\pm 1000$	V

**Notes**

(1) Human body model (HBM), per AEC-Q100-002-RevD  
(2) Charged device model (CDM), per AEC-Q100-011-RevB

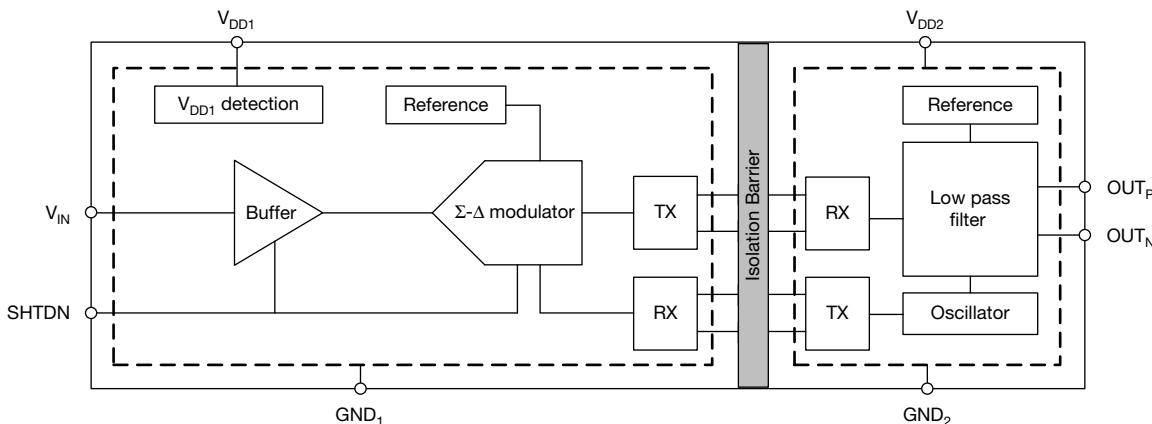
**FUNCTIONAL BLOCK DIAGRAM**


Fig. 1 - VIA2000SD Block Diagram

<b>RECOMMENDED OPERATING CONDITIONS</b> ( $T_{amb} = 25^{\circ}C$ , unless otherwise specified)						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Side 1 power supply	$V_{DD1}$	3.0	5.0	5.5	V	
Side 2 power supply	$V_{DD2}$	3.0	3.3	5.5	V	
VIA2000SD	Differential input voltage before clipping output	$V_{clipping}$	-	2.56	-	V
	Linear differential input full scale voltage	$V_{FSR}$	0.02	-	2	V
	Digital input voltage	SHTDN	GND <sub>1</sub>	-	$V_{DD1}$	
Operating ambient temperature	$T_{amb}$	-40	-	+125	$^{\circ}C$	

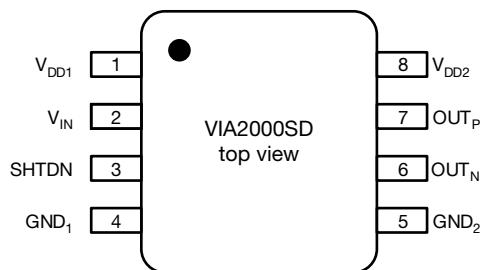
**PIN CONFIGURATION AND FUNCTIONS**


Fig. 2 - VIA2000SD Package

PIN CONFIGURATION AND DESCRIPTION		
PIN NO.	SYMBOL	FUNCTION
1	$V_{DD1}$	Power supply for isolator side 1 (3.0 V to 5.5 V)
2	$V_{IN}$	Analog input
3	SHTDN	Shutdown input, active high, pulled up internally (typical resistor value: 100 k $\Omega$ )
4	$GND_1$	Ground 1, the ground reference for isolator side 1
5	$GND_2$	Ground 2, the ground reference for isolator side 2
6	$OUT_N$	Negative output
7	$OUT_P$	Positive output
8	$V_{DD2}$	Power supply for isolator side 2 (3.0 V to 5.5 V)

<b>ELECTRICAL CHARACTERISTICS: VIA2000SD</b> ( $V_{DD1}, V_{DD2} = 3 \text{ V to } 5.5 \text{ V}$ , $V_{IN} = 0.1 \text{ V to } 2 \text{ V}$ , and $SHTDN = GND_1 = 0 \text{ V}$ , $T_{amb} = -40 \text{ }^{\circ}\text{C} \text{ to } +125 \text{ }^{\circ}\text{C}$ ) ( $V_{DD1} = 5 \text{ V}$ , $V_{DD2} = 3.3 \text{ V}$ , $T_{amb} = 25 \text{ }^{\circ}\text{C}$ , unless otherwise noted)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>POWER SUPPLY</b>						
Side 1 supply voltage		$V_{DD1}$	3.0	5.0	5.5	V
Side 2 supply voltage		$V_{DD2}$	3.0	3.3	5.5	V
Side 1 supply current	SHTDN = low	$I_{DD1}$	-	11.4	15.1	mA
	SHTDN = high		-	1	-	μA
Side 2 supply current		$I_{DD2}$	-	6.3	8.4	mA
$V_{DD1}$ undervoltage detection threshold voltage	$V_{DD1}$ falling	$V_{DD1\_UV}$	1.8	2.3	2.7	V
<b>ANALOG INPUT</b>						
Input offset voltage	$V_{IN} = 1 \text{ V}$	$V_{OS}$	-1.5	$\pm 0.4$	+1.5	mV
Input offset drift		$TCV_{OS}$	-5	10	30	μV/°C
Input resistance		$R_{IN}$	-	1	-	GΩ
Input capacitance	$f_{IN} = 275 \text{ kHz}$	$C_{IN}$	-	7	-	pF
Input bias current	$V_{IN} = GND_1$	$I_{IB}$	-15	3.5	15	nA
Input bias current drift		$TCI_{IB}$	-	$\pm 10$	-	pA/°C
<b>ANALOG OUTPUT</b>						
Nominal gain			-	1	-	V/V
Gain error		$E_G$	-0.3	$\pm 0.05$	+0.3	%
Gain error thermal drift		$TCE_G$	-45	$\pm 5$	+45	ppm/°C
Non-linearity			-0.04	$\pm 0.01$	+0.04	%
Non-linearity drift			-	$\pm 1$	-	ppm/°C
Total harmonic distortion	$V_{IN} = 1.8 \text{ V}$ , $f_{IN} = 10 \text{ kHz}$ , $BW = 100 \text{ kHz}$	THD		-87	-	dB
Output noise	$V_{IN} = 1 \text{ V}$ , $BW = 100 \text{ kHz}$		-	210	-	μV <sub>RMS</sub>
Signal to noise ratio	$V_{IN} = 1.8 \text{ V}$ , $f_{IN} = 1 \text{ kHz}$ , $BW = 10 \text{ kHz}$	SNR	78	82	-	dB
	$V_{IN} = 1.8 \text{ V}$ , $f_{IN} = 10 \text{ kHz}$ , $BW = 100 \text{ kHz}$		-	70	-	dB
Common-mode output voltage		$V_{CMout}$	1.36	1.4	1.45	V
Fail-safe differential output voltage	SHTDN active or $V_{DD1}$ missing	$V_{Fail-Safe}$	-	-2.53	-2.44	V
Output bandwidth		$BW$	-	400	-	kHz
Power supply rejection ratio (1)	PSRR vs. $V_{DD1}$ , at DC	PSRR <sub>DC</sub>	-	-78	-	dB
	PSRR vs. $V_{DD1}$ , 100 mV and 10 kHz ripple	PSRR <sub>AC</sub>	-	-75	-	dB
	PSRR vs. $V_{DD2}$ , at DC	PSRR <sub>DC</sub>	-	-82	-	dB
	PSRR vs. $V_{DD2}$ , 100 mV and 10 kHz ripple	PSRR <sub>AC</sub>	-	-74	-	dB
Output resistance		$R_{OUT}$	-	< 0.2	-	Ω
Common-mode transient immunity		CMTI	100	150	-	kV/μs
<b>DIGITAL INPUT (SHTDN)</b>						
Input current	$GND_1 \leq V_{SHTDN} \leq V_{DD1}$	$I_{IN}$	-70		1	μA
Input capacitance		$C_{IN}$	-	5	-	pF
High level input voltage		$V_{IH}$	$0.7 \times V_{DD1}$	-	$V_{DD1} + 0.3$	ppm/°C
Low level input voltage		$V_{IL}$	-0.3	-	$0.3 \times V_{DD1}$	%
<b>TIMING</b>						
Rising time of $OUT_P$ , $OUT_N$		$t_r$	-	1.3	-	μs
Falling time of $OUT_P$ , $OUT_N$		$t_f$	-	1.3	-	μs
$IN_P$ , $IN_N$ to $OUT_P$ , $OUT_N$ signal delay (50 % to 50 %)		$t_{PD}$	-	1.6	2.1	μs
Analog setting time	$V_{DD1}$ step to 3.0 V with $V_{DD2} \geq 3.0 \text{ V}$ , to $OUT_P$ , $OUT_N$ valid, 0.1 % settling	$t_{AS}$	-	0.5	-	ms
Device enable time	SHTDN high to low	$t_{EN}$	-	80	100	μs
Shutdown time	SHTDN low to high	$t_{SHTDN}$	-	1.2	5	μs

**Note**
<sup>(1)</sup> Input referred

**THERMAL INFORMATION**

PARAMETER	SYMBOL	VALUE	UNIT
Junction to ambient thermal resistance	$R_{\theta JA}$	86	°C/W
Junction to case (top) thermal resistance	$R_{\theta JC(\text{top})}$	28	°C/W
Junction to board thermal resistance	$R_{\theta JB}$	42	°C/W
Junction to top characterization parameter	$\Psi_{JT}$	4	°C/W
Junction to board characterization parameter	$\Psi_{JB}$	42	°C/W

**TYPICAL CHARACTERISTICS**

(Unless otherwise noted,  $V_{DD1} = 5$  V,  $V_{DD2} = 3.3$  V, 0.1 V to 2 V, and SHTDN = GND<sub>1</sub> = 0 V,  $f_{IN} = 1$  kHz, BW = 10 kHz)

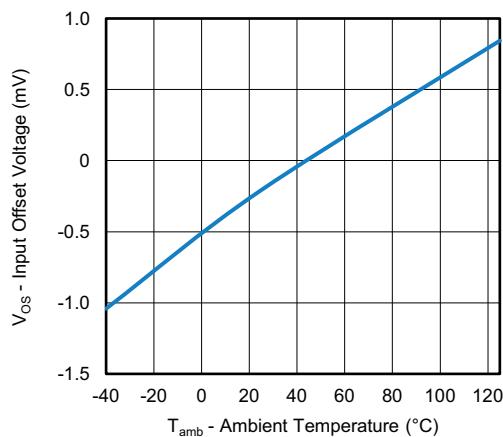


Fig. 3 - Input Offset Voltage vs. Ambient Temperature

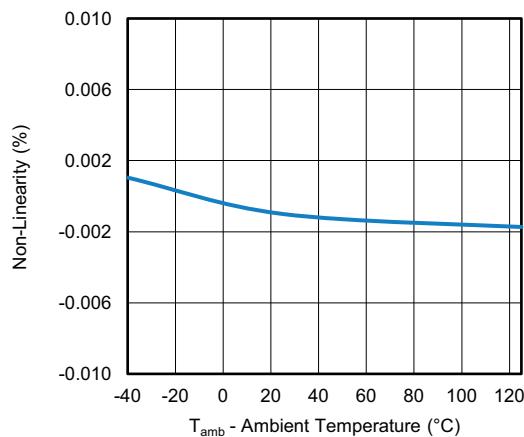


Fig. 5 - Non-Linearity vs. Ambient Temperature

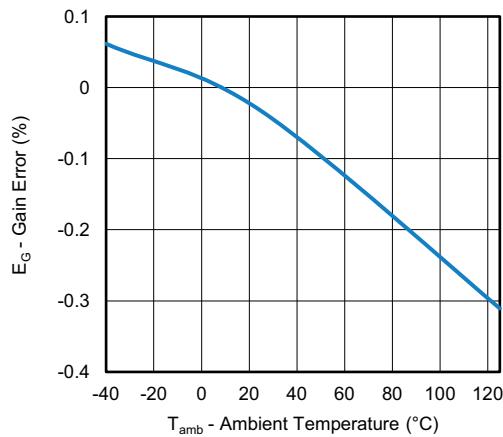


Fig. 4 - Gain Error vs. Ambient Temperature

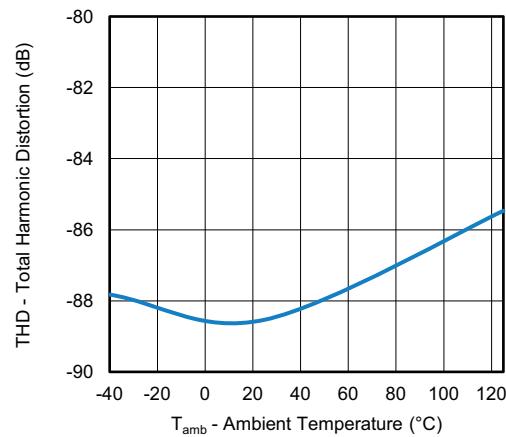


Fig. 6 - Total Harmonic Distortion vs. Ambient Temperature

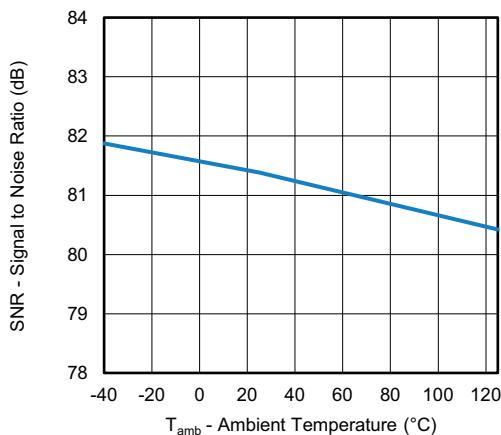


Fig. 7 - Signal to Noise Ratio vs. Ambient Temperature

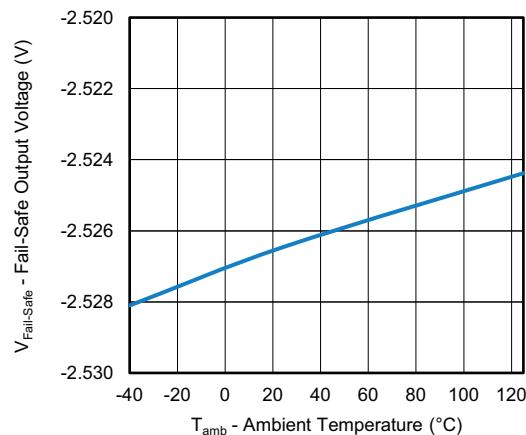


Fig. 10 - Fail-Safe Output Voltage vs. Ambient Temperature

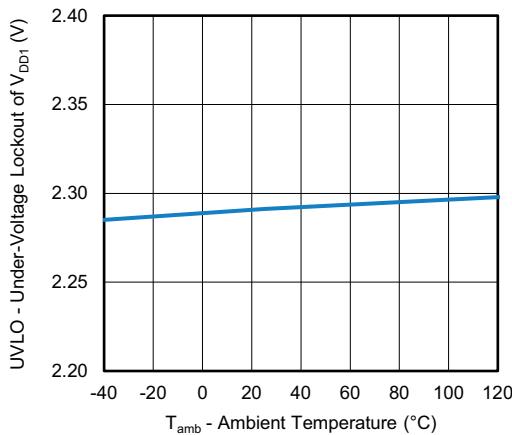


Fig. 8 - Under-Voltage Lockout of  $V_{DD1}$  vs. Ambient Temperature

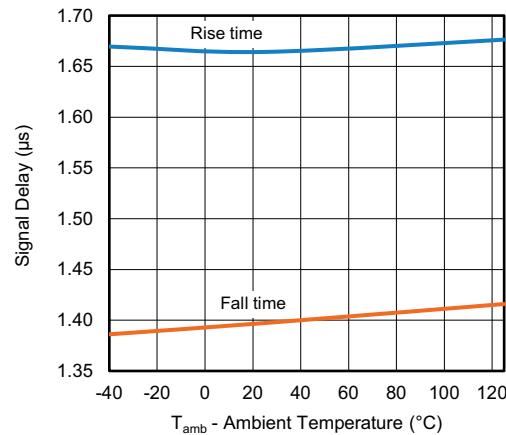


Fig. 11 - Signal Delay vs. Ambient Temperature

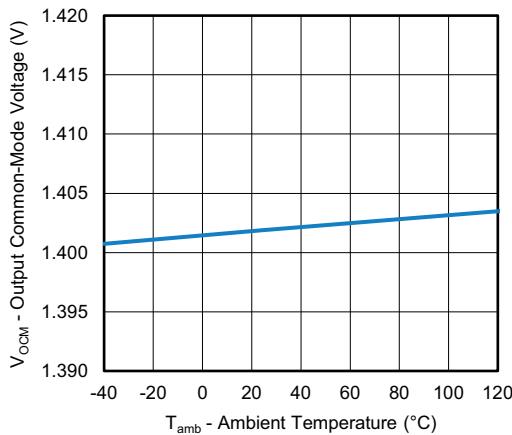


Fig. 9 - Output Common-Mode Voltage vs. Ambient Temperature

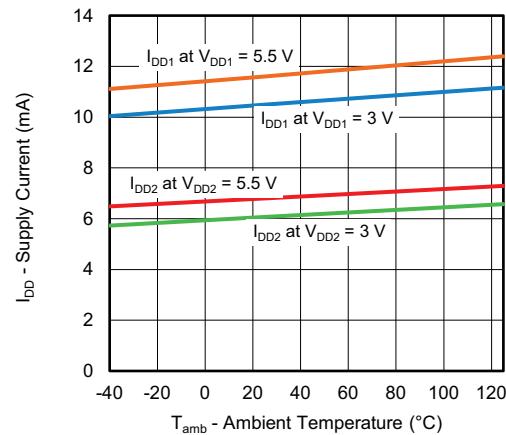


Fig. 12 - Supply Current vs. Ambient Temperature

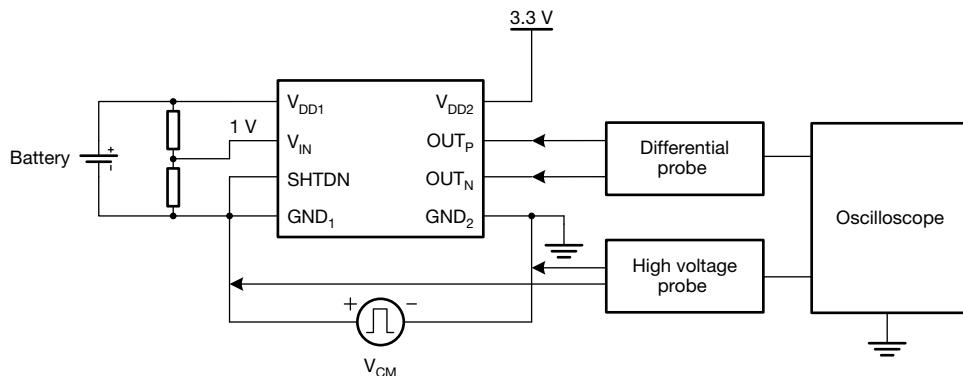
**PARAMETER MEASUREMENT INFORMATION**


Fig. 13 - Common-Mode Transient Immunity Test Circuit

SAFETY AND INSULATION RATINGS				
PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Climatic classification	According to IEC 68 part 1		40 / 125 / 21	
Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	CTI	> 600	
Maximum rated withstanding isolation voltage	$V_{TEST} = V_{ISO}$ , $t = 1$ min (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ , $t = 1$ s (100 % production test)	$V_{ISO}$	5000	$V_{RMS}$
Maximum transient isolation voltage	$t = 1$ min	$V_{IOTM}$	8000	$V_{peak}$
Maximum repetitive isolation voltage		$V_{IORM}$	2121	$V_{peak}$
Maximum surge isolation voltage	Test method per IEC 60065, 1.2/50 $\mu$ s waveform, $V_{TEST} = V_{IOSM} \times 1.6$	$V_{IOSM}$	6250	$V_{peak}$
Maximum working isolation voltage	AC voltage	$V_{IOWM}$	1500	$V_{RMS}$
	DC voltage		2121	$V_{DC}$
Isolation resistance	$T_{amb} = 25$ °C, $V_{IO} = 500$ V	$R_{IO}$	> $10^{12}$	$\Omega$
	$T_{amb} = 125$ °C, $V_{IO} = 500$ V	$R_{IO}$	> $10^{10}$	$\Omega$
	$T_{amb} = 150$ °C, $V_{IO} = 500$ V	$R_{IO}$	> $10^9$	$\Omega$
Total power dissipation at 25 °C	$\theta_{JA} = 86$ °C/W, $V_I = 5.5$ V, $T_j = 150$ °C, $T_{amb} = 25$ °C	$P_S$	1430	mW
Safety input, output, or supply current	$\theta_{JA} = 86$ °C/W, $V_I = 5.5$ V, $T_j = 150$ °C, $T_{amb} = 25$ °C	$I_S$	260	mA
Maximum safety temperature		$T_S$	150	°C
Creepage distance	SOP-8 (300 mils)		≥ 8	mm
Clearance distance			≥ 8	mm
Insulation thickness	Distance through insulation	DTI	28	$\mu$ m
Material group	IEC 60664-1		I	
For rated mains voltage ≤ 150 $V_{RMS}$			I to IV	
For rated mains voltage ≤ 300 $V_{RMS}$			I to IV	
For rated mains voltage ≤ 400 $V_{RMS}$			I to IV	
Pollution degree per DIN VDE 0110, table 1			2	
Input to output test voltage, method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$ , 100 % production test; $t_{ini} = t_m = 1$ s, partial discharge < 5 pC	$V_{pd(m)}$	3977	$V_{peak}$
After environmental tests subgroup 1	$V_{IORM} \times 1.6 = V_{pd(m)}$ , $t_{ini} = 1$ s, $t_m = 10$ s, partial discharge < 5 pC	$V_{pd(m)}$	3394	$V_{peak}$
After input and / or safety test subgroup 2 and subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$ , $t_{ini} = 1$ s, $t_m = 10$ s, partial discharge < 5 pC	$V_{pd(m)}$	2545	$V_{peak}$
Isolation capacitance	$f = 1$ MHz	$C_{IO}$	0.8	pF

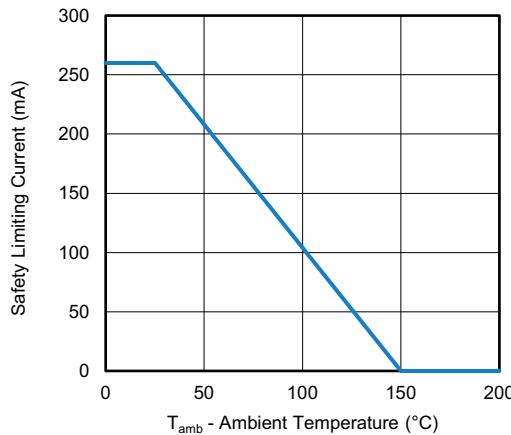


Fig. 14 - VIA2000SD Thermal Derating Curve, Dependence of Safety Limiting Values With Case Temperature per DIN VOE V0884-11

## FUNCTION DESCRIPTION

### Overview

The VIA2000SD is a high performance isolated amplifier with a high input impedance that accept wide range single-ended input. The singled-ended input is suited to bus voltage monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order  $\Sigma - \Delta$  modulator in the device. With the internal voltage reference and clock generator, the modulator convert the analog input signal to a digital bitstream. The output of the modulator is transferred by the drivers (called TX in the functional block diagram) across the isolation barrier that separates the isolated side 1 and side 2 voltage. The received bitstream and clock are synchronized and processed, as shown in the functional block diagram, by a fourth-order analog filter on the side 2 and has a differential output.

SHTDN pin is used to disable the conversion. Since SHTDN is an active high signal and is pulled up by a 100 k $\Omega$  (typical) internally, it should be connected to GND<sub>1</sub> or logic low in normal operation.

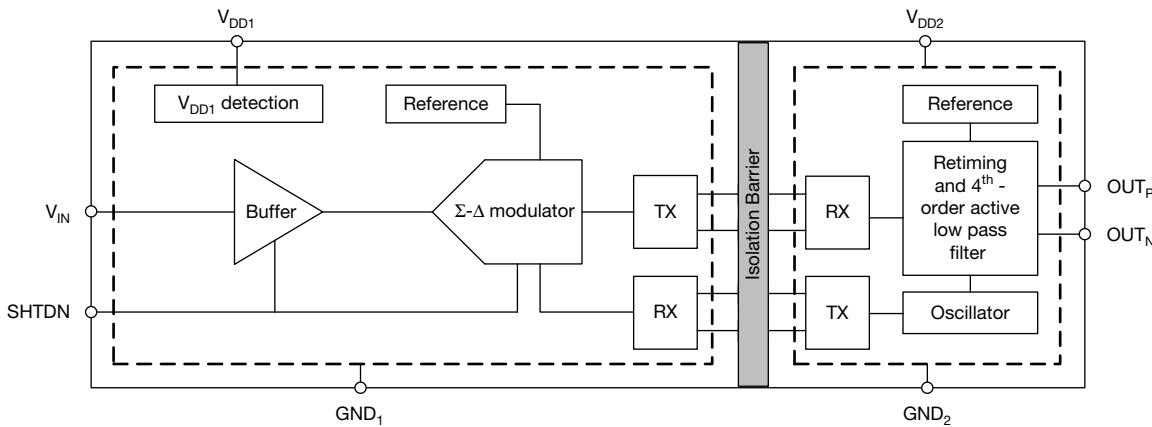


Fig. 15 - Function Block Diagram

### Analog Input

Below mentioned are the restrictions on the analog input signal ( $V_{IN}$ ).

1. If the input voltage exceeds the range  $GND_1 - 6\text{ V}$  to  $V_{DD1} + 0.5\text{ V}$ , the input current must be limited to  $10\text{ mA}$  because the device input electrostatic discharge (ESD) diodes turn on
2. The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR)

### Analog Output

For linear input range, VIA2000SD provides an analog differential output which has a fixed gain of 1. If a full-scale input signal is applied to the VIA2000SD ( $V_{IN} \geq V_{Clipping}$ ), the analog output will be clipped.

In addition, VIA2000SD integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail safe output is a negative differential output voltage that is activated in the conditions mentioned below. Please note that the fail safe output does not occur during normal operation.

1. When the undervoltage of  $V_{DD1}$  is detected ( $V_{DD1} < V_{DD1uv}$ )
2. When SHTDN signal is activated (pulled high)

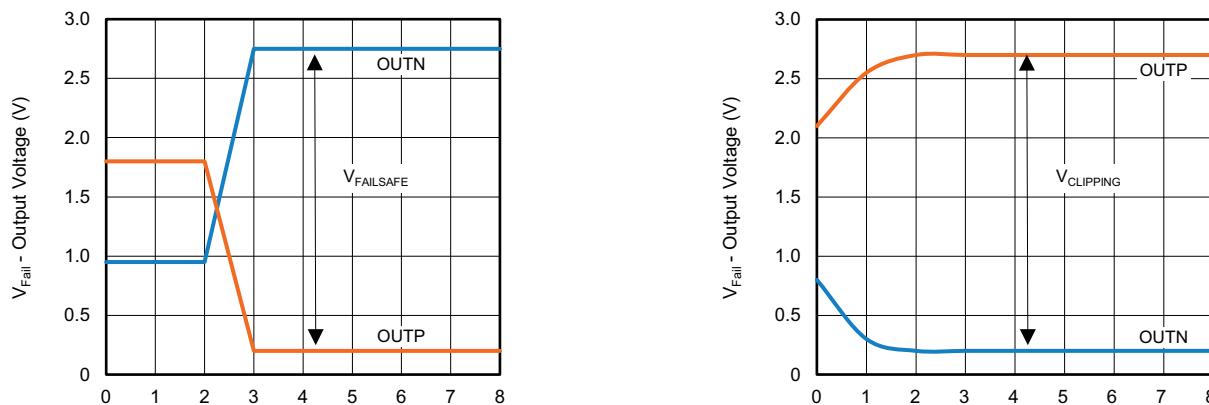


Fig. 16 - Typical Fail-Safe Output When Clipping Output

## APPLICATION NOTE

## Typical Application Circuit

VIA2000SD has an input impedance of up to  $1\text{ G}\Omega$ , and has a wide input voltage range as well. These features make VIA2000SD ideally suitable for isolated voltage sensing applications such as frequency inverters. The typical application circuit is shown in Fig. 17.

The bus voltage of the frequency inverter is divided by a resistance network, and the divided voltage is applied to the input of VIA2000SD through a RC filter. The differential output of the isolated amplifier is converted to a single-ended analog output with an operational amplifier based circuit. An analog to digital converter usually receives the analog output and converts to digital signal for controller processing.

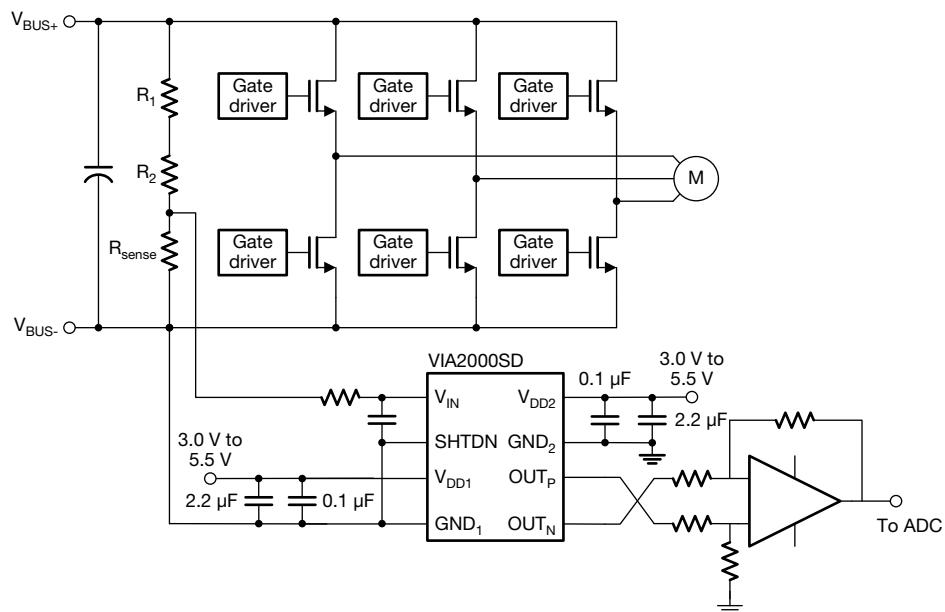


Fig. 17 - Typical Application Circuit in Voltage Sensing

## Shunt Resistor Selection

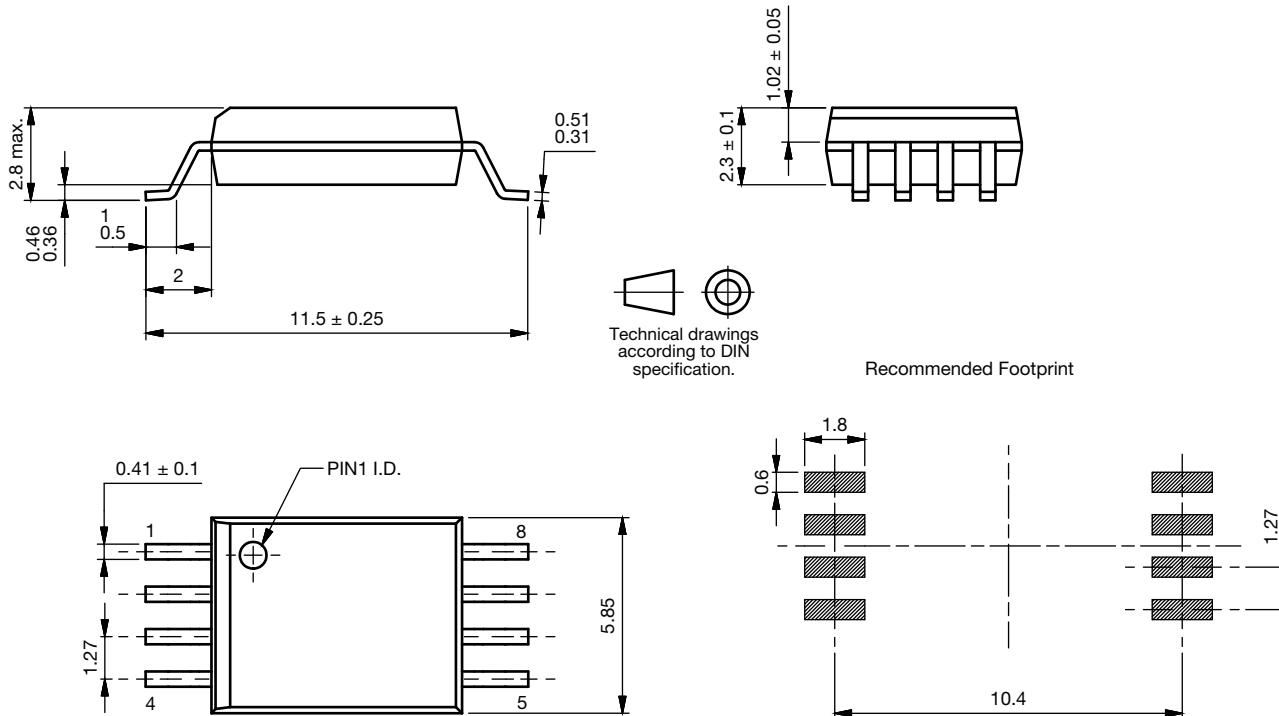
There are two other factors should be considered when selecting the sense resistor:

- The voltage-drop on  $R_{sense}$  divided by nominal  $V_{BUS}$  must not exceed the recommended linear input voltage range:  $V_{IN} \leq FSR$
- The voltage-drop on  $R_{sense}$  divided by  $V_{BUS}$  in maximum allowed overvoltage condition must not exceed the input voltage that causes a clipping output:  $V_{IN} \leq V_{Clipping}$

## PCB Layout

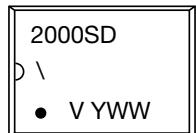
There are some key guidelines or considerations for optimizing performance in PCB layout:

- VIA2000SD requires a 0.1  $\mu$ F bypass capacitor between  $V_{DD1}$  and GND<sub>1</sub>,  $V_{DD2}$  and GND<sub>2</sub>. The capacitor should be placed as close as possible to the  $V_{DD}$  pin. If better filtering is required, an additional 1  $\mu$ F to 10  $\mu$ F capacitor may be used

**PACKAGE DIMENSIONS** (in millimeters)


Drawing-No.: 6.544-5451.1-4  
Issue: 1VK; 12.02.2024

Fig. 18 - SOP-8 (300 mil) Package Shape and Dimensions

**PACKAGE MARKING** (example)

**Note**

- Tape and reel suffix (TR) is not part of the package marking.

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