Getting started with EVL-L98GD8E evaluation board based on configurable HS/LS driver L98GD8E

Introduction

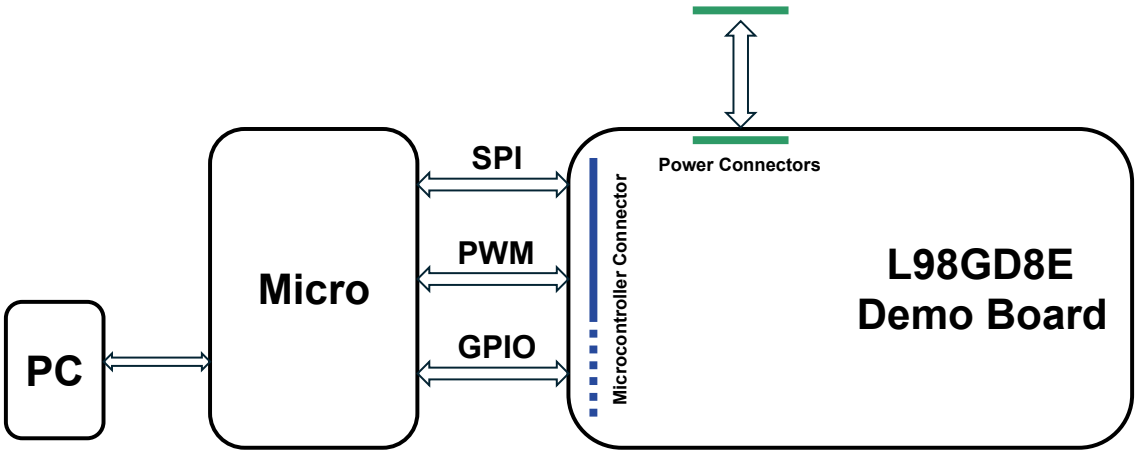
The EVL-L98GD8E is an evaluation board designed to provide the user with a set of tools for the evaluation of the product L98GD8E, a configurable HS/LS driver for automotive applications. The board provides all the main input/output capabilities needed to drive all the supported loads, along with diagnostic functionalities.

1 Hardware description

The EVL-L98GD8E board offers maximum flexibility, providing access to all pins to simplify the evaluation and debug phases.

1.1 Block diagram

Figure 1. Application block diagram

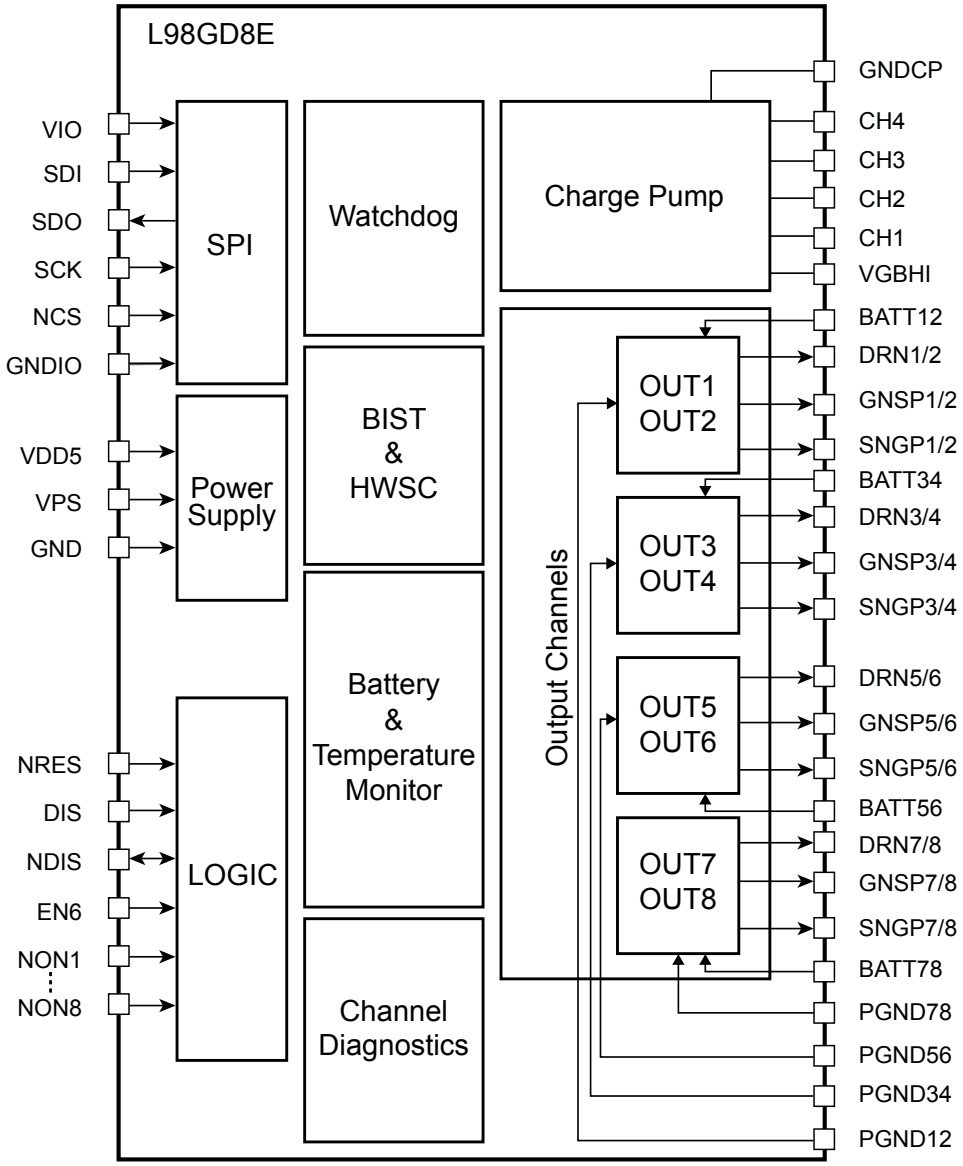


1.1.1 Microcontroller

- 4x36 connector for SPC56M-DIS (Discovery+ board featuring SPC563M64L7)
- GPIO/PWM output
- Configuration and diagnostics through SPI interface
- Possibility to easily connect the board to other microcontroller boards through a wire adaptor

2 L98GD8E block diagram

Figure 2. **L98GD8E block diagram**



3 L98GD8E pinout and description

Figure 3. **L98GD8E pinout**

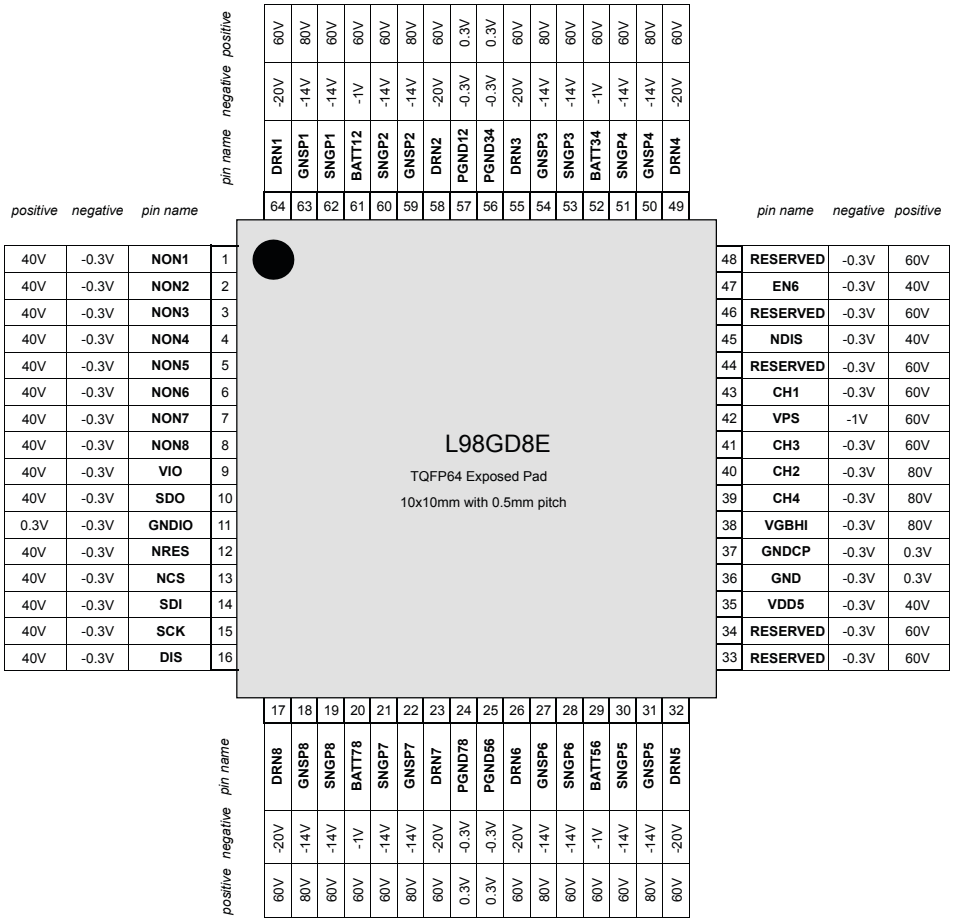


Table 1. **L98GD8E pin description**

Pin number	Pin name	Description	Active state	I/O type
1	NON1	Input channel 1	L	I
2	NON2	Input channel 2	L	I
3	NON3	Input channel 3	L	I
4	NON4	Input channel 4	L	I
5	NON5	Input channel 5	L	I
6	NON6	Input channel 6	L	I
7	NON7	Input channel 7	L	I
8	NON8	Input channel 8	L	I
9	VIO	Supply voltage for digital portion	N. A.	Power
10	SDO	SPI data out	N. A.	O
11	GNDIO	Ground for VIO (shorted to GNDCP)	N. A.	Power
12	NRES	Reset input	L	I

Pin number	Pin name	Description	Active state	I/O type
13	NCS	SPI chip select	L	I
14	SDI	SPI data in	N. A.	I
15	SCK	SPI clock	N. A.	I
16	DIS	Disable 0	H	I
17	DRN8	FET drain 8		I
18	GNSP8	NFET gate / PFET source 8		O
19	SNGP8	NFET source/PFET gate 8		O
20	BATT78	Battery for 7 & 8		Power
21	SNGP7	NFET source/PFET gate 7		O
22	GNSP7	NFET gate/PFET source 7		O
23	DRN7	FET drain 7		I
24	PGND78	Power ground 7 & 8		Power
25	PGND56	Power ground 5 & 6		Power
26	DRN6	FET drain 6		I
27	GNSP6	NFET gate/PFET source 6		O
28	SNGP6	NFET source/PFET gate 6		O
29	BATT56	Battery for 5 & 6		Power
30	SNGP5	NFET source/PFET gate 5		O
31	GNSP5	NFET gate/PFET source 5		O
32	DRN5	FET drain 5		I
33	Not used	To be connected to GND		
34	Not used	To be connected to GND		
35	VDD5	5 V input	N. A.	Power
36	GND	Ground	N. A.	Power
37	GNDCP	Ground for charge pump (shorted to GNDIO)		
38	VGBHI	Charge pump output	N. A.	Power
39	CH4	Charge pump		Power
40	CH2	Charge pump		Power
41	CH3	Charge pump		Power
42	VPS	Battery input	N. A.	Power
43	CH1	Charge pump		Power
44	Not used	To be connected to GND		
45	NDIS	Disable 1	L	I
46	Not used	To be connected to GND		
47	EN6	Enable of channel 6	H	I
48	Not used	To be connected to GND		
49	DRN4	FET drain 4		I
50	GNSP4	NFET gate/PFET source 4		O
51	SNGP4	NFET source/PFET gate 4		O
52	BATT34	Battery for 3 & 4		Power
53	SNGP3	NFET source/PFET gate 3		O

Pin number	Pin name	Description	Active state	I/O type
54	GNSP3	NFET gate/PFET source 3		O
55	DRN3	FET drain 3		I
56	PGND34	Power ground 3 & 4		Power
57	PGND12	Power ground 1 & 2		Power
58	DRN2	FET drain 2		I
59	GNSP2	NFET gate/PFET source 2		O
60	SNGP2	NFET source/PFET gate 1		O
61	BATT12	Battery for 1 & 2		Power
62	SNGP1	NFET source/PFET gate 1		O
63	GNSP1	NFET gate/PFET source 1		O
64	DRN1	FET drain 1		I

4 Board layout

Figure 4. **Board top layer**

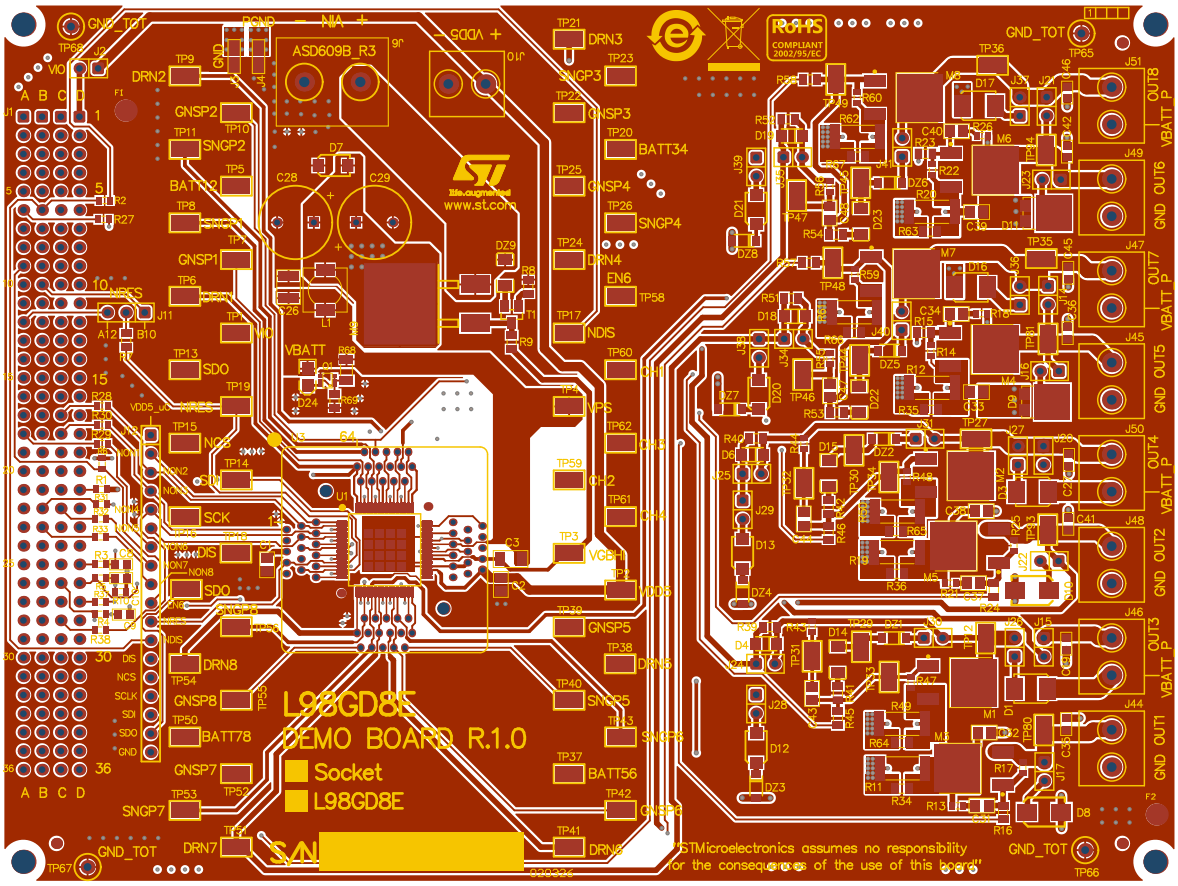


Figure 5. **Board midlayer 1**

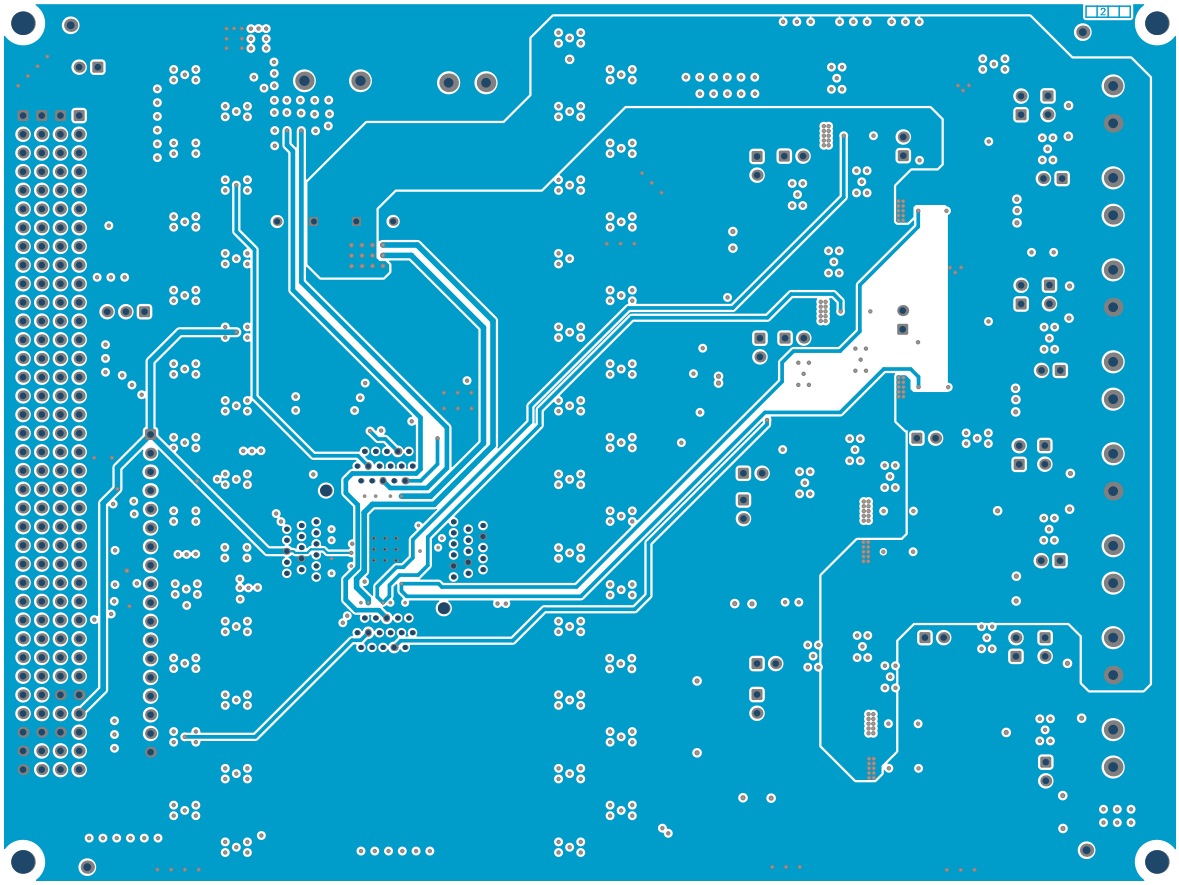


Figure 6. **Board midlayer 2**

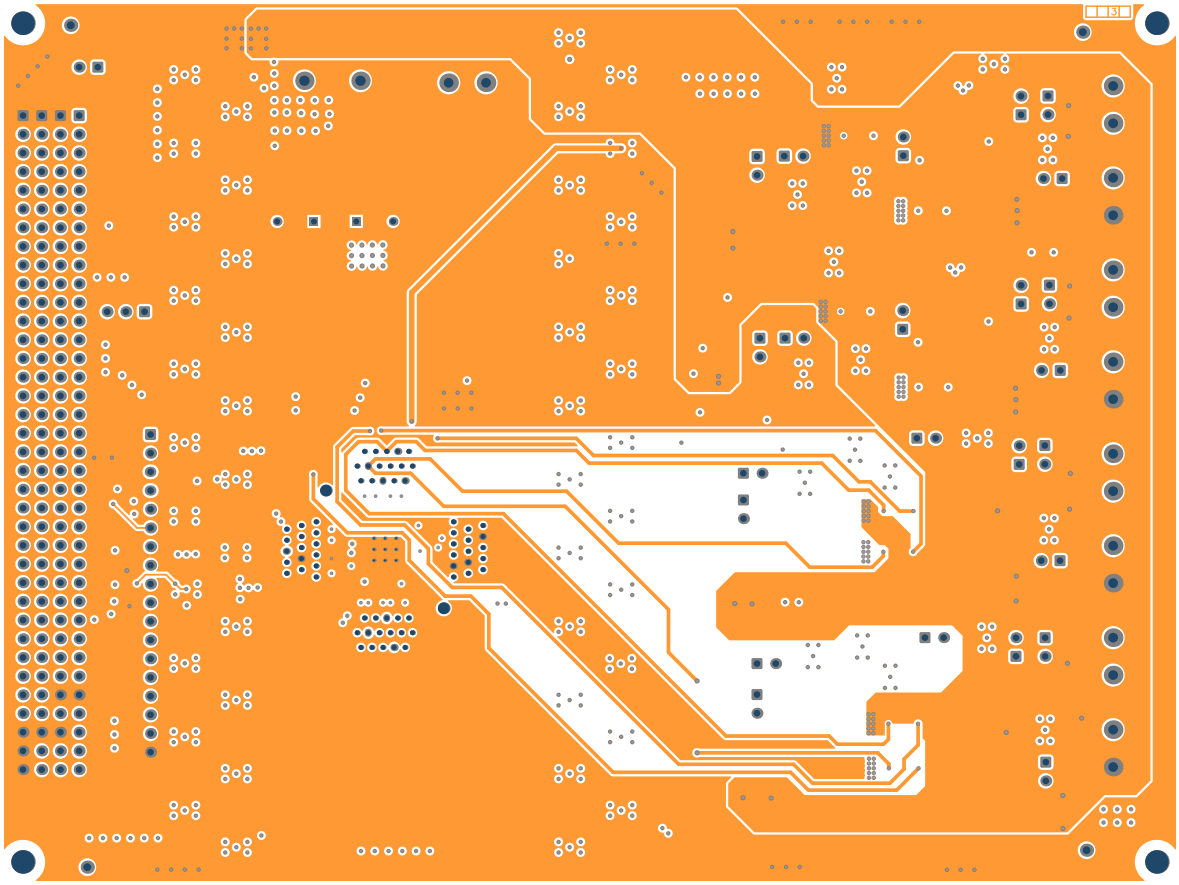


Figure 7. **Board bottom layer**

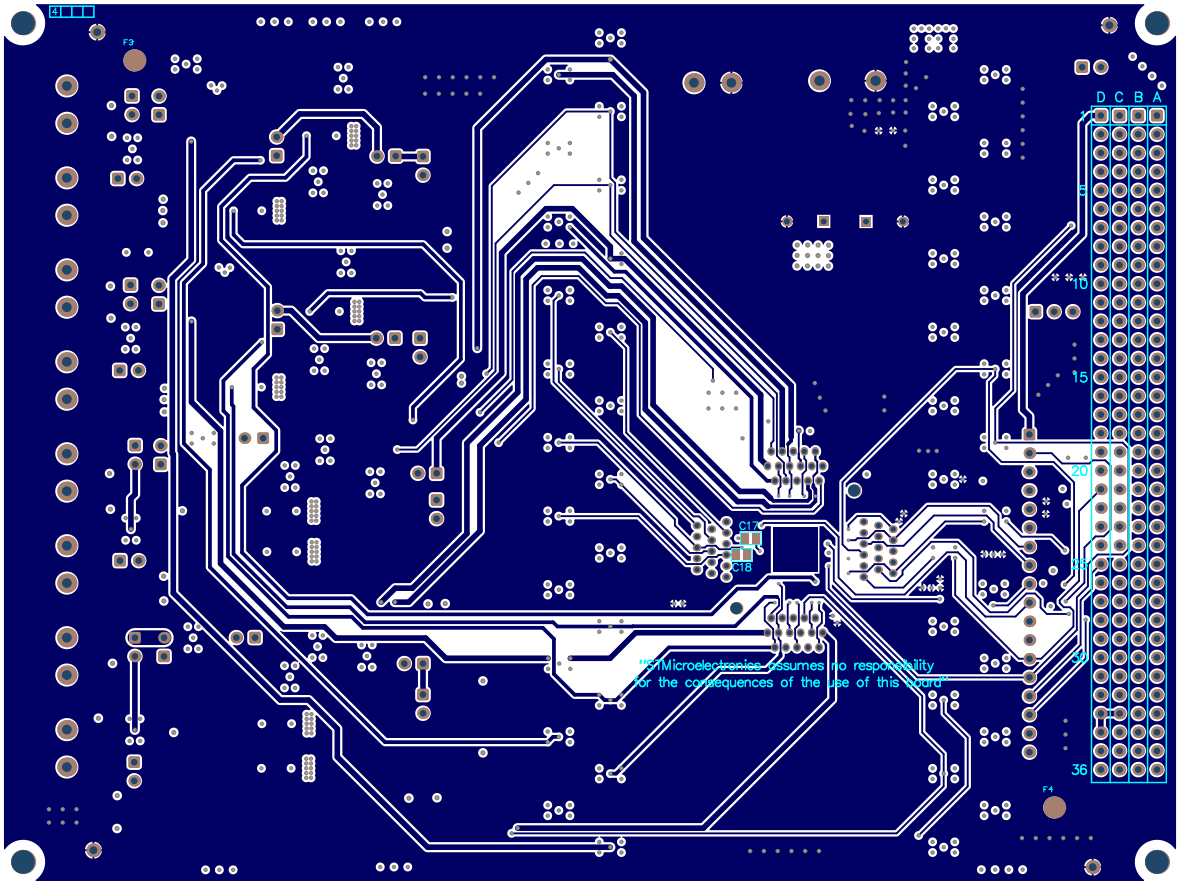
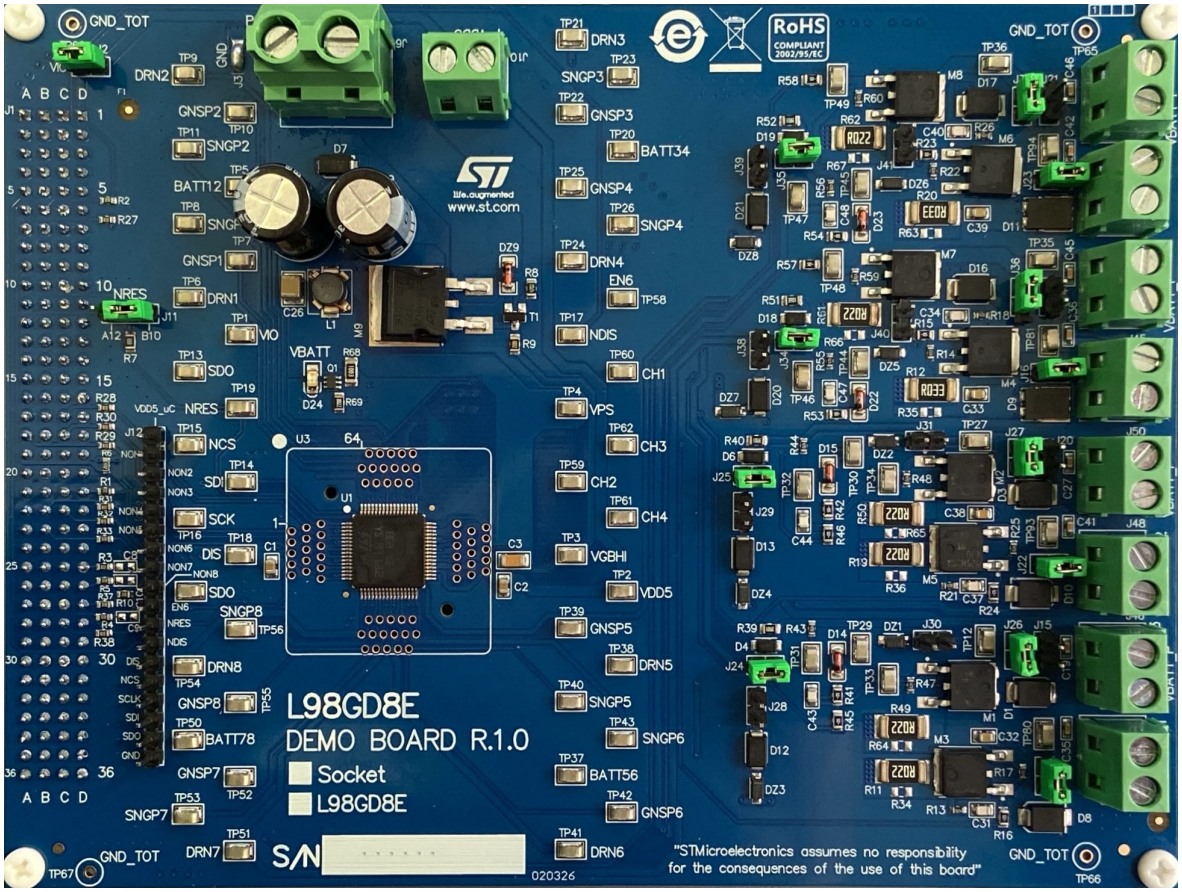
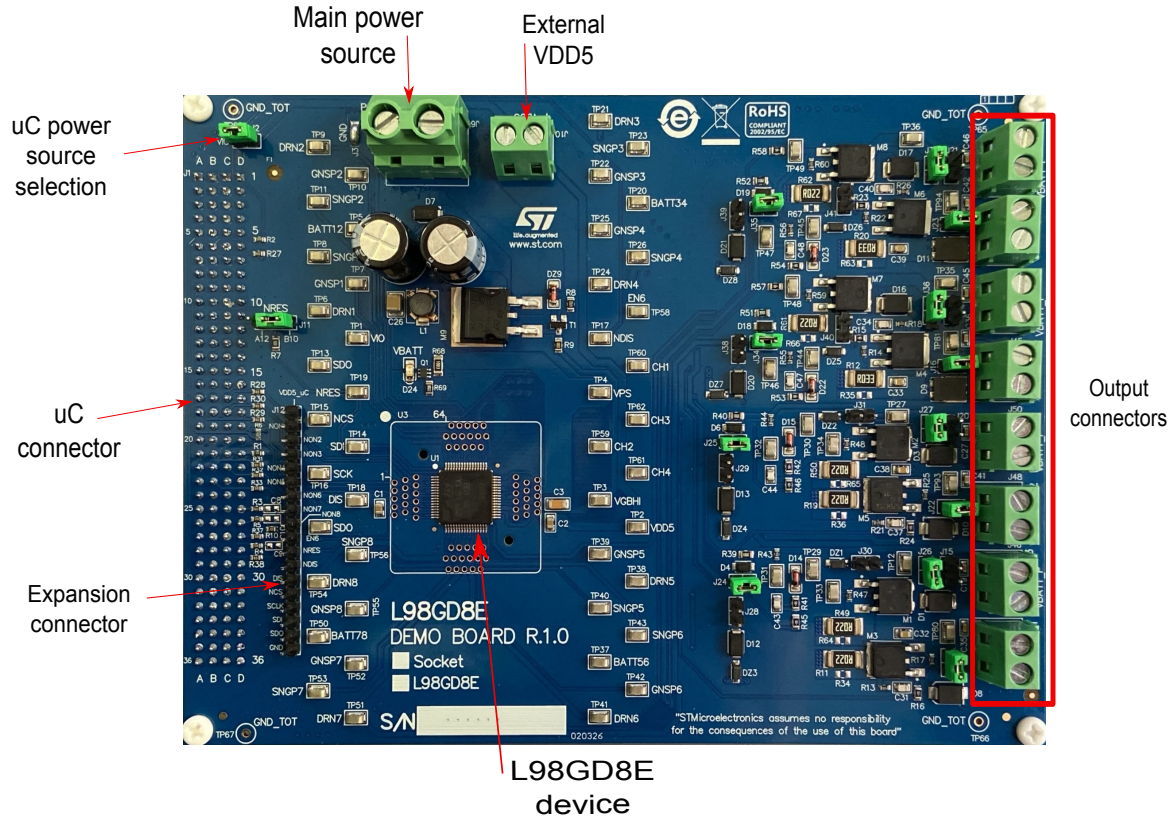


Figure 8. **Board top view**



5 Evaluation board main components and connectors

Figure 9. Motherboard main components and connectors



6 Jumpers and connectors

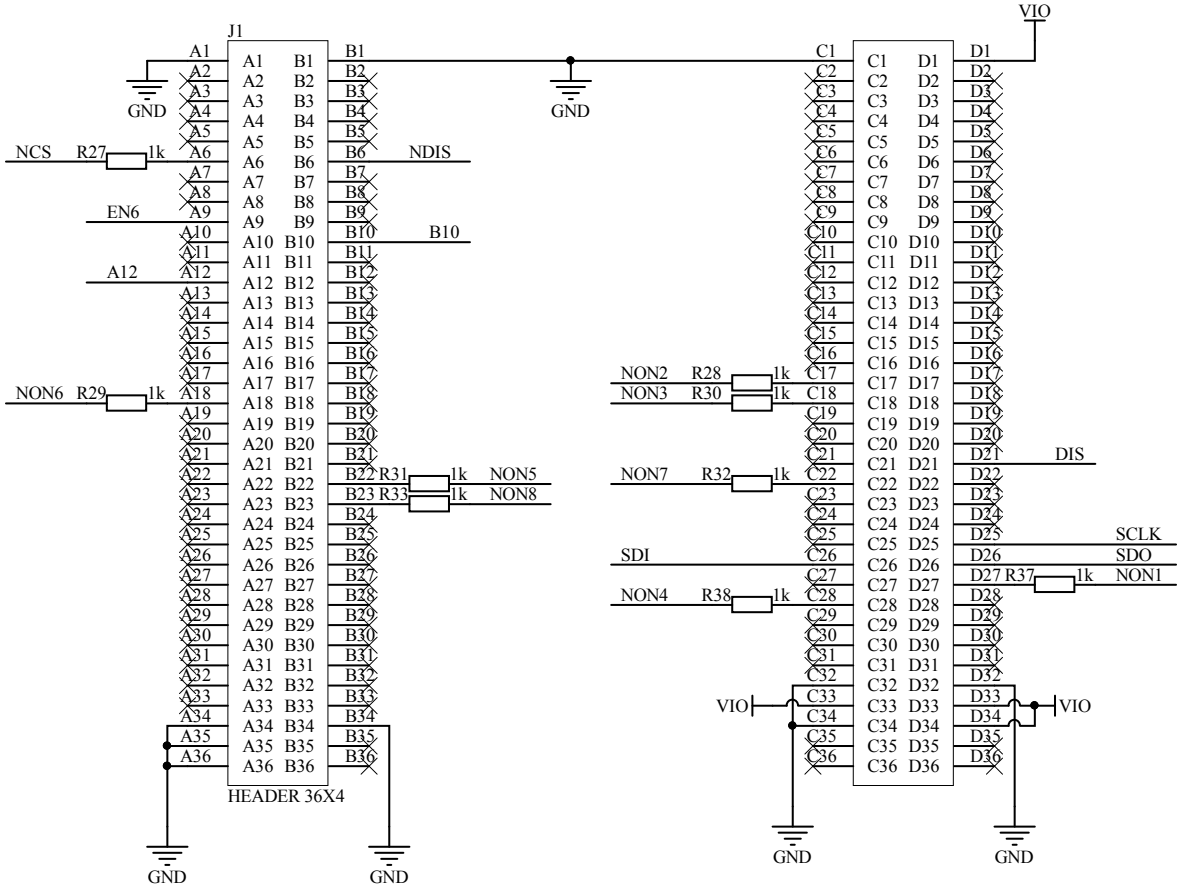
6.1 Mother board jumpers and connectors

Table 2. Mother board jumpers and connectors

Name	Description	Type
J1	Microcontroller board connector	4x36 multi pin connector
J2	µC power supply selection	Closed: µC supplied by EVL-L98GD8E 5 V Open: µC supplied externally
J3	GND_TOT and GND net interconnection	Closed: nets connected Open: nets not connected
J4	GND_TOT and PGND net interconnection	Closed: nets connected Open: nets not connected
J6	Main power supply	Screw connector
J10	External voltage for VIO and µC (depending on J2 setting)	Screw connector
J11	NRES connection	1-2 (A12): NRES connected to µC GPIO 2-3 (B10): NRES connected to µC RESET pin
J12	Expansion connector	1x18 multipin connector
J14	H_Bridge 2 configurator	Closed: OUT5-OUT7 shorted for H-Bridge configuration Open: OUT5 and OUT7 independent output
J15	H_Bridge 1 configurator	Closed: OUT1-OUT3 shorted for H-Bridge configuration Open: OUT1 and OUT3 independent output
J16	High-side recirculation diode Channel 5	Closed: clamp diode connected Open: Clamp diode not connected-s
J17	High-side recirculation diode Channel 1	Closed: diode connected Open: diode not connected-s
J20	H_Bridge 1 configurator	Closed: OUT2-OUT4 shorted for H-Bridge configuration Open: OUT2 and OUT4 independent output
J21	H_Bridge 2 configurator	Closed: OUT6-OUT8 shorted for H-Bridge configuration Open: OUT6 and OUT8 independent output
J22	High-side recirculation diode Channel 2	Closed: diode connected Open: diode not connected
J23	High-side recirculation diode Channel 6	Closed: diode connected Open: diode not connected
J24	Snubber selection Channel 3	Closed: Snubber net excluded Open: Snubber net connected
J25	Snubber selection Channel 4	Closed: Snubber net excluded Open: Snubber net connected

Name	Description	Type
J26	Low-side output recirculation diode Channel 3	Closed: diode connected Open: diode not connected
J27	Low-side output recirculation diode Channel 4	Closed: diode connected Open: diode not connected
J28	Low-side output clamp network Channel 3	Closed: net connected Open: net not connected
J29	Low-side output clamp network Channel 4	Closed: net connected Open: net not connected
J30	Low-side VGD clamp network Channel 3	Closed: net connected Open: net not connected
J31	Low-side VGD clamp network Channel 4	Closed: net connected Open: net not connected
J34	Snubber selection Channel 7	Closed: Snubber net excluded Open: Snubber net connected
J35	Snubber selection Channel 8	Closed: Snubber net excluded Open: Snubber net connected
J36	Low-side output recirculation diode Channel 7	Closed: diode connected Open: diode not connected
J37	Low-side output recirculation diode Channel 8	Closed: diode connected Open: diode not connected
J38	Low-side output clamp network Channel 7	Closed: net connected Open: net not connected
J39	Low- side output clamp network Channel 8	Closed: net connected Open: net not connected
J40	Low-side VGD clamp network Channel 7	Closed: net connected Open: net not connected
J41	Low-side VGD clamp network Channel 8	Closed: net connected Open: net not connected
J44	OUT 1 connector	Screw connector
J45	OUT 5 connector	Screw connector
J46	OUT 3 connector	Screw connector
J47	OUT 7 connector	Screw connector
J48	OUT 2 connector	Screw connector
J49	OUT 6 connector	Screw connector
J50	OUT 4 connector	Screw connector
J51	OUT 8 connector	Screw connector

Figure 10. **Microcontroller connectors**



7 Functional description

In the default state, the board hardware is configured as follows:

- OUT1 high-side NMOS
- OUT2 high-side NMOS
- OUT3 low-side NMOS
- OUT4 low-side NMOS
- OUT5 high-side PMOS
- OUT6 high-side PMOS
- OUT7 low-side NMOS
- OUT8 low-side NMOS

7.1 Default jumper setting

Table 3. Configuration jumpers

Name	Description	Configuration
J2	µC supplied by EVL-L98GD8E 5 V	Closed
J3	GND_TOT and GND net interconnection	Closed
J4	GND_TOT and PGND net interconnection	Closed
J11	NRES connected to µC GPIO	2-3 (B10)
J14	OUT5 and OUT7 independent output	Open
J15	OUT1 and OUT3 independent output	Open
J16	High-side recirculation diode channel 5 connected	Closed
J17	High-side recirculation diode channel 1 connected	Closed
J20	OUT2 and OUT4 independent output	Open
J21	OUT6 and OUT8 independent output	Open
J22	High-side recirculation diode channel 2 connected	Closed
J23	High-side recirculation diode channel 6 connected	Closed
J24	Snubber selection channel 3 connected	Closed
J25	Snubber selection channel 4 connected	Closed
J26	Low-side output recirculation diode channel 3 connected	Closed
J27	Low-side output recirculation diode channel 4 connected	Closed
J28	Low-side output clamp network channel 3 connected	Open
J29	Low-side output clamp network channel 4 connected	Open
J30	Low-side VGD clamp network channel 3 connected	Open
J31	Low-side VGD clamp network channel 4 connected	Open
J34	Snubber selection channel 7 connected	Closed
J35	Snubber selection channel 8 connected	Closed
J36	Low-side output recirculation diode channel 7 connected	Closed
J37	Low-side output recirculation diode channel 8 connected	Closed
J38	Low-side output clamp network channel 7 connected	Open
J39	Low-side output clamp network channel 8 connected	Open
J40	Low-side VGD clamp network channel 7 connected	Open

Name	Description	Configuration
J41	Low-side VGD clamp network channel 8 connected	Open

7.2 Getting started

7.2.1 Start up

1. Configure all jumpers according to Table 3
2. Connect a power supply to J6, respecting the correct polarity
3. Configure the power supply to 13.5 V and limit the current to 1 A
4. Switch on the power supply
5. For further information, connect a µC and follow the related documentation to check the L98GD8E internal register status

Appendix A EVL-L98GD8E evaluation board schematics

Figure 11. EVL-L98GD8E evaluation board schematics (part 1/3)

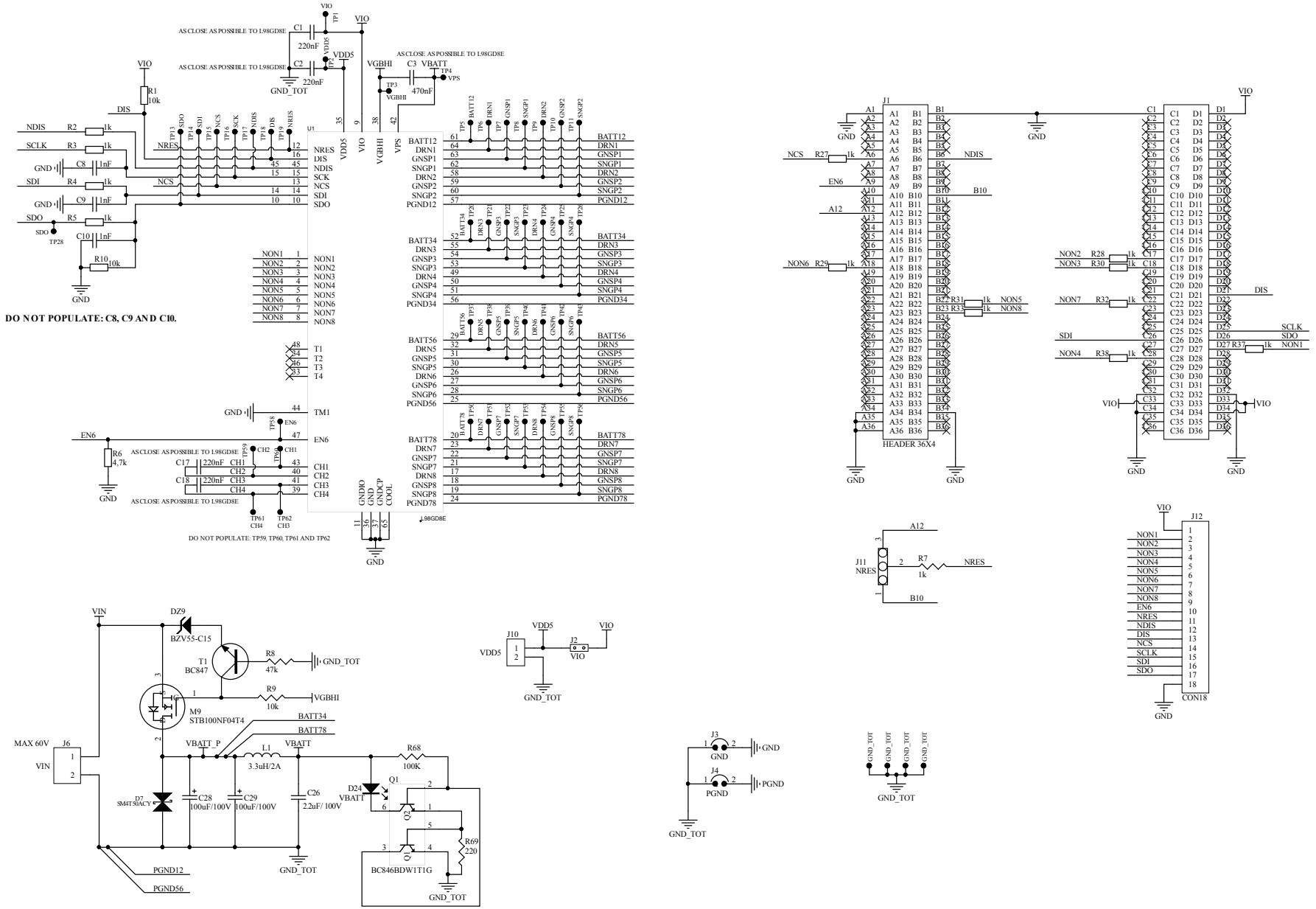


Figure 12. EVL-L98GD8E evaluation board schematics (part 2/3)

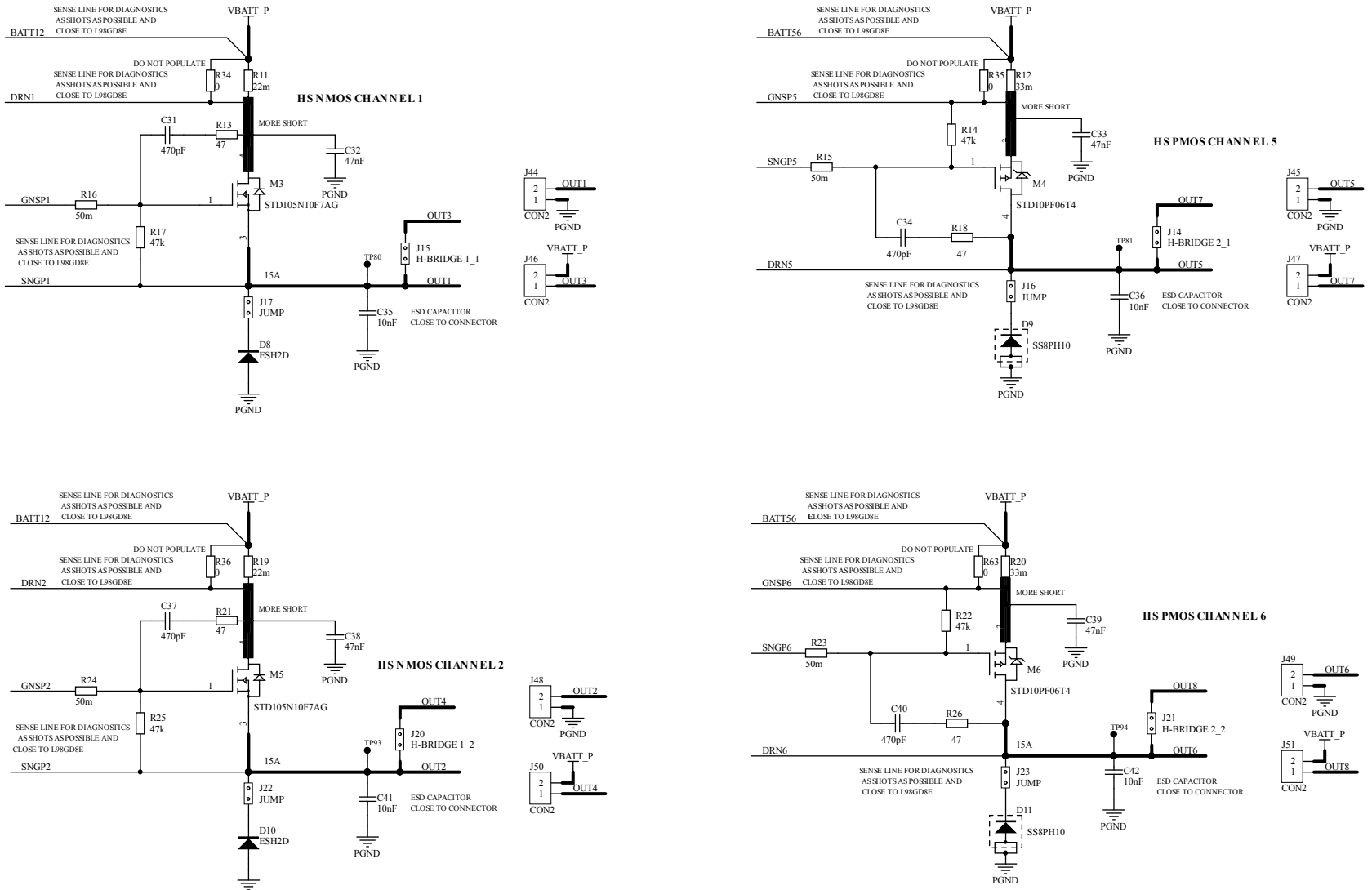
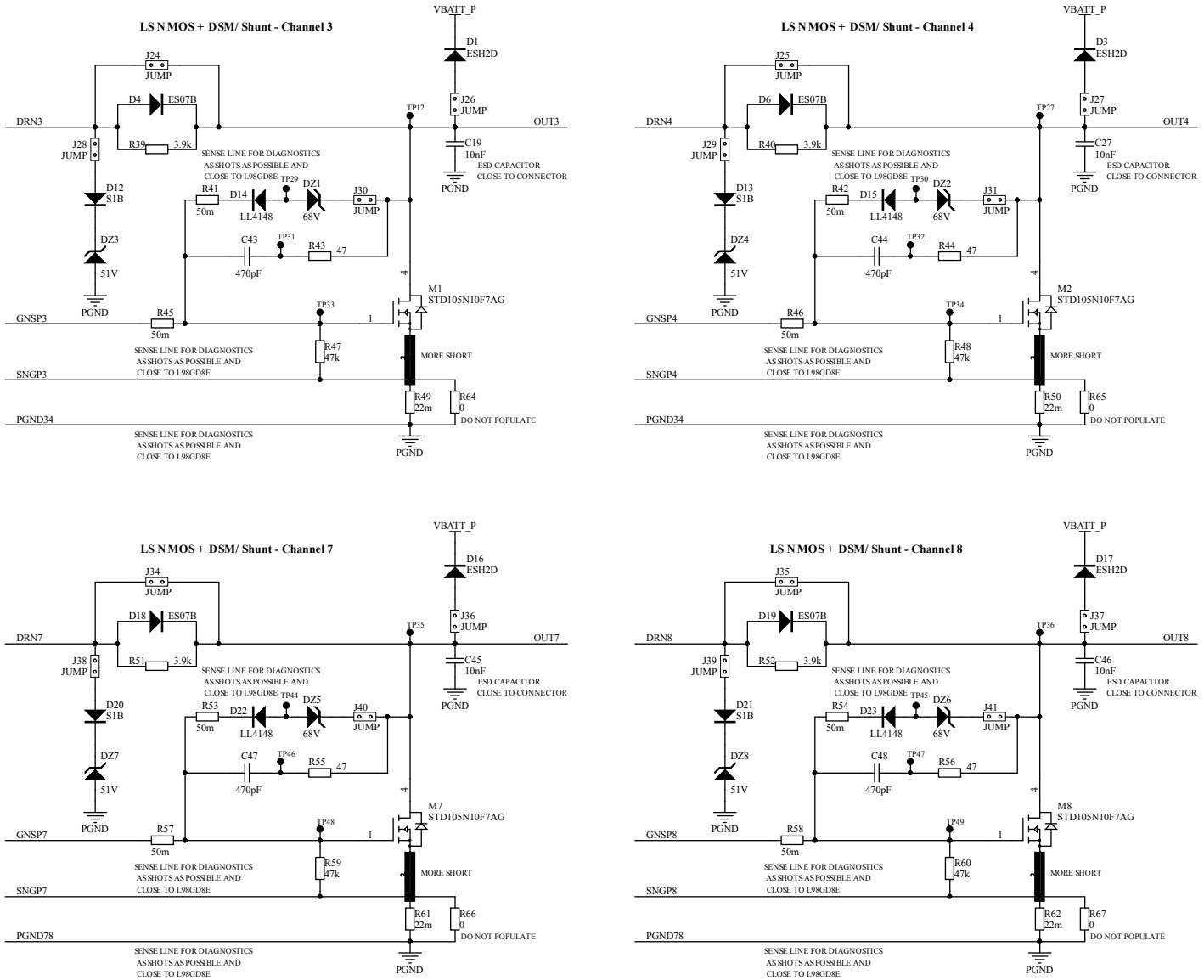


Figure 13. EVL-L98GD8E evaluation board schematics (part 3/3)

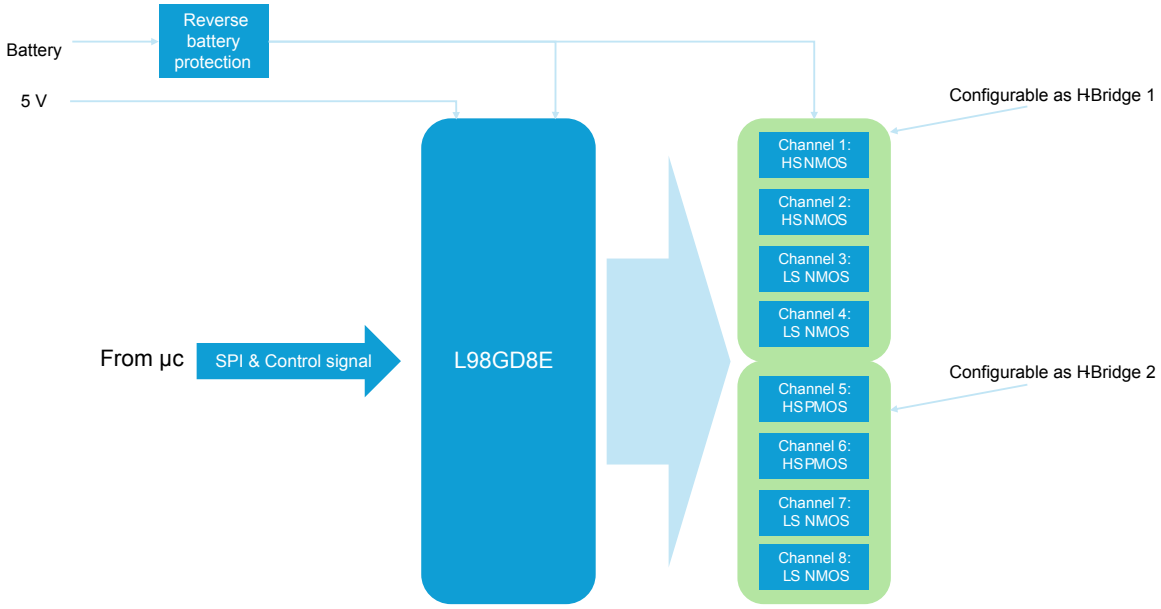


Appendix B EVL-L98GD8E evaluation board bill of materials

Refer to the EVL-L98GD8E evaluation board ST official page.

Appendix C EVL-L98GD8E evaluation board configuration block diagram

Figure 14. **EVL-L98GD8E evaluation board configuration block diagram**



Revision history

Table 4. **Document revision history**

Date	Revision	Changes
11-Jun-2026	1	Initial release.

Contents

List of tables

List of figures