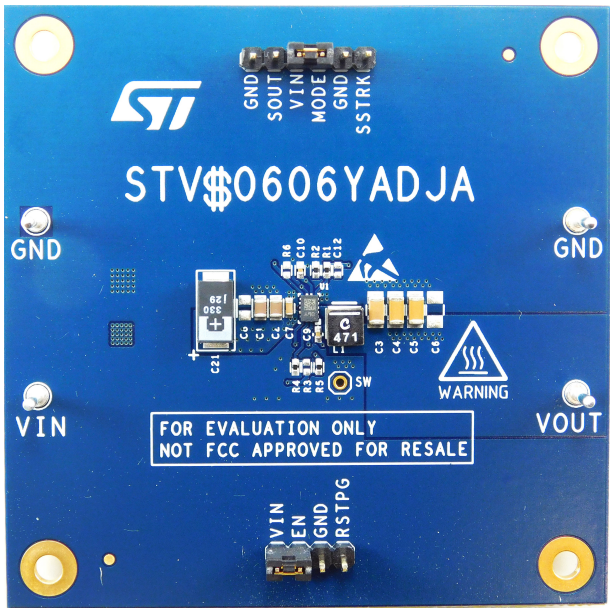
Getting started with STEVAL-0606YADJ evaluation board based on DCP0606QTRY, automotive 6 V - 6 A step-down converter

Introduction

The STEVAL-0606YADJ product evaluation board is a step-down switching power supply based on the DCP0606QTRY regulator. The target application is 5 V to 3.3 V with up to 6 A continuous load, 2.25 MHz programmed switching frequency and 3 ms soft-start. With minor BOM changes, the programmed output voltage, switching frequency and soft-start can be arranged to meet different requirements. The DCP0606Y is a high efficiency monolithic step-down synchronous switching regulator designed to deliver up to 6 A continuous current, operating from 2.9 V to 6 V input voltage. The DCP0606Y features low-resistance integrated N-channel MOSFETs (11 mΩ typ.) and diode emulation working mode for optimum efficiency over all the loading range. The integrated 0.6V reference allows the regulation of output voltages with ±1.5% accuracy over temperature variations. The switching frequency with ±5% dithering is externally selectable between 1.8 MHz and 4 MHz. The high power conversion efficiency over all the load range is guaranteed when the low consumption Mmode (LCM) is selected, whereas the constant frequency operation with minimum output voltage noise is achieved when the low noise mode (LNM) is chosen. MODE/SIN input pin can be exploited to implement dynamic transitions between LCM – LNM during the regulator operation or to synchronize the DCP0606Y to an external clock. The soft-start duration can be adjusted with external capacitor or the same SS/TRK pin can be used for output voltage sequencing while RST/PGOOD pin provides real-time information on the output voltage. On SOUT pin the clock-out signal is available to synchronize up to 3 DCP0606Y slaves, with selectable phase shifting, to minimize the RMS input current and improve EMC. The DCP0606Y is available in QFN11 2x3 mm with wettable flanks.

Figure 1. STEVAL-0606YADJ evaluation board



Notice: *For dedicated assistance, submit a request through our online support portal at **www.st.com/support**.*

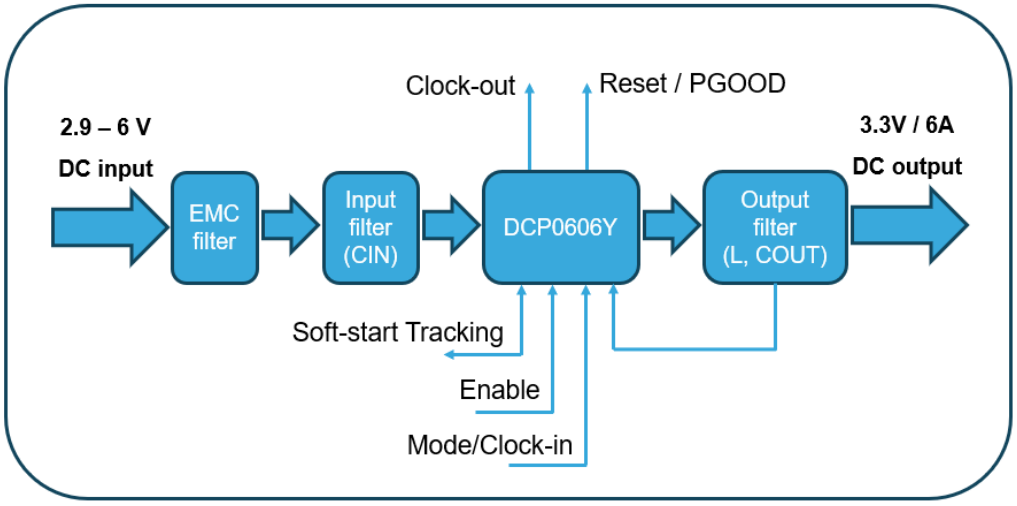
1 Getting started

1.1 Safety instructions

This board is intended for use by skilled technical personnel who are suitably qualified and familiar with the installation, use and maintenance of power electronic systems. The same personnel must be aware of and must apply national accident prevention rules. The electrical installation shall be completed in accordance with the appropriate requirements (e.g., cross-sectional areas of conductors, fusing, and GND connections).

Functional block diagram

Figure 2. STEVAL-0606YADJ block diagram



Features

- Step-down DC/DC switching converter
- AEC-Q100 Grade 1 qualified
- Operating Junction Temperature range: -40°C to +150°C
- 3.3 V output , up to 6 A load
- 2.25 MHz switching frequency with dithering
- Programmed 3 ms soft-start
- Up to 6 V DC input voltage
- 3 µA typ. shutdown current
- 70 µA typ. operating quiescent current (LCM, SOUT=GND)
- Peak current mode architecture with integrated compensation
- Dynamically selectable low noise mode (LNM) or low consumption mode (LCM) operation
- Autorecovery Overvoltage / Overcurrent / Overtemperature protection
- Reset / Power good with 2 ms typ. assertion delay
- Synchronizable to external clock
- QFN11 2x3 mm package

2 How to use the board

To properly evaluate the STEVAL-0606YADJ board, the below listed steps should be followed.
For a more detailed understanding of the DCP0606Y operation, refer to DS14883.

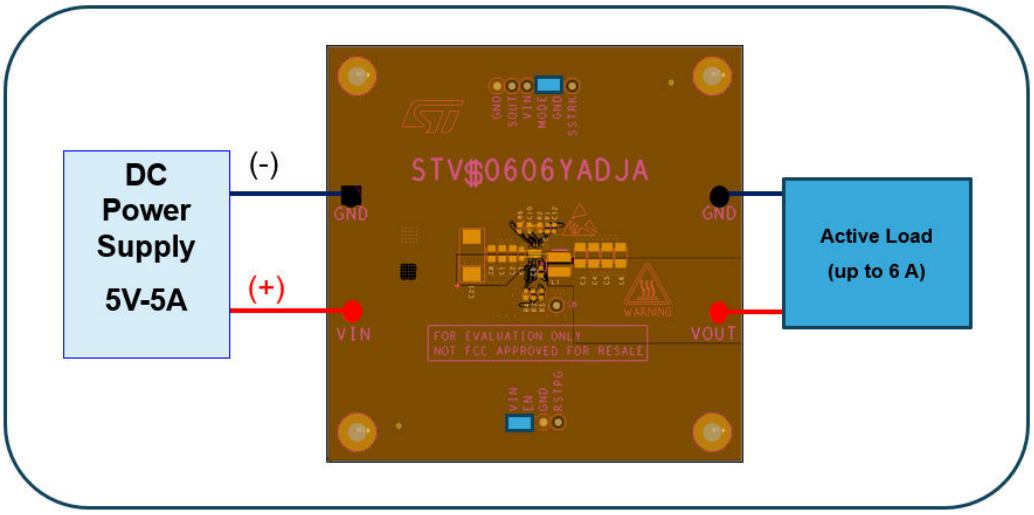
Step 1. Connect the power supply to the terminal pin of VIN and GND

Step 2. Connect the load to the terminal pin of VOUT and GND

Step 3. Set the supply voltage VIN to 5 V and switch the power supply on

Step 4. Vary the active load in the range 0 - 6 A

Figure 3. STEVAL-0606YADJ testing setup



3 Connectors and test points

3.1 Connectors

VIN

The input voltage is provided, through the EMC filter, to the pin VIN of the device. A power supply ranging from 2.9V to 6V should be connected to this test point, setting a proper current limit depending on the expected maximum load.

The wire connection should be as short as possible to avoid or limits oscillations due to the parasitic inductance of the wire and the input capacitor.

GND

Return of the terminal of the input and output capacitors.

VOUT

Regulated output voltage, 3.3 V programmed.

3.2 Test points

EN

The ENABLE input must be forced above 1.2 V to turn-on the DCP0606Y. This can be achieved by shorting to VIN through a jumper, as shown in Figure 3.

RSTPG

This test point is directly connected to the RESET / PGOOD output pin. A 100 kΩ pull-up resistor to VIN is already mounted in the board.

SSTRK

This test point is directly connected to SS/TRK pin. A 10 nF capacitor mounted between the pin and GND programs 3ms soft-start.

MODE

Directly connected to MODE/SIN pin to enable the LCM working mode (when forced to GND) or the LNM working mode (when forced to VIN) or to synchronize to an external clock. MODE can be toggled during DCP0606Y operation to implement dynamic transition between LCM – LNM.

SOUT

Clock-out signal with programmable phase shift to synchronize up to 3 additional DCP0606Y. If not required, it can be shorted to GND through a jumper before powering up the regulator.

4 STEVAL-0606YADJ layout

The STEVAL-0606YADJ is a 4-layer PCB, 70 x 70 mm with 1oz copper thickness.

Figure 4. PCB layout (top)

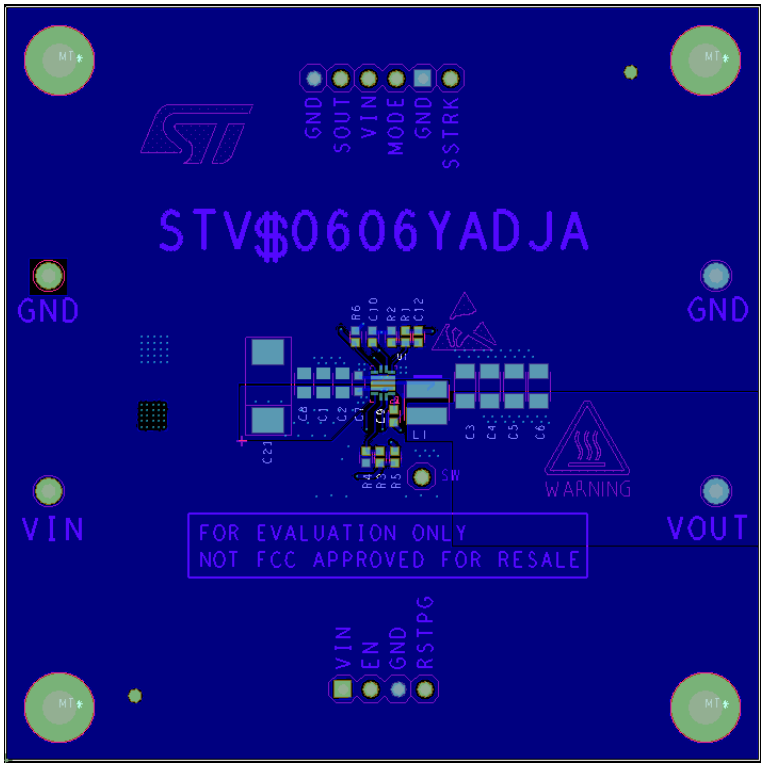


Figure 5. PCB layout (internal layer 1)

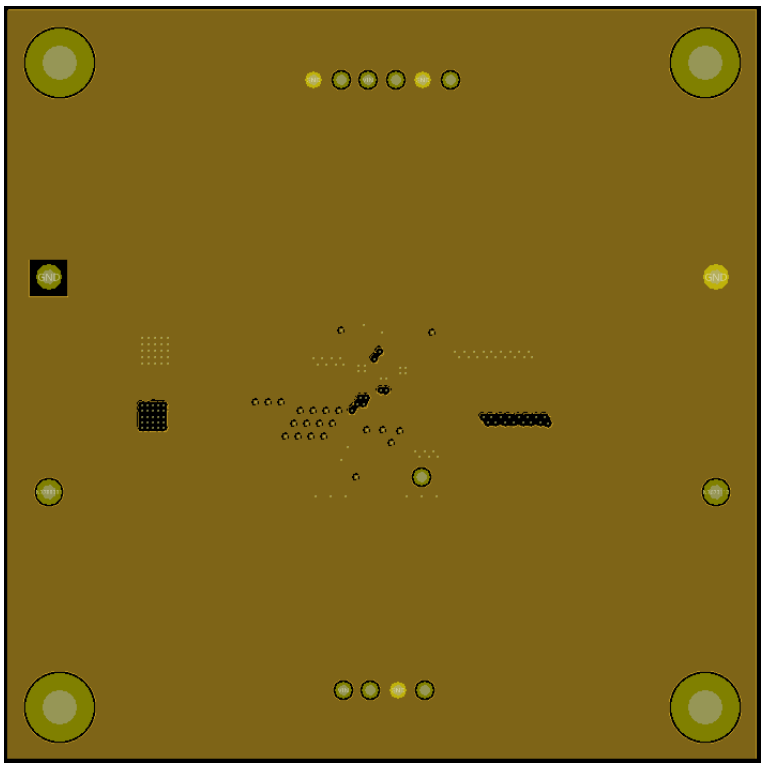


Figure 6. **PCB layout (internal layer 2)**

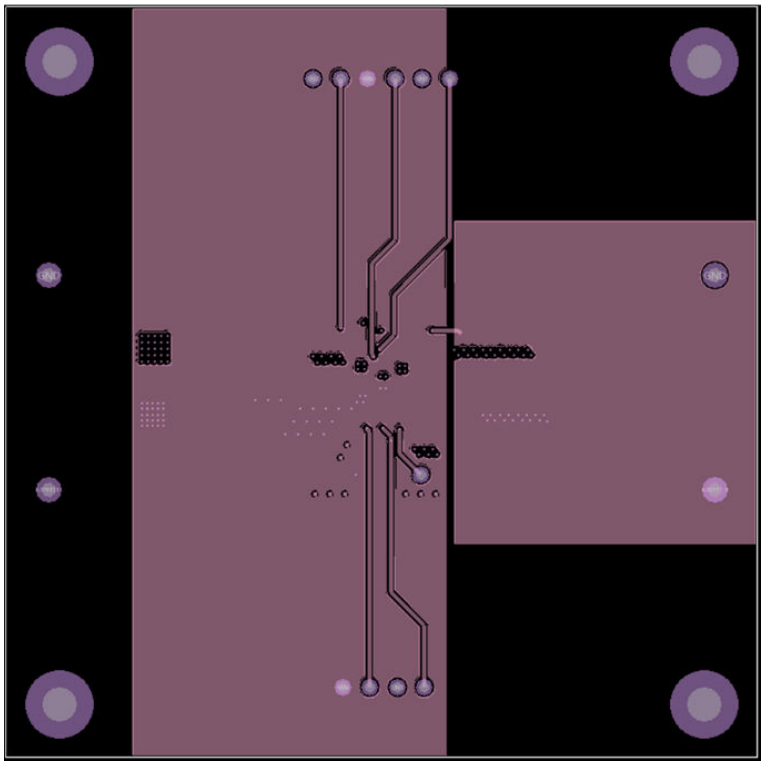
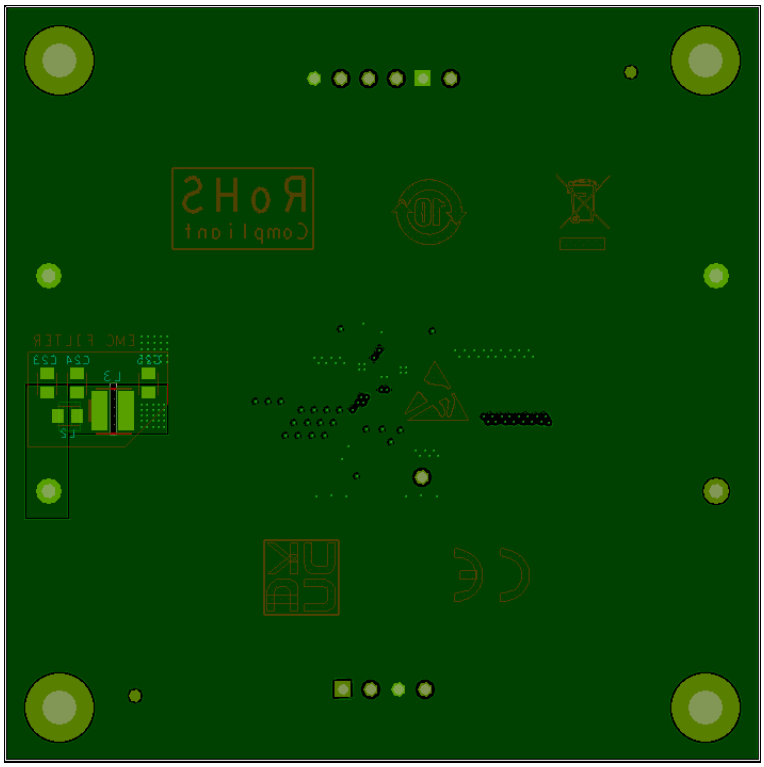


Figure 7. **PCB layout (bottom)**



5 STEVAL-0606YADJ performance and waveforms

Figure 8. Efficiency (log. Scale, EMC filter excluded)

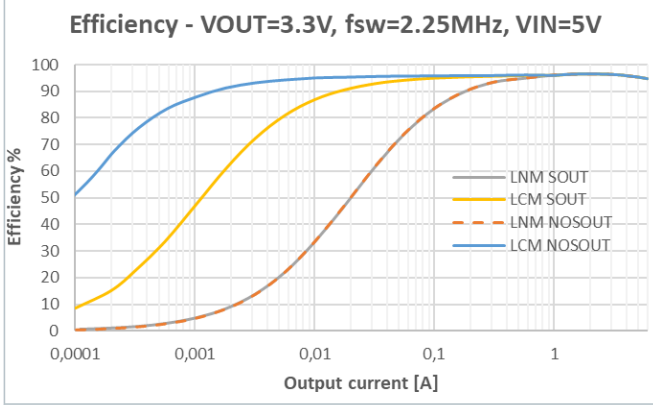


Figure 9. Efficiency (linear scale, EMC filter excluded)

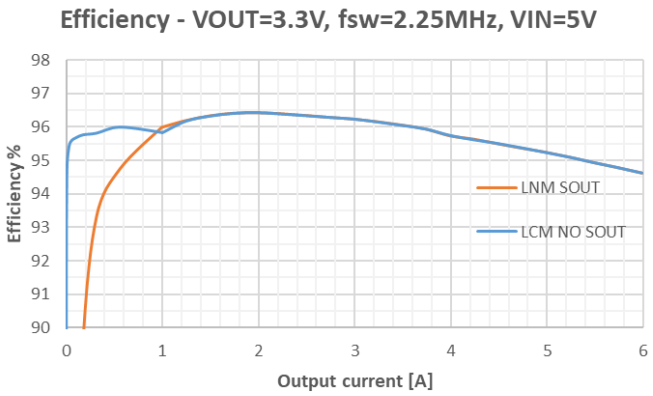


Figure 10. Load regulation

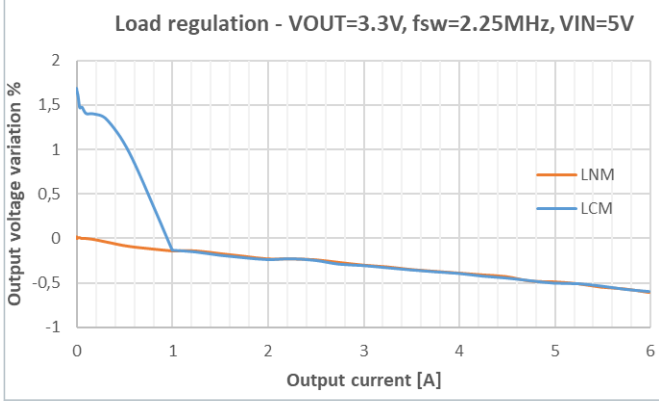


Figure 11. Total losses (log. Scale, EMC filter excluded)

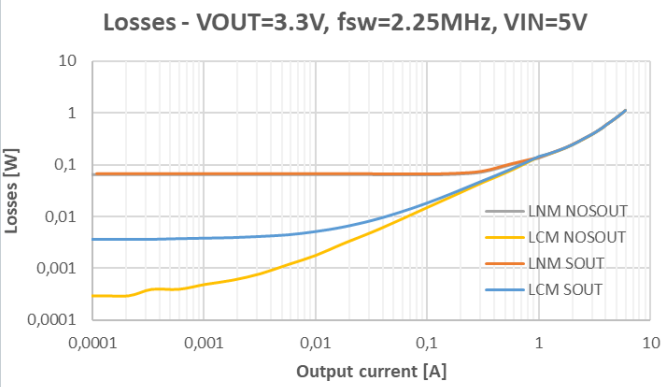


Figure 12. Thermal behavior – VIN=5 V, IOUT=6 A, 5 minutes settlement time, Tamb=25°C

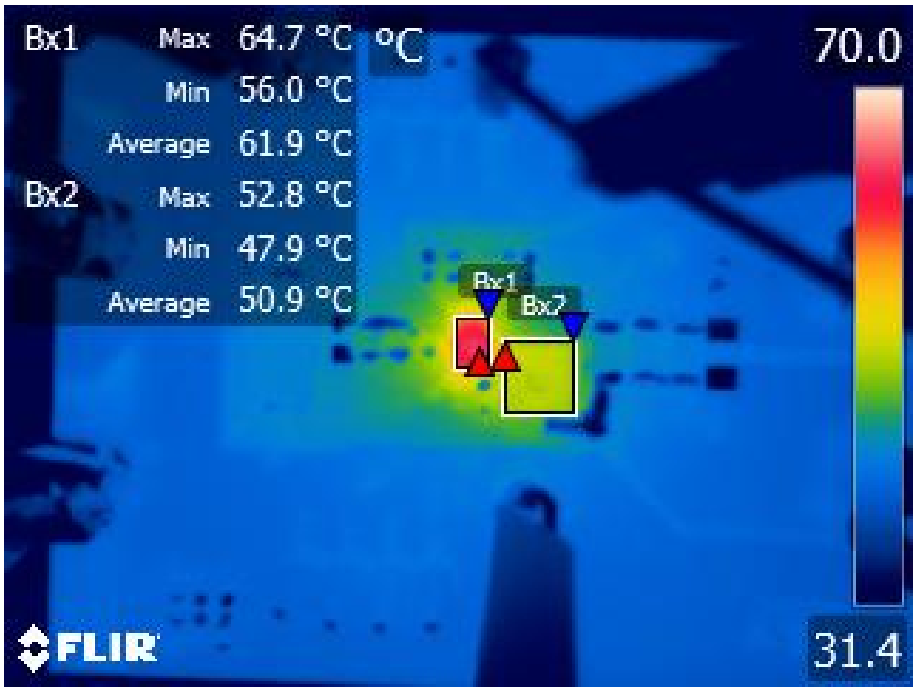


Figure 13. Oscilloscope waveform – LCM, no load

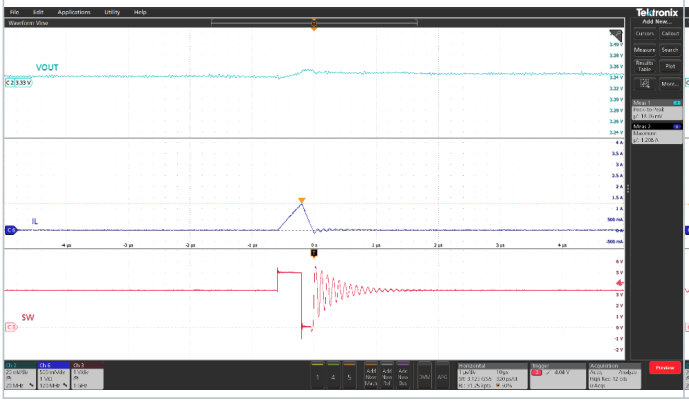


Figure 14. Oscilloscope waveform – LCM, 100 mA load

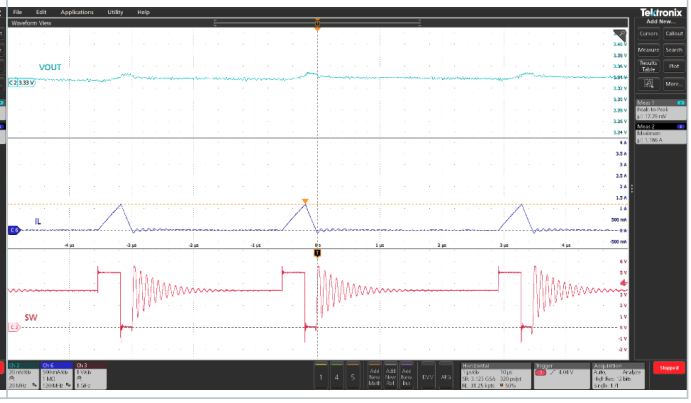


Figure 15. Oscilloscope waveform – LCM, 6 A load

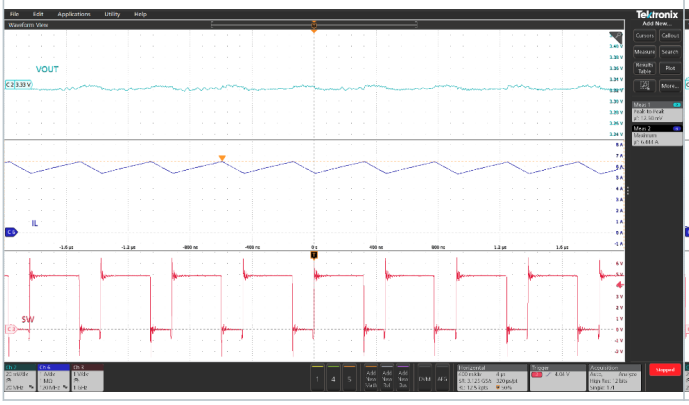


Figure 16. Oscilloscope waveform – LNM, no load

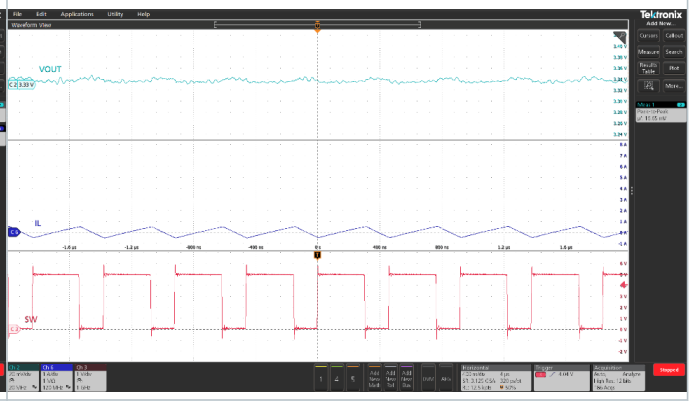


Figure 17. Oscilloscope waveform – LNM, load transient

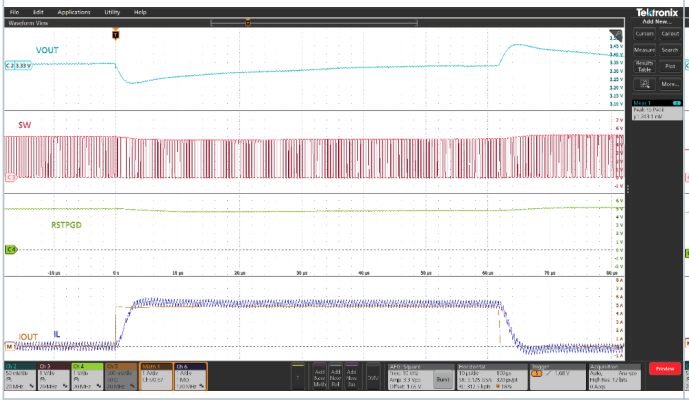


Figure 18. Oscilloscope waveform – LCM, load transient

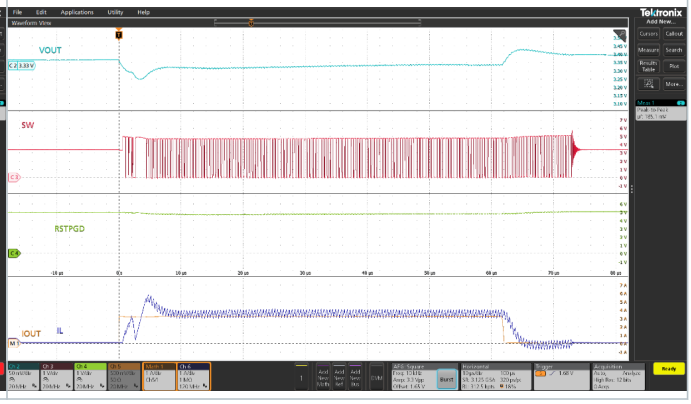


Figure 19. Oscilloscope waveform – LCM to LNM transition

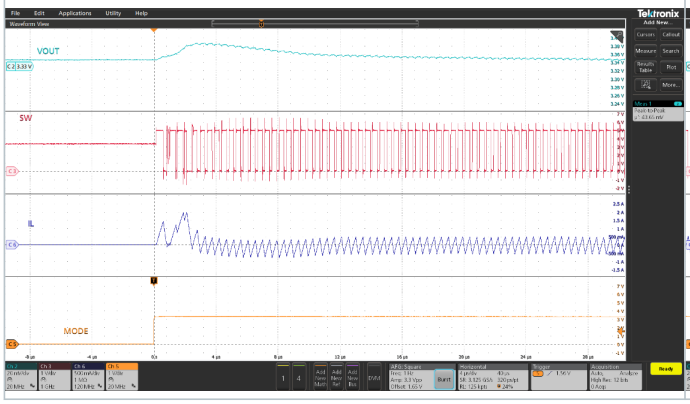
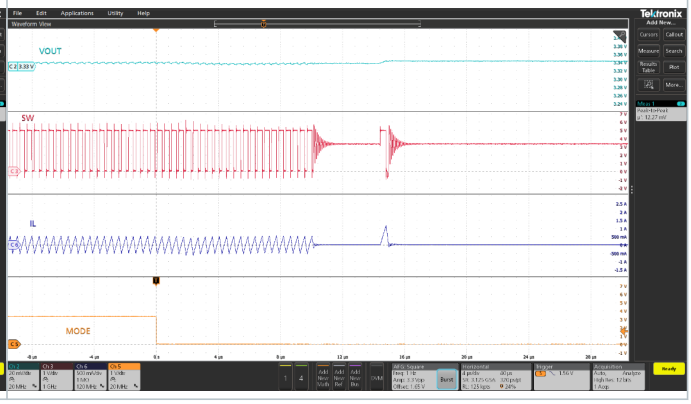


Figure 20. Oscilloscope waveform – LNM to LCM transition



6 STEVAL-0606YADJ EMC compliance

The STEVAL-0606YADJ is certified by an external supervisor company and is Class A compliant with the following standards, for industrial use only:

Table 1. List of standards which the STEVAL-0606YADJ complies

Reference standard	Standard application
CISPR 32:2015 +A1:2019 / EN 55032:2015 + A1:2020 CISPR 35:2016 / EN 55035:2017 + A11:2020 IEC 61000-3-2:2018 + A1:2020 EN IEC 61000-2-3:2019 + A1:2021 IEC 61000-3-3:2013 + A1:2017 + A2:2021 EN 61000-3-3:2013 + A1:2019 + A2:2021	Full
FCC CFR 47 Part 15 Subpart B	Full
ICES-003 Issue 7 (2020)	Full

The input EMC filter made of C24 and L3, mounted in the bottom side of the board, has the main purpose of reducing the EMI noise to guarantee the STEVAL-0606YADJ compliance with CISPR16-4-2 test standard and the other specifications listed above.

7 Disclaimer

The certification of the STEVAL-0606YADJ is fulfilled with the schematic, the layout and the BOM indicated in the sections Section 11, Section 4 and Section 12.

Any drift from the schematic, the layout and the BOM described in the sections Section 11, Section 4 and Section 12 invalidates the certification and the EMC compliance of the STEVAL-0606YADJ is no longer ensured.

Any change in the schematic, layout and BOM implemented by the user of the STEVAL-0606YADJ are under the user's responsibility.

The recommended changes in the BOM described in the next chapters should be considered as possible application ideas in case the user wish to adapt the board to other typical application requirements.

Although the recommended modifications can be considered as minor changes, the certification of the STEVAL-0606YADJ remains valid only under the conditions mentioned in the sections Section 11, Section 4 and Section 12.

8 Board setting capability

The STEVAL-0606YADJ provides the possibility to change some setting in accordance with the application conditions.

Output voltage

The regulated output voltage is set to 3.3 V. If a different voltage is desired, the output resistor divider should be adjusted according to the following equation:

$$V_{OUT} = 0.6 \cdot \left(1 + \frac{R_1}{R_2}\right)$$

Switching frequency and COUT

The switching frequency can be changed by selecting the appropriate resistor value, R4=RFSET, as described in the table below:

Table 2. Switching frequency and COUT configuration

RFSET [kΩ] 1%	FSW [MHz]	KC [µF*V]
FSET=VIN	2.25 (No dithering)	100
100	1.8	200
82	2.25	200
68	3.5	200
47	4	200
33	1.8	100
27	2.25	100
22	3.5	100
15	4	100
10	1.8	50
8.2	2.25	50
6.8	3.5	50
4.7	4	50
FSET=GND	2.25 (No dithering)	50

The spread spectrum feature (dithering) is always implemented unless FSET is shorted to VIN or GND.

RFSET value is also impacting the integrated compensation network, summarized in the KC parameter (third column).

KC is providing the minimum suggested output capacitance value to guarantee a stable operation:

$$C_{OUT} \geq \frac{K_C}{V_{OUT}}$$

To optimize the DCP0606Y dynamic behavior, choose the RFSET resistor that select the required switching frequency and program the KC value closer to the actual output capacitance value (considering the expected derating due to the working voltage).

Soft start

The soft start interval is 3 ms. It can be modified by selecting a different C10=CSS capacitor, following the equation below, considering ISS=2 uA and VREF=VFB=0.6 V:

$$C_{SS} = \frac{T_{SS} \cdot I_{SS}}{V_{REF}}$$

Until SS pin is kept lower than VFB (0.6 V typ.) the tracking function is enabled. This feature can be exploited to program a proportional power-up and ramp-up sequence. As soon as SS voltage is higher than 0.6 V, the control loop reference switches to the internal voltage reference and SS pin is left in high impedance.

Clock-out (SOUT)

SOUT pin is providing the clock-out signal, available on SOUT test point. Based on the R6=RSOUT resistor, the following phase shifting can be programmed on the clock-out:

Table 3. SOUT phase shifting programming

RSOUT [kΩ]	Phase shift [°]	Devices
N.M.	180	Master + 1
100	120	Master + 2
75	90	Master + 3

In this way, up to four DCP0606Y can be synchronized with proportional phase shift.

If the clock-out feature is not required, SOUT test point must be shorted to GND before powering up the regulator, to improve light load efficiency above all in LCM mode.

9 eDesignSuite

The eDesignSuite software available on the www.st.com website helps in the selection of the devices as well as in the design of the external components suitable for a certain application.

After inserting the application conditions, the device can be selected and the design of the external components is automatically carried out.

10 Application idea

10.1 Typical applications

With minor changes in the BOM, the most used voltage conversions are achieved, as summarized in table below.

Table 4. Typical applications (fsw = 2.25 MHz)

VIN [V]	VOUT [V]	Inductor (L1) [nH]	COUT (C3 to C6) [uF]	R4 [kΩ]	R1 [kΩ]	R2 [kΩ]
5	3.3	470	3x 22 uF	27	68	15
5	3.0	470	3x 22 uF	27	30	7.5
3.3 – 5	2.5	400	3x 22 uF	27	51	16
3.3 – 5	1.8	300	2x 47 uF	27	30	15
3.3 – 5	1.5	240	2x 47 uF	27	30	20
3.3 – 5	1.2	240	3x 47 uF	27	20	20
3.3 – 5	1.0	200	3x 47 uF	27	10	15
3.3	0.82	200	3x 47 uF	8.2	11	30

The expected performance is shown in the curves below:

Figure 21. Efficiency vs. VOUT – VIN = 5 V - LNM

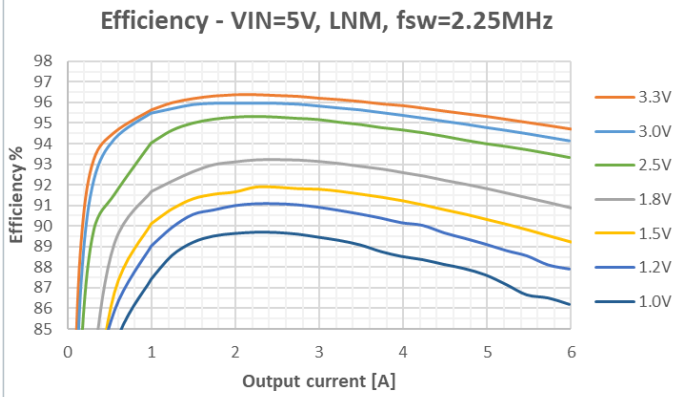


Figure 22. Efficiency vs. VOUT – VIN = 5 V - LCM (SOUT=GND)

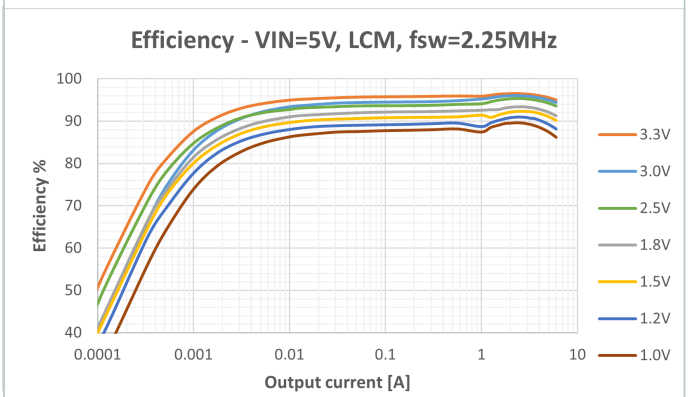


Figure 23. **Efficiency vs VOUT – VIN = 3.3 V - LNM**

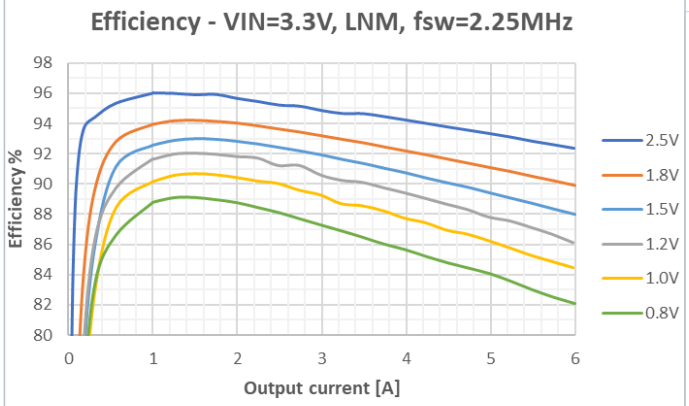


Figure 24. **Efficiency vs. VOUT – VIN = 3.3 V - LCM (SOUT=GND)**

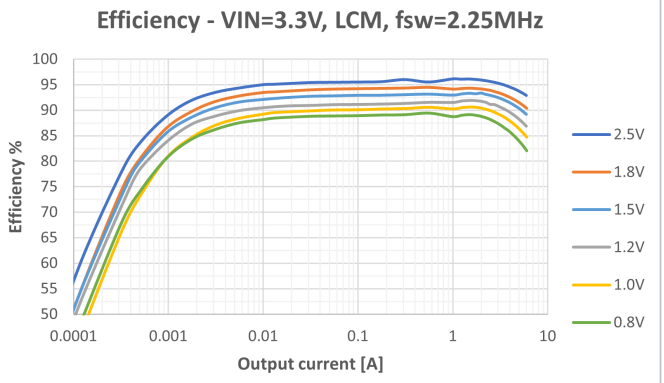


Figure 25. **Total losses vs VOUT – VIN = 5 V – LNM**

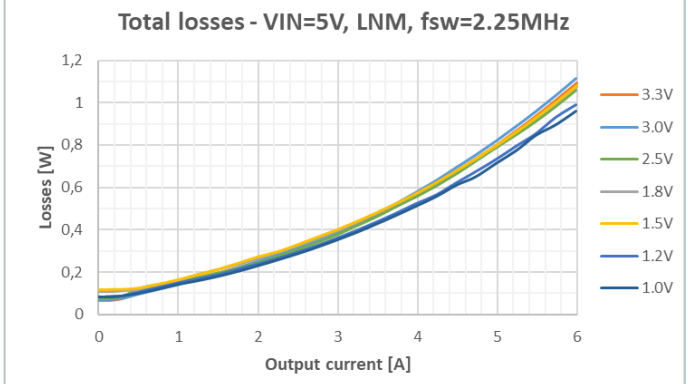
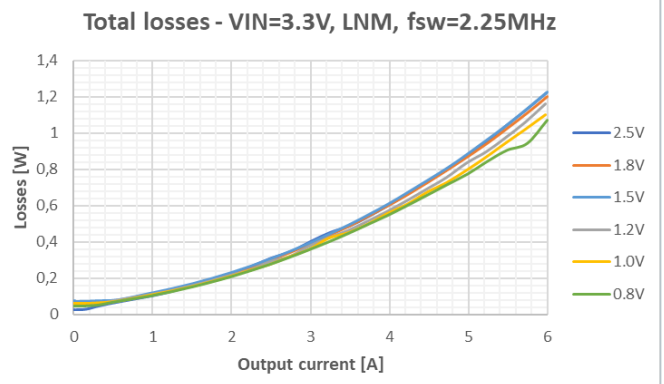
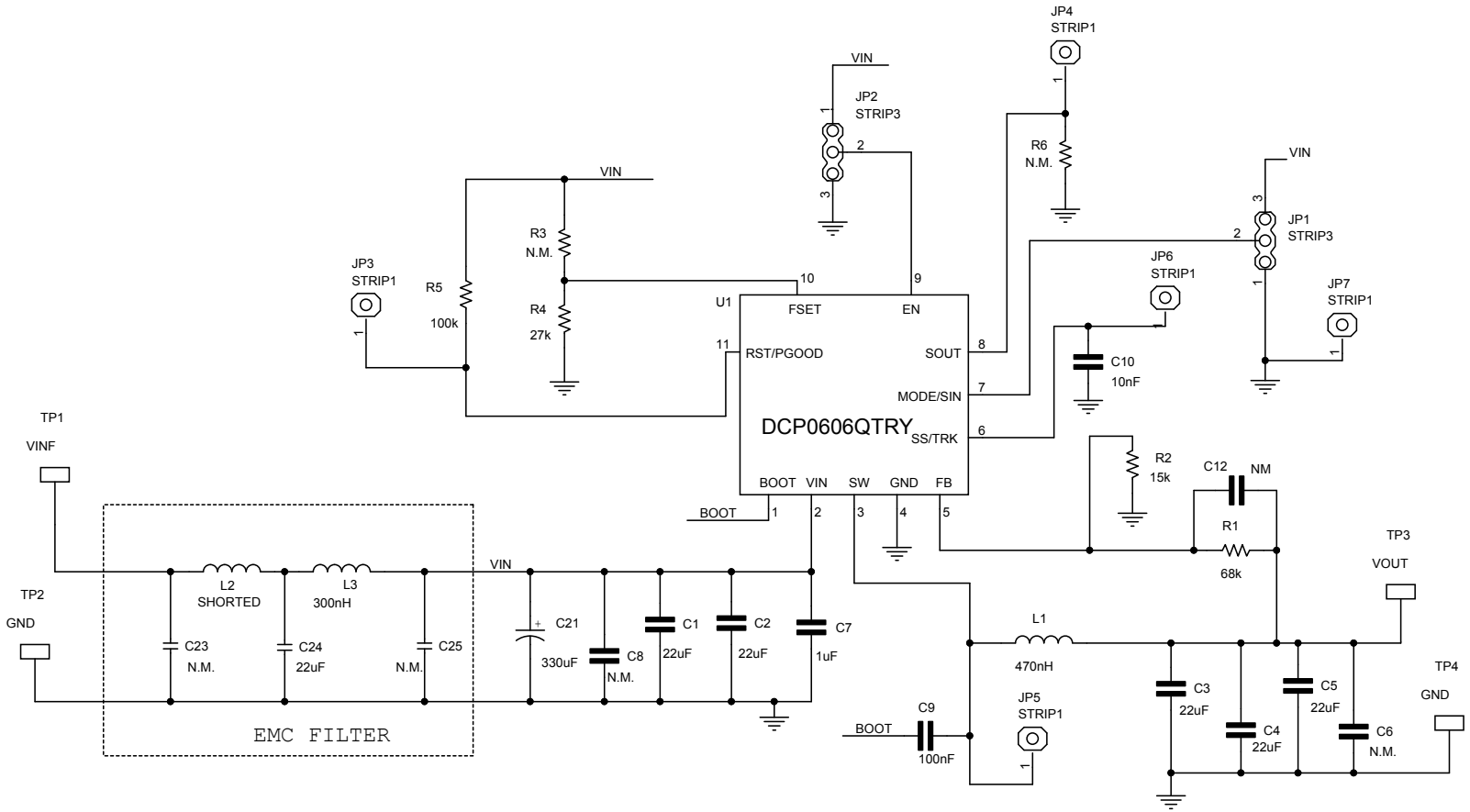


Figure 26. **Total losses vs. VOUT – VIN = 3.3 V – LNM**



11 Schematic diagrams

Figure 27. **STEVAL-0606YADJ circuit schematic**



12 Bill of materials

Table 5. **STEVAL-0606YADJ bill of materials**

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	3	C1, C2, C24	22 uF	Ceramic capacitor X7T/10V/20%	Murata	GRT21BD71A226ME13
2	3	C3, C4, C5	22 uF	Ceramic capacitor X7R/10V/10%	Murata	GCM31CR71A226KE
3	1	C7	1 uF	Ceramic capacitor X7R/25V/10%	Murata	GCM188R71E105KA
4	1	C9	100 nF	Ceramic capacitor X7R/16V/10%	Murata	GRT155R71C104KE
5	1	C10	10 nF	Ceramic capacitor X7R/25V/5%	KEMET YAGEO	C0402C103J3RACAUTO
6	1	C21	330 uF	Polymer Tantalum Capacitor	Panasonic	6TAE330ML
7	4	C6, C8, C12, C23, C25		(not mounted)		
8	1	L1	470 nH	Shielded Power Inductor	Coilcraft	XGL4030-471ME
9	1	L3	300 nH	Shielded Power Inductor	Coilcraft	XGL3020-301ME
10	1	L2		(not mounted)		
11	1	R1	68 k	Thick film resistor	MULTICOMP PRO	MP003495
12	1	R2	15 k	Thick film resistor	MULTICOMP PRO	MP003483
13	1	R4	27 k	Thick film resistor	MULTICOMP PRO	MP003487
14	1	R5	100 k	Thick film resistor	MULTICOMP PRO	MP003498
15	2	R3, R6		(not mounted)		
16	1	JP1 + JP4 + JP6 + JP7	header	6 Way, 1 Row, Straight Pin Header, 2,54 mm pitch, 6mm height	TE Connectivity	826936-6
17	1	JP2 + JP3	header	4 Way, 1 Row, Straight Pin Header, 2,54 mm pitch, 6mm height	TE Connectivity	826936-4
18	1	JP5		(not mounted)		
19	4	TP1, TP2, TP3, TP4	terminal pin	Brass terminal pin	Ettinger	013.14.239
20	1	U1	DCP0606QTRY QFN 2x3 11 Leads	Automotive 6V - 6A step-down DC/DC regulator	ST	DCP0606QTRY
21	2	Jumpers		Female Straight Black Open 2 Way 1 Row 2.54mm Pitch	RS PRO	251-8682

13 Board versions

Table 6. **STEVAL-0606YADJ versions**

Finished good	Schematic diagrams	Bill of materials
STV$0606YADJA(1)	STV$0606YADJA schematic diagrams	STV$0606ADJA bill of materials

1. *This code identifies the STEVAL-0606YADJ evaluation board first version.*

14 Regulatory compliance information

Notice for US Federal Communication Commission (FCC)

For evaluation only; not FCC approved for resale

FCC NOTICE - This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine

whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter 3.1.2.

Notice for Innovation, Science and Economic Development Canada (ISED)

For evaluation purposes only. This kit generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to Industry Canada (IC) rules.

À des fins d'évaluation uniquement. Ce kit génère, utilise et peut émettre de l'énergie radiofréquence et n'a pas été testé pour sa conformité aux limites des appareils informatiques conformément aux règles d'Industrie Canada (IC).

Notice for the European Union

This device is in conformity with the essential requirements of the Directive 2014/30/EU (EMC) and of the Directive 2011/65/EU (RoHS II), including subsequent revisions and additions, as well as amended by the Delegated Directive 2015/863/EU (RoHS III).

Notice for the United Kingdom

This device is in compliance with the UK Electromagnetic Compatibility Regulations 2016 (UK S.I. 2016 No. 1091) and with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations 2012 (UK S.I. 2012 No. 3032).

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
03-Jun-2025	1	Initial release.

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