UltraScale+ FPGAs
Product Tables and Product Selection Guide

KINTEX UltraSCALE+ VIRTEX UltraSCALE+

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Kintex® UltraScale+™ FPGAs

	Device Name	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P
Logic	System Logic Cells (K)	356	475	600	653	747	1,143
	CLB Flip-Flops (K)	325	434	548	597	683	1,045
	CLB LUTs (K)	163	217	274	299	341	523
Memory	Max. Distributed RAM (Mb)	4.7	6.1	8.8	9.1	11.3	9.8
	Total Block RAM (Mb)	12.7	16.9	32.1	21.1	26.2	34.6
	UltraRAM (Mb)	13.5	18.0	0	22.5	31.5	36.0
Clocking	Clock Mgmt Tiles (CMTs)	4	4	4	8	4	11
Integrated IP	DSP Slices	1,368	1,824	2,520	2,928	3,528	1,968
	PCIe® Gen3 x16	1	1	0	4	0	5
	150G Interlaken	0	0	0	1	0	4
	100G Ethernet w/RS-FEC	0	1	0	2	0	4
I/O	Max. Single-Ended HD I/Os	96	96	96	96	96	96
	Max. Single-Ended HP I/Os	208	208	208	416	208	572
	GTH 16.3Gb/s Transceivers	0	0	28	32	28	44
	GTY 32.75Gb/s Transceivers	16	16	0	20	0	32
Speed Grades	Extended[1]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
	Industrial	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2	-1 -1L -2

	Footprint[2, 3]	Dimensions (mm)	HD I/O, HP I/O, GTH 16.3Gb/s, GTY 32.75Gb/s					
Footprint compatible with 20nm UltraScale Devices with same footprint identifier	B784[4]	23x23[5]	96, 208, 0, 16	96, 208, 0, 16				
	A676[4]	27x27	48, 208, 0, 16	48, 208, 0, 16				
	B676	27x27	72, 208, 0, 16	72, 208, 0, 16				
	D900[4]	31x31	96, 208, 0, 16	96, 208, 0, 16		96, 312, 16, 0		
	E900	31x31			96, 208, 28, 0		96, 208, 28, 0	
	A1156[4]	35x35				48, 416, 20, 8		48, 468, 20, 8
	E1517	40x40				96, 416, 32, 20		96, 416, 32, 24
	A1760	42.5x42.5						96, 416, 44, 32
	E1760	42.5x42.5						96, 572, 32, 24

Notes:
1. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS890, UltraScale Architecture and Product Overview.
2. Maximum achievable performance is device and package dependent; consult the associated data sheet for details.
3. For full part number details, see the Ordering Information section in DS890, *UltraScale Architecture and Product* Overview.
4. GTY transceiver line rates are package limited: B784 to 12.5 Gb/s; A676, D900, and A1156 to 16.3 Gb/s. Refer to data sheet for details.
5. The B784 package is only offered in 0.8mm ball pitch. All other packages are 1.0mm ball pitch.

Virtex® UltraScale+™ FPGAs

			Foundation							58G PAM4	
		Device Name	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU19P	VU27P	VU29P
		System Logic Cells (K)	862	1,314	1,724	2,586	2,835	3,780	8,938	2,835	3,780
		CLB Flip-Flops (K)	788	1,201	1,576	2,364	2,592	3,456	8,172	2,592	3,456
		CLB LUTs (K)	394	601	788	1,182	1,296	1,728	4,086	1,296	1,728
		Max. Dist. RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	58.4	36.2	48.3
		Total Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	75.9	70.9	94.5
		UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	90.0	270.0	360.0
		HBM DRAM (GB)	–	–	–	–	–	–	–	–	–
		HBM AXI Interfaces	–	–	–	–	–	–	–	–	–
		Clock Mgmt Tiles (CMTs)	10	20	20	30	12	16	40	16	16
		DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	3,840	9,216	12,288
		Peak INT8 DSP (TOP/s)	7.1	10.8	14.2	21.3	28.7	38.3	10.4	28.7	38.3
		PCIe® Gen3 x16	2	4	4	6	3	4	0	1	1
		PCIe Gen3 x16/Gen4 x8 / CCIX[1]	–	–	–	–	–	–	8	–	–
		150G Interlaken	3	4	6	9	6	8	0	8	8
		100G Ethernet w/ KR4 RS-FEC	3	4	6	9	9	12	0	15	15
		Max. Single-Ended HP I/Os	520	832	832	832	624	832	1,976	676	676
		Max. Single-Ended HD I/Os							96		
		GTY 32.75Gb/s Transceivers	40	80	80	120	96	128	80	32	32
		GTM 58Gb/s PAM4 Transceivers							–	48	48
		100G / 50G KP4 FEC							–	24 / 48	24 / 48
		Extended[2]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2	-1 -2 -2L -3	-1 -2 -2L -3
		Industrial	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	–	-1 -2	-1 -2
	Footprint[3,4,5]	Dim. (mm)	HP I/O, GTY						HP I/O, HD I/O, GTY	HP I/O, GTY, GTM	
Footprint compatible with 20nm UltraScale Devices with same footprint identifier	C1517	40x40	520, 40								
	F1924[6]	45x45					624, 64				
	A2104	47.5x47.5		832, 52	832, 52	832, 52					
		52.5x52.5[7]						832, 52			
	B2104	47.5x47.5		702, 76	702, 76	702, 76	572, 76				
		52.5x52.5[7]						702, 76			
	C2104	47.5x47.5		416, 80	416, 80	416, 104	416, 96				
		52.5x52.5[7]						416, 104			
	D2104	47.5x47.5				676, 76	572, 76				
		52.5x52.5[7]						676, 76		676, 16, 30	676, 16, 30
	A2577	52.5x52.5				448, 120	448, 96	448, 128		448, 32, 48	448, 32, 48
	A3824	65x65							1976, 96,48		
	B3824	65x65							1664, 96, 80		

1. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213.
2. -2LE (Tj = 0°C to 110°C). See Ordering Information in DS890.
3. For full part number details, see DS890, *UltraScale Architecture and Product Overview*.
4. All packages are 1.0mm ball pitch.
5. Consult UG583, *UltraScale Architecture PCB Design User Guide* for specific migration details.
6. The GTY transceiver line rate in the F1924 footprint is package limited to 16.3Gb/s. Refer to data sheet for details.
7. These 52.5x52.5mm packages have the same PCB ball footprint as the 47.5x47.5mm packages and are footprint compatible.

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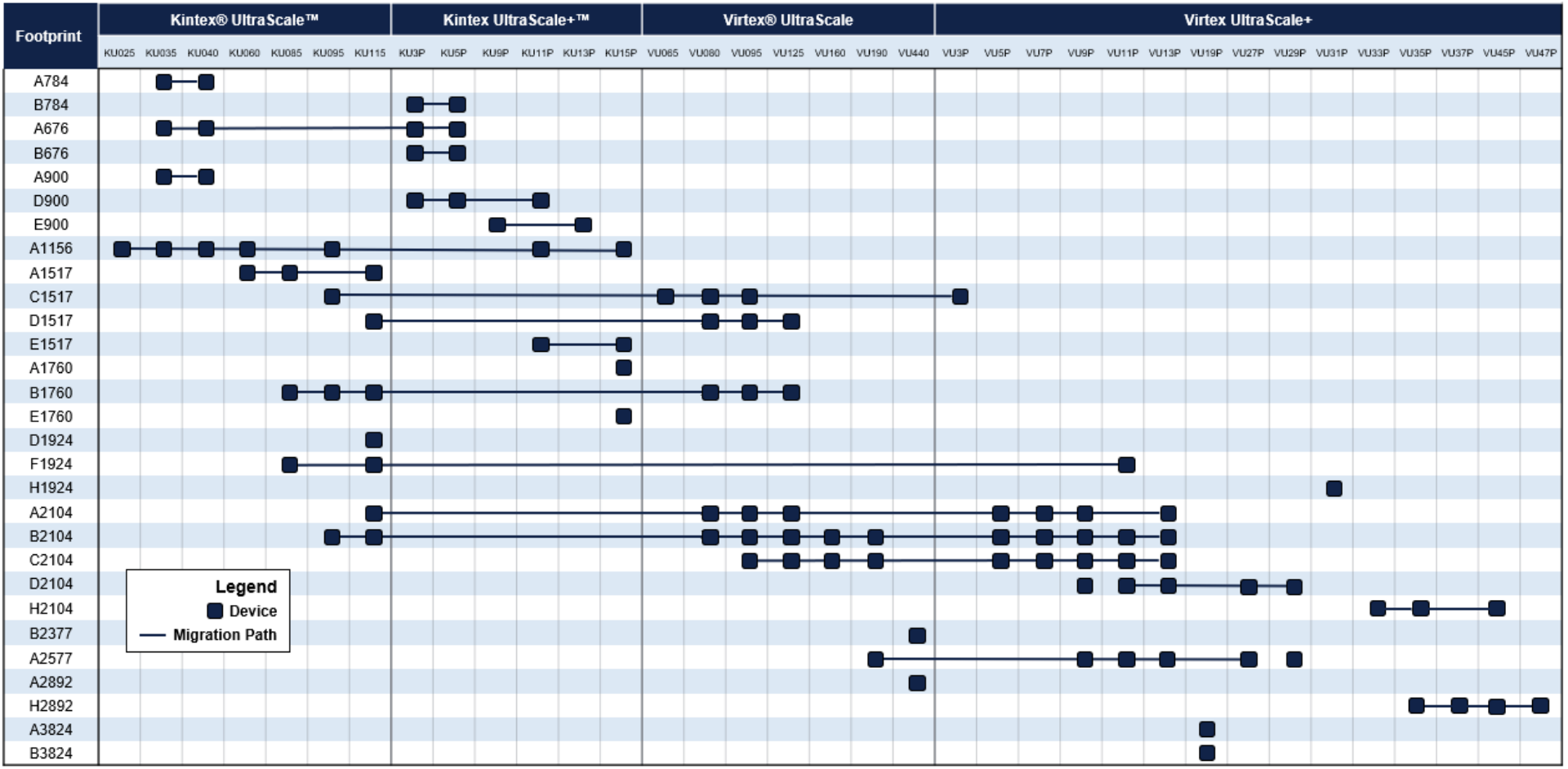
	HBM (4GB)	HBM (8GB)			HBM (16GB)	
Device Name	VU31P	VU33P	VU35P	VU37P	VU45P	VU47P
System Logic Cells (K)	962	962	1,907	2,852	1,907	2,852
CLB Flip-Flops (K)	879	879	1,743	2,607	1,743	2,607
CLB LUTs (K)	440	440	872	1,304	872	1,304
Max. Dist. RAM (Mb)	12.5	12.5	24.6	36.7	24.6	36.7
Total Block RAM (Mb)	23.6	23.6	47.3	70.9	47.3	70.9
UltraRAM (Mb)	90.0	90.0	180.0	270.0	180.0	270.0
HBM DRAM (GB)	4	8	8	8	16	16
HBM AXI Interfaces	32	32	32	32	32	32
Clock Mgmt Tiles (CMTs)	4	4	8	12	8	12
DSP Slices	2,880	2,880	5,952	9,024	5,952	9,024
Peak INT8 DSP (TOP/s)	8.9	8.9	18.6	28.1	18.6	28.1
PCIe® Gen3 x16	0	0	1	2	1	2
PCIe Gen3 x16/Gen4 x8 / CCIX[1]	4	4	4	4	4	4
150G Interlaken	0	0	2	4	2	4
100G Ethernet w/ KR4 RS-FEC	2	2	5	8	5	8
Max. Single-Ended HP I/Os	208	208	416	624	416	624
GTY 32.75Gb/s Transceivers	32	32	64	96	64	96
GTM 58Gb/s PAM4 Transceivers	–	–	–	–	–	–
100G / 50G KP4 FEC	–	–	–	–	–	–
Extended[2]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3
Industrial	–	–	–	–	–	–

Footprint[3, 4, 5, 6]	Dim. (mm)	HP I/O, GTY				
H1924	45x45	208, 32				
H2104	47.5x47.5		208, 32	416, 64		416, 64	
H2892	55x55			416, 64	624, 96	416, 64	624, 96

1. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213.
2. -2LE (Tj = 0°C to 110°C). See Ordering Information in DS890.
3. For full part number details, see DS890, *UltraScale Architecture and Product Overview*.
4. All packages are 1.0mm ball pitch.
5. Consult UG583, *UltraScale Architecture PCB Design User Guide* for specific migration details.
6. Footprint compatible with 20nm UltraScale Devices with same footprint identifier.

UltraScale Architecture Migration Table

UltraScale and UltraScale+ families provide footprint compatibility to enable users to migrate designs from one device or family to another. Any two packages with the same footprint identifier code are footprint compatible.



Notes:

1.The body size of the VU13P device in the A2104, B2104, C2104, and D2104 packages is 52.5mm. These packages are footprint compatible with the corresponding 47.5mm body size packages. See UG583, *UltraScale Architecture PCB Design User Guide* for important migration details.

2.Virtex UltraScale+ HBM devices migrate among each other but do not migrate to other devices.

Kintex® UltraScale+™ FPGA Speed Grades

		Device Name[1]					
	Speed Grade	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P
Extended[2]	-1	•	•	•	•	•	•
	-2	•	•	•	•	•	•
	-2L	•	•	•	•	•	•
	-3	•	•	•	•	•	•
Industrial	-1	•	•	•	•	•	•
	-1L	•	•	•	•	•	•
	-2	•	•	•	•	•	•

Notes:
1. For full part number details, see the Ordering Information section in DS890, *UltraScale Architecture and Product Overview*.
2.-2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS890, *UltraScale Architecture and Product Overview*.

- • :: available
- – :: not offered

Virtex® UltraScale+™ FPGA Speed Grades

		Device Name[1]														
	Speed Grade	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU19P	VU27P	VU29P	VU31P	VU33P	VU35P	VU37P	VU45P	VU47P
Extended[2]	-1	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	-2	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	-2L	•	•	•	•	•	•	–	•	•	•	•	•	•	•	•
	-3	•	•	•	•	•	•	–	•	•	•	•	•	•	•	•
Industrial	-1	•	•	•	•	•	•	–	•	•	–	–	–	–	–	–
	-2	•	•	•	•	•	•	–	•	•	–	–	–	–	–	–

Notes:
1. For full part number details, see the Ordering Information section in DS890, *UltraScale Architecture and Product Overview*.
2.-2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS890, *UltraScale Architecture and Product Overview*.

- • :: available
- – :: not offered

UltraScale+ Device Ordering Information

Footprint

XC	V	U	#	P	-1	F	L	V	A	#	E
Xilinx Commercial	V: Virtex K: Kintex	UltraScale	Value Index	Denotes UltraScale+ Device	Speed Grade -1 = Slowest -L1 = Low Power -2 = Mid -L2 = Low Power -3 = Fastest	F: Flip-Chip (1.0mm) S: Flip-Chip (0.8mm)	F: Lid L: Lid SSI B: Lidless S: Lidless Stiffener H: Overhang SSI I: Overhang Lidless Stiffener	V: RoHS 6/6 G: RoHS 6/6 w/ Exemption 15	Package Designator	Package Pin Count	Temperature Grade (E, I)

E = Extended (Tj = 0°C to +100°C)
I = Industrial (Tj = –40°C to +100°C)

For valid part/package combinations,
go to DS890, *UltraScale Architecture and Product Overview:* Device-Package Combinations and Maximum I/Os Tables

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

References

DS890, *UltraScale™ Architecture and Product Overview*

DS922, *Kintex® UltraScale+™ FPGAs Data Sheet: DC and AC Switching Characteristics*

DS923, *Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics*

UG570, *UltraScale Architecture Configuration User Guide*

UG571, *UltraScale Architecture SelectIO™ Resources User Guide*

UG572, *UltraScale Architecture Clocking Resources User Guide*

UG573, *UltraScale Architecture Memory Resources User Guide*

UG574, *UltraScale Architecture Configurable Logic Block User Guide*

UG575, *UltraScale and UltraScale+ FPGAs Packaging and Pinouts Product Specification*

UG576, *UltraScale Architecture GTH Transceivers User Guide*

UG578, *UltraScale Architecture GTY Transceivers User Guide*

UG579, *UltraScale Architecture DSP Slice User Guide*

UG580, *UltraScale Architecture System Monitor User Guide*

UG583, *UltraScale Architecture PCB Design User Guide*

PG150, *UltraScale Architecture-Based FPGAs Memory IP Product Guide*

PG182, *UltraScale FPGAs Transceivers Wizard Product Guide*

Important: Verify all data in this document with the device data sheets found at www.xilinx.com