SCU35 Evaluation Board

User Guide

UG1713 (v1.0) November 21, 2025

AMD

Table of Contents

Chapter 1

Introduction

Overview

The SCU35 is an evaluation platform for the AMD Spartan™ UltraScale+™ XCSU35P FPGA. Spartan UltraScale+ devices and the SCU35 target industrial and healthcare applications with high I/O count, low power, and state-of-the-art security features enabled. The primary focus for the SCU35 is to enable solution demos for the development of applications.

The SCU35 evaluation board is equipped with many of the common board-level features needed for design development, including:

- Arduino Shield I/O expansion
- HSIO I/O expansion
- Raspberry Pi HAT I/O expansion
- HyperRAM memory
- PMOD I/O expansion
- Ethernet networking interface

Models of Boards

The following table lists the models for the evaluation board. See the SCU35 Evaluation Board product page for details.

Table 1: **Models of Evaluation Boards**

Kit	Description
EK-SCU35-G	AMD Spartan UltraScale+ evaluation kit

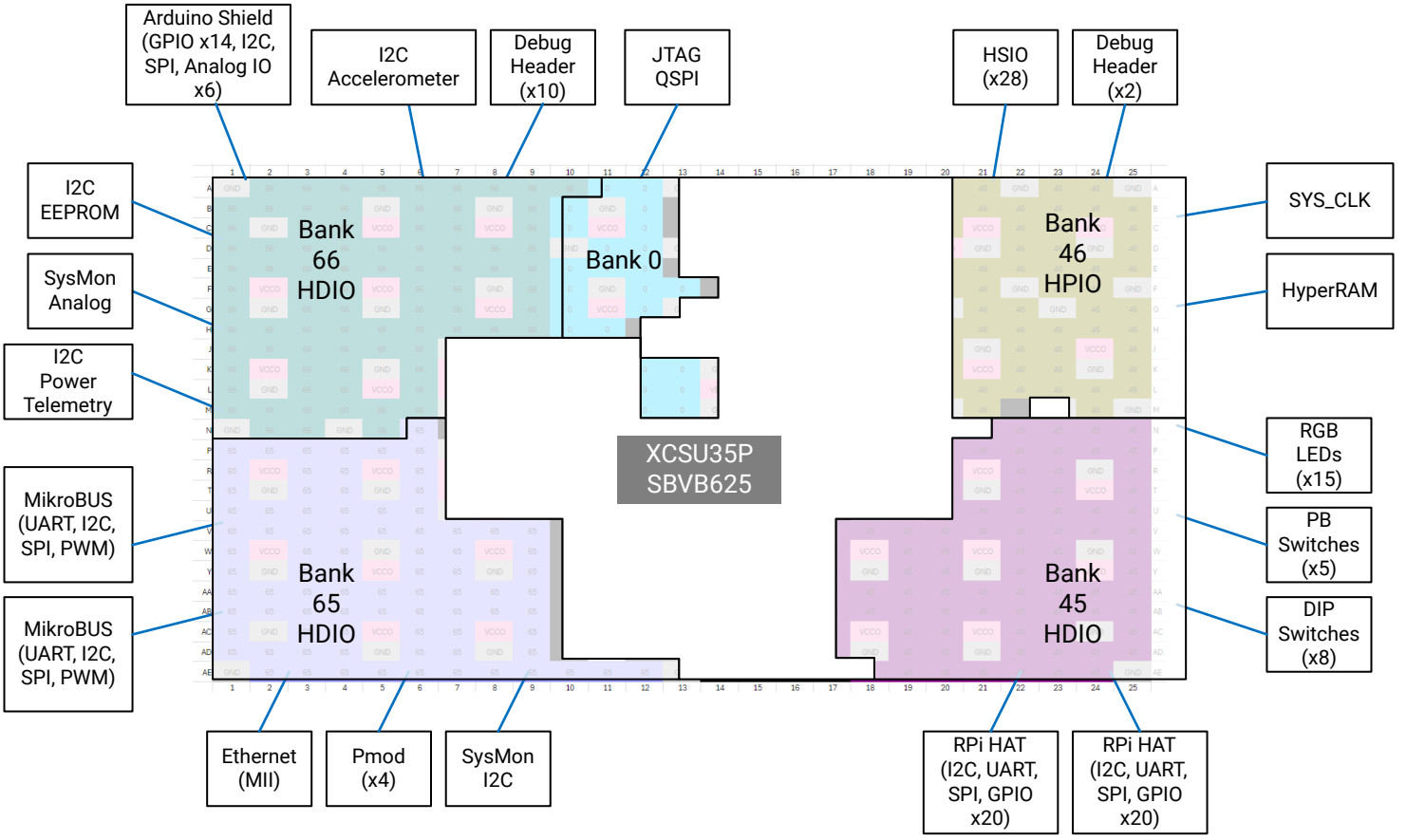
Additional Resources

See Appendix B: Additional Resources and Legal Notices for references to documents, files, and resources relevant to the SCU35 evaluation board.

Block Diagram

A block diagram of the SCU35 evaluation board is shown in the following figure.

Figure 1: **Evaluation Board Block Diagram**



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Board Features

The SCU35 evaluation board features are listed here. Detailed information for each feature is provided in Chapter 3: Board Component Descriptions.

- XCSU35P
- SBVB625 package
- Form factor: see Board Specifications.
- Onboard configuration from:
  - USB-to-JTAG bridge
  - JTAG pod 2 mm 2x7 flat cable connector
  - Quad SPI (QSPI) SPI_24 mode
- Clocks
  - FPGA bank 47 System clock LVDS 100 MHz
  - FPGA bank 47 HyperRAM 200MHz
  - FPGA bank 47 HSIO_CLK_IN design dependent
  - FPGA bank 47 HSIO_CLK_OUT design dependent
- HyperRAM (8 MB)
- I/O Expansion
  - Arduino Shield
    - Analog, GPIO, I2C, SPI
  - HSIO
    - I2C, high speed differential and single-ended I/O
  - MikroBUS (Click) (2)
    - I2C, PWM, SPI, UART
  - Pmods
    - GPIO
  - Raspberry Pi HAT (2)
    - GPIO, I2C, SPI, UART
- User GPIO
  - DIP switch (8-position)

  - Pushbutton switches (5)
  - RGB LEDs (5)
- UARTs (3)
- Three axis linear accelerometer (I2C)
- EEPROM (I2C)
- Power telemetry (I2C)
- USB-C power status and control (I2C)
- SYSMON header
- MII 10/100 Ethernet
- Cooling fan 5V (optional)
- Operational switches and jumper (PROGRAM_B, PUDC_B, boot mode)
- Operational status LEDs (INIT_B, DONE, SYS_PG, PLUG_EVENT, CAP_MIS)
- Debug headers
  - HPIO (2 I/O)
  - HDIO (10 I/O)

The SCU35 evaluation board provides a rapid prototyping platform using the XCSU35P-2SBVB625E device. See the *UltraScale Architecture and Product Data Sheet: Overview* (DS890) for a feature set overview, description, and ordering information.

Board Specifications

Dimensions

- **PCB:**

  Height: 5.512 inches (14.0 cm)

  Length: 5.512 inches (14.0 cm)

  Thickness: 64.12 mil ±5 mil (1.63 mm ±0.13 mm)

- **Evaluation Board:**

  Thickness fully assembled: 1.379 inches (3.503 cm)

  Fully assembled, from table to bottom of PCB: 0.315 inches (8.0 mm)

***Note*:** A 3D model of this board is not available.

See the SCU35 Evaluation Kit website for the XDC listing and board schematics.

Environmental

***Note*:** The operating temperature range is not fully tested across the specified temperature range. It is for general guidelines only. Customers should use the SCU35 evaluation board for evaluation purposes only in a normal lab environment and should not operate beyond room temperature.

- **Temperature:**

  Operating: 0°C to +45°C

  Storage: –25°C to +60°C

- **Humidity:** 5% to 95% non-condensing

Operating Voltage

+9-20 V_{DC}

Chapter 2

Board Setup and Configuration

Standard ESD Measures

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Attach a wrist strap to an unpainted metal surface of your hardware to prevent electrostatic discharge from damaging your hardware.
- When you are using a wrist strap, follow all electrical safety procedures. A wrist strap is for static control. It does not increase or decrease your risk of receiving electric shock when you are using or working on electrical equipment.
- If you do not have a wrist strap, before you remove the product from ESD packaging and installing or replacing hardware, touch an unpainted metal surface of the system for a minimum of five seconds.
- Do not remove the device from the antistatic bag until you are ready to install the device in the system.
- With the device still in its antistatic bag, touch it to the metal frame of the system.
- Grasp cards and boards by the edges. Avoid touching the components and gold connectors on the adapter.
- If you need to lay the device down while it is out of the antistatic bag, lay it on the antistatic bag. Before you pick it up again, touch the antistatic bag and the metal frame of the system at the same time.
- Handle the devices carefully to prevent permanent damage.

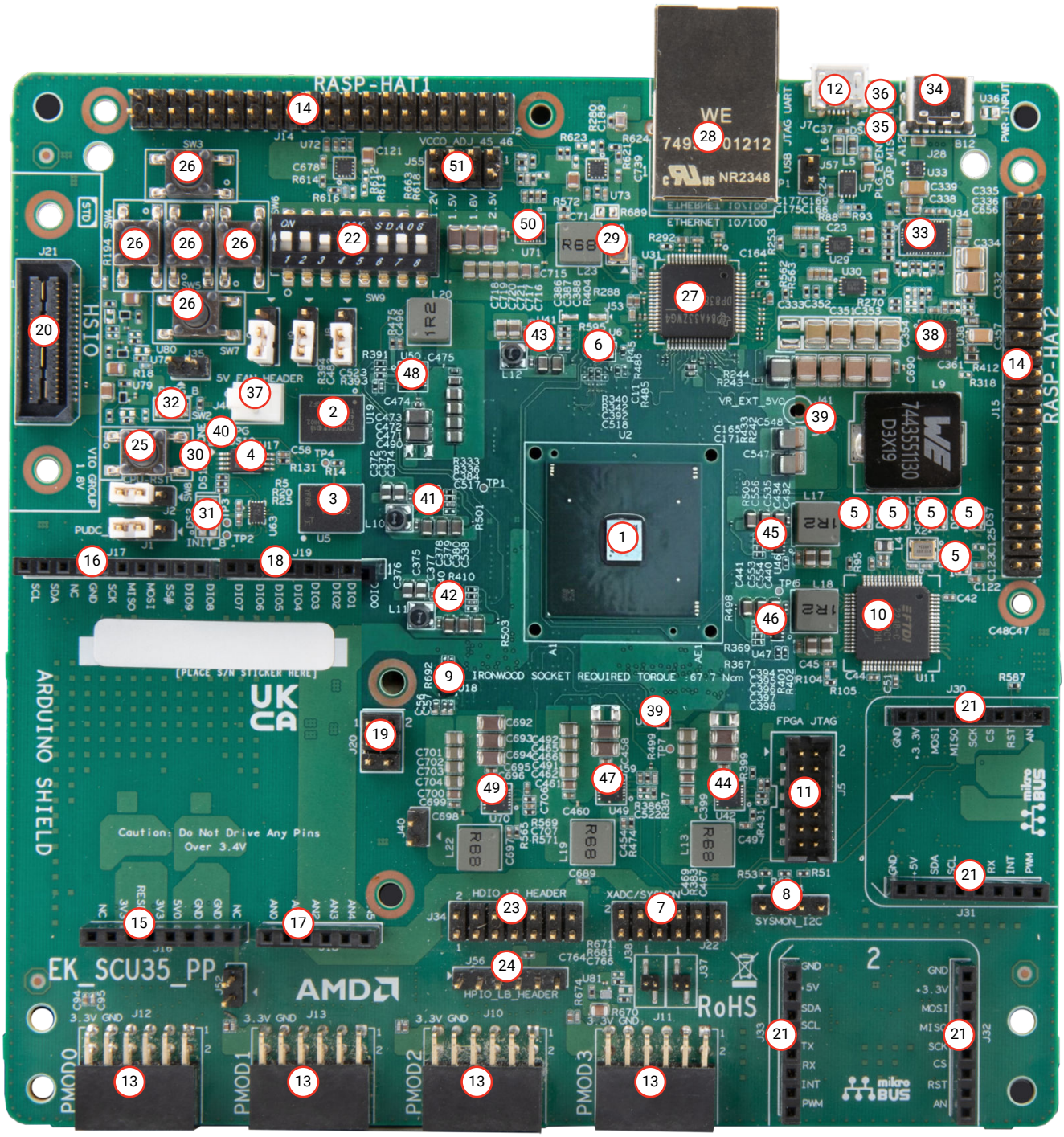
Board Component Location

The following figure shows the SCU35 board component locations. Each numbered component shown in the figure is keyed to the table in Board Component Descriptions.

IMPORTANT! *The following figure is for visual reference only and might not reflect the current revision of the board.*

IMPORTANT! *There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific SCU35 version of interest for such details.*

Figure 2: **Evaluation Board Component Locations**



Board Component Descriptions

The following table identifies the components on the board.

Table 2: **Board Component Locations**

Callout No.	Ref. Des.	Feature	Notes
1	U2	AMD Spartan™ UltraScale+™ FPGA	XCSU35P-2SBVB625E (heatsink not shown)
2	U19	HyperRAM 64 Mb memory	Infineon S27KS0642 (64 Mb x 8) 200 MHz 1.8 V
3	U5	QSPI Flash 128 Mb memory	Micron MT25QU128ABA8E12-0SIT 128 Mb 166 MHz 1.8 V
4	U17	EEPROM 64 Kb memory	ST M24C64-DRDW8 64 Kb 3.3 V I2C
5	DS3, DS4, DS5, DS6, DS7	User LEDs	Kingbright APTF1616LSEEZGKQBKC RGB LED 3.3 V
6	U6	System Clock 100 MHz	Transko TLSM2-L50CQ18ST1-100.000M-TR ceramic LVDS oscillator 100 MHz 1.8 V
7	J22	SYSMON header	Sullins PBC06DAAN Conn. hdr. vert. male 12 pos. 2x6 2.54 mm
8	J4	SYSMON I2C	Sullins PBC04SAAN Conn. hdr. vert. male 12 pos. 1x4 2.54 mm
9	U18	Accelerometer sensor	ST LIS2DE12TR three axis linear accelerometer I2C 3.3 V
10	U11	USB-UART bridge	FTDI FT4232HL_LQFP64 Quad channel serial UART/JTAG 3.3 V
11	J5	JTAG 2 mm 2x7 flat-cable connector	Molex 0878321420 Conn. hdr. vert. male 14 pos 2x7 2 mm
12	J7	USB micro-B JTAG/UART	Hirose ZX62D_AB_5P8(30) USB micro-B connector receptacle
13	J10, J11, J12, J13	Pmod 2x6 connector	Sullins PPPC062LJBN-RC Conn. hdr. RA female 12 pos. 2x6 2.54 mm
14	J14, J15	Raspberry Pi HAT connector	Sullins PBC40DAAN Conn. hdr. vert. male 40 pos. 2x20 2.54 mm
15	J16	Arduino shield pwr and gnd	Sullins PPPC081LFBN Conn. hdr. vert. female 8 pos. 1x8 2.54 mm
16	J17	Arduino shield I2C and digital I/O	Sullins PPPC101LFBN Conn. hdr. vert. female 10 pos. 1x10 2.54 mm
17	J18	Arduino shield analog I/O	Sullins PPPC061LFBN Conn. hdr. vert. female 6 pos. 1x6 2.54 mm
18	J19	Arduino shield digital I/O	Sullins PPPC081LFBN Conn. hdr. vert. female 8 pos. 1x8 2.54 mm
19	J20	Arduino shield ICSP and digital I/O	Sullins PBC03DAAN Conn. hdr. vert. male 6 pos. 2x3 2.54 mm

Table 2: **Board Component Locations** *(cont'd)*

Callout No.	Ref. Des.	Feature	Notes
20	J21	HSIO connector	Samtech QSE-020-01-F-D-A Conn. vert. female 40 pos. 0.80 mm
21	J30, J31, J32, J33	MikroBUS connector	Sullins PPPC081LFBN Conn. hdr. vert. female 8 pos. 1x8 2.54 mm
22	SW9	User DIP switches	C&K SDA08H1SBD SPST 8 pos 2.54 mm
23	J34	Debug loopback header HDIO	Sullins PBC07DAAN Conn. hdr. vert. male 14 pos. 2x7 2.54 mm
24	J56	Debug loopback header HPIO	Sullins PBC06SAAN Conn. hdr. vert. male 6 pos. 1x6 2.54 mm
25	SW8	CPU reset switch	TL3301EF100QG SPST mom. pb switch 6x6 mm
26	SW3, SW4, SW5, SW6, SW7	User PB switches	TL3301EF100QG SPST mom. pb switch 6x6 mm
27	U31	Ethernet PHY MII	TI DP83867IRPAP Ethernet PHY 10/100 Mb/s MII
28	P1	Ethernet RJ45	Würth 74990101212 RJ45 connector w/magnetics
29	X3	Ethernet PHY crystal oscillator	Epson FA-238_25.0000MB-C3 Xtal 25MHz 18pF 80PPM
30	DS1	DONE FPGA config LED	Lumex SML-LX0603GW-TR LED green
31	DS2	FPGA config LED	Broadcom HSMF-C155 LED bi-color green/red
32	SW2	PROGRAM_B FPGA configuration switch	Omron B3U-1000P SPST mom. pb switch
33	U34	USB-C power controller	TI TPS25730D USB-C PD controller
34	J28	USB-C power connector	Amphenol 10164359 Conn. female USB-C power
35	DS8	USB-C power capability mismatch LED	Broadcom HSMS-C190 LED red
36	DS9	USB-C power detect LED	Broadcom HSML-C197 LED orange
37	J47	FPGA cooling fan header w/ friction lock	Molex 0022112022 Conn. hdr. vert. male 2 pos. 2.54 mm
38	U38	Power V regulator main 9-20 V in 5 V out	MPS MP2422GLUTH Step-down V reg. DC/DC sync
39	U61, U64	Power monitor	TI INA700AYWFR Power monitor I2C
40	DS10	Power good LED	Lumex SML-LX0603GW-TR LED green

Table 2: **Board Component Locations** *(cont'd)*

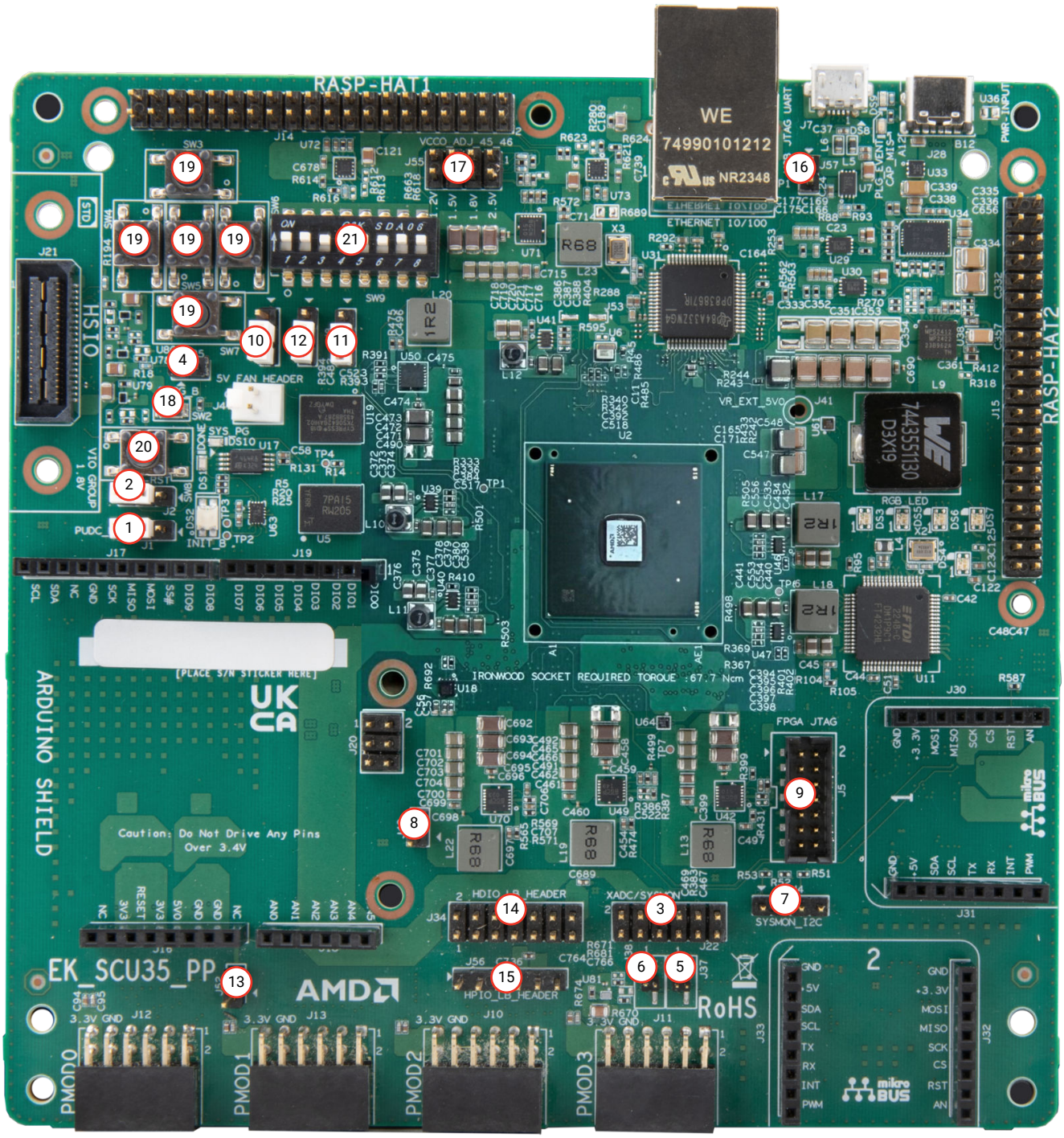
Callout No.	Ref. Des.	Feature	Notes
41	U39	Power V regulator VR_VCCADC_1V8	MPS MP2181GTL Step-down V reg. DC/DC sync
42	U40	Power V regulator VR_VCCO_0_1V8	MPS MP2181GTL Step-down V reg. DC/DC sync
43	U41	Power V regulator VR_VCCAUX_HPIO_1V8	MPS MP2181GTL Step-down V reg. DC/DC sync
44	U42	Power V regulator VR_VCCINT_0V85	MPS MP8770CGQ Step-down V reg. DC/DC sync
45	U46	Power V regulator VR_VCCAUX_HDIO_1V8	MPS MP2183CGTL Step-down V reg. DC/DC sync
46	U47	Power V regulator VR_VCCINT_IO_BRAM_0V85	MPS MP2183CGTL Step-down V reg. DC/DC sync
47	U49	Power V regulator VR_UTIL_3V3	MPS MP8770CGQ Step-down V reg. DC/DC sync
48	U50	Power V regulator VR_VCCO_47_1V8	MPS MP8770CGQ Step-down V reg. DC/DC sync
49	U70	Power V regulator VR_VCCO_65_66_67_68_3V3	MPS MP8770CGQ Step-down V reg. DC/DC sync
50	U71	Power V regulator VR_VCCO_45_46_ADJ	MPS MP8770CGQ Step-down V reg. DC/DC sync
51	J55	I/O Bank 45 & 46 V select	Sullins PBC04DAAN Conn. hdr. vert. male 8 pos. 2x4 2.54 mm

Default Jumper and Switch Settings

The following figure shows the SCU35 board jumper header and switch locations. Each numbered component shown in the figure is keyed to the applicable table in this section.

Figure 3: **Board Jumper Header and Switch Locations**

00 Round callout references a component on the front side of the board



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Jumpers

The following table lists the default jumper settings.

Table 3: **Default Jumper Settings**

Callout Number	Ref. Des.	Function	Default
1	J1	PUDC_B 1-2: Strapped low. Internal pull-up resistors are enabled on each SelectIO pin 2-3: Strapped high. Internal pull-up resistors are disabled on each SelectIO pin	2-3
2	J2	Power good select 1-2: PGood drives INIT_B 2-3: PGood drives PROG_B	Open
3	J22	SysMon header Open: Header for test access	Open
4	J35	Configuration mode select Open: JTAG Jumpered: QSPI	Open
5	J37	SysMon I2C VP Open: SysMon VP measures external V Jumpered: SysMon VP not used	Jumpered
6	J38	SysMon I2C VN Open: SysMon VN measures external V Jumpered: SysMon VN not used	Jumpered
NA	J53 (DNP)	Factory Only	Open
NA	J54 (DNP)	Factory Only	Open
7	J4	SysMon I2C	Open
8	J40	Debug header	Open
9	J5	PC4 JTAG	Open
10	J6	UART B handshake 1-2: UART CTS strapped to GND 2-3: UART RTS and CTS loopback	2-3
11	J8	UART C handshake 1-2: UART CTS strapped to GND 2-3: UART RTS and CTS loopback	2-3
12	J9	UART D handshake 1-2: UART CTS strapped to GND 2-3: UART RTS and CTS loopback	2-3
13	J52	Arduino Vin	Open
14	J34	Debug header HDIO	Open
15	J56	Debug header HPIO	Open
16	J57	Disable 5V	Open

Table 3: **Default Jumper Settings** *(cont'd)*

Callout Number	Ref. Des.	Function	Default
17	J55	Bank 45 Vcco select Open: 3.3V 1-2: 2.5V 3-4: 1.8V 5-6: 1.5V 7-8: 1.197V	Open

Notes:

1. The SCU35 kit does not include a power supply. It is recommended that users purchase an FSP power supply (part number FSP065-D3MR3C). For more information on power supply purchasing options refer to the SCU35 Product Page. See USB-C Power Input for more information.

Switches

The following table lists the default switch settings.

Table 4: **Default Switch Settings**

Callout Number	Ref. Des.	Function	Default
18	SW2	PROGRAM_B (Not pressed, pulled high)	Open
19	SW3-SW7	GPIO PB (Not pressed, pulled low)	Open
20	SW8	CPU Reset PB (Not pressed, pulled high)	Open
21	SW9	GPIO DIP OFF = 0 = low ON = 1 = high	OFF, OFF, OFF, OFF, OFF, OFF, OFF, OFF

Spartan UltraScale+ Device Configuration

The Configuration Engine section of the *Spartan UltraScale+ FPGAs Configuration User Guide* (UG860) describes the Spartan UltraScale+ XCSU35P device boot process. The SCU35 board supports a subset of the modes documented in the configuration user guide via onboard boot options. The header J35 configuration option settings are listed in the following table.

Table 5: **Mode Configuration Header J35 Option Settings**

Boot Mode	Mode Pins [0:2]
JTAG (default)	0x5 [101] – J35 open

Table 5: **Mode Configuration Header J35 Option Settings** *(cont'd)*

Boot Mode	Mode Pins [0:2]
QSPI SPI_24	0x4 [100] – J35 jumpered

JTAG

The AMD Vivado™, AMD SDK, or third-party tools can establish a JTAG connection to the Spartan UltraScale+ device in the two ways described in this section.

- FTDI FT4232 USB-to-JTAG/USB-UART device (U11) connected to USB 2.0 type-C connector (J7), which requires:
  - Set boot mode selection header J35 for JTAG as indicated in the "Mode Configuration Header J35 Option Settings" table in Spartan UltraScale+ Device Configuration.
  - Power-cycle the evaluation board or press the program (PROGRAM_B) pushbutton (SW2). SW2 is near the HSIO connector J21 in the figure in Board Component Location.
- JTAG pod flat cable connector J5 (2 mm 2x7 shrouded/keyed), which requires:
  - Set boot mode selection header J35 for JTAG as indicated in the "Mode Configuration Header J35 Option Settings" table in Spartan UltraScale+ Device Configuration.
  - Power-cycle the SCU35 board or press the program (PROGRAM_B) pushbutton (SW2). SW2 is near the HSIO connector J21 in the figure in Board Component Location.

  ***Note*:** In this mode, the FT4232 device (U11) UART functionality continues to be available.

QSPI

This boot mode is supported onboard and is wired to the XCSU35P U2 bank 0 pins. The master SPI configuration mode supports multiple data bus widths and setups. The master SPI configuration mode can read from standard 1-bit (x1), 2-bit (x2), and 4-bit (x4) SPI flash devices. The SCU35 uses the Master SPI_24 (M[0:2]=100), 24-bit addressing variant of the master SPI configuration mode, which supports QSPI flash devices up to 128 Mb.

See the Master SPI Configuration Mode section of the *Spartan UltraScale+ FPGAs Configuration User Guide* (UG860) for more information. To boot from QSPI:

1. Store a valid XCSU35P FPGA boot image file in the QSPI.
2. Set boot mode selection header J35 for QSPI as indicated in the "Mode Configuration Option Header J35 Settings" table in Spartan UltraScale+ Device Configuration.
3. Power-cycle the SCU35 board or press the program (PROGRAM_B) pushbutton SW2. SW2 is near the HSIO connector J21 in the figure in Board Component Location.

Chapter 3

Board Component Descriptions

Overview

This chapter provides a detailed functional description of the board's components and features. The "Board Component Locations" table in Board Component Descriptions identifies the components. Component locations are shown in the "Evaluation Board Component Locations" figure in Board Component Location.

Component Descriptions

Spartan UltraScale+ Device

The evaluation board is populated with the AMD Spartan™ UltraScale+™ XCSU35P-2SBVB625E FPGA device, which is optimized for cost-sensitive applications requiring high I/O count, low power, and state-of-the-art security features. Additionally, the XCSU35P device can be configured to integrate a MicroBlaze™-V processing system. For additional information on the Spartan UltraScale+ XCSU35P-2SBVB625E FPGA device, see the *Spartan UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS930). See the *Spartan UltraScale+ FPGAs Configuration User Guide* (UG860) for more information about Spartan UltraScale+ device configuration options.

I/O Voltage Rails

The XSU35P device I/O bank voltages on the board are listed in the following table.

***Note*:** See the *Spartan UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS930) for more information.

Table 6: **I/O Voltage Rails**

SU+ Device (U2) Bank	Power Supply Rail Net Name	Voltage	Description
PMC Bank 0	VR_VCCO_0_1V8	1.8V	JTAG, QSPI, SYSMON
HDIO Bank 45	VR_VCCO_45_46_ADJ	1.197 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V (default)	Raspberry Pi HATs, GPIO LEDs, GPIO DIP switches
HDIO Bank 46	VR_VCCO_45_46_ADJ	1.197 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V (default)	Raspberry Pi HATs
HPIO Bank 47	VR_VCCO_47_1V8	1.8V	HyperRAM, HSIO, system clock, HPIO loopback
HDIO Bank 66	VR_VCCO_65_66_67_68_3V3	3.3V	Pmods, SYSMON I2C, MikroBUS (Click)
HDIO Bank 67	VR_VCCO_65_66_67_68_3V3	3.3V	Accelerometer I2C and interrupts, MikroBUS (Click) analog, debug header, CPU reset, INA alert, HSIO I2C, load switch enables, USB-C fault, HDIO loopback, USB-C PD I2C, INA I2C, EEPROM I2C.
HDIO Bank 68	VR_VCCO_65_66_67_68_3V3	3.3 V	Arduino, XADC VCCAUX, load switch enables, MikroBUS (Click) analog, fan enable.

HyperRAM Memory

The provides 64Mb of external Infineon HyperRAM memory to enable software applications that are too large to fit in the XCSU35P FPGA Block RAM. This interface is connected to HPIO bank 47. Use of this HyperRAM memory device in a MicroBlaze™ V system requires an IP core that is provided by Infineon. An example design and accompanying application note will be available when the kit is in full production.

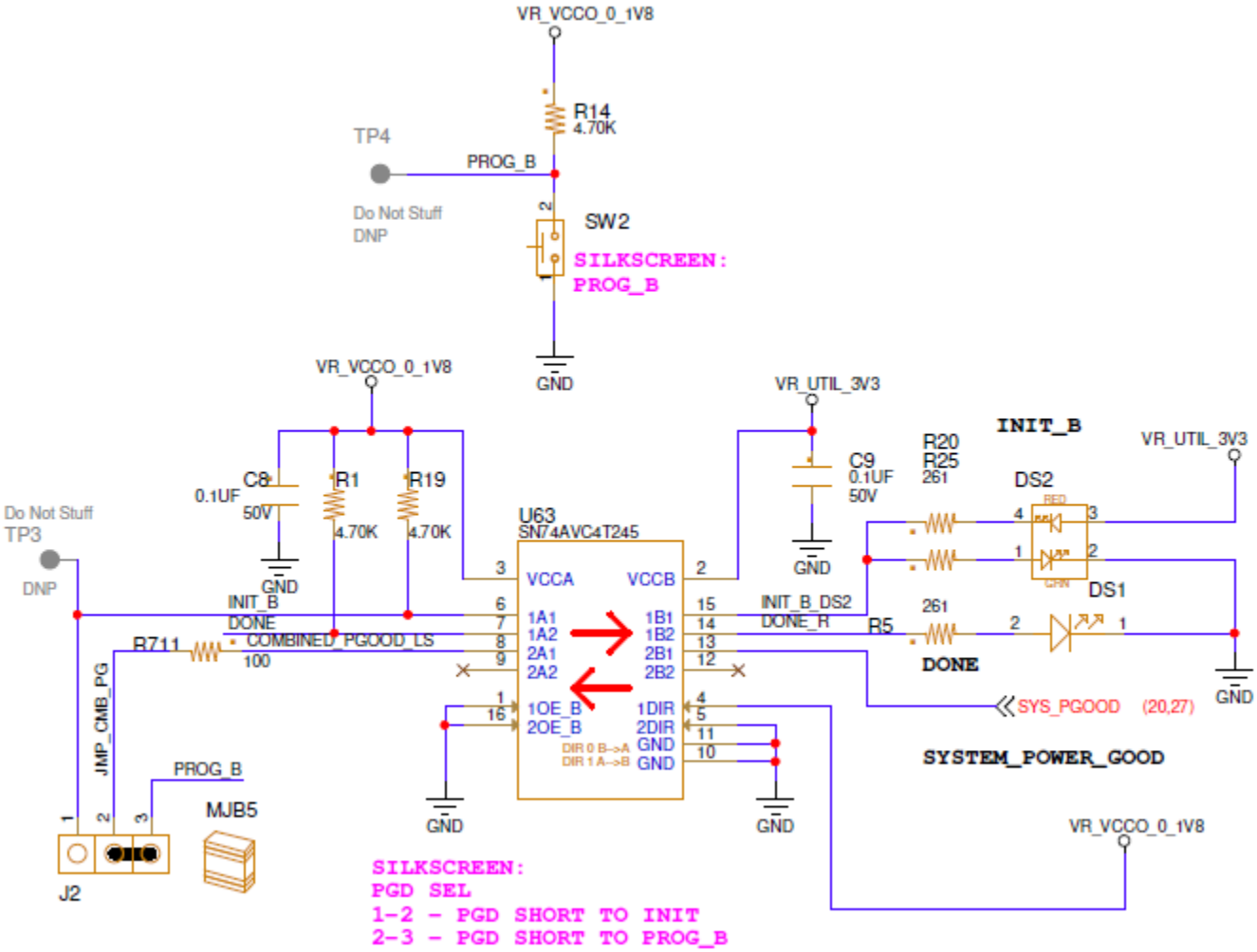
For more memory component details see the Infineon S27KS0642 data sheet on the Infineon website. For the most current part number, see the Bill of Materials (BOM) located on the lounge. The detailed device connections for the feature described in this section are documented in the board XDC file, which is located in the lounge.

Device Reconfiguration PROGRAM_B

PROGRAM_B is the Spartan UltraScale+ input to reconfigure the device. It is controlled using a push button for easy access. The pin must be held high during the configuration process.

The board PROGRAM_B circuit is shown in the following figure. U63 allows bidirectional level shifting for the INIT_B, DONE, and SYS_PGOOD signals. The PROGRAM_B signal can be configured via the J2 jumper to be controlled by the SYS_PGOOD signal until power is valid.

Figure 4: **PROGRAM_B Reset Circuit**



I2C Buses and Connections

There are several I2C interfaces on the XCSU35P FPGA that connect to devices on the SCU35 board:

Table 7: **I2C Interfaces**

I2C Interface	Purpose	Ref Des	I2C Address
SySMon	System Monitor	J4	0x##[1]
I2C0	EEPROM	U17	0x50 & 0x58
I2C1	Power telemetry	U61	0x44
I2C1	Power telemetry	U64	0x45
I2C2	USB-C PD	U34	0x20

Table 7: **I2C Interfaces** *(cont'd)*

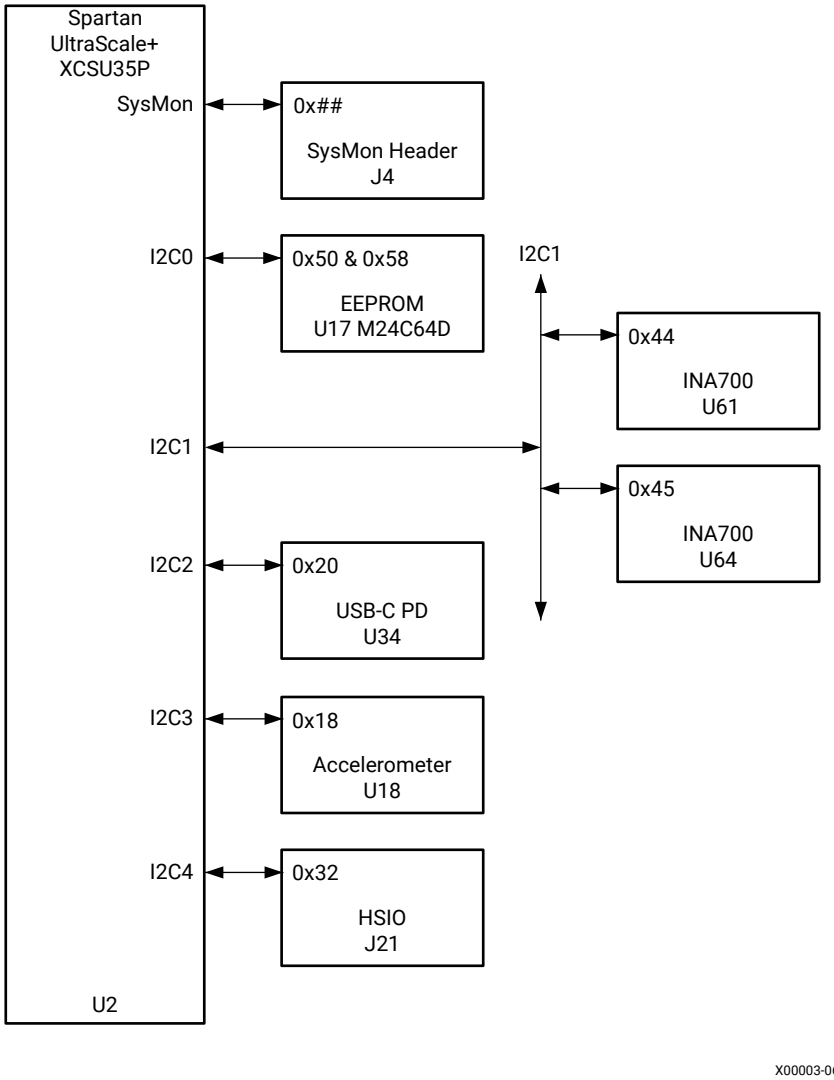
I2C Interface	Purpose	Ref Des	I2C Address
I2C3	Accelerometer	U18	0x18
I2C4	HSIO	J21	0x32

Notes:

1. Configurable.

The following figure shows the I2C bus connectivity detailed in the table above. Discrete I2C interfaces on the FPGA eliminate the need for I2C multiplexers on the board and provide great flexibility to include only those interfaces in the FPGA design that are required for the user application.

Figure 5: **I2C Bus Connectivity**



The detailed FPGA connections for the feature described in this section are documented in the SCU35 evaluation board schematic and XDC file.

EEPROM

The EEPROM (U17) is a 64 Kbit I2C compatible device organized as 8K x 8 bits, and has two addresses associated with it. Address 0x50 is used to access the memory array and address 0x58 is used to access the identification page. Details for controlling the M24C64D EEPROM is available in the data sheet on the ST website.

Accelerometer

The accelerometer (U18) is a ST LIS2DE12TR device at I2C address 0x18. This is a three axis linear accelerometer device targeted to industrial applications. This sensor also features two configurable interrupt outputs which are connected to the XCSU35P FPGA. Details for interacting with the this sensor are available on the ST website.

USB-C PD Power Delivery

The TI TPS25730 USB-C PD device is at I2C address 0x20 and provides power over a USB-C cable to the SCU35 board. This I2C interface can be used to provide general status information about the TI TPS25730 USB-C PD device as well as the ability to control the device behavior. More information about using the TPS25730 device can be found at the TI website.

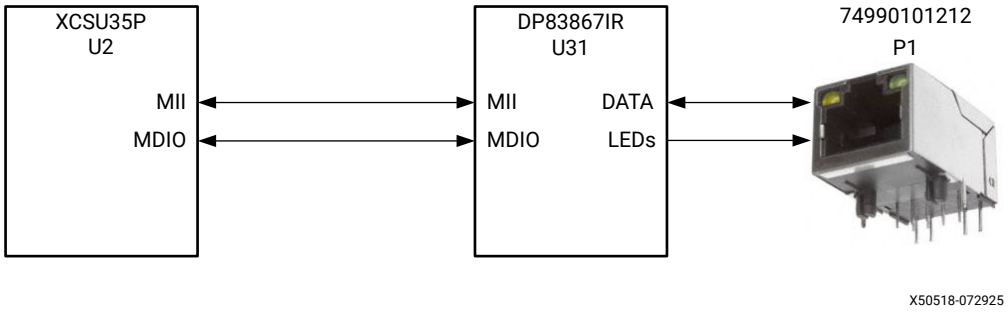
INA700 Devices

The INA700 devices are digital power monitors specifically designed for current sensing applications. The INA700 devices report current, bus voltage, die temperature, power, energy and charge accumulation. The INA700 device at I2C address 0x44 measures power on the VR_INT_5V0 voltage rail and the device at I2C address 0x45 measures power on the VR_VCCINT_0V85 voltage rail. More information about the power system can be found in Monitoring Voltage and Current. More information about the INA700 devices and how to interact with them can be found at the TI website.

Ethernet

A MII Ethernet MAC IP in the XCSU35P FPGA implements a 10/100 Mb/s Ethernet interface. In the following figure, the FPGA (U2) is connected to a TI DP83867IR Ethernet MII PHY (U31) before being routed to an RJ45 Ethernet connector (P1). The MII Ethernet PHY is strapped to PHY address 0x01 and Auto Negotiation is set to Enable. More information on this Ethernet PHY can be found on the TI website.

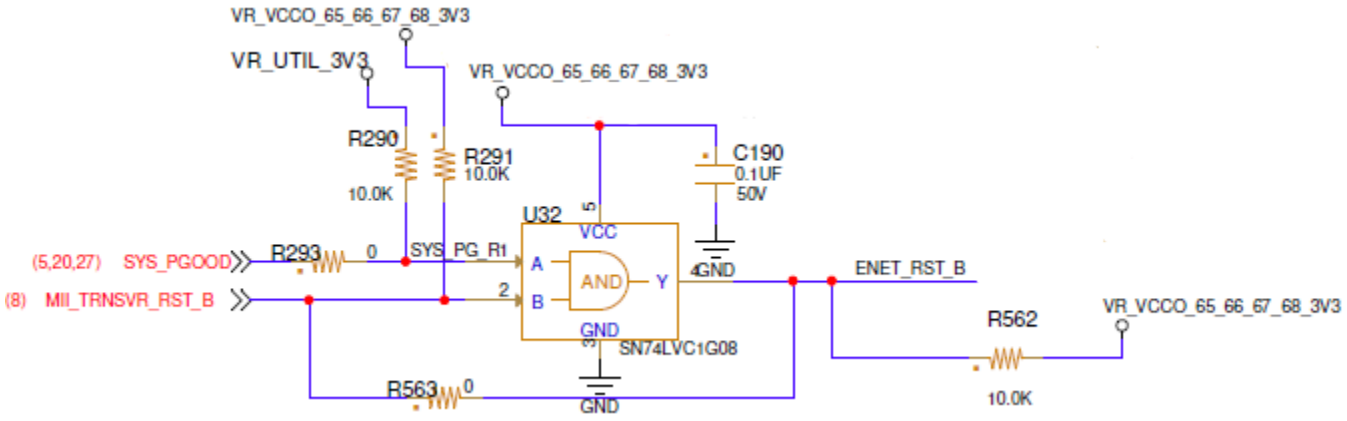
Figure 6: **MII Ethernet**



Ethernet PHY Resets

The DP83867 PHY (U31) is reset by its ENET_RST_B generated by system power good and FPGA I/O signals as shown in the following figure. The SYS_PGOOD signal generated by the MP2002A (U30) and MP2181 (U39) devices (open drain outputs) is wired to the Ethernet PHY reset circuit. The SYS_PGOOD signal is controlled by pushbutton SW2. See Device Reconfiguration PROGRAM_B for more details.

Figure 7: **Ethernet PHY Reset Circuit**



Ethernet PHY LED Interface

The DP83867IR PHY (U31) controls two LEDs in the RJ45 connector (P1). The PHY signal LED0 drives the green LED, and LED1 drives the yellow LED.

The LED functional description is listed in the following table.

Table 8: **Ethernet PHY LED Functional Description**

DP83867IR PHY Pin		Description
Name	Number	
LED_1	62	By default, this pin indicates that 100BASE-T link is established. Additional functionality is configurable using LEDCR1[7:4] register bits.
LED_0	63	By default, this pin indicates that link is established. Additional functionality is configurable using LEDCR1[3:0] register bits.

The LED functions can be reconfigured with writes to the LEDCR1, LEDCR2, and LEDCR3 LED control registers via the PHY's management data interface, MDIO/MDC.

See the TI DP83867IR PHY data sheet at the TI website for component details.

The detailed device connections for the feature described in this section are documented in the SCU35 board XDC file, referenced in Chapter 4: Xilinx Design Constraints.

UARTs

The SCU35 board provides three (3) UART interfaces connected between the XCSU35P FPGA and FTDI FT4232HL (U11) USB-to-Quad-UART bridge device through TI SN74AVC4T245 level-shifters U8, U9, U12, and U14. The FT4232HL (U11) port assignments are listed in the following table.

Table 9: **FT4232HL Port Assignments**

FT4232HL	XCSU35P SU+ Device
Port AD (JTAG)	XCSU35P JTAG chain
Port BD (UARTB)	SCU35_UARTB
Port CD (UARTC)	SCU35_UARTC
Port DD (UARTD)	SCU35_UARTD

The FT4232HL UART interface connections are shown in the following figure. For more information on the FT4232HL, see the Future Technology Devices International Ltd. website.

***Note*:** The FTDI configuration image can be programmed with the Vivado tools. See the Programming FTDI Devices for Vivado Hardware Manager Support section in the *Vivado Design Suite User Guide: Programming and Debugging* (UG908). Alternatively, a JTAG-SMT2 or similar from Digilent is recommended. The detailed device connections for the feature described in this section are documented in the SCU35 board XDC file, referenced in Chapter 4: Xilinx Design Constraints.

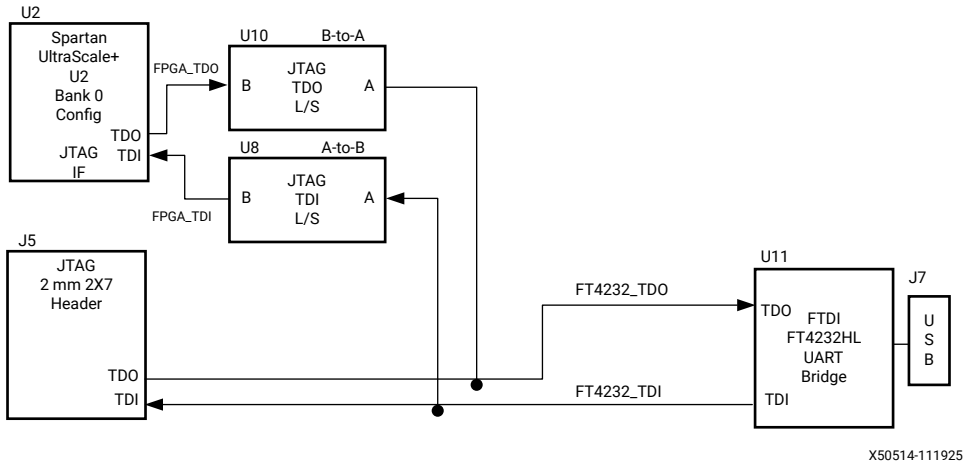
JTAG Chain

The JTAG chain includes:

- J5 2x7 2 mm shrouded, keyed JTAG pod flat cable connector

- J7 USB micro-B connector connected to U11 FT4232HL USB-JTAG bridge

Figure 8: **JTAG Chain Block Diagram**



See Spartan UltraScale+ Device Configuration for information on JTAG programming via:

- FTDI FT4232 USB-to-JTAG/USB-UART device (U11) connected to USB micro-B connector (J7)
- JTAG pod flat cable connector J35 (2 mm 2x7 shrouded/keyed)

Clock Generation

The board provides several clock sources for the XCSU35P U2 device and other function blocks. The following table lists the source devices for each clock.

Table 10: **Clock Sources**

Ref. Des.	Feature	Notes
U6	AMD Spartan UltraScale+ FPGA 100 MHz, 1.8 V, LVDS	Transko TLSM2-L50CQ18ST1-100.000M-TR
U2	HyperRAM 64 Mb memory 200 MHz, 1.8 V, LVDS	AMD Spartan UltraScale+ FPGA
U85	QSPI Flash 128 Mb memory 100 MHz, LVCMOS	EMCCLK
U31	Ethernet PHY 25 MHz xtal	Epson FA-238_25.0000MB-C3
U11	USB UART/JTAG 12 MHz xtal	ECS ECS-120-18-33-JGN-TR
U2	HSIO Expansion 312/625 MHz, 1.8 V, LVDS	AMD Spartan UltraScale+ FPGA

The detailed device connections for the feature described in this section are documented in the board XDC file, referenced in Chapter 4: Xilinx Design Constraints.

User I/O

See Switches for default values.

The following table lists the net names and reference designators for the user I/O.

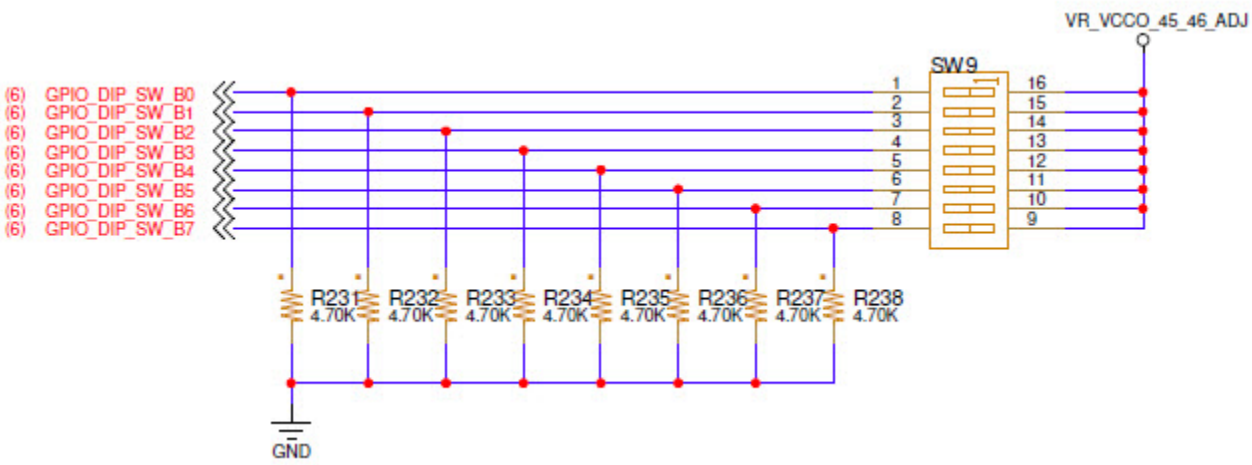
Table 11: **User I/O**

Net Name	Ref. Des.
GPIO_SW_N	SW3
GPIO_SW_S	SW7
GPIO_SW_E	SW6
GPIO_SW_W	SW4
GPIO_SW_C	SW5
GPIO_DIP_SW_B0	SW9
GPIO_DIP_SW_B1	SW9
GPIO_DIP_SW_B2	SW9
GPIO_DIP_SW_B3	SW9
GPIO_DIP_SW_B4	SW9
GPIO_DIP_SW_B5	SW9
GPIO_DIP_SW_B6	SW9
GPIO_DIP_SW_B7	SW9
LED0_RED	DS3
LED0_GREEN	DS3
LED0_BLUE	DS3
LED1_RED	DS4
LED1_GREEN	DS4
LED1_BLUE	DS4
LED2_RED	DS5
LED2_GREEN	DS5
LED2_BLUE	DS5
LED3_RED	DS6
LED3_GREEN	DS6
LED3_BLUE	DS6
LED4_RED	DS7
LED4_GREEN	DS7
LED4_BLUE	DS7

DIP Switches

The board provides an 8-position DIP switch for user GPIO use. The switch I/Os are pulled low by default (off) and strapped to VR_VCCO_45_46_ADJ when switched on.

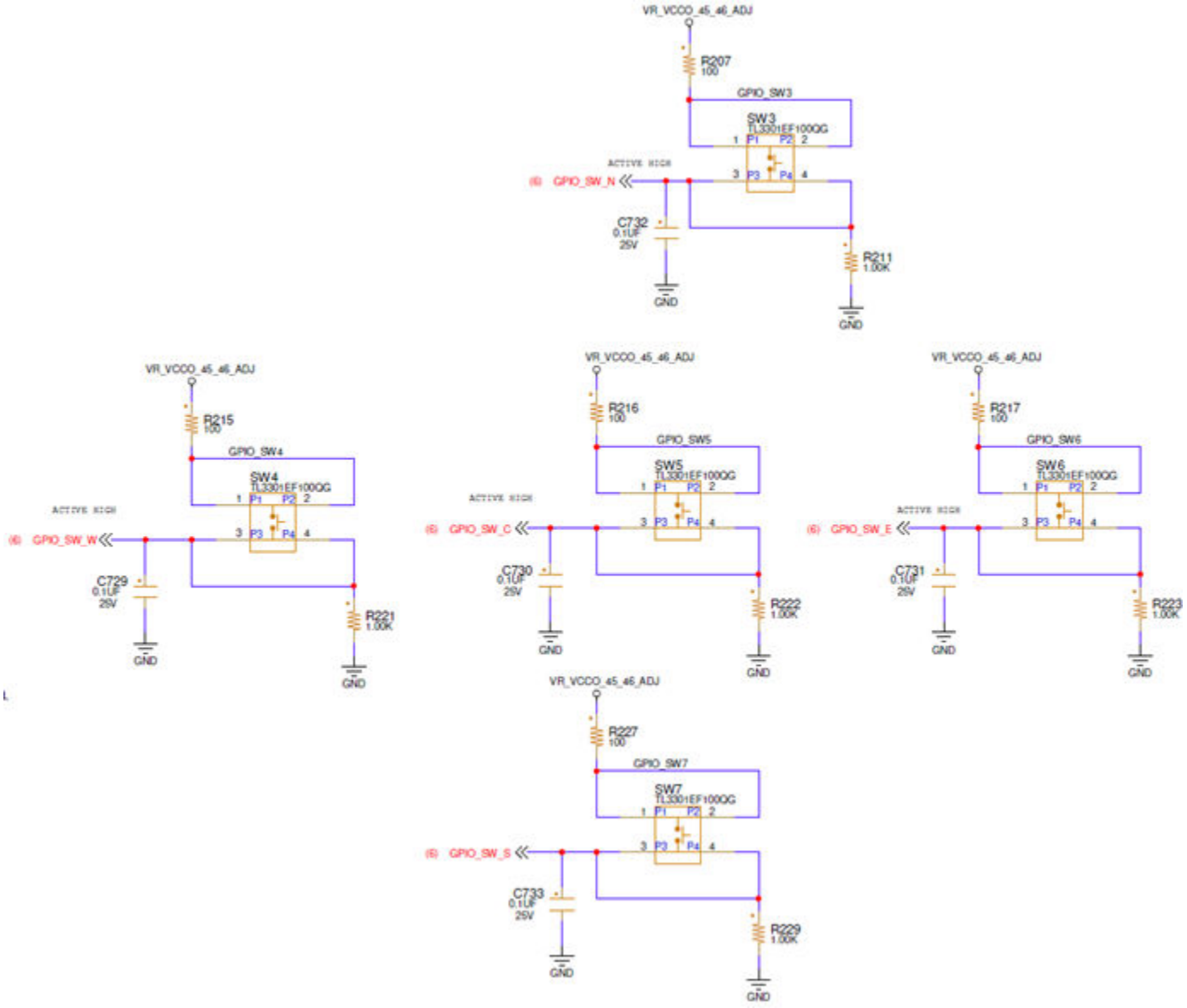
Figure 9: **SCU35 DIP Switches**



PB Switches

The board provides five (5) pushbutton switches arranged in a cardinal direction pattern (north, east, south, west) with the fifth switch in the center. The switch I/Os are pulled low by default (off) and pulled high to VR_VCCO_45_46_ADJ when pressed (on).

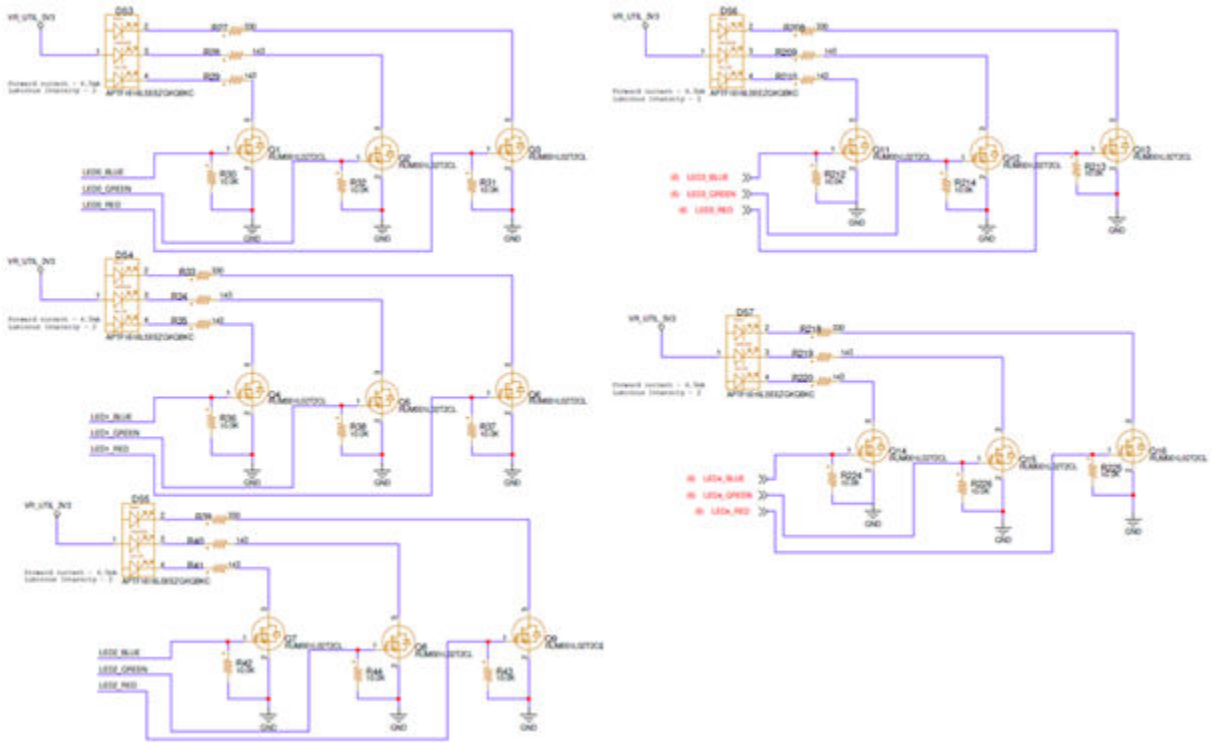
Figure 10: **SCU35 PB Switches**



LEDs

The board provides five (5) RGB LEDs using 15 FPGA I/Os for user GPIO use. The LED I/Os are pulled low by default (off) and illuminated (on) when writing a logic '1' to each red, green, or blue LED I/O.

Figure 11: **SCU35 RGB LEDs**



I/O Expansion

Arduino

The board provides an Arduino® Shield interface. This interface is connected to XCSU35P HDIO bank 68. The Arduino Shield interface provides 14 digital I/O, 6 analog I/O, 2 power pins, and 2 ground pins.

All XCSU35P I/Os connected to the Arduino Shield interface support single-ended line rate of 250 Mb/s.

The Arduino Shield power pins are supplied by 3.3 V and 5 V. Reverse current blocking eFuses are provided for overcurrent and reverse current protection. A maximum current of 0.5 A may be drawn from the 3.3 V rail and 1 A from the 5 V rail.

Note: The board does not support Arduino Shield boards that supply power. The Arduino Shield VIN pin is unconnected.

IMPORTANT! *The XCSU35P FPGA I/Os are not 5V tolerant! Arduino Shields that use 5V I/O cannot be used with the SCU35 board. The maximum voltage that can be applied to the XCSU35P FPGA HD I/Os is Vcco + 0.550V. Additionally, the FPGA bank I/O voltage must match the requirements for the I/O standards that have been assigned to the I/O bank.*

HSIO

The board provides a single-width HSIO Standard interface. All HSIO I/O, except for I2C signals, are connected to HPIO bank 47. The I2C signals are on bank 67.

The XCSU35P differential I/O pairs connected to this HSIO interface operate at 1500 Mb/s line rate.

The HSIO power pins are supplied by 1.8 V, 3.3 V, and 5 V. Load switches are provided for overcurrent and reverse current protection and are enabled by the HSIO_1V8_ON, HSIO_3V3_ON, and HSIO_5V0_ON FPGA I/O signals on bank 6. A combined maximum current of 2.0 A may be drawn from the 1.8 V, 3.3 V, and 5 V rails.

***Note*:** The HSIO interface on the board is based on the Opal Kelly SYZYGY® Standard. However, the SCU35 board does not provide a SmartVIO Controller for VIO voltage configuration as described in the SYZYGY specification. As a result, all SCU35 HSIO I/Os (VIO) are limited to 1.8 V.

More information about SYZYGY boards, mechanical specification, etc. can be found at the SYZYGY website.

IMPORTANT! *The XCSU35P FPGA I/Os are not 5V tolerant. The maximum voltage that can be applied to the XCSU35P FPGA HP I/Os (bank 47) is Vcco + 0.550V. HSIO boards that require VIO greater than 1.8V cannot be used with the board. Additionally, the FPGA bank I/O voltage must match the requirements for the I/O standards that have been assigned to the I/O bank.*

MikroBUS (Click)

The board provides 2 MikroE mikroBus™ expansion interfaces for use with MikroE Click boards™. These interfaces are connected to XCSU35P HDIO banks 65 & 66. Each mikroBUS interface provides 11 Digital I/O, 1 Analog input, 2 power pins, and 2 ground pins. The analog input (AN) pin is connected to the SYSMON XADC pins on bank 66.

All XCSU35P I/Os connected to the mikroBUS interfaces support single-ended line rate of 250 Mb/s.

The mikroBUS power pins are supplied by 3.3V. Load switches are provided for overcurrent and reverse current protection and are enabled by the MCLICK1_3V3_ON and MCLICK2_3V3_ON FPGA I/O signals on bank 67. A maximum current of 1.0A may be drawn from 3.3V rail.

For more information about the MikroE mikroBUS, see https://www.mikroe.com/mikrobus.

IMPORTANT! *The XCSU35P FPGA I/Os are not 5V tolerant. MikroE Click boards™ that use 5V I/O cannot be used with the SCU35 board. The maximum voltage that can be applied to the XCSU35P FPGA HD I/Os is Vcco + 0.550V. Additionally, the FPGA bank I/O voltage must match the requirements for the I/O standards that have been assigned to the I/O bank.*

Pmods

The board provides four Digilent Pmod interfaces. These interfaces are connected to XCSU35P HDIO bank 66. Each Pmod interface provides 8 digital I/O, 2 power pins, and 2 ground pins. The PMOD connectors are placed to support the use of dual-wide Pmod boards.

All XCSU35P I/Os connected to the Pmod interfaces support single-ended line rate of 250 Mb/s.

The Pmod power pins are supplied by 3.3 V. A load switch is provided for overcurrent and reverse current protection and is enabled by the PMOD_3V3_ON FPGA I/O signal on bank 68. A maximum current of 1.0 A may be drawn from 3.3 V rail.

For more information about the Digilent Pmod interface, see https://digilent.com/reference/pmod/start.

IMPORTANT! *The XCSU35P FPGA I/Os are not 5V tolerant. Pmods that use 5V I/O cannot be used with the SCU35 board. The maximum voltage that can be applied to the XCSU35P FPGA HD I/Os is Vcco + 0.550V. Additionally, the FPGA bank I/O voltage must match the requirements for the I/O standards that have been assigned to the I/O bank.*

Raspberry Pi HATs

The SCU35 board provides two Raspberry Pi HAT expansion headers connected to XCSU35P HDIO banks 45 & 46.

All XCSU35P I/Os connecting to HAT interface support single-ended line rate of:

- 250 Mb/s for LVCMOS 3.3/2.5V, SSTL/HSTL 3.3/2.5V
- 300 Mb/s for LVCMOS 1.8/1.5/1.2V
- 400 Mb/s at SSTL/HSTL 1.8/1.5V

A maximum current of 0.5 A may be drawn from the 3.3 V rail and 1.5 A from the 5 V rail. Load switches with reverse current protection are provided on both rails.

For more information about HAT boards, mechanical specification, etc., see https://github.com/raspberrypi/hats.

Note: The SCU35 board does not support HAT boards that supply power.

IMPORTANT! *The XCSU35P FPGA I/Os are not 5V tolerant. Raspberry Pi HATs that use 5V I/O cannot be used with the SCU35 board. The maximum voltage that can be applied to the XCSU35P FPGA HD I/Os is Vcco + 0.550V. Additionally, the FPGA bank I/O voltage must match the requirements for the I/O standards that have been assigned to the I/O bank.*

Power Load Switches

The SCU35 board provides load switches on the HSIO, MikroBUS (Click), and Pmod I/O expansion interfaces. The load switches provide output current limiting, reverse current blocking, and thermal shutdown protection. The switches are disabled by default at power on (an internal pull-down resistor on the enable input) and are controlled by signals connected to FPGA I/O pins described in the following table. It is up to the user to control these enable signals in their Vivado design when using the associated I/O expansion interface. Unused I/O expansion interfaces can leave the corresponding load switch(es) disabled.

The detailed FPGA connections for the feature described in this section are documented in the SCU35 evaluation board schematic and XDC file, referenced in Chapter 4: Xilinx Design Constraints.

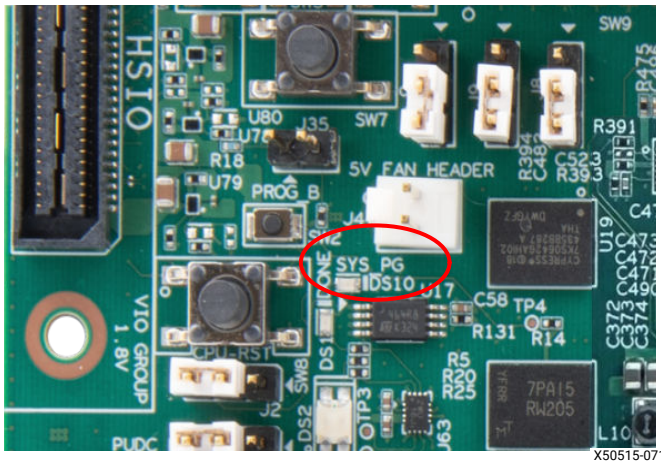
Table 12: **Power Load Switches**

Ref. Des.	Voltage Rail	Enable Net Name	FPGA Pin
U78	VR_HSIO_1V8	HSIO_1V8_ON	K3
U79	VR_HSIO_3V3	HSIO_3V3_ON	L6
U80	VR_HSIO_5V0	HSIO_5V0_ON	M6
U81	VR_PMOD_3V3	PMOD_3V3_ON	F4
U82	VR_MCLICK1_3V3	MCLICK1_3V3_ON	F1
U83	VR_MCLICK2_3V3	MCLICK2_3V3_ON	N5

Power Good LED

The status of the power system on the SCU35 board is indicated via SYS_PG LED (DS10), which is shown in the following figure.

Figure 12: **Power Good LED**

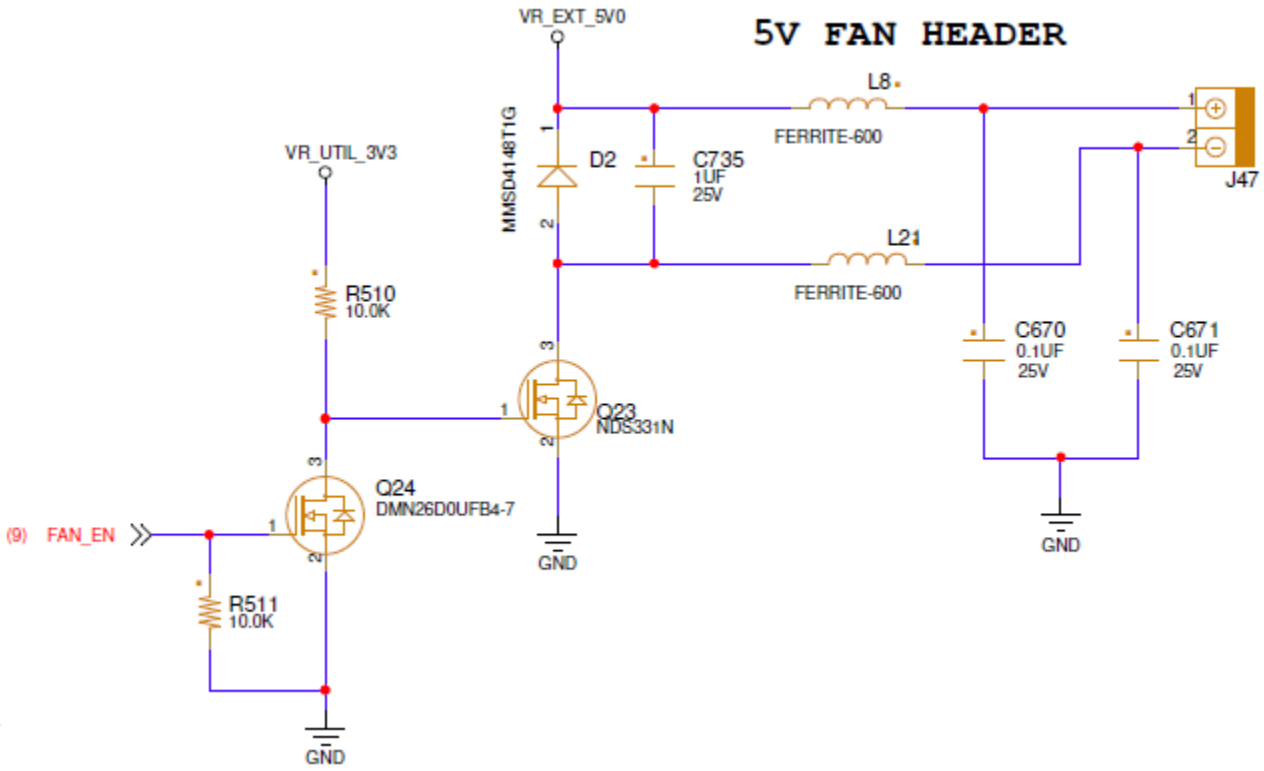


Cooling Fan Connector

The cooling fan connector is shown in the following figure. The can use the FPGA I/O FAN_EN signal (bank 68, pin A9) to autonomously control the fan speed by controlling the pulse width modulation (PWM) signal to the fan. A controlling software application must be created to monitor the XCSU35P FPGA temperature and drive this logic. A FPGA PWM IP is required in the user design.

The board provides a fan controller header J47 to permit control by the Spartan UltraScale+ device. See the Default Jumper and Switch Settings for more details.

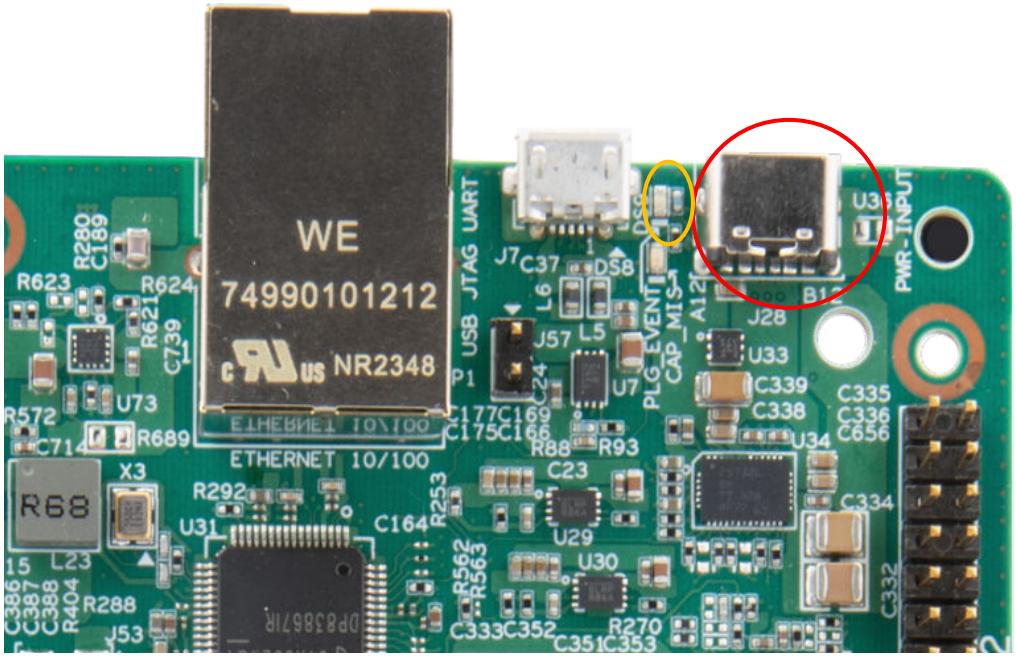
Figure 13: **5V Fan Header**



USB-C Power Input

The orange LED DS9 illuminates when the SCU35 board is connected to a valid 9-20 V, 3A (min) USB-C power supply. See Board Power System for details on the onboard power system.

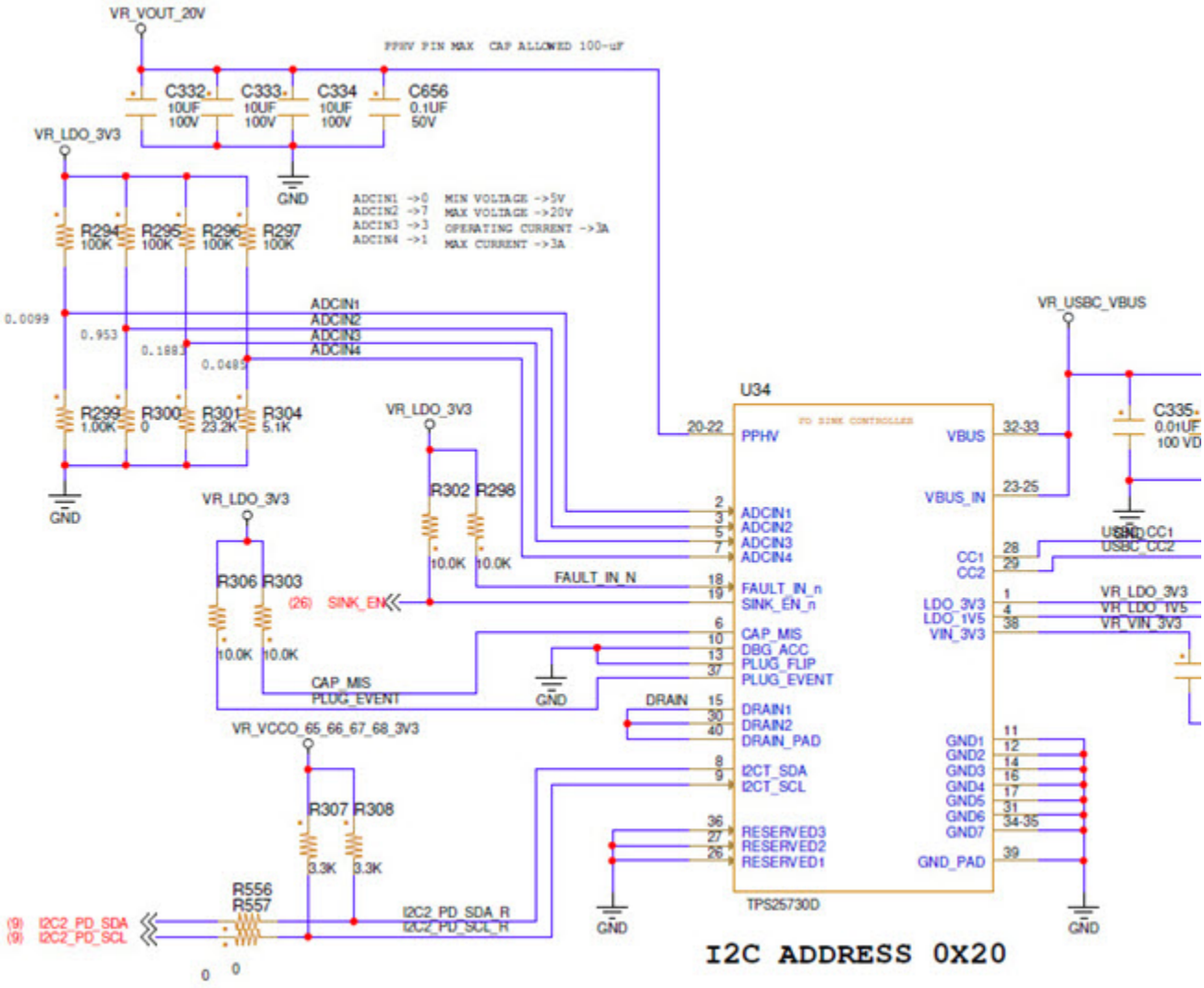
Figure 14: **Power Input**



X50516-071825

The following figure shows the USB-C Power Delivery (PD) Sink Controller (U34). Power (9-20 V DC) is applied to the board via the USB-C connector (J28 not shown) and input to the sink controller on the VBUS and VBUS_IN pins. As long as the input power is valid, it is passed to the PPHV output pins to provide the main power system voltage. The ADCIN [x] pins strap the configuration settings for minimum voltage input, maximum voltage input, operating current, and maximum current. For more information see the datasheet for the TPS25730D device at the TI website.

Figure 15: **Power Input**



Board Power System

The evaluation board uses power management ICs (PMIC) and power regulators from Monolithic Power Systems to supply the core and auxiliary voltages listed in the following tables. The detailed device connections for the feature described in this section are documented in the SCU35 board schematic.

Table 13: **Power System - Voltage Regulators and INA700 Map**

Rail Name	Nominal Voltage (V)	Max Current (A)	Device	INA700 Addr
VR_OUT_20V	9-20	3	TI TPS25730D	NA
VR_EXT_5V0	5.0	13	MP2422	NA
VR_INT_5V0	5.0	13	MP2422	0x44 I2C1
VR_UTIL_3V3	3.3	5	MP8770CGQ	NA
VR_VCCINT_0V85	0.85	5	MP8770CGQ	0x45 I2C1
VR_VCCINT_IO_BRAM_0V85	0.85	1	MP2183C	NA
VR_VCCADC_1V8	1.8	0.5	MP2181	NA
VR_VCCAUX_HDIO_1V8	1.8	1	MP2183C	NA
VR_VCCAUX_HPIO_1V8	1.8	0.5	MP2181	NA
VR_VCCO_0_1V8	1.8	0.5	MP2181	NA
VR_VCCO_45_46_ADJ	1.2, 1.5, 1.8, 2.5, 3.3 (deafult)	5	MP8770CGQ	NA
VR_VCCO_47_1V8	1.8	4	MP8770CGQ	NA
VR_VCCO_65_66_67_68_3V3	3.3	5	MP8770CGQ	NA

***Note*:** Bus short names are decoded as:

I2C1 = I2C1_INA_SCL/SDA

See I2C Buses and Connections for I2C diagrams and more details.

The PCB layout and power system design meet the recommended criteria described in the *UltraScale Architecture PCB Design User Guide* (UG583).

More information about the power system regulator components can be found at the Monolithic Power Systems (MPS) website.

IMPORTANT! *This power delivery solution is not recommended to be copied into your system as-is. Power subsystems for evaluation boars are over designed for silicon evaluation. For more information and guidelines for an optimal solution, see Answer Record 000037816.*

Monitoring Voltage and Current

Two rails have a TI INA700 digital power monitor circuit with connections to the rail series current sense resistor. This arrangement permits the INA700 to report the sensed parameters separately on the I2C bus. The rails equipped with the INA700 power monitors are shown in the power system table in Board Power System. As described in I2C Buses and Connections, the I2C1 bus provides access to the INA700 power monitors.

For connectivity details see the schematic, which can be accessed through the SCU35 Evaluation Board website.

Chapter 4

Xilinx Design Constraints

Overview

The Xilinx design constraints (XDC) file template for the board provides for designs targeting the evaluation board. Net names in the constraints listed correlate with net names on the latest evaluation board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL.

See the *Vivado Design Suite User Guide: Using Constraints* (UG903) for more information.

The FPGA I/O Banks 45 and 46 are powered by the adjustable voltage VR_VCCO_45_46_ADJ, which can be set to 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V (default). This allows great flexibility when using Raspberry Pi HAT modules. Because different HAT modules implement different circuitry, the I/O standards for banks 45 and 46 must be uniquely defined by each customer design for all I/Os used in these banks. For example, if a HAT that requires 1.8 V I/Os is used and also the GPIOs for the LEDs and switches, the I/O standard for all the I/Os used in these banks must be set to 1.8V.

IMPORTANT! *See the SCU35 board documentation ("Board Files" check box) for the XDC file.*

Appendix A

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

For Technical Support, open a Support Service Request.

CE Information

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

CE Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

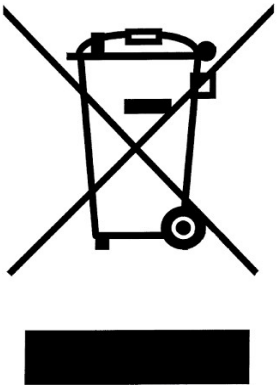
This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

CE Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Compliance Markings



In August of 2005, the European Union (EU) implemented the EU Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU. These directives require Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

AMD has met its national obligations to the EU WEEE Directive by registering in those countries to which AMD is an importer. AMD has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased AMD-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. AMD has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Appendix B

Additional Resources and Legal Notices

Finding Additional Documentation

Technical Information Portal

The AMD Technical Information Portal is an online tool that provides robust search and navigation for documentation using your web browser. To access the Technical Information Portal, go to https://docs.amd.com.

Documentation Navigator

Documentation Navigator (DocNav) is an installed tool that provides access to AMD Adaptive Computing documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the AMD Vivado™ IDE, select **Help → Documentation and Tutorials**.
- On Windows, click the **Start** button and select **Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

***Note*:** For more information on DocNav, refer to the *Documentation Navigator User Guide* (UG968).

Design Hubs

AMD Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- Go to the Design Hubs web page.

Support Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Support.

References

The most up to date information related to the SCU35 board and its documentation is available on this website:

SCU35 Evaluation Board

SCU35 Evaluation Kit — Answer Record 000037816

These documents provide supplemental material useful with this guide:

1. *UltraScale Architecture and Product Data Sheet: Overview* (DS890)
2. *Spartan UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS930)
3. *Spartan UltraScale+ FPGAs Configuration User Guide* (UG860)
4. *Spartan UltraScale+ FPGAs SelectIO Resources User Guide* (UG861)
5. *UltraScale Architecture PCB Design User Guide* (UG583)
6. *UltraScale Architecture Memory Resources User Guide* (UG573)
7. *UltraScale Architecture System Monitor User Guide* (UG580)
8. *UltraScale Architecture Clocking Resources User Guide* (UG572)
9. *Tera Term Terminal Emulator Installation Guide* (UG1036)
10. *Vivado Design Suite User Guide: Using Constraints* (UG903)
11. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
12. Micron Technology (MT25QU128ABA8E12-0SIT)
13. Texas Instruments (INA700, DP83867IR, TPS25730D, TPS259474ARPWR, TPS22950)
14. Samtec, Inc. (QSE series connectors)
15. Infineon Integrated Circuits (S27KS0642)
16. Future Technology Devices International Ltd. (FT4232HL)
17. ST Microelectronics (LIS2DE12TR)
18. Monolithic Power Systems (MP2422, MP8770CGQ, MP2183C, MP2181)

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
11/21/2025 Version 1.0	
Initial release.	N/A

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