VEK385 Evaluation Board

User Guide

UG1712 (v1.0) February 18, 2026

AMD

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Introduction

Overview

The VEK385 board is an evaluation platform for the 2VE3858, which is an AMD Versal™ AI Edge Series Gen 2 adaptive SoC. The VEK385 device targets AI-ML applications with increased compute performance, lower latency, and a higher level of integration enabled by the Versal AI Edge Series Gen 2 devices. The primary focus for the VEK385 board is to serve as a vehicle to deliver solution demonstrations, enable developers with a platform to evaluate the adaptive SoC technology, and begin targeting their own end applications to hardware.

- Automotive
- Aerospace and defense
- Data center compute acceleration
- Test and measurement
- Fiber optic
- Communications

The VEK385 evaluation board is equipped with many of the common board-level features needed for design development, including:

- HDMI 2.1/DisplayPort 1.4 support
- PCIe® support
- CAN support
- PMOD support
- SFP28 optical transceiver support
- QSFP optical transceiver support
- LPDDR5X component memory
- USB 2/USB 3.2
- UFS
- SD 2.0

- Ethernet networking interfaces
- One FMC+ expansion port

Models of Boards

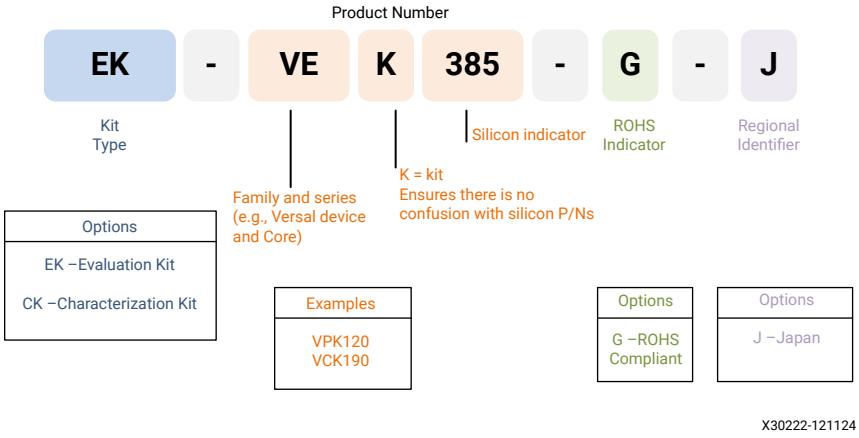
The following table lists the models for the evaluation board. See the Evaluation Board product page for details.

Table 1: **Models of Evaluation Boards**

Kit	Description
EK-VEK385-G	AMD Versal adaptive SoC evaluation kit
EK-VEK385-G-J	AMD Versal adaptive SoC evaluation kit, Japan specific

Versal Device Kit Numbering

The Versal device kit numbering is illustrated in the following figure.



Navigating Content by Design Process

AMD Adaptive Computing documentation is organized around a set of standard design processes to help you find relevant content for your current development task. You can access the AMD Versal™ adaptive SoC design processes on the Design Hubs page. You can also use the Design Flow Assistant to better understand the design flows and find content that is specific to your intended design needs. This document covers the following design processes:

- **Board System Design:** Designing a PCB through schematics and board layout. Also involves power, thermal, and signal integrity considerations. For more information, see Versal Adaptive SoC Design Process Documentation Board System Design.

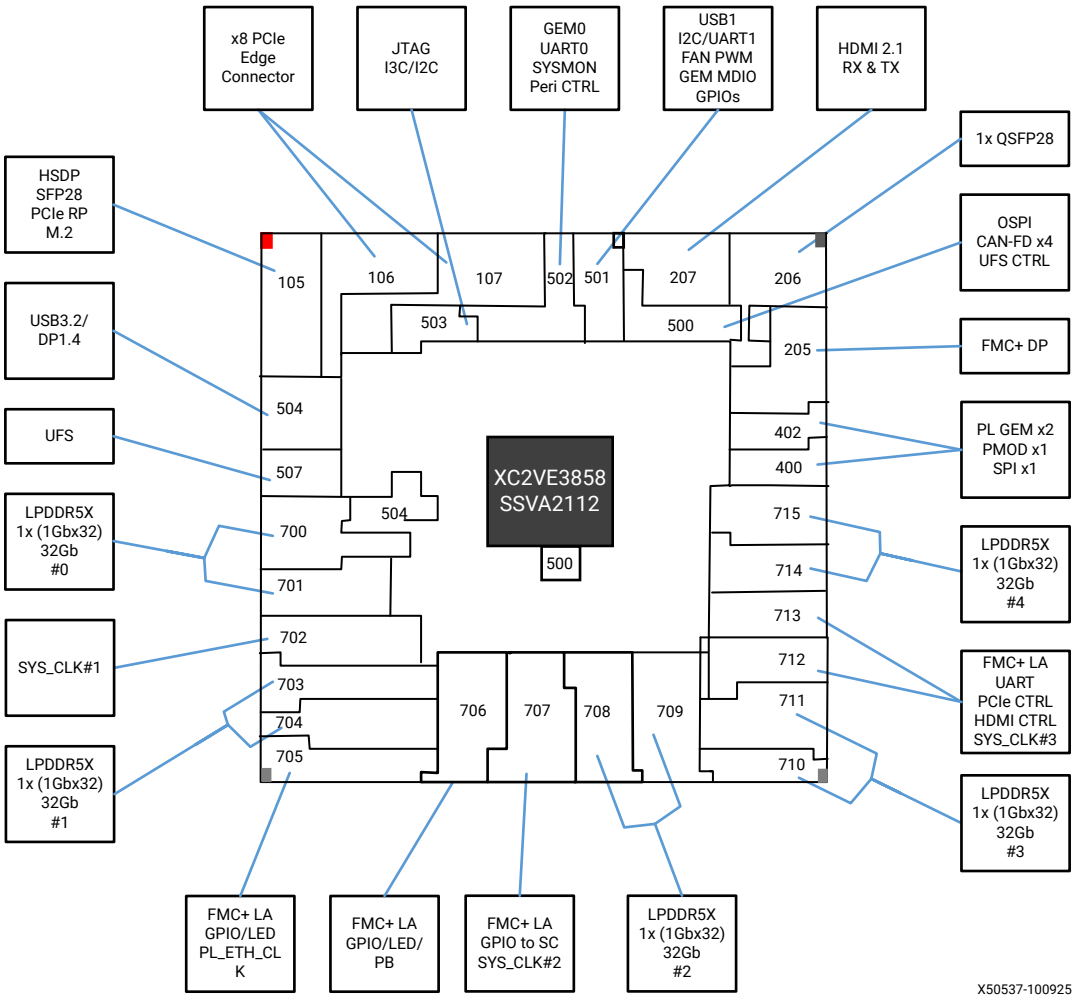
Additional Resources

See Appendix C: Additional Resources and Legal Notices for references to documents, files, and resources relevant to the evaluation board.

Block Diagram

A block diagram of the VEK385 evaluation board is shown in the following figure.

Figure 1: **Evaluation Board Block Diagram**



Board Features

The VEK385 evaluation board features are listed here.

- 2VE3858 device
- SSVA2112 package
- Form factor: see Board Specifications
- Onboard configuration from:
  - USB-to-JTAG bridge
  - JTAG pod 2 mm 2x7 flat cable connector

    - eUFS (PS MIO interface)
    - OSPI
- System Controller from:
    - Quad SPI (QSPI)
    - eMMC
- Clock generation for all board interfaces and peripherals
- Five pin-efficient mode LPDDR5X interfaces (1x32 -bit 4GB components each)
- PL FMCP HSPC (FMC+) connectivity
    - FMCP1 HSPC full LA[00:33] bus
    - GTYP transceivers x4
- PL GPIO connections
    - PL GPIO DIP switch (4-position)
    - PL GPIO LEDs (four)
    - PL GPIO pushbuttons (two)
    - PL System Controller GPIO[8]
        - DUT_IN_SC_GP0[1:4]
        - DUT_OUT_SC_GPI[4:7]
- PL GTYP transceivers (20)
    - FMCP1 (4)
    - QSFP1 (4)
    - HDMI 2.1 (4)
    - PCIe EP (8)
- MMI (PS) GTYP transceivers (4)
    - PCIe RP (2)
    - HSDP (1)
    - SFP28 (1)
- PS PMC MIO connectivity
    - PMC MIO[0:10,12]: boot configuration OSPI (boot configuration)
    - PMC MIO[11]: Full Power Domain Power Down

    - PMC MIO[13]: TP132
    - PMC MIO[14]: SYSTEM_PD
    - PMC MIO[15]: PL_PD
    - PMC MIO[16:23]: CANFD[0:3]
    - PMC MIO[24]: UFS_CFG_CLK
    - PMC MIO[25]: UFS_RST_B
    - PMC MIO[26]: BaseCamp recovery button
    - PMC MIO[27:39]: USB 2.0
    - PMC MIO[40]: System Controller MIO
    - PMC MIO[41]: AIE_PD
    - PMC MIO[42:45]: I2C[0:1]
    - PMC MIO[46:47]: UART1
    - PMC MIO[48]: DP_HPD
    - PMC MIO[49]: Fan PWM
    - PMC MIO[50:51]: GEM0 Control
- PS LPD MIO connectivity
    - LPD_MIO[0:11]: GEM0 Interface
    - LPD_MIO[12:13]: CAN0 Sideband
    - LPD_MIO[14]: USB_HUB_RST_B
    - LPD_MIO[15]: FAN_TACH
    - LPD_MIO[16:17]: UART0
    - LPD_MIO[18:20]: System Controller SYSMON Interface
    - LPD_MIO[21:22]: CAN1 Sideband
    - LPD_MIO[23]: TP141
    - LPD_MIO[24]: TSU_CLK
    - LPD_MIO[25]: GEM0 Reset
- Security: PSBATT button battery backup
- SYSMON header
- Operational switches (power on/off, POR_B, boot mode DIP switch)

- Operational status LEDs (ERROR_OUT, DONE, PS STATUS, PGOOD)
- Power management
- System controller (AMD Kria™ SOM SM-K24-XCL2GC)

The VEK385 evaluation board provides a rapid prototyping platform using the XC2VE3858-2MSESSVA2112 device.

Board Specifications

Dimensions

- **PCB:**

  Height: 8.000 inches (20.32 cm)

  Length: 9.500 inches (24.13 cm)

  Thickness: 65.83 mil ±5 mil (1.67 mm ±0.13 mm)

- **Evaluation Board:**

  Thickness fully assembled: 2.010 inches (5.105 cm)

  Fully assembled, from table to bottom of PCB: 0.667 inches (1.694 cm)

***Note*:** A 3D model of this board is not available.

See the VEK385 Evaluation Kit website for the XDC listing and board schematics.

Environmental

***Note*:** The operating temperature range is not fully tested across the specified temperature range. It is for general guidelines only. Customers should use the evaluation board for evaluation purposes only in a normal lab environment and should not operate beyond room temperature.

- **Temperature:**

  Operating: 0°C to +45°C

  Storage: –25°C to +60°C

- **Humidity:**

  Operating: 8% - 90%

  Storage: 5% - 95%

Operating Voltage

+12 V_{DC}

Mechanical

The VEK385 evaluation board includes a mechanical stiffener to help ensure success with the board under normal lab conditions and use. While it is recommended to not remove this stiffener, it is understood that it might be necessary to remove it for continued evaluation.

The mechanical stiffener is attached with fasteners torqued at 2.5 in-lbs. The 4-40 screws are distributed around the assembly to provide robust mechanical support. When attaching or removing the mechanical stiffener, ensure proper ESD precautions are taken. See Standard ESD Measures for suggestions on best practices.

- Removing the Stiffener

  With power and other cabling unplugged, carefully unscrew the fasteners in any order. Care needs to be taken with the cooling solution as the board is manipulated due to potential excessive forces.

- Attaching the Stiffener

  With power and other cabling unplugged, carefully align the PCBA standoff holes to the sheet metal tray (stiffener) standoffs. Next, it is suggested to insert two screws in opposite corners of the board/tray combination. Loosely tighten the screws to aid in alignment. Add the remaining screws and loosely tighten. Finally, in a left to right or right to left pattern, tighten all screws to 2.5 in-lbs.

***Note*:** The tray will only fit one direction with the screw pattern matching between the PCBA and the mechanical stiffener.

Chapter 2

Board Setup and Configuration

Standard ESD Measures

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

To prevent ESD damage:

- Attach a wrist strap to an unpainted metal surface of your hardware to prevent electrostatic discharge from damaging your hardware.
- When you are using a wrist strap, follow all electrical safety procedures. A wrist strap is for static control. It does not increase or decrease your risk of receiving electric shock when you are using or working on electrical equipment.
- If you do not have a wrist strap, before you remove the product from ESD packaging and installing or replacing hardware, touch an unpainted metal surface of the system for a minimum of five seconds.
- Do not remove the device from the antistatic bag until you are ready to install the device in the system.
- With the device still in its antistatic bag, touch it to the metal frame of the system.
- Grasp cards and boards by the edges. Avoid touching the components and gold connectors on the adapter.
- If you need to lay the device down while it is out of the antistatic bag, lay it on the antistatic bag. Before you pick it up again, touch the antistatic bag and the metal frame of the system at the same time.
- Handle the devices carefully to prevent permanent damage.

Board Component Location

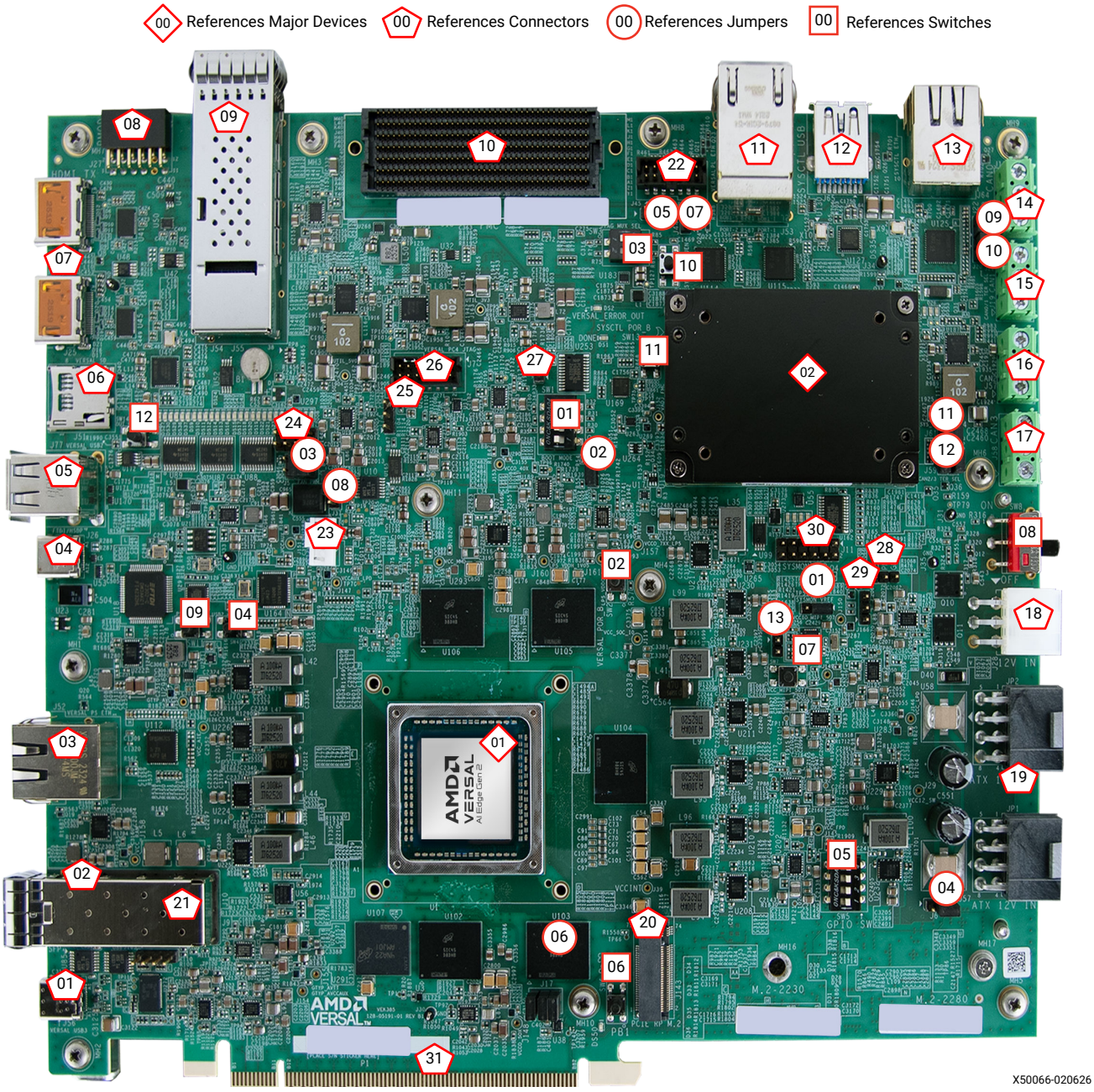
The following figure shows the VEK385 board component locations. Each numbered component shown in the figure is keyed by shape and number. The component details can be located in the associated table.

- Diamond 00 references Major Devices.
- Pentagon 00 references Connectors and Headers.
- Circle 00 references Jumpers.
- Square 00 references Switches.

IMPORTANT! *The following figure is for visual reference only and might not reflect the current revision of the board.*

IMPORTANT! *There could be multiple revisions of this board. The specific details concerning the differences between revisions are not captured in this document. This document is not intended to be a reference design guide and the information herein should not be used as such. Always refer to the schematic, layout, and XDC files of the specific VEK385 version of interest for such details.*

Figure 2: **Evaluation Board Component Locations**



Major Devices

The following table identifies the major devices for the VEK385. The table lists major devices numerically and can be located in Figure 2 by referring to the callout number located in a diamond 00 shape. Major devices can be located in the schematic for more details.

Table 2: **Major Devices**

Callout Number	Ref. Des.	Feature	Notes
1	U1	AMD Versal™ AI Edge Series Gen 2 adaptive SoC	AMD XC2VE3858-2MSESSVA2112 (1)
2	JA1, JA2	AMD Kria™ K24 SOM	AMD SM-K24-XCL2GC

Notes:

1. The VEK385 evaluation board includes a heatsink with a thermal resistance of 0.307°C/W.

Connectors and Headers

The following table identifies the connectors for the VEK385. The table lists connectors and headers numerically and can be located in Figure 2 by referring to the callout number located in a pentagon 00 shape. Connectors and headers can be located in the schematic for more details.

CAUTION! *Do NOT plug a PC ATX power supply 6-pin connector into the VEK385 board power connector J16. The ATX 6-pin connector has a different pinout than J16. Connecting an ATX 6-pin connector into J16 damages the VEK385 board and voids the board warranty.*

Table 3: **Connectors and Headers**

Callout Number	Ref. Des.	Feature	Notes
1	J56	Versal AI Edge Series Gen 2 adaptive SoC USB 3.1 Gen 2 Type C RA	Amphenol 12401598E4#2A
2	J9, J10	zSFP+ RA	Molex 1703820001
3	J52	RJ-45 Tri-Ethernet Gigabit RA	HALO HFJ11-1G01E-L12RL
4	J26	FTDI (JTAG)/HSDP USB 3.1 Gen 2 Type C RA	Amphenol 12401598E4#2A
5	J77	Dual USB 2.0 Type A RA	Amphenol GSB12221LRSEU
6	J51	Micro SD Card RA	Molex 5025700893
7	J24, J25	HDMI 2.1 RA	Molex 2086581061
8	J27	PMOD 2x6 connector	Samtec SSQ-106-02-F-D-RA 2.54mm pitch
9	J54, J55	zQSFP+ RA	Molex 1000141901-2
10	J13	FMCP1	Samtec ASP-184329-01 560 position connector 14x40 1.27mm
11	J53	Versal AI Edge Series Gen 2 adaptive SoC RJ-45 Stacked Dual Tr-Ethernet Gigabit RA	Bel Fus 0879-2C1R-54
12	J65	USB 3.0 Type A RA	Wurth 692122030100
13	J64	System Controller RJ-45 Tri-Ethernet Gigabit RA	HALO HFJ11-1G01E-L12RL
14	J18	CAN0	Phoenix 1935174 Screw terminal block
15	J19	CAN1	Phoenix 1935174 Screw terminal block

Table 3: **Connectors and Headers** *(cont'd)*

Callout Number	Ref. Des.	Feature	Notes
16	J57	CAN2	Phoenix 1935174 Screw terminal block
17	J58	CAN3	Phoenix 1935174 Screw terminal block
18	J28	Power connector, 2x3, for ACDC power adapter	Molex 0039301060 Conn. ddr. RA 6 pos. 2x3 4.2 mm
19	JP1, JP2	Power connect, 2x4, for ATX PCIe power	Astron Technology 6652208-T0003T-H Conn. hdr. male RA 8 pos. 2x4 4.2 mm
20	J143	PCIe M.2 Gen 5 Card Edge Connectors	Amphenol MDT420M01501 Female Connector M.2 75 Position 0.020" (0.50mm)
21	J165	USB 3.2 PD controller direct I2C Interface	
22	J45	PC4 JTAG Header for System Controller	
23	J38	12V 4 pin fan header	Refer to the PMXC_MIO[49] and PSXC_MIO[15] Fan Control section for more information.
24	J144	PL GPIO (PL_SPI_1O(0:5))	**CAUTION!** *Caution must be taken as this header has a direct connection to U1. Refer to Standard ESD Measures for more information.*
25	J74	I2C Header for SiT95314 (U164) external memory (U165)	Refer to Table 10 for more information.
26	J7	PC4 JTAG Header for Versal AI Edge Series Gen 2 (U1)	
27	J75	I2C Header for SiT95211 (U101) external memory (U166)	Refer to Table 10 for more information.
28	J1	PMBUS 1 Header	
29	J166	PMBUS2 Header	
30	J11	SYSMON Header	
31	P1	PCIe Edge Connector	PL PCIE5x8 Card Edge

Jumpers

The following table identifies the default jumper settings for the VEK385. The table lists jumpers numerically and can be located in Figure 2 by referring to the callout number located in a circle (00) shape. Jumpers can be located in the schematic for more details.

Table 4: **Default Jumper Settings**

Callout Number	Ref. Des.	Function	Default
1	J12	SYSMON VREFP SEL 1-2: External VREF 2-3: Disable external VREF	1-2 jumpered
2	J4	POR_B supervisor SENSE input 1-2: VCCO_MIO ramp-up sense (1.8V) 2-3: VCCAUX_PMC ramp-up sense (1.5V)	2-3 jumpered
3	J5	POR_B enable header 1-2: SYSCTLR can drive POR_B 3-4: PC4 can drive POR_B 5-6: FTDI can drive POR_B Open: POR_B source not connected	1-2 jumpered 3-4 jumpered 5-6 open
4	J6	VCC Fuse enable 1-2: Fuse enabled 2-3: Fuse disabled	2-3 jumpered
5	J8	JTAG source enable 1-2: JTAG sources disabled 2-3: JTAG sources enabled	2-3 jumpered
6	J17	PCIE PRSNT_B WIDTH SEL 1-2: x1 3-4: x4 5-6: x8	1-2 jumpered 3-4 jumpered 5-6 jumpered
7	J44	System Controller Boot Mode Pin	Open: QSPI Boot Jumpered: JTAG Boot
8	J37	Fan type 1-2: System controller PWM 2-3: Versal adaptive SoC MIO PWM	1-2 jumpered
9	J22, J23	CAN0 BUS termination option (60.4ohm resistors)	Installed
10	J20, J21	CAN1 BUS termination option (60.4ohm resistors)	Installed
11	J61, J64	CAN2 BUS termination option (60.4ohm resistors)	Installed
12	J59, J60	CAN3 BUS termination option (60.4ohm resistors)	Installed
13	J43	Factory Only	Open

Switches

The following table identifies the default switch settings for the VEK385. The table lists switches numerically and can be located in Figure 2 by referring to the callout number located in a square 00 shape. Switches can be located in the schematic for more details.

Table 5: **Default Switch Settings**

Callout Number	Ref. Des.	Function	Default
1	SW1	U1 mode 4-pole DIP switch Mode = SW1[1:4] = Mode[0:3] UFS = OFF,OFF,ON,OFF = 1101 OSPI = ON,ON,ON,OFF = 0001 JTAG = ON,ON,ON,ON = 0000	ON,ON,ON,ON
2	SW2	VEK385 power-on reset (POR_B)	OPEN
3	SW3	SYSCTLR JTAG source selection Switch OFF = 1 = high; ON = 0 = low SYSCTLR JTAG SOURCE SEL = SW3[1:2] = SEL[0:1] PL JTAG = ON,ON = 00 FTDI JTAG = OFF,ON = 10	OFF,ON
4	SW4	User USB reset	OPEN
5	SW5	GPIO DIP switch Switch OFF = 0 = low; ON = 1 = high	OFF,OFF,OFF,OFF
6, 7	SW6, SW7	User push-button inputs ***Note***: Pushbutton switch default = open = logic low (not pressed).	OPEN
8	SW8	Main power	OFF
9	SW11	User GEM Reset	OPEN
10	SW12	System controller FWUEN push-button SYSCTRL_FWUEN_C2M_B	OPEN
11	SW13	System controller power-on reset (SYSCTL_POR_B)	OPEN
12	SW14	BaseCamp Image Recovery Button	OPEN

Versal Device Configuration

The “Platform Boot, Control, and Status” section of the *Versal AI Edge Series Gen 2 and Prime Series Gen 2 Technical Reference Manual* (AM026) describes the Versal 2VE3858 device boot process. The VEK385 board supports a subset of the modes documented in the technical reference manual via onboard boot options. The mode DIP switch SW1 configuration option settings are listed in the following table.

Table 6: **Mode Switch SW1 Configuration Option Settings**

Boot Mode	Mode Pins [0:3][2]	Mode SW1 [1:4][2]
JTAG	0000[1,3]	ON, ON, ON, ON
OSPI	0001	ON, ON, ON, OFF

Table 6: **Mode Switch SW1 Configuration Option Settings** *(cont'd)*

Boot Mode	Mode Pins [0:3][2]	Mode SW1 [1:4][2]
UFS	1101	OFF, OFF, ON, OFF

Notes:

1. Default switch setting.
2. Mode DIP SW1 poles [1:4] correspond to U1 2VE3858 MODE[0:3].
3. Mode DIP SW1 individual switches ON=LOW (p/d to GND)=0, OFF=HIGH (p/u to VCCO)=1.

JTAG

The AMD Vivado™, Vitis, or third-party tools can establish a JTAG connection to the Versal Gen 2 device in the two ways described in this section.

- FTDI FT4232 USB-to-JTAG/USB-UART device (U18) connected to USB3 type-C connector (J26), which requires:
  - Set boot mode SW1 for JTAG as indicated in the "Mode Switch SW1 Configuration Option Settings" table in Versal Device Configuration.
  - Place a shunt on pins 2-3 of the JTAG mux enable header (J8) to enable the JTAG interface. See Table 5 for defaults.
  - Set 2-pole DIP SW3[1:2] to 10 (OFF, ON) to select JTAG MUX channel 2 from the FT4232 U18 USB to JTAG bridge.
  - Power-cycle the evaluation board or press the power-on reset (POR) pushbutton (SW2). SW2 is near the USB-C JTAG port J26.
- JTAG pod flat cable connector J7 (2 mm 2x7 shrouded/keyed), which requires:

  ***Note*:** In this mode, the FT4232 device (U18) UART functionality continues to be available.
  - Set boot mode SW1 for JTAG as indicated in the "Mode Switch SW1 Configuration Option Settings" table in Versal Device Configuration.
  - Place a shunt on pins 1-2 of the JTAG mux enable header (J8) to disable the JTAG interface. See Table 5 for defaults.
  - The 2-pole DIP SW3[1:2] setting does not matter as the MUX is inhibited/turned off.
  - Power-cycle the board or press the POR pushbutton SW2. SW2 is near the center of the board, between the system controller and the 2VE3858 in Figure 2. SW2 can be located by referencing Table 5.

OSPI

This boot mode is supported onboard and is wired to the 2VE3858 U1 bank 500 PMC_MIO[0:10,12] pins. The octal SPI controller can access the device using several different methods. See the Flash Memory Controllers section of the *Versal AI Edge Series Gen 2 and Prime Series Gen 2 Technical Reference Manual* (AM026) and *Vivado Design Suite User Guide: Programming and Debugging* (UG908) for more information. To boot from the OSPI flash:

1. Store a valid 2VE3858 adaptive SoC boot image file in the OSPI.
2. Set boot mode SW1 for OSPI as indicated in the "Mode Switch SW1 Configuration Option Settings" table in Versal Device Configuration.
3. Power-cycle the VEK385 board or press the POR pushbutton SW2. SW2 is near the center of the board, between the system controller and the 2VE3858 in Figure 2. SW2 can be located by referencing Table 5.

***Note*:** For timing consideration of an OSPI design, refer to the *Versal Adaptive SoC PCB Design User Guide* (UG863) to determine MAX configuration rates.

UFS

This boot mode is supported onboard and is wired to the 2VE3858 (U1) bank 500 and 507. To boot from UFS Flash:

1. Store a valid 2VE3858 boot image file in the UFS device.
2. Set boot MODE SW1 for UFS as indicated in the "Mode Switch SW1 Configuration Option Settings" table in Versal Device Configuration.
3. Power-cycle the VEK385 board or press the POR pushbutton SW2. SW2 is near the center of the board, between the system controller and the 2VE3858 in Figure 2. SW2 can be located by referencing Table 5.

Chapter 3

Board Component Descriptions

Component Descriptions

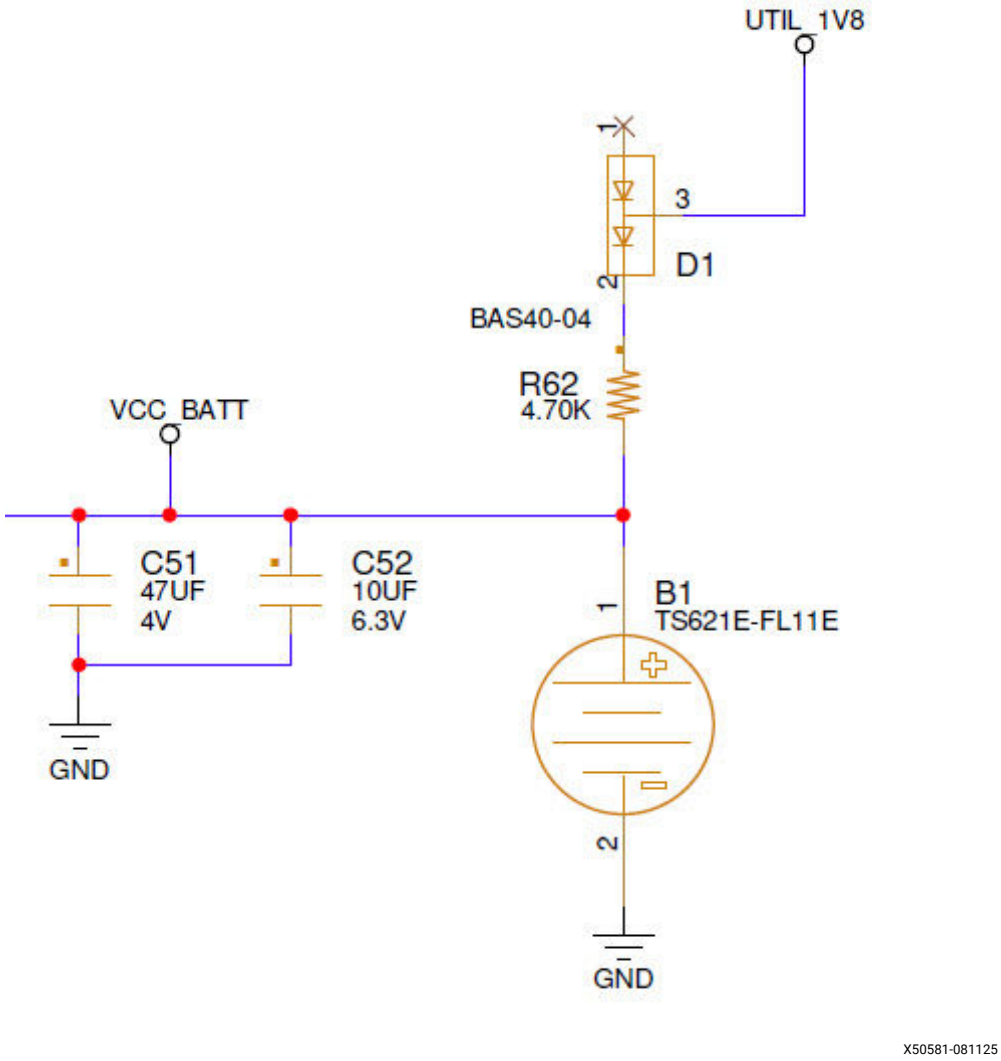
Versal Device

The VEK385 evaluation board is populated with the AMD Versal™ AI Edge Series Gen 2 adaptive SoC XC2VE3858-2MSESSVA2112 device, which combines a powerful processing system (PS) and programmable logic (PL) in the same device. The PS in a Versal AI Edge Series Gen 2 adaptive SoC device features the Arm® flagship Cortex®-A78 64-bit dual-core quad cluster processor and Cortex-R52 dual-core quint cluster real-time processor. For additional information on the Versal AI Edge Series Gen 2 adaptive SoC XC2VE3858-2MSESSVA2112 device, see the *Versal AI Edge Series Gen 2 Data Sheet: DC and AC Switching Characteristics* (DS1021). See the *Versal AI Edge Series Gen 2 and Prime Series Gen 2 Technical Reference Manual* (AM026) for more information about Versal device configuration options.

Encryption Key Battery Backup Circuit

The 2VE3858 device U1 implements bitstream encryption key technology. The VEK385 board provides the encryption key backup battery circuit as shown in the following figure.

Figure 3: **Encryption Key Backup Circuit**



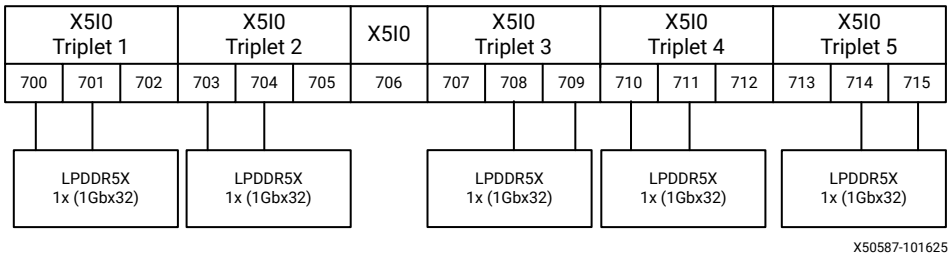
The Seiko TS621E rechargeable 1.5V lithium button-type battery B1 is soldered to the board with the positive output connected to the 2VE3858 device U1 VCC_BATT bank pin AM16. The battery supply current ICC_BATT specification is 160 nA maximum when board power is off. Battery B1 is charged from the UTIL_1V8 1.8V rail through a series diode with the first forward drop to yield between 0.24V to 0.46V over temperature per fixed 5 mA load, limiting 1.56V max at the device pin, VCC_BATT. The diode with 4.7 kΩ current limit resistor allows the battery to trickle charge and prevent battery B1 from back powering UTIL_1V8.

LPDDR5X Component Memory

The 2VE3858 device PL DDR memory interface performance is documented in the *Versal AI Edge Series Gen 2 Data Sheet: DC and AC Switching Characteristics* (DS1021). The VEK385 board LPDDR5X component memory interfaces adhere to the constraints guidelines documented in the "PCB guidelines for Memory Interfaces" section of the *Versal Adaptive SoC PCB Design User Guide* (UG863). The VEK385 LPDDR5X component interface is a 40Ω impedance implementation. Other memory interface details are also available in the *Programmable Network on Chip (NoC2) LogiCORE IP Product Guide* (PG406) and the *Integrated DDR5/LPDDR5/5X Memory Controller LogiCORE IP Product Guide* (PG456). For more memory component details, refer to the below part number and manufacturer details. For the most current part number, see the Bill of Materials (BOM). The detailed device connections for the feature described in this section are documented in the VEK385 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

The VEK385 evaluation board hosts five LPDDR5X memory systems, each with a dual die 1G x 32 component for a total of 20 GB of LPDDR5X SDRAM as detailed below.

Figure 4: **LPDDR5X Component Memory**



2VE3858 U1 has been configured with five triplet banks using pin efficient layout. This allows bank 702, 705, 706, 707, 712, and 713 to be assigned to other features.

- X5IO triplet 1 (banks 700/701/702)
- X5IO triplet 2 (banks 703/704/705)
- X5IO triplet 3 (banks 707/708/709)
- X5IO triplet 4 (banks 710/711/712)
- X5IO triplet 5 (banks 713/714/715)

Each VEK385 triplet supports one 32-bit 1 Gb component interface (4 GB per triplet). The VEK385 evaluation board uses the LPDDR5X memory components as follows:

- Manufacturer: Micron
- Part number: MT62F1G32D2DS-023 WT:C
- Component description
  - 32 Gb (1 Gb x 32)

- 1.05V 315-ball TFBGA
- LPDDR5X (8533 Mb/s)

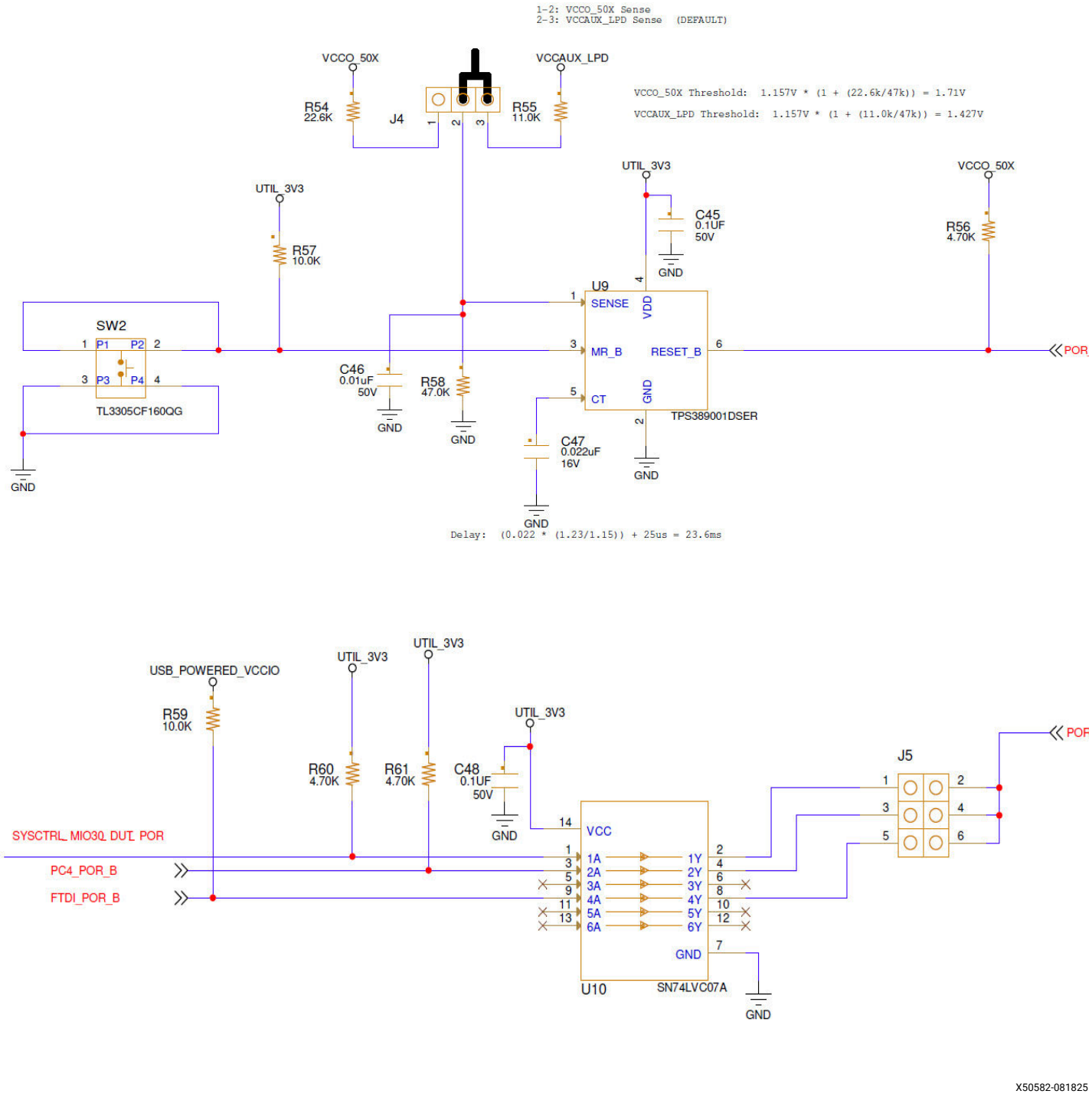
System Reset POR_B

POR_B is the Versal device processor reset, which can be controlled by:

- AMD Kria™ K24 SYSCTLR (JA1)
- PC4 header (J7)
- FTDI USB JTAG chip (U18)
- Reset Push Button (SW2)

The VEK385 board POR circuit is shown in the following figure. U10 allows directional open drain level shifting for all of these masters and J5 allows them to be bused together if desired. The TPS389001 U9 supervisor chip holds POR_B off until power is valid.

Figure 5: **POR_B Reset Circuit**



PMC and LPD MIO

The following sections provide the MIO peripheral mapping implemented on the VEK385 evaluation board. See the *Versal AI Edge Series Gen 2 and Prime Series Gen 2 Technical Reference Manual* (AM026) for more information on MIO peripheral mapping. Additional signal connectivity can be located in the following schematic sections:

- Bank 500: See schematic page 15
- Bank 501: See schematic page 15
- Bank 502: See schematic page 16

The following table provides MIO peripheral mapping implemented on the VEK385 evaluation board. The Versal device bank 500, 501, and 502 mappings are listed in the following table.

Table 7: **MIO Peripheral Mapping**

Bank	MIO #	Device	Signal	Notes
500	0	OSPI	PMXC_MIO0_OSPI_CLK	
	1		PMXC_MIO1_OSPI_DQ0	
	2		PMXC_MIO2_OSPI_DQ1	
	3		PMXC_MIO3_OSPI_DQ2	
	4		PMXC_MIO4_OSPI_DQ3	
	5		PMXC_MIO5_OSPI_DQ4	
	6		PMXC_MIO6_OSPI_DQS	
	7		PMXC_MIO7_OSPI_DQ5	
	8		PMXC_MIO8_OSPI_DQ6	
	9		PMXC_MIO9_OSPI_DQ7	
	10		PMXC_MIO10_OSPI0_CS_B	
	11	Power Management	PMXC_MIO11_FPD_PD	See Board Power System
	12	OSPI	PMXC_MIO12_OSPI_RST_B	
	13	Test Point	TP132	
	14	Power Management	PMXC_MIO14_SYSTEM_PD	See Board Power System
	15		PMXC_MIO15_PL_PD	See Board Power System
	16	CAN	PMXC_MIO16_CANFD0_RX	
	17		PMXC_MIO17_CANFD0_TX	
	18		PMXC_MIO18_CANFD1_TX	
	19		PMXC_MIO19_CANFD1_RX	
	20		PMXC_MIO20_CANFD2_RX	
	21		PMXC_MIO21_CANFD2_TX	
	22		PMXC_MIO22_CANFD3_RX	
	23		PMXC_MIO23_CANFD3_TX	
	24	UFS	CLK95211_OUT4P_UFS_CFG_CLK	
	25		PMXC_MIO25_UFS_RST_B	

Table 7: **MIO Peripheral Mapping** *(cont'd)*

Bank	MIO #	Device	Signal	Notes
501	26	Recovery	SW14	BaseCamp Image Recovery Button
	27	USB 2.0 Hub	PMXC_MIO27_USB2PHY_RST_B	Hub provides
	28		PMXC_MIO28_ULPI_TXD0	P1: SD Card 2.0
	29		PMXC_MIO29_ULPI_TXD1	P2: USB Downstream
	30		PMXC_MIO30_ULPI_TXD2	P3: USB Downstream
	31		PMXC_MIO31_ULPI_TXD3	See schematic page 45-47
	32		PMXC_MIO32_ULPI_CLK	
	33		PMXC_MIO33_ULPI_TXD4	
	34		PMXC_MIO34_ULPI_TXD5	
	35		PMXC_MIO35_ULPI_TXD6	
	36		PMXC_MIO36_ULPI_TXD7	
	37		PMXC_MIO37_ULPI_DIR	
	38		PMXC_MIO38_ULPI_STP	
	39		PMXC_MIO39_ULPI_NXT	
	40	Factory Reserved	PMXC_MIO40_SYSCTRL_MIO64	K24 System Controller Signal
	41	Power Management	PMXC_MIO41_AIE_PD	
	42	I2C	PMXC_MIO42_I2C0_SCL	
	43		PMXC_MIO43_I2C0_SDA	
	44		PMXC_MIO44_I2C1_SCL	
	45		PMXC_MIO45_I2C1_SDA	
	46	UART	PMXC_MIO46_UART1_TXD	
	47		PMXC_MIO47_UART1_RXD	
	48	I3C	PMXC_MIO48_DP_HPD	
	49	Fan Control	PMXC_MIO49_FAN_PWM	
	50	GEM	PMXC_MIO50_GEM0_MDC	
	51		PMXC_MIO51_GEM0_MDIO	

Table 7: **MIO Peripheral Mapping** *(cont'd)*

Bank	MIO #	Device	Signal	Notes
502	0	GEM	PSXC_MIO0_RGMII_TX_CLK	
	1		PSXC_MIO1_RGMII_TXD0	
	2		PSXC_MIO2_RGMII_TXD1	
	3		PSXC_MIO3_RGMII_TXD2	
	4		PSXC_MIO4_RGMII_TXD3	
	5		PSXC_MIO5_RGMII_TX_CTL	
	6		PSXC_MIO6_RGMII_RX_CLK	
	7		PSXC_MIO7_RGMII_RXD0	
	8		PSXC_MIO8_RGMII_RXD1	
	9		PSXC_MIO9_RGMII_RXD2	
	10		PSXC_MIO10_RGMII_RXD3	
	11		PSXC_MIO11_RGMII_RX_CTL	
	12	CAN	PSXC_MIO12_CANFD0_INH	
	13		PSXC_MIO13_CAN0_nSTB	
	14	USB	PSXC_MIO14_USB_HUB_RST_B	
	15	Fan Control	PSXC_MIO15_FAN_TACH	
	16	UART	DUT_MIO16_UART0_RXD	
	17		DUT_MIO17_UART0_TXD	
	18	System Controller SYSMON Interface	SC_HPA07N_DUT_MIO18_SMON_SCL	
	19		SC_HPA06P_DUT_MIO19_SMON_SDA	
	20		SC_HPA06N_DUT_MIO20_SMON_ALERT	
	21	CAN	PSXC_MIO21_CANFD1_INH	
	22		PSXC_MIO22_CAN1_nSTB	
	23	Test Point	TP141	
	24	GEM	CLK95211_OUT5P_TSU_CLK	
	25		PSXC_MIO25_GEM_RST_B	

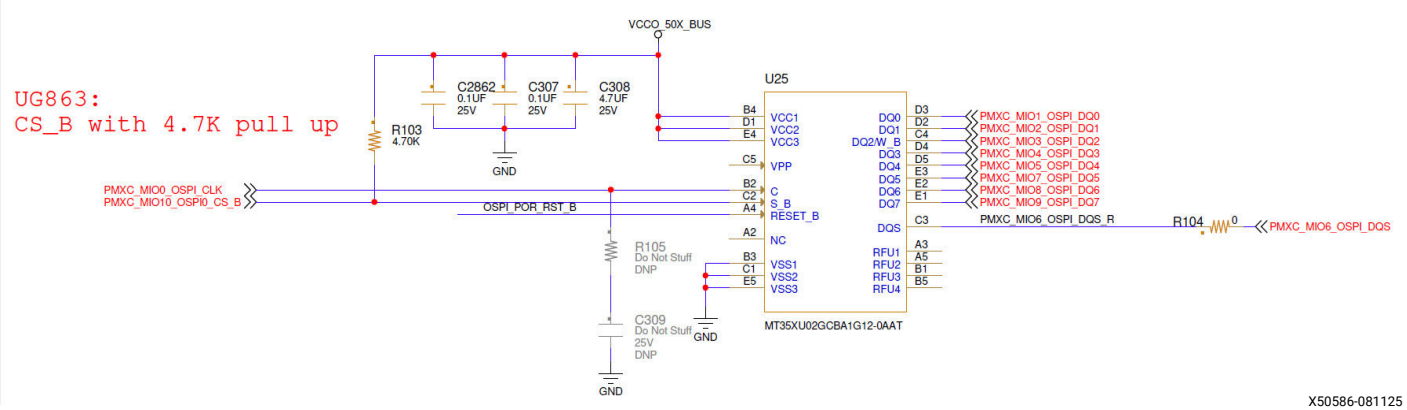
PMXC_MIO[0:10,12] OSPI

The VEK385 evaluation board uses one Micron MT35XU02GCBA1G12-0AAT 8-bit serial peripheral interface (octal SPI) flash device. This 2 Gb NOR flash device can be used as onboard boot, as well as non-volatile storage memory. When used as a boot source, it is selectable from SW1. See Switches for more information.

Refer to the OSPI topic for configuration and design tips.

See schematic page 44.

Figure 6: **OSPI Circuit**



PMXC_MIO[11,14,15,41] Power Enable

The VEK385 allows the Versal device to control the power to the various power domains. This is an active-High signal. It is connected to the components that are controlled using an open-drain buffer. Signals are listed in the following table with their associated power domains. The output of the buffers are pulled up with a 4.7K resistor to aid in the default boot state being set properly. When J43 is installed, the associated power enables and, consequently, power supplies are disabled. This can be useful when changing the programmable power supply default programming. When not installed, the master power switch (SW8) and MPS MPQ4385 step-down switching regulator (U186) device shares control. Further the MPS MPQ79730F PMIC (U256) controls the Low Power Domain (LPD), whereas the Versal does not have control over this domain. See schematic page 3, 4, 76, 101, 105 for more information (see Jumpers for defaults).

Table 8: **PMXC_MIO[11,14,15,41] Power Domains**

Versal Device Pin	Signal	Power Domains
PMXC_MIO11	PMXC_MIO11_FPD_PD	Full Power Domain (FPD)
PMC MIO14	PMXC_MIO14_SYSTEM_PD	System Power Domain (SoC)
PMXC_MIO15	PMXC_MIO15_PL_PD	Programmable Logic Domain (PL)
PMXC_MIO41	PMXC_MIO41_AIE_PD	AIE Domain (AIE)

***Note*:** See Board Power System for more information. The PMIC controls many other domains listed in the Table 22. Thus proper sequencing is maintained where necessary.

PMXC_MIO[13] and PSXC_MIO[23] Test Points

The VEK385 provides two test points for use in accelerating development. Test point TP132 is connected to PMXC_MIO[13]. Test point TP141 is connected to PSXC_MIO[23]. Refer to schematic page 15 and 16 for more information.

CAUTION! *Care needs to be taken when using these test pads, as they directly connect to the 2VE3858. The test pads do not have protection against ESD or other potential sources of damage. Refer to Standard ESD Measures for basic ESD safety. Refer to a proper source on ESD safety before using these test points.*

PMXC_MIO[16:23] and PSXC_MIO[12-13,21-22] CAN Interface

The VEK385 board provides four CAN-FD buses. These can be used for prototyping and support classic CAN and CAN FD up to 8 Mb/s. While many configurations are available, the design intention is for the VEK385 board to be a device on the bus.

CAN I/O interface

The four provided CAN-FD capable buses are identical, with the exception that CAN0 and CAN1 supports sleep mode while CAN2 and CAN3 does not. Sleep mode is connected such that when the VEK385 is a device, it can be put to sleep through CAN functions provided for in the transceiver. For more information, see the TI TCAN1043N datasheet and the VEK385 schematic pages 48 and 49.

Buses are connected from the 2VE3858 through various pins. PMXC_MIO[16:17] and PSXC_MIO[12:13] make up CAN0 and PMXC_MIO[18:19] and PSXC_MIO[21:22] make up CAN1. CAN0 and CAN1 have additional pins allocated to enable sleep mode.

CAN0 connects to a TI TCAN1043N CAN FD transceiver (U39). The output bus connects to screw terminal J18 for easy prototyping. Separate 60.4Ω resistors can be added to CAN0_CANL and CAN0_CANH using J22 and J23, respectively. CAN0 also has the INH and nSTB pins connected between U39 and the 2VE3858 (U1) to aid in sleep mode control. See the VEK385 schematic pages 15, 16, and 48 for details.

CAN1 connects to a TI TCAN1043N CAN FD transceiver (U40). The output bus connects to screw terminal J19 for easy prototyping. Separate 60.4Ω resistors can be added to CAN1_CANL and CAN1_CANH using J20 and J21, respectively. CAN1 also has the INH and nSTB pins connected between U40 and the 2VE3858 (U1) to aid in sleep mode control. See the VEK385 schematic pages 15, 16, and 48 for details.

CAN2 connects to a TI TCAN1043N CAN FD Transceiver (U119). The output bus connects to screw terminal J57 for easy prototyping. Separate 60.4Ω resistors can be added to CAN2_CANL and CAN2_CANH using J61 and J62 respectively. Refer to VEK385 schematic page 15, 49 for details.

CAN3 connects to a TI TCAN1043N CAN FD Transceiver (U120). The output bus connects to screw terminal J58 for easy prototyping. Separate 60.4Ω resistors can be added to CAN3_CANL and CAN3_CANH using J59 and J60 respectively. Refer to VEK385 schematic page 15, 49 for details.

Figure 7: **CAN Interfaces 0-1**

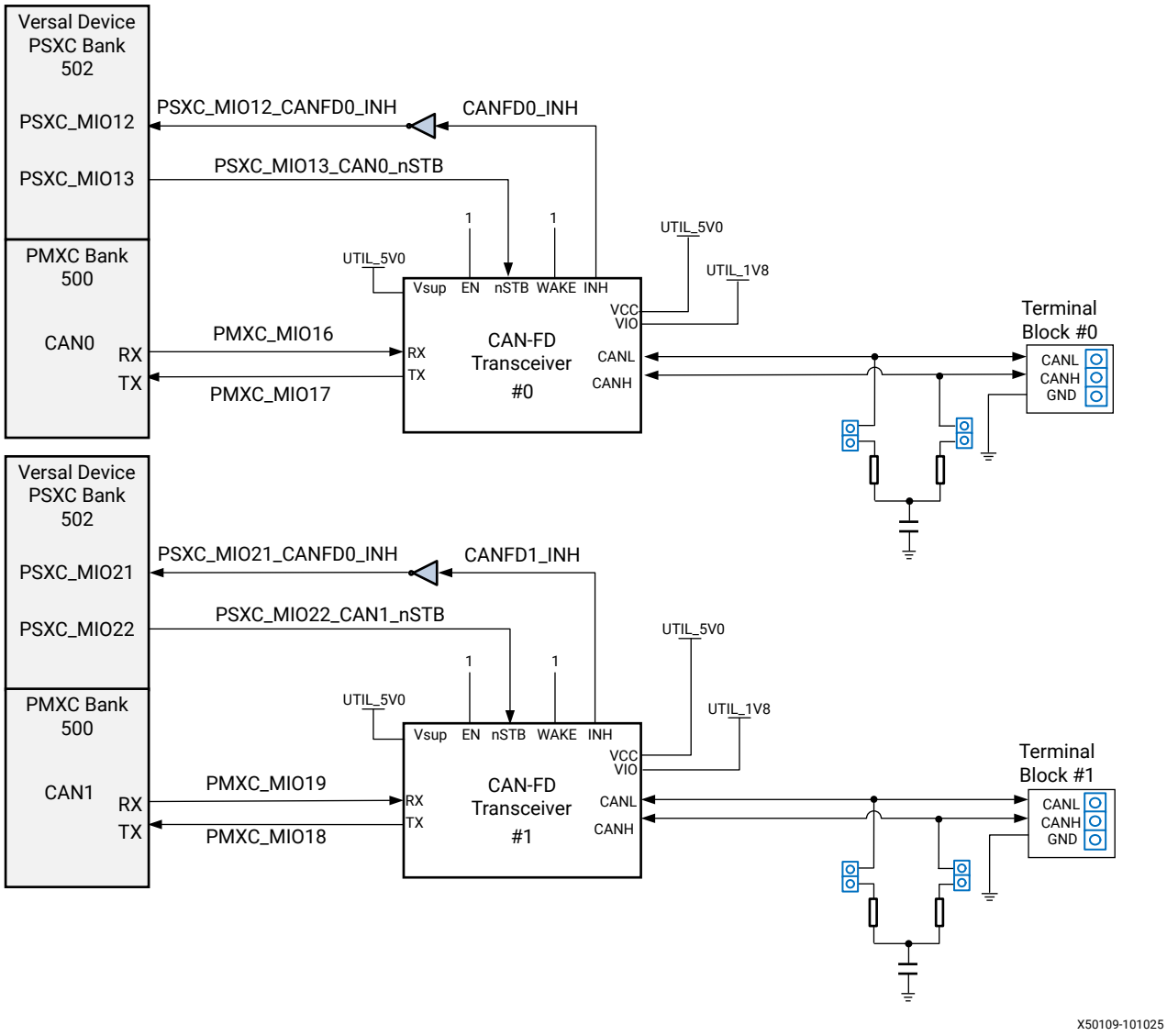
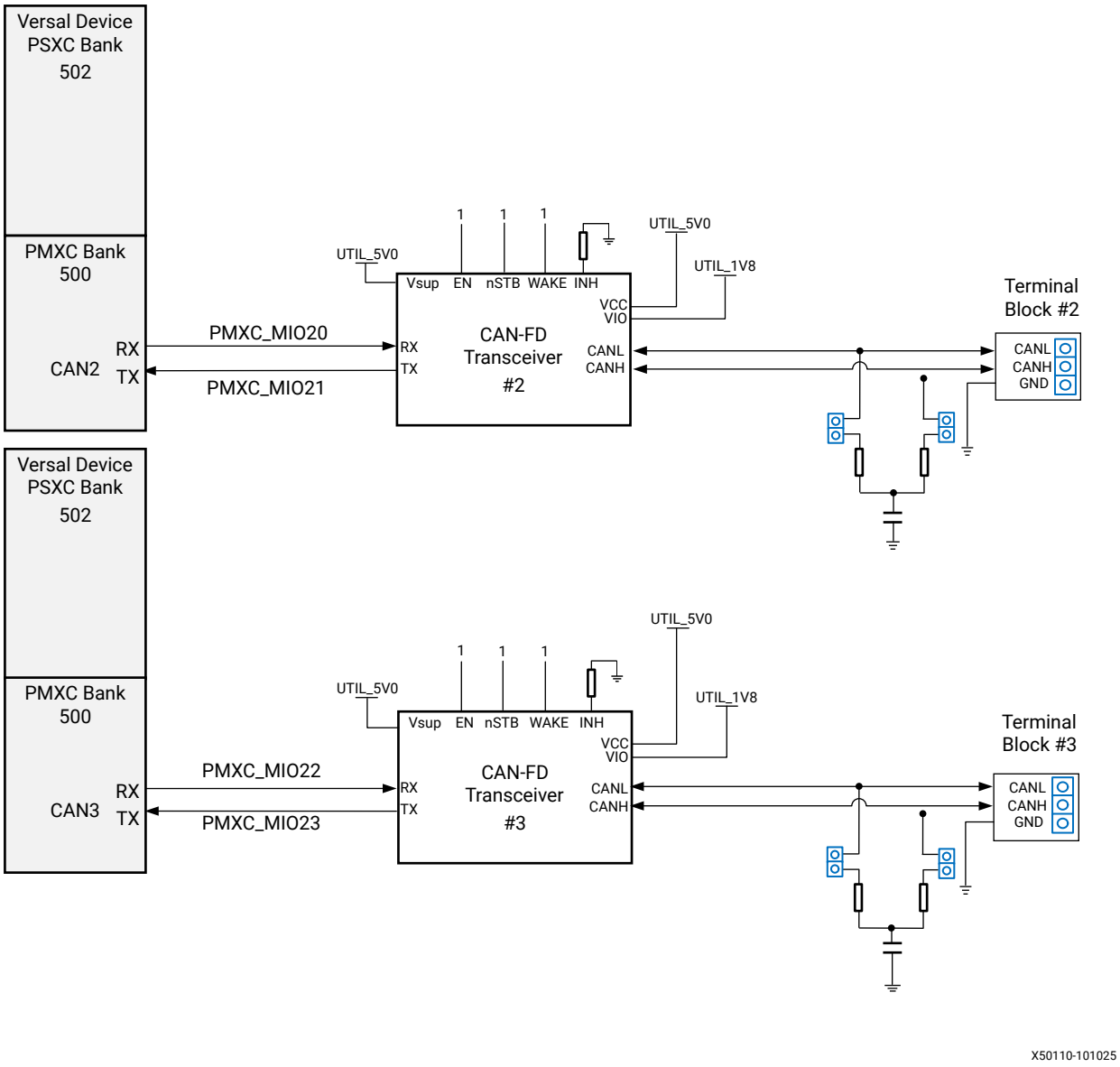


Figure 8: **CAN Interfaces 2-3**



PMXC_MIO[24:25] and Bank 507 UFS

The VEK385 evaluation board includes a universal flash storage (UFS) interface to provide access to general purpose non-volatile flash memory. This interface is used for mass storage from a Micron 64 GB UFS and NAND flash component.

The UFS interface signals PMXC_MIO[24:25] are connected to 2VE3858 device bank 500 and bank 507. The following figures show the connections of the UFS interface on the VEK385 evaluation board.

Figure 9: **UFS Clock and Reset Connections**

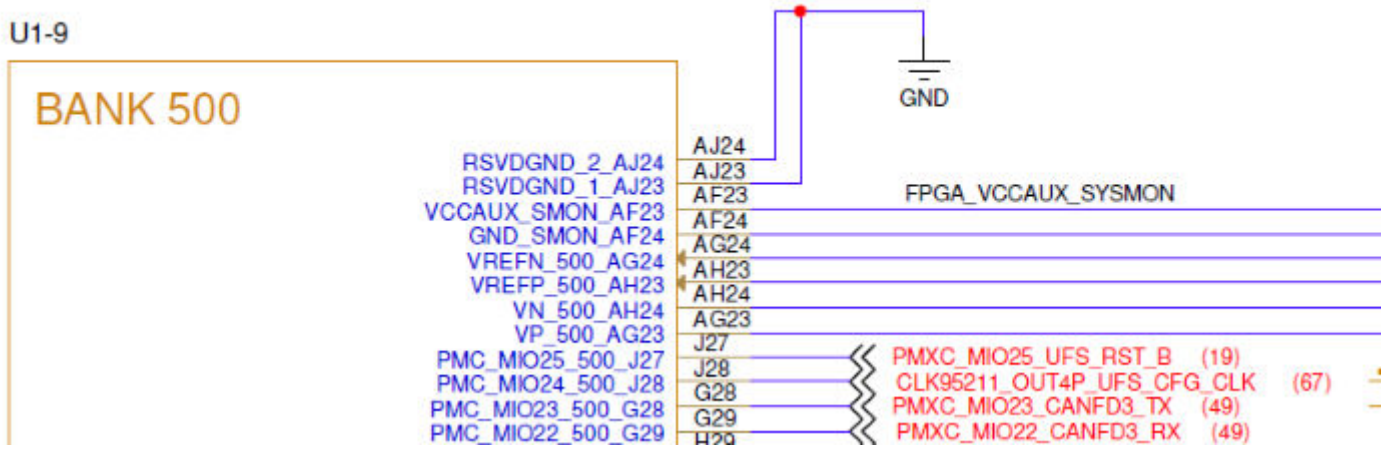


Figure 10: **UFS Interface Connections**

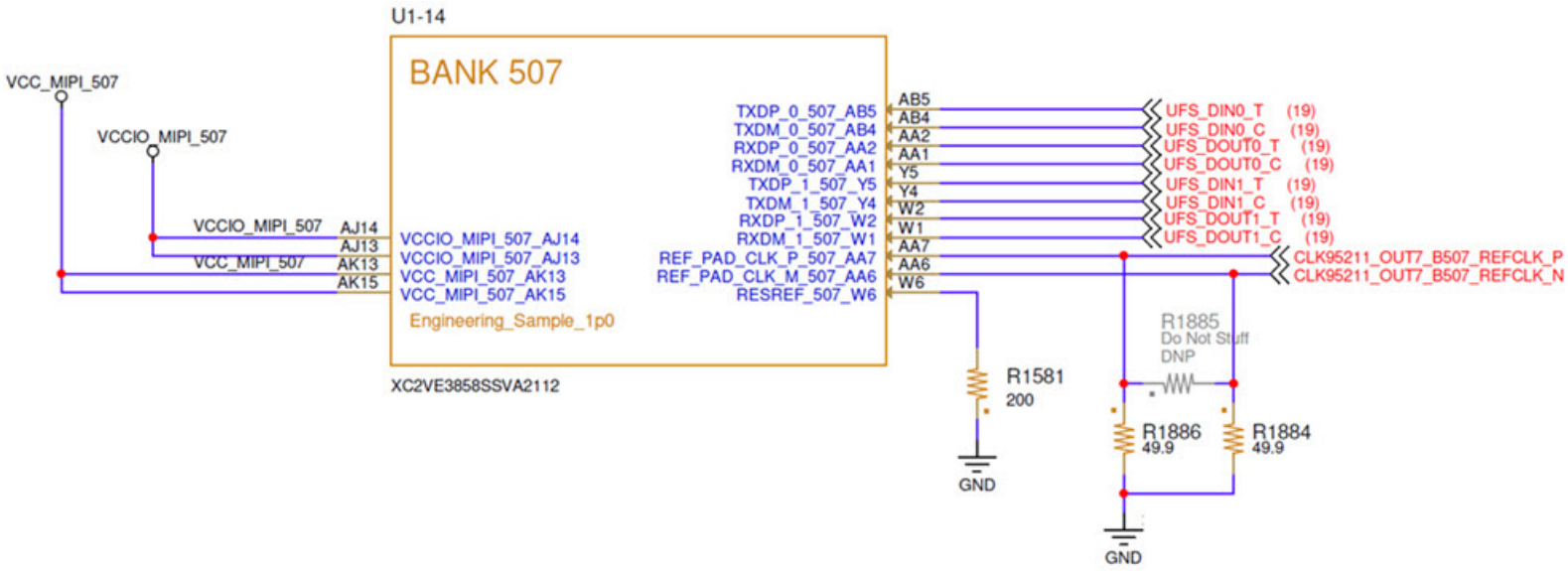
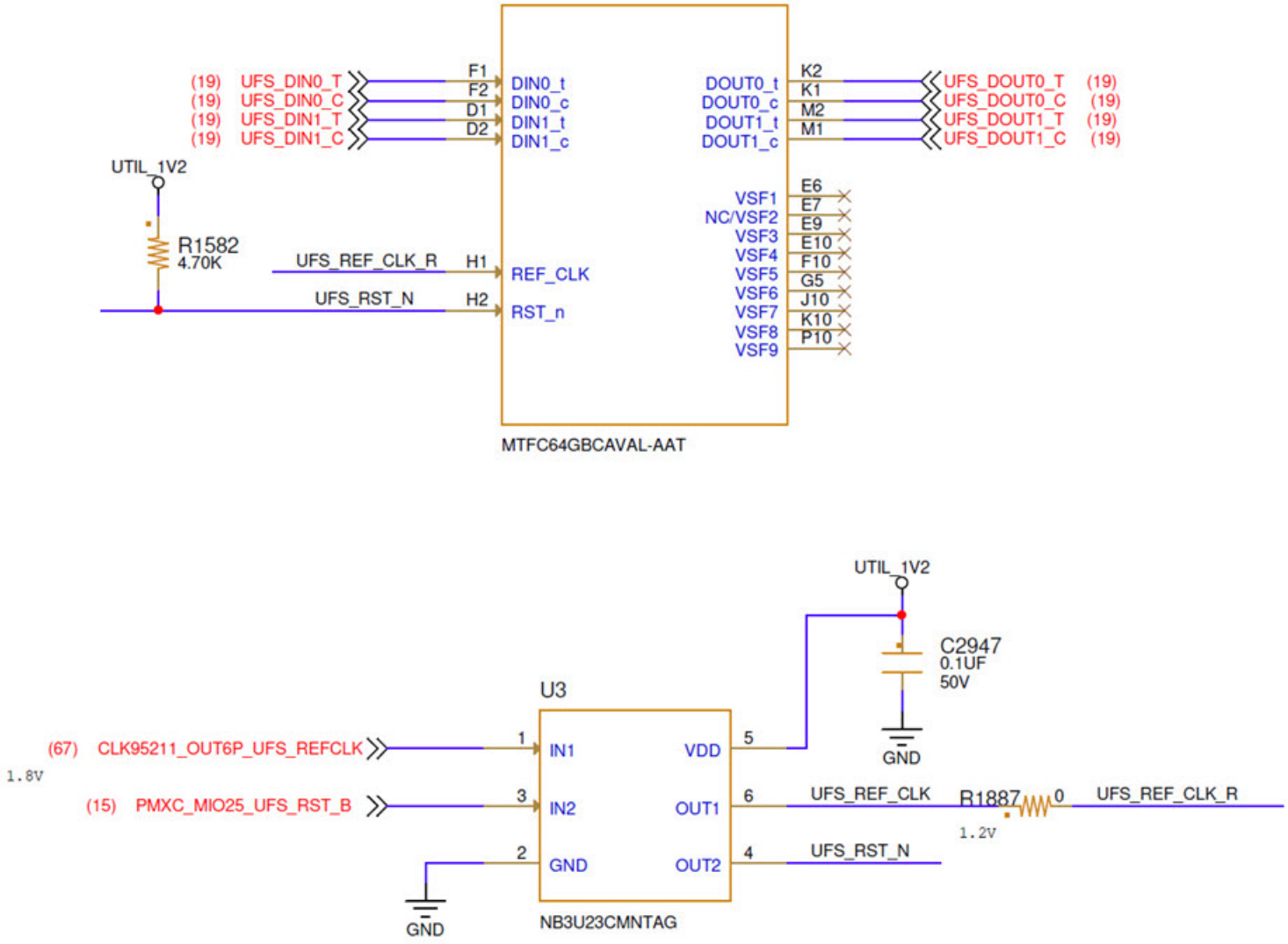


Figure 11: **UFS Memory Interface Connectivity**



For more information, refer to the JEDEC Specification.

The VEK385 UFS configuration boot modes are documented in the *Versal AI Edge Series Gen 2 and Prime Series Gen 2 Technical Reference Manual* (AM026). See schematic page 15, 19, and 67 for more details.

For MTFC64GBCAVAL-AAT component details, see the data sheet on the Micron Technology, Inc. website.

The detailed Versal device connections for the feature described in this section are documented in the VEK385 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

PMXC_MIO[26] BaseCamp Image Recovery Button

The VEK385 includes many safeguards to allow easy recovery after many different types of corruption and mistakes made in the development process. One such method is SW14. This is the BaseCamp Image Recovery Button.

Pressing the recovery image button forces the DUT (Versal AI Edge Series Gen 2 device) to load the AMD Embedded Development Framework (EDF) recovery boot firmware image. This allows users to connect to the recovery console or web interface. Within these recovery options, new images can be loaded/programed. The recovery allows the boot.bin, boot.pdi, and U-Boot to be loaded on the OSPI via Ethernet or USB.

- For Information, refer to Common Specifications: Image Recovery Application
- For a tutorial, refer to Discovery and Evaluation AMD Versal Device Portfolio: Image Recovery Application

PMXC_MIO[27:39] USB 2.0 ULPI PHY / SDCARD Interface

The VEK385 evaluation board uses a Microchip Technology Inc. USB3320 USB 2.0 ULPI transceiver (U29) to support a stacked dual USB 2.0 type-A connector (J77). This is accomplished through connectivity with a Microchip Technology Inc. USB5744 4-Port USB SS/Hi-Speed Hub Controller. The USB3320 is a high-speed USB 2.0 PHY supporting the UTMI+ low pin interface (ULPI) interface standard. The ULPI standard defines the interface between the USB controller IP and the PHY device, which drives the physical USB signaling. Using the ULPI standard reduces the interface pin count between the USB controller IP and the PHY device.

The USB3320 is clocked by a 24 MHz crystal (X3). See the Microchip Technology Inc. USB3320 data sheet for clocking mode details. The interface to the USB3320 PHY is implemented through the IP in the 2VE3858 device processing system.

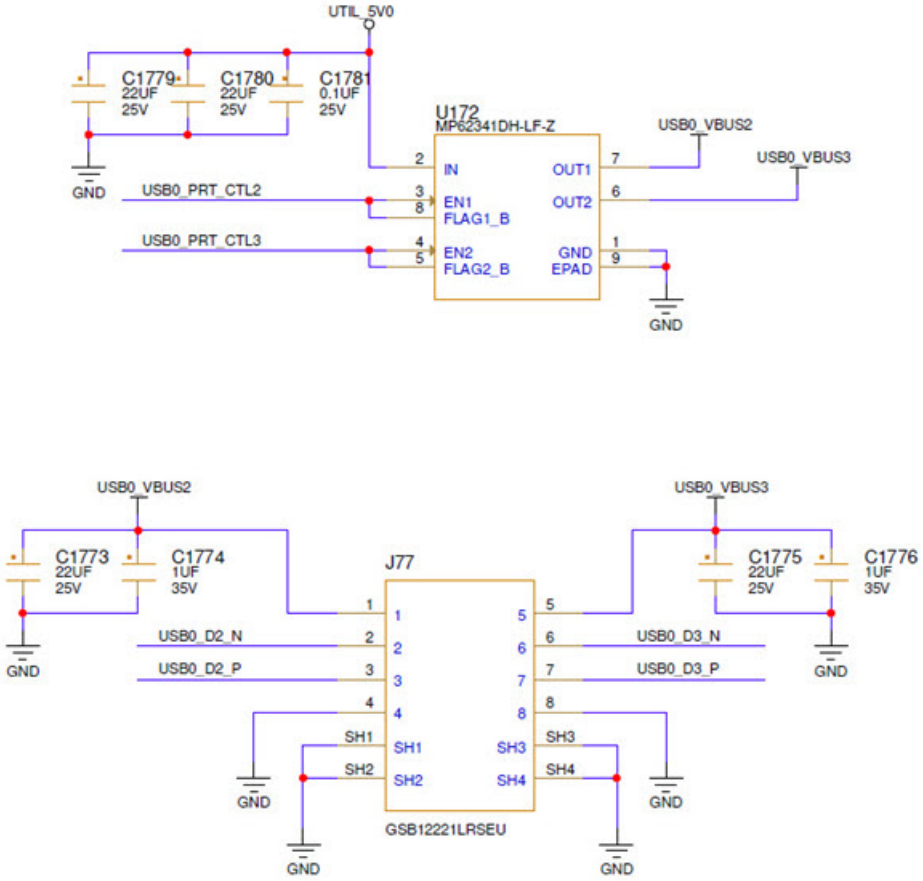
The USB5744 circuit has a Monolithic Power Systems, Inc (MPS) MP62341Dual-Channel 1A Current-Limited Power Distribution Switch (U172). This switch has separate enable inputs controlled by the USB5744 hub.

The USB5744 circuit has three connections. Port 1 has been wired to the onboard SD Card interface. Port 2 and 3 are wired to the previously mentioned dual stack USB 2.0 connector (J77).

***Note*:** The fourth port of the USB5744 USB hub is tied off using 10.0K pull ups and not available for use.

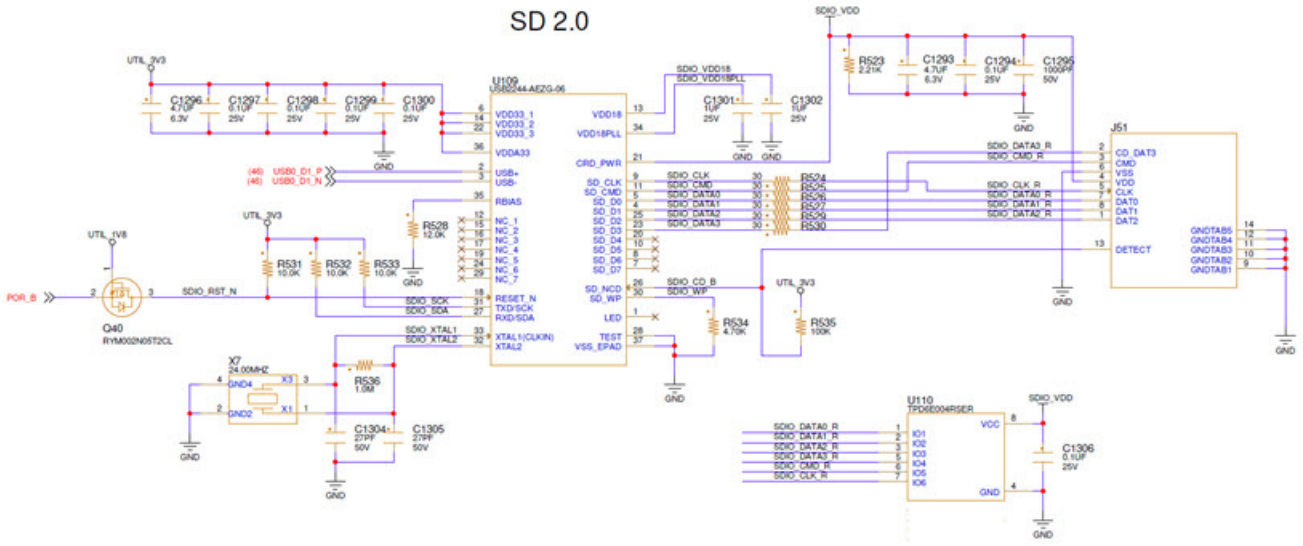
Refer to schematic pages 15, 45-47 for further details.

Figure 12: **USB5744 USB2.0 Power and Connector Interface**



The VEK385 utilizes port 1 on the USB5744 to interface with a Microchip Technology Inc. USB2244 USB 2.0 Multi-Format, SD/MMC, and Flash Media Controller (U109). This is in turn wired to a microSD memory card push type connector (J51). This circuit and connector allows the 2VE3858 to interface to easily accessible mass storage through the processing system and advanced Linux architecture.

Figure 13: **SD 2.0 USB Circuit and Memory Card Connector**



PMXC_MIO[40] Reserved

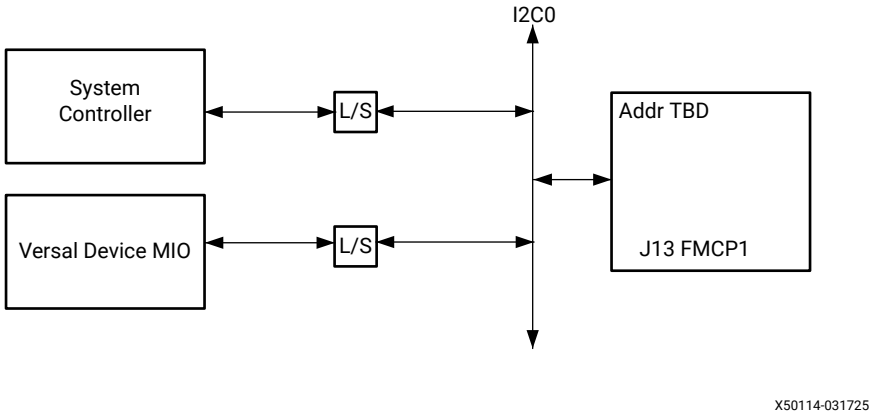
The Versal AI Edge Series Gen 2 device PS bank 501 PMXC_MIO40 is system controller factory reserved pin.

PMXC_MIO[42:43] I2C0 Bus

Bus I2C0 connects the 2VE3858 U1 PS bank 501 and the K24 system controller PS bank to the FMC+ connector for control over FMCP expansion boards.

The following figure shows the I2C0 bus connectivity. The I2C0 bus connects the K24 system controller and the 2VE3858 Bank 501 to the FMC+ connector. This allows flexibility to interface with any accessories added to the evaluation platform.

Figure 14: **I2C0 Bus Topology**



PMXC_MIO[44:45] I2C1 Bus

Bus I2C1 connects the 2VE3858 U1 PS bank 501 and the Kria K24 SOM system controller PS bank to two GPIO port expanders and two I2C switches. The two GPIO port expanders are TCAL6416 U37, U266. The two I2C switches are PCA9848 U162, U253.

These devices enable interfacing with various SFP, QSFP, FMCP connector, PCIe, USB, and power system status inputs and outputs.

To further create a compatible multi-master circuit, the VEK385 has a PCA9541 (U161) I2C switch in circuit. This switch is an arbiter and can be leveraged to eliminate congestion and interference as each I2C Master interacts with the I2C bus.

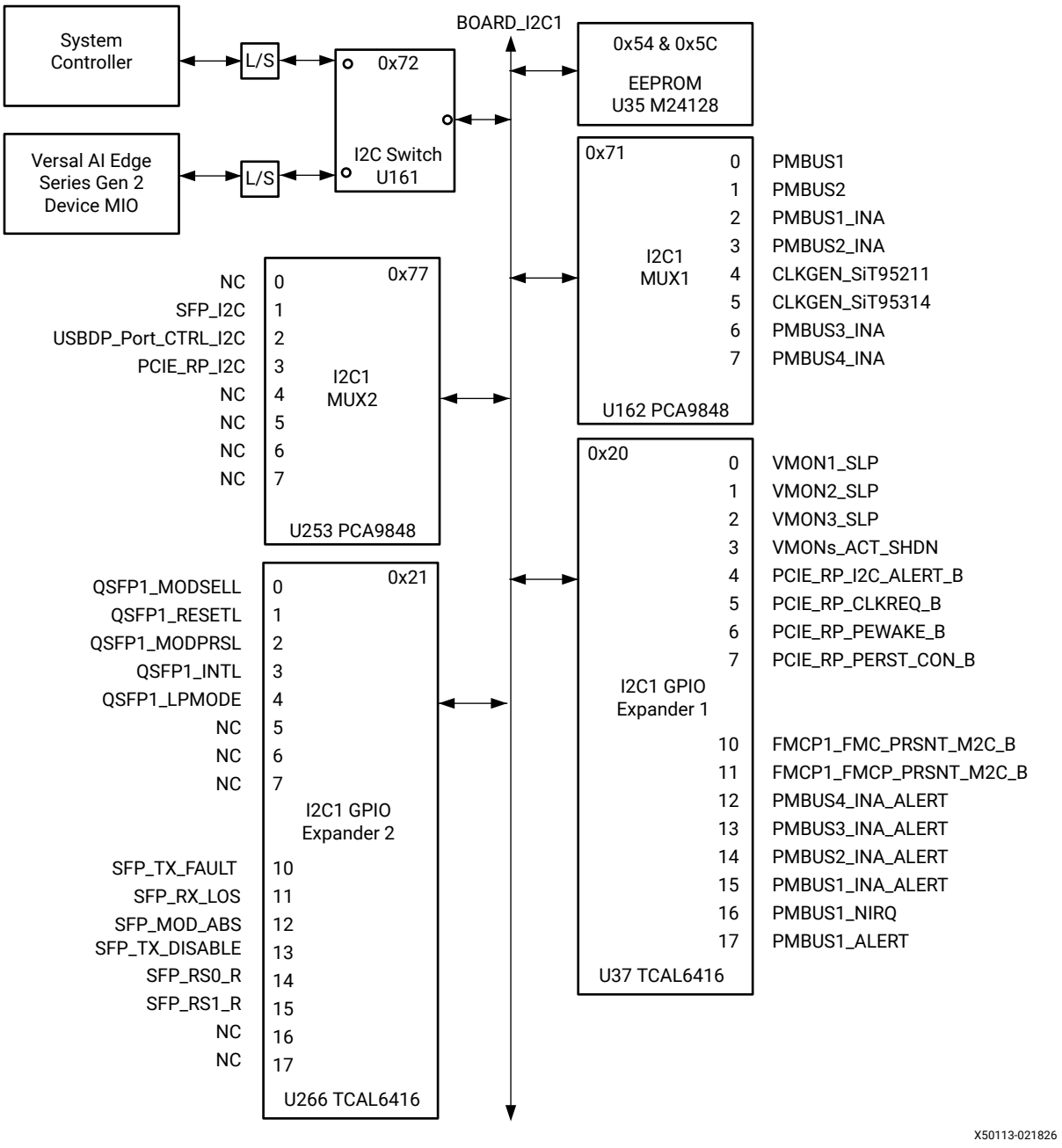
The expanders, multiplexors, and arbiter switch are pin strapped to the addresses specified in the following table.

Table 9: **I2C1 Interface Addresses**

Ref Des	I2C Address
U161	0x72
U37	0x20
U266	0x21
U162	0x71
U253	0x77

The following figure shows the I2C1 bus connectivity detailed in the following table.

Figure 15: **I2C1 Bus Topology**



U35 is an I2C addressable 128-Kbit serial I2C bus EEPROM. It has two addresses associated with it. Address `0x54` is used when the memory array is accessed. When using `0x5C`, the identification page is accessed.

The devices on each bus of the I2C1 U162 and U253 PCA9848 switches are listed in the following tables.

Refer to the VEK385 schematic pages 15, 62-64 for further details.

Table 10: **I2C1 Multiplexer 1 PCA9848 U162 Address 0x71 Connections**

I2C Devices	I2C Switch Pos.	I2C Address	Devices
PMBUS1	0	See schematic/Board Power Table	
PMBUS2	1	See schematic/Board Power Table	
PMBUS1_INA	2	See schematic/Board Power Table	
PMBUS2_INA	3	See schematic/Board Power Table	
CLKGEN_SiT95211	4	0x57, 0x5F	U166
		0x69	U101
CLKGEN_SiT95314	5	0x57, 0x5F	U165
		0x69	U164
PMBUS3_INA	6	See schematic/Board Power Table	
PMBUS4_INA	7	See schematic/Board Power Table	

Table 11: **I2C1 Multiplexer 2 PCA9848 U253 Address 0x77 Connections**

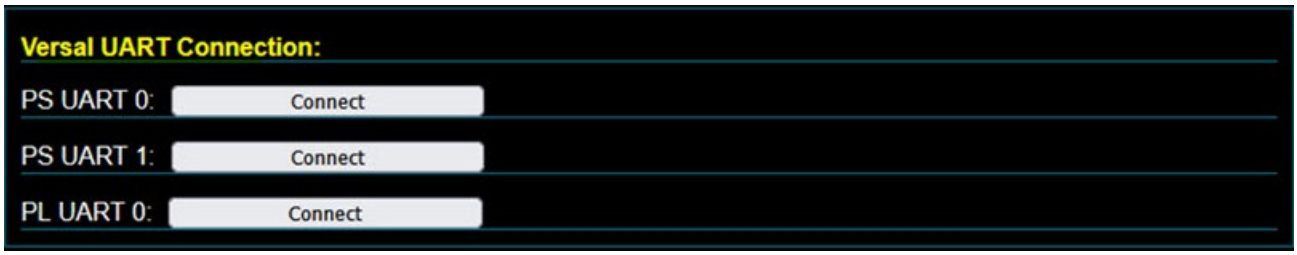
I2C Devices	I2C Switch Pos.	I2C Address	Devices
No connect	0	N/A	
SFP_I2C	1	0x##	
USBDP_PORT_CTRL_I2C	2	Refer to the schematic/PMXC_MIO[48] I3C (I3CI2C Bus)	
PCIE_RP_I2C	3	0x##	
No connect	4	N/A	
No connect	5	N/A	
No connect	6	N/A	
No connect	7	N/A	

Details for controlling the TCAL6416 port expanders is available in the data sheet on the Texas Instruments website. Details for controlling the PCA9848 switches is available in the data sheet on the NXP Semiconductors website. Details for controlling the M24128 EEPROM is available in the data sheet on the ST Microelectronics website.

UART Interfaces

The Versal AI Edge Series Gen 2 device includes circuitry for three UARTs. These are connected to the FTDI FT4232HL U18 USB-to-Quad-UART bridge. The VEK385 has added circuitry to allow easier remote control and interface. As part of this feature, a series of multiplexors allows the UARTs to be shunted to the system controller. This allows a SmartLynq or similar networked JTAG to be connected to the PC4 interface (J7), then remote serial connectivity can be achieved through BEAM. The remote interface is shown in the following figure and can be found under the Versal Device Control menu in BEAM. Refer to Versal Evaluation Board System Controller Wiki for more information.

Figure 16: **BEAM Versal UART Connections**



The FT4232HL U18 port assignments are listed in the following table. Details of the circuit can be found on schematic pages 60 and 61.

Table 12: **FT4232HL Port Assignments**

FT4232HL U34	Versal Device U1
Port ADBUS JTAG	VEK385 JTAG chain
Port BDBUS UART0	PS UART1 (PMXC_MIO[46-47])
Port CDBUS UART1	PS UART0 (PSXC_MIO[16-17])
Port DDBUS UART2	SYSCTRL_MIO[36:37] UART1

The FT4232HL UART interface connections are shown in the following figure.

Figure 17: **FT4232HL UART Connections**

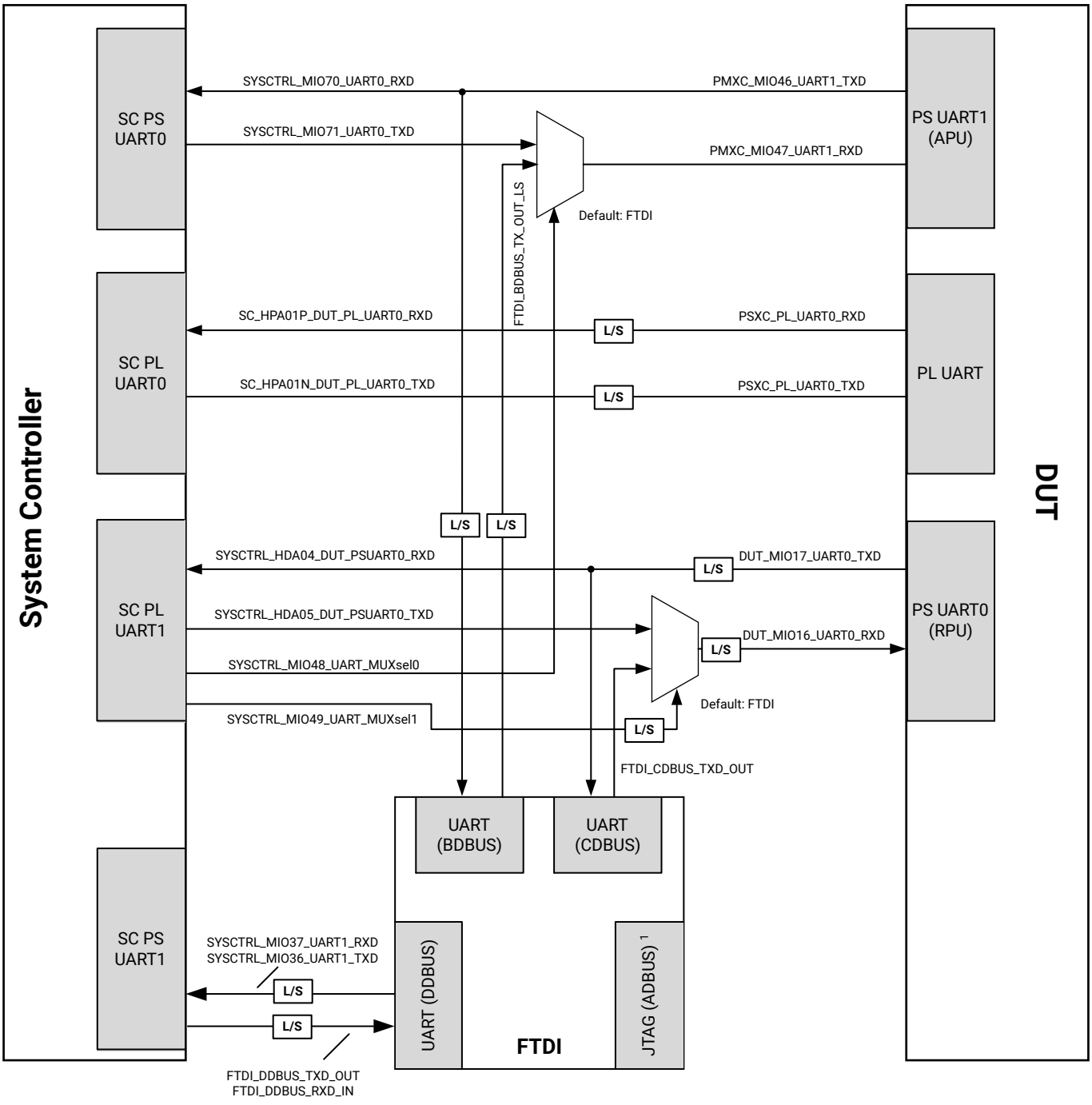


Figure Notes:
1. For details, see the JTAG Chain Block Diagram.

X50643-011526

For more information on the FT4232HL, see the Future Technology Devices International Ltd. website.

***Note*:** The FTDI configuration image can be programmed with the Vivado tools. See the Programming FTDI Devices for Vivado Hardware Manager Support section in the *Vivado Design Suite User Guide: Programming and Debugging* (UG908). Alternatively, a JTAG-SMT2 or similar from Digilent is recommended.

The detailed device connections for the feature described in this section are documented in the VEK385 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

PMXC_MIO[46:47] UART1

This is the primary Versal AI Edge Series Gen 2 device PS-side UART interface. This is used by U-Boot and Linux. MIO47 (RX_IN) and MIO46 (TX_OUT) are connected to FTDI FT4232HL U18 USB-to-Quad-UART bridge port BD through level-shifters. This can also be accessed remotely by use of BEAM UART Interfaces. Details of the circuit can be found on schematic pages 60 and 61.

The detailed device connections for the feature described in this section are documented in the VEK385 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

DUT_MIO[16:17] UART0

This is the secondary Versal AI Edge Series Gen 2 device PS-side UART interface. This is for use with auxiliary software (PLM, ASU, RPU). MIO16 (RX_IN) and MIO17 (TX_OUT) are connected to FTDI FT4232HL U18 USB-to-Quad-UART bridge port CD through level-shifters. This can also be accessed remotely by use of BEAM (see UART Interfaces). Details of the circuit can be found on schematic pages 60 and 61.

***Note*:** The VEK385 UART0 can only be accessed through remote means using BEAM when a powered USB-C cable is connected to the FTDI/JTAG/UART connector J26.

System Controller UART1

This is the primary System Controller UART interface. This is used as the primary method BEAM uses to output U-Boot and Linux messages. This is also used with technical support for low level system interactions and troubleshooting. It is recommended to only use this for read-only debug and troubleshooting unless directed otherwise with technical support. Incorrect configurations or unauthorized changes to BEAM and the associated firmware, software, and configurations might cause damage to your evaluation platform. SYSCTRL_MIO37_UART1_RXD (K24 MIO37) and SYSCTRL_MIO36_UART1_TXD (K24 MIO36) are the signals of interest for this circuit. Details of the circuit can be found on schematic pages 60, 61, and 70.

PSXC_PL_UART0

This is the primary Versal AI Edge Series Gen 2 device PL-side UART interface. This is used by solution specific needs for PL UART interfacing. If more PL UART ports are necessary, a PMOD has been provided for use case specific expansion for solution development. PSXC_PL_UART0_RXD (RX_IN) and PSXC_PL_UART0_TXD (TX_OUT) are connected to the System Controller through level-shifters. This can also be accessed remotely by use of BEAM (see UART Interfaces). Details of the circuit can be found on schematic pages 60 and 61.

PMXC_MIO[48] I3C (I3CI2C Bus)

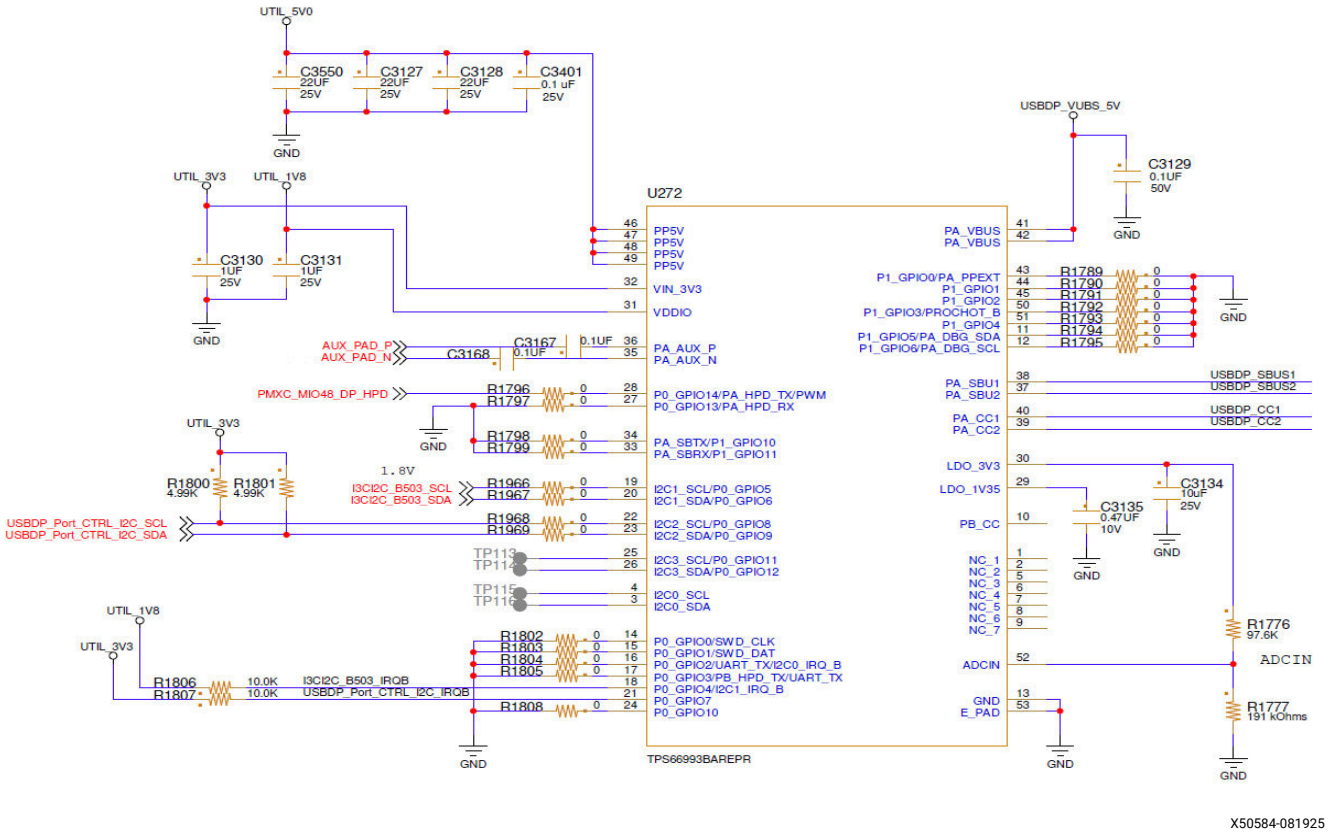
Bus I3CI2C connects the 2VE3858 U1 PS bank 503 to the USB3.2 Type-C connector (J56) through a Texas Instruments TPS66993 USB Type-C and USB PD Dual-Role Port (DRP) Controller with Integrated Source Power Switch (U272). The datasheet for this component is available from TI.

The TPS66993 has four ports of connectivity. Ports 1, 3, and 4 are controller/target type. Port 2 is target only. Of the four available I2C ports, the VEK385 is designed to provide I3CI2C pin mapping to the TPS66993 I2C Port 1 and I2C MUX connectivity to TPS66993 I2C Port 2.

The 2VE3858 connects to the TPS66993 through two busses. To access Port 1, the VEK385 provides direct access through the I3CI2C bus. Signal I3CI2C_B503 is connected in the schematic between these devices, reference pages 17 and 35 of the schematic. To access Port 2, signal USBDP_Port_CTRL_I2C is connected between an I2C multiplexor and the TPS66993. The 2VE3858 connects to the I2C multiplexor. Refer to PMXC_MIO[44:45] I2C1 Bus for details on connectivity and control options for this signal.

Header J165 is also provided on the VEK385 to allow direct programming access of the TPS66993.

Figure 18: **I3C**



X50584-081925

During power up, programming, and post configuration loading, the TPS66993 can have varied addresses on the various ports. Refer to the following table for details regarding accessible addresses.

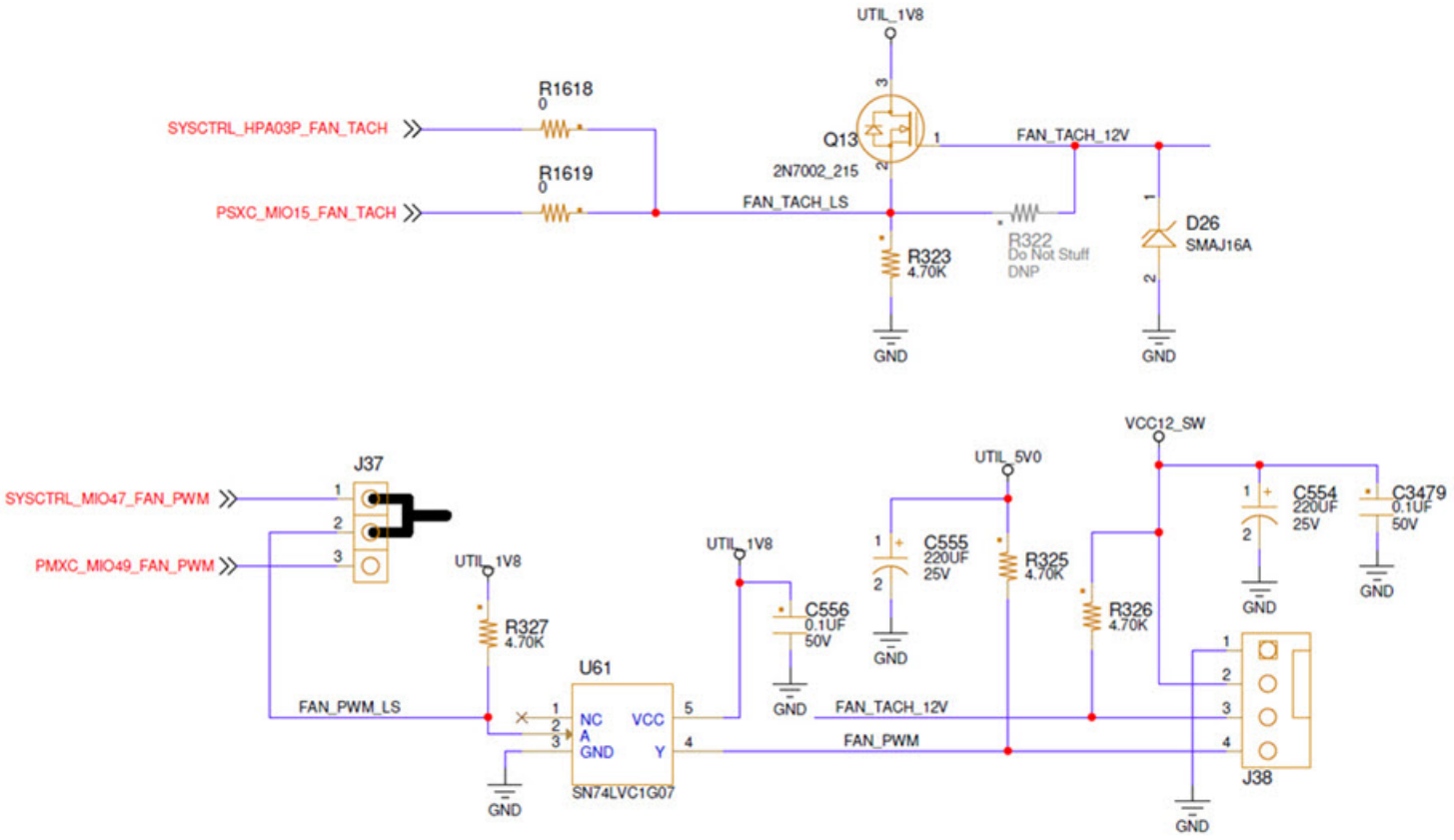
Table 13: **I3CI2C Interface Addresses**

I2C Port	Update/Programming	Post Config Load
1	0x22	0x22
2	0x12	0x52
1	0x22	0x22
2	0x52	0x52

PMXC_MIO[49] and PSXC_MIO[15] Fan Control

The Versal AI Edge Series Gen 2 device bank 501 PMXC_MIO49_FAN_PWM is connected to J37 pin 3. When J37 is selected as 2-3 (see Jumpers for defaults), the Versal AI Edge Series Gen 2 device is able to control the fan PWM speed. A controller application must be created to drive this logic. The Versal device bank 502 PSXC_MIO15_FAN_TACH is connected to a 2N7002 MOSFET (Q13). In turn, Q13 is connected to the 12V fan tachometer feedback. The 2N7002 is a N-Channel 60 V MOSFET. For more details, see Cooling Fan Connector. Refer to schematic pages 16, 76 for more information.

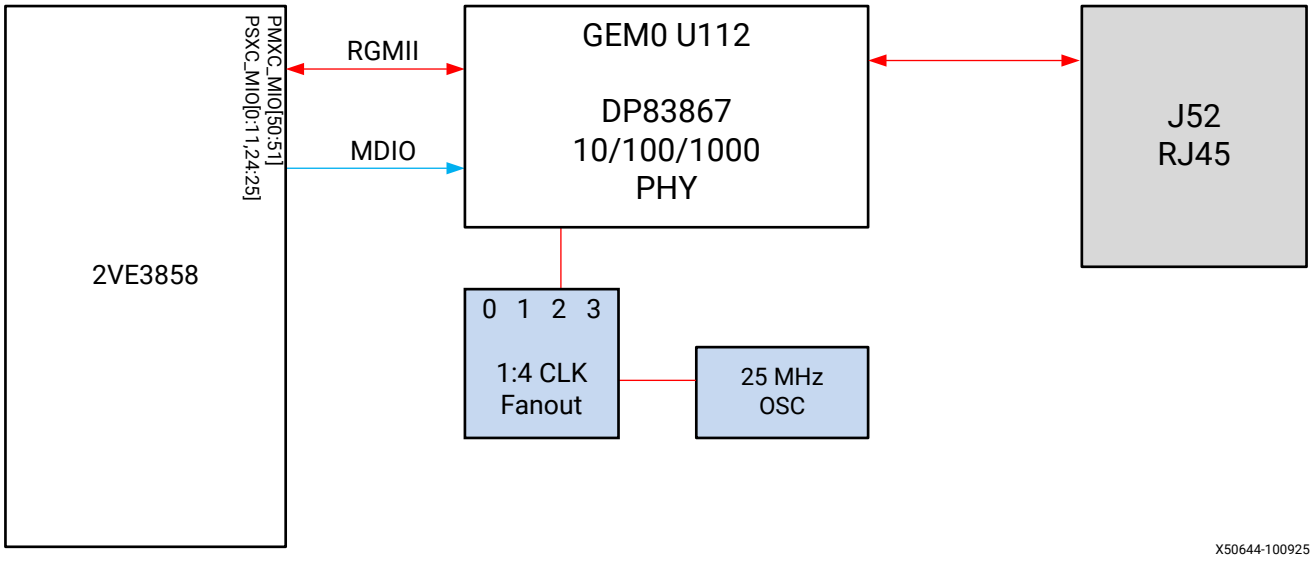
Figure 19: **USB PD Dual-Role Port (DRP) Controller**



PMXC_MIO[50:51] and PSXC_MIO[0:11,24:25] PS GEM0 Ethernet

A PS Gigabit Ethernet MAC (GEM) implements a 10/100/1000 Mb/s Ethernet interface. In the following figure, Versal AI Edge Series Gen 2 (U1) is connected to TI DP83867 U112 Ethernet RGMII PHY before being routed to an RJ45 Ethernet connector J52. The RGMII Ethernet PHY is boot strapped to PHY address (`0x01`) and Auto Negotiation is set to Enable.

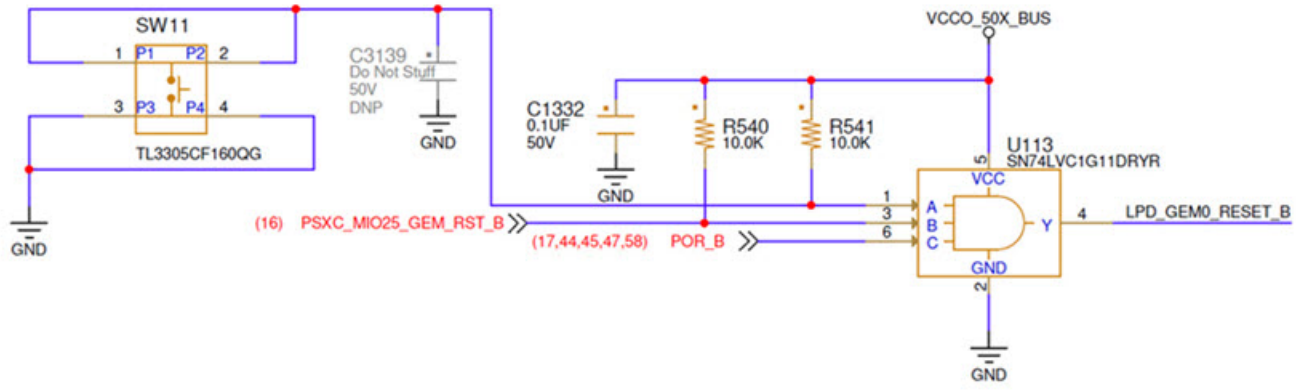
Figure 20: **PS Ethernet**



PS GEM0 Ethernet PHY Reset Circuit

The DP83867 PHY (GEM0 U112) is reset by its LPD_GEM0_RESET_B generated by the dedicated push button switch (SW11) and PSXC_MIO signals as shown in the following figure. The POR_B signal generated by the TPS389001DSER U9 POR device is wired in parallel to each Ethernet PHY reset circuit. The POR device is activated by push button SW2. See System Reset POR_B for more details.

Figure 21: **Ethernet PHY Reset Circuit**



PS GEM0 Ethernet PHY LED Interface

Each DP83867 PHY (GEM0 U112) controls two LEDs in the J52 connector bezel. The PHY signal LED0 drives the green LED, and LED1 drives the yellow LED. The LED2 signal is not used.

The LED functional description is listed in the following table.

Table 14: **Ethernet PHY LED Functional Description**

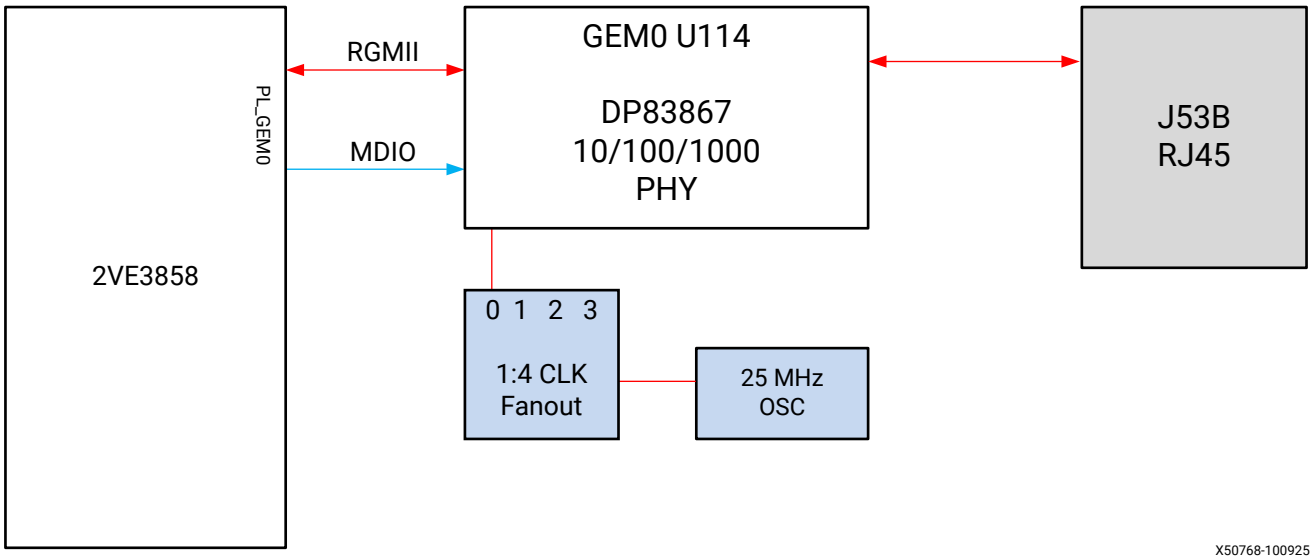
DP83867 PHY Pin		Type	Description
Name	Number		
LED_2	45	S, I/O, PD	By default, this pin indicates receive or transmit activity. Additional functionality is configurable using LEDCR1[11:8] register bits.
LED_1	46	S, I/O, PD	By default, this pin indicates that 1000Base-T link is established. Additional functionality is configurable using LEDCR1[7:4] register bits.
LED_0	47	S, I/O, PD	By default, this pin indicates that link is established. Additional functionality is configurable using LEDCR1[3:0] register bits.

The LED functions can be re-purposed with a LEDCR1 register write available via the PHY's management data interface, MDIO/MDC. See the TI DP83867 RGMII PHY data sheet at the Texas Instruments website for component details. The detailed *Versal AI Edge Series Gen 2 and Prime Series Gen 2 Technical Reference Manual* (AM026) connections for the feature described in this section are documented in the VEK385 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

PL GEM0 Ethernet

The P_GEM0 Gigabit Ethernet MAC (GEM) implements a 10/100/1000 Mb/s Ethernet interface. In the following figure, Versal AI Edge Series Gen 2 (U1) is connected to TI DP83867 U114 Ethernet RGMII PHY before being routed to an RJ45 Ethernet connector J53B. The RGMII Ethernet PHY is boot strapped to PHY address (`0x02`) and Auto Negotiation is set to Enable.

Figure 22: **RGMII Ethernet**



PL GEM0 Ethernet PHY LED Interface and Reset

The DP83867 PHY (GEM0 U114) controls two LEDs in the J53B two port connector bezel. The PHY signal LED0 drives the green LED, and LED1 drives the yellow LED. The LED2 signal is not used.

The DP83867 has the reset signal pulled up with a 10K resistor to help align the chip during power up of the evaluation board. This reset is controlled by a dedicated PL pin. Refer to the schematic page 12 and 51, signal PL_GEM0_RST_B.

The LED functional description is listed in the following table.

***Note*:** Unlike the PS GEM0 circuit, as the PL GEM circuit utilizes a dedicated PL pin to control the reset signal. This reset is not directly affected by POR_B. Thus, the DP83867 PHY will not be reset while the 2VE3858 is resetting. Solutions may need to account for this behavior.

Table 15: **Ethernet PHY LED Functional Description**

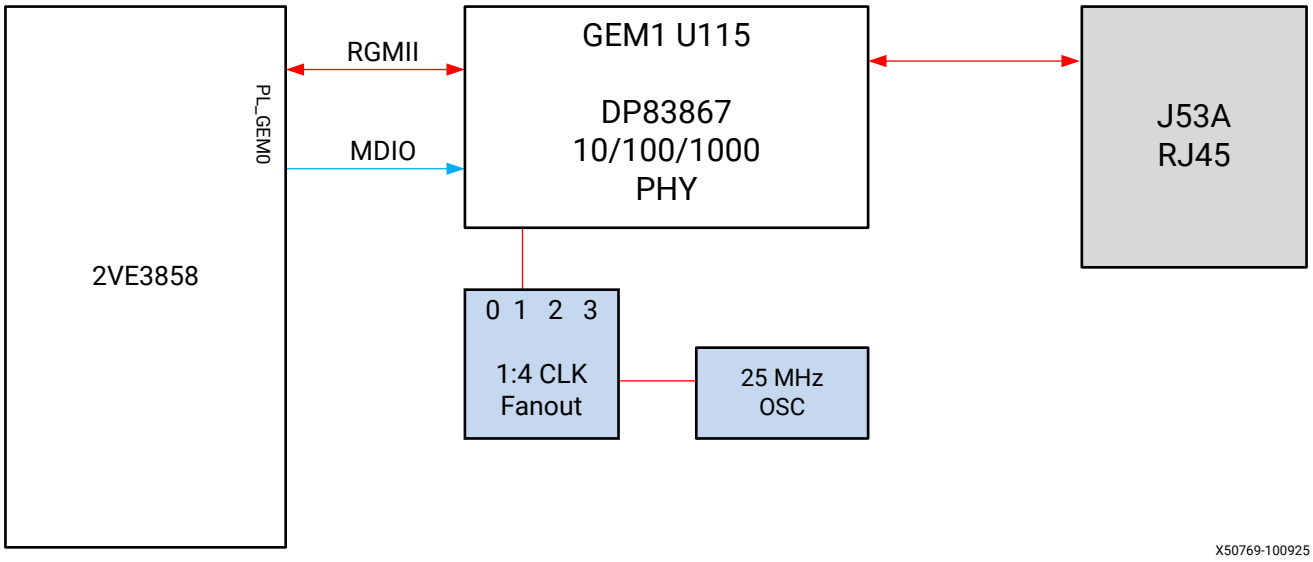
DP83867 PHY Pin		Type	Description
Name	Number		
LED_2	45	S, I/O, PD	By default, this pin indicates receive or transmit activity. Additional functionality is configurable using LEDCR1[11:8] register bits.
LED_1	46	S, I/O, PD	By default, this pin indicates that 1000Base-T link is established. Additional functionality is configurable using LEDCR1[7:4] register bits.
LED_0	47	S, I/O, PD	By default, this pin indicates that link is established. Additional functionality is configurable using LEDCR1[3:0] register bits.

The LED functions can be re-purposed with a LEDCR1 register write available via the PHY's management data interface, MDIO/MDC. See the TI DP83867 RGMII PHY data sheet at the Texas Instruments website for component details. The detailed *Versal AI Edge Series Gen 2 and Prime Series Gen 2 Technical Reference Manual* (AM026) connections for the feature described in this section are documented in the VEK385 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

PL GEM1 Ethernet

The P_GEM1 Gigabit Ethernet MAC (GEM) implements a 10/100/1000 Mb/s Ethernet interface. In the following figure, Versal AI Edge Series Gen2 (U1) is connected to TI DP83867 U115 Ethernet RGMII PHY before being routed to an RJ45 Ethernet connector J53A. The RGMII Ethernet PHY is boot strapped to PHY address (`0x03`) and Auto Negotiation is set to Enable.

Figure 23: **RGMII Ethernet**



PL GEM1 Ethernet PHY LED Interface and Reset

The DP83867 PHY (GEM0 U115) controls two LEDs in the J53A two port connector bezel. The PHY signal LED0 drives the green LED, and LED1 drives the yellow LED. The LED2 signal is not used.

The DP83867 has the reset signal pulled up with a 10K resistor to help align the chip during power up of the evaluation board. This reset is controlled by a dedicated PL pin. Refer to schematic pages 12 and 52, signal PL_GEM1_RST_B

The LED functional description is listed in the following table.

Note: Unlike the PS GEM0 circuit, as the PL GEM circuit utilizes a dedicated PL pin to control the reset signal. This reset is not directly affected by POR_B. Thus, the DP83867 PHY will not be reset while the 2VE3858 is resetting. Solutions may need to account for this behavior.

Table 16: **Ethernet PHY LED Functional Description**

DP83867 PHY Pin		Type	Description
Name	Number		
LED_2	45	S, I/O, PD	By default, this pin indicates receive or transmit activity. Additional functionality is configurable using LEDCR1[11:8] register bits.
LED_1	46	S, I/O, PD	By default, this pin indicates that 1000Base-T link is established. Additional functionality is configurable using LEDCR1[7:4] register bits.
LED_0	47	S, I/O, PD	By default, this pin indicates that link is established. Additional functionality is configurable using LEDCR1[3:0] register bits.

The LED functions can be re-purposed with a LEDCR1 register write available via the PHY's management data interface, MDIO/MDC. See the TI DP83867 RGMII PHY data sheet at the Texas Instruments website for component details. The detailed *Versal AI Edge Series Gen 2 and Prime Series Gen 2 Technical Reference Manual* (AM026) connections for the feature described in this section are documented in the VEK385 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

PSXC_MIO[18:20] System Monitor I2C

The Versal AI Edge Series Gen 2 device PS bank 502 SC_HPA07N_DUT_MIO18_SMON_SCL, SC_HPA06P_DUT_MIO19_SMON_SDA, and SC_HPA06N_DUT_MIO20_SMON_ALERT are connected to the system controller for use with system controller related applications and alerts. One example of this is leveraging the System Monitor's temperature reporting. This allows the system controller to vary the speed of the cooling solution to provide optimal cooling for the evaluation platform.

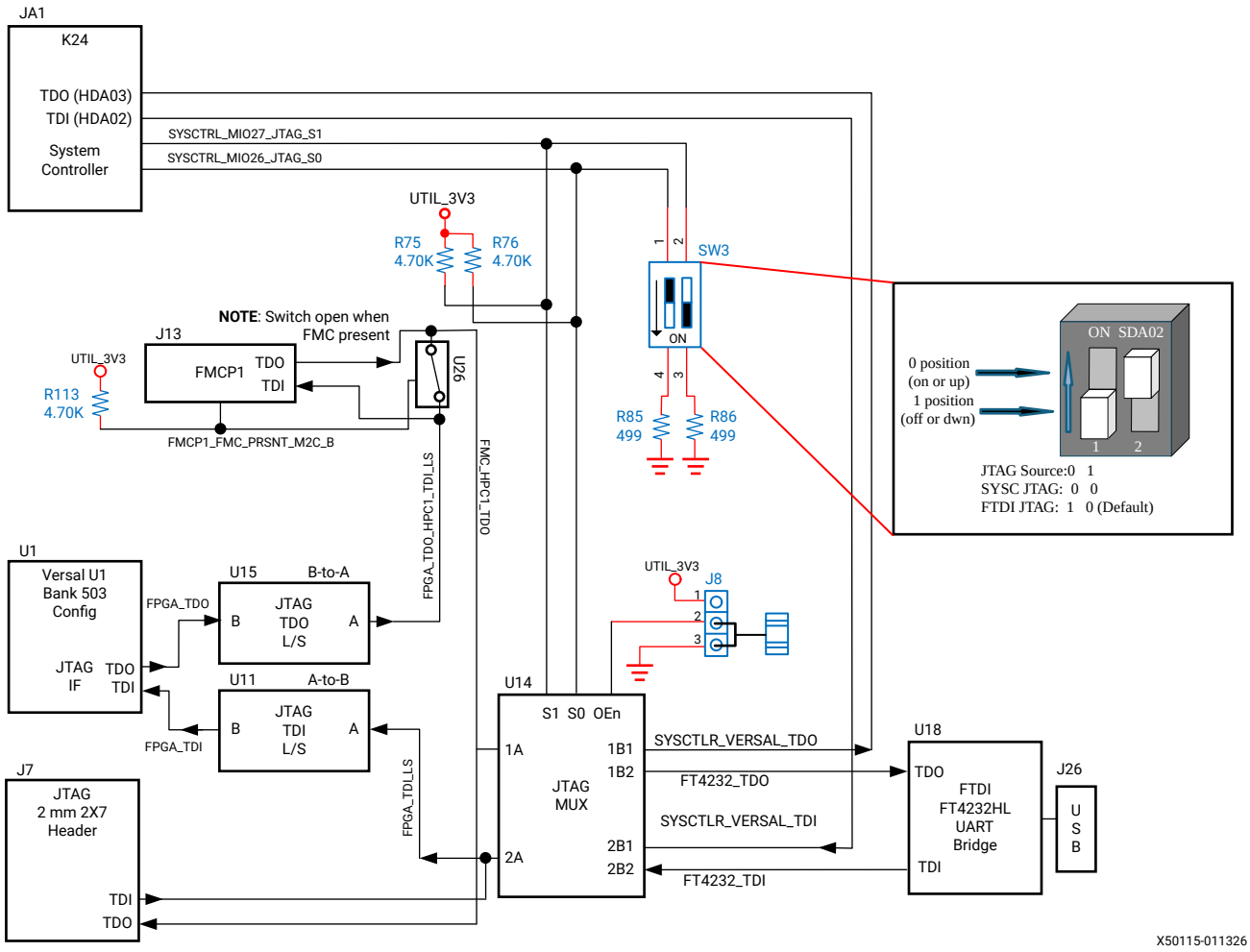
Note: When configuring the System Monitor I2C within the processing system configuration, BEAM expects the address to be set to `0x18`, and the above listed pins need to be selected to ensure design compatibility with the VEK385's layout.

JTAG Chain

The JTAG chain includes:

- J7 2x7 2 mm shrouded, keyed JTAG pod flat cable connector
- J26 USB3 type-C connector connected to U18 FT4232HL USB-JTAG bridge
- JA K24 System Controller HDA[02:03]

Figure 24: **JTAG Chain Block Diagram**



See Versal Device Configuration for information on JTAG programming via:

- FTDI FT4232 USB-to-JTAG/USB-UART device (U18) connected to USB 3.1 type-C connector (J26)
- JTAG pod flat cable connector J7 (2 mm 2x7 shrouded/keyed)

See the "FT4232HL UART Connections" figure in UART Interfaces for an overview of FT4232 U18 JTAG and USB-UART connectivity.

Clock Generation

The VEK385 board provides fixed and variable clock sources for the 2VE3858 U1 device and other function blocks. The following table lists the source devices for each clock.

Table 17: **Clock Sources**

Ref. Des.	Description	Signal	Frequency
U101	LPDDR5, LVDS	CLK95211_OUT0_SYSCLK2	320 MHz
U101	LPDDR5, LVDS	CLK95211_OUT1_SYSCLK1	320 MHz
U101	LPDDR5, LVDS	CLK95211_OUT2_SYSCLK0	320 MHz
U101	UFS Config, LVCMOS 1.8V	CLK95211_OUT4P_UFS_CFG_CLK	26 MHz
U101	PS Eth, LVCMOS 1.8V	CLK95211_OUT5P_TSU_CLK	250 MHz
U101	UFS Ref, LVCMOS 1.8V	CLK95211_OUT6P_UFS_REFCLK	26 MHz
U101	UFS, HCSL	CLK95211_OUT7_B507_REFCLK	26 MHz
U101	QSFP28, LVDS	CLK95211_OUT9_B206_REFCLK0	322.265 MHz
U101	HSDP / 10 GbE, LVDS	CLK95211_OUT10_B105_REFCLK1	156.25 MHz
U101	Spare, LVDS	CLK95211_OUT11	N/A
U164	PCIe RP, LVDS	CLK95314_OUT0_PCIE_RP_CLK	100 MHz
U164	PS Ref, LVCMOS 1.8V	CLK95314_OUT1_PS_REFCLK	33.333 MHz
U164	QSFP28, LVDS	CLK95314_OUT2_B206_REFCLK1	400 MHz
U164	USB Ref, HCSL	CLK95314_OUT3_B504_REFCLK	24 MHz
U49	HDMI Rx, LVDS, Recovered	HDMI_8T49N241_OUT	61.25 – 297 MHz
U45	HDMI Rx, LVDS, Recovered	HDMI_RCLK_OUT	61.25 – 297 MHz
X1	RTC xtal	RTC_PAD	32.768 KHz

The detailed device connections for the feature described in this section are documented in the VEK385 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

Programmable Reference Clocks

The VEK385 evaluation board has two I2C programmable clock generators. One clock generator is an ultra low jitter, programmable frequency, 12 output, quad pll clock generator. The second clock generator is a quad PLL frequency translator, jitter cleaner, and network / port synchronizer. The outputs have been configured in various outputs, and cover the majority of VEK385 clocking needs. Refer to schematic pages 63, 67, and 68.

At power-up, the clock generators default to various application specific frequencies preloaded into a dedicated clock generator EEPROM. See Table 17 in the Clock Generation section for more details on default frequencies.

User applications or the system controller can change the output frequency through the I2C bus interface. Unless expressly setting a frequency at boot using "Set at Boot" BEAM, or reprogramming the EEPROM, power cycling the VEK385 evaluation board reverts these user clocks to the default frequencies listed previously. BEAM also contains a restore EEPROM capability for the clock EEPROMs.

Clock Generator #1: SiT95211 (U101)

- MEMS Clock Generator: SiT95211AI-B00116
- 0.5 Hz - 2.94912 GHz
- I2C address 0x69(See note)
- EEPROM U165 M24C64-DRDW8
- EEPROM Addresses: 0x57 and 0x5F(See note)
- Refer to schematic page 63, 67

Clock Generator #1: SiT95314AI

- Jitter Cleaner: SiT95314AI-B00116 (U164)
- 0.5 Hz – 2.94912 GHz
- I2C address 0x69(See note)
- EEPROM U165 M24C64-DRDW8
- EEPROM Addresses: 0x57 and 0x5F(See note)

Refer to schematic page 63, 68.

***Note*:** I2C addressing is performed through the use of an I2C MUX, isolating each component to their respective I2C addressing range.

Transceivers

The Versal AI Edge Series Gen 2 device has 24 PL GTYP transceivers. The following table contains the mapping to hardened features, quads, channel locations, as well as general features.

Table 18: **Transceiver Mapping**

		2VE3858							
HDMI 2.1	HDMI_[T/R]X3	CH3	GTYP Quad 207 X1Y2 CC [L]	PCIe X1Y3	MRMAC X0Y2	GTYP Quad 107 X0Y2 BC [RN] (RCAL)	CH3	PCIE_[T/R]X0	PCIe Gen5x4 or PCIe Gen4x8
	HDMI_[T/R]X2	CH2					CH2	PCIE_[T/R]X1	
	HDMI_[T/R]X1	CH1					CH1	PCIE_[T/R]X2	
	HDMI_[T/R]X0	CH0					CH0	PCIE_[T/R]X3	
	HDMI_8T49N241_OUT	REFCLK1					REFCLK1	[UNUSED]	
	HDMI_RCLK_OUT	REFCLK0					REFCLK0	PCIE_EP_CLK0	
QSFP28	QSFP1_[T/R]X3	CH3	GTYP Quad 206 X1Y1 CB [L]	MRMAC X1Y1	PCIe X0Y2	GTYP Quad 106 X0Y1 BB [RN]	CH3	PCIE_[T/R]X4	
	QSFP1_[T/R]X1	CH2					CH2	PCIE_[T/R]X5	
	QSFP1_[T/R]X2	CH1					CH1	PCIE_[T/R]X6	
	QSFP1_[T/R]X4	CH0					CH0	PCIE_[T/R]X7	
	CLK95314_OUT2[1]	REFCLK1					REFCLK1	[UNUSED]	
	CLK95211_OUT9[2]	REFCLK0					REFCLK0	PCIE_EP_CLK1	

Table 18: **Transceiver Mapping** *(cont'd)*

			2VE3858						
FMC+	FMCP1_DP3	CH3	GTYP Quad 205 X1Y0 CA [L] (RCAL)	PCIe X1Y1	MMI	GTYP Quad 105 X0Y0 BA [RS] (RCAL)	CH3	SFP28	10GbE
	FMCP1_DP2	CH2					CH2	Versal_HSDP_TX	HSDP
	FMCP1_DP1	CH1					CH1	PCIE_RP_PET[p/n1	PCIe RP
	FMCP1_DP0	CH0					CH0	PCIE_RP_PET[p/n]0	
	FMCP1_GBTCLK1_M2C	REFCLK1					REFCLK1	CLK95211_OUT10[3]	
	FMCP1_GBTCLK0_M2C	REFCLK0					REFCLK0	PCIE_RP_REFCLK0	
			ISP	MRMAC X1Y0	MMI	MMI			
			VCU	PCIe X0Y0					
				HDIO		UFS			
				HDIO	PMCDIO	LPDMIO			
			VDU	HDIO	PMCMIO	PMCMIO/PMCDIO			

Notes:

1. Schematic Signal Name: CLK95314_OUT2_B206_REFCLK1
2. Schematic Signal Name: CLK95211_OUT9_B206_REFCLK0
3. Schematic Signal Name: CLK95211_OUT10_B105_REFCLK1

GTYP Transceivers

The GTY/GTYP transceivers in the Versal AI Edge Series Gen 2 device architecture are power-efficient transceivers, supporting line rates from 1.25 Gb/s to 32.75 Gb/s. The GTY/GTYP transceivers are highly configurable and tightly integrated with the programmable logic resources of the Versal architecture. For more information, see the *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* (AM002).

GTYP105: MMI Interconnectivity

The multi media interconnect (MMI) allows various resources to be shared with the GTYP transceivers in QUAD105. Table 18 shows the configuration selected for the VEK385 evaluation board. For more information on the various application specific configurations for the MMI connectivity and configuration, refer to *Versal AI Edge Series Gen 2 and Prime Series Gen 2 Technical Reference Manual* (AM026).

GTYP106/107: PCI Express Card Edge Connectivity

For information about the PL PCIE5 hard block, which can be mapped to the PCIe Edge Fingers of the VEK385 to implement a PCIe Endpoint, consult sections of *Versal Adaptive SoC Integrated Block for PCI Express LogiCORE IP Product Guide* (PG343). For information about the corresponding soft DMA IP core solutions which works with PL PCIE5, consult sections of *Versal Adaptive SoC DMA and Bridge Subsystem for PCI Express Product Guide* (PG344).

See schematic pages 14, and 36 for more details on connectivity. See schematic page 69 for details on the clocking configuration.

GTYP205: FPGA Mezzanine Card Interface

The Versal device (U1) bank 205 GTYP transceivers are wired to the FMCP connector (J13). See schematic pages 13 and 53-56 for details. The detailed non-transceiver Versal device connections for the feature described in this section are documented in the VEK385 board XDC file, referenced in Appendix A: Xilinx Design Constraints.

VITA 57.4 FMC+ Connector Pinouts

FMC+ Connector Type

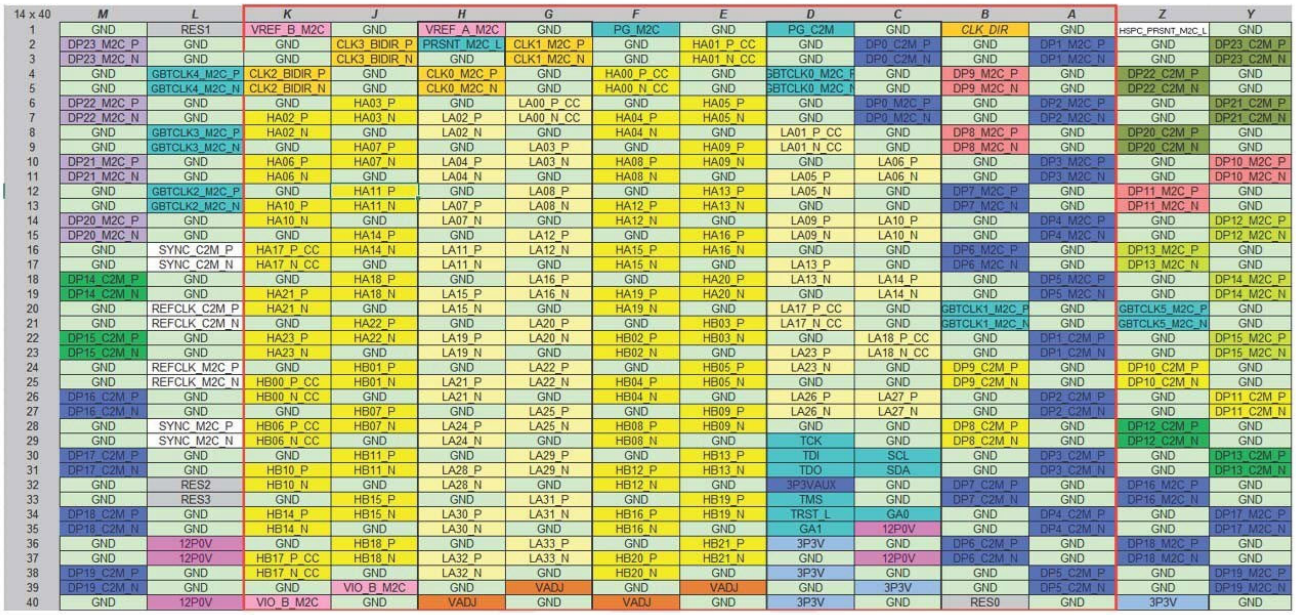
The Samtec SEAF series 1.27 mm (0.050 in) pitch mates with the SEAM series connector. For more information about the SEAF series connectors, see the Samtec, Inc. website. The 560-pin FMC+ connector defined by the FMC specification provides connectivity for up to:

- 160 single-ended or 80 differential user-defined signals
- 24 transceiver differential pairs
- 6 transceiver (GBTCLK) differential clocks
- 4 differential (CLK) clocks
- 1 differential (REFCLK) clock (both C2M and M2C pairs)
- 1 differential (SYNC) clock (both C2M and M2C pairs)
- 239 ground and 17 power connections

For board specific details, see Board Features.

The following figure shows the pinout of the FPGA plus mezzanine card (FMCP) high pin count (HSPC) connector defined by the VITA 57.4 FMC specification.

Figure 25: **FMCP HSPC Connector Pinout**



14 x 40	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	REFCLK_C2M_N	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	REFCLK_M2C_N	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	SYNC_M2C_P	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	SYNC_M2C_N	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	RES2	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	RES3	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

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For more information about the VITA 57.4 FMC+ specification, see the VITA FMC Marketing Alliance website.

GTYP206: QSFP28 Connectivity

The VEK385 has four transceivers, or one QUAD dedicated to the QSFP28 (J54) interface. While the GTYP transceivers can operate above this data rate, note that the components selected for these lanes limit performance to a maximum of 28 Gb/s. Refer to *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* (AM002) for more information on GTYP.

QSFP28 and zSFP+ Control Signals

The transceiver control signals can be asserted in multiple ways. The main control mechanism is through an I2C connection to the I2C1 bus through the I2C multiplexer (U253) as shown in the PMXC_MIO[44:45] I2C1 Bus section. The remaining control signals are connected to a GPIO expander (U266) also on the I2C1 bus as shown in the PMXC_MIO[44:45] I2C1 Bus.

The following table lists the transceiver module control signals.

Table 19: **Transceiver Module Control Signals**

Signal Name	Feature	Notes
QSFP1_I2C	Two-wire interface	U253 I2C MUX P2

Table 19: **Transceiver Module Control Signals** *(cont'd)*

Signal Name	Feature	Notes
QSFP1_MODSELL	Module select	U266 I2C GPIO expander P0
QSFP1_RESETL	Module reset	U266 I2C GPIO expander P1
QSFP1_MODPRSL	Module present	U266 I2C GPIO expander P2
QSFP1_INTL	Interrupt	U266 I2C GPIO expander P3
QSFP1_LPMODE	Low Power Mode	U266 I2C GPIO expander P4
SFP_I2C	Two-wire interface	U253 I2C MUX P1
SFP_TX_FAULT	Module to U1 - fault condition detected	U266 I2C GPIO expander P10
SFP_RX_LOS	Module to U1 - RX signal loss	U266 I2C GPIO expander P11
SFP_MOD_ABS	Logic High when module absent	U266 I2C GPIO expander P12
SFP_TX_DISABLE	U1 to module - transmitter disable	U266 I2C GPIO expander P13
SFP_RS0	Pulled up to UTIL_3V3	U266 I2C GPIO expander P14
SFP_RS1	Pulled up to UTIL_3V3	U266 I2C GPIO expander P15

HDMI

The VEK385 has one HDMI™ 2.1 source and one HDMI 2.1 sink. This is provided by HDMI 2.1 compatible redrivers and miscellaneous control signals. A separate high quality programmable clock has been provided for driving this entire circuit to allow flexibility and tuning.

GTYP207: HDMI Connectivity

The VEK385 has four transceivers, or one QUAD dedicated to the HDMI (J24, J25) interfaces. Refer to *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* (AM002) for more information on GTYP.

HDMI Video Input/Output

The TMDS1204 HDMI redrivers are used in both transmit and receive of HDMI 2.1 video. TMDS1204 redriver supports data rates up to 12 Gb/s. It is backwards compatible with HDMI 1.4b and HDMI 2.0b. The TMDS1204 can support both three and four lane HDMI 2.1 FRL at 3, 6, 8, 10, and 12-Gb/s.

The HDMI 2.1 circuitry includes a Renesas 8T49N241 frequency translator as a jitter attenuator. HDMI 2.1 RX subsystem outputs a differential recovered clock for jitter attenuation. The jitter-attenuated clock from 8T49N241 is routed back to reference clock 1 of Quad 207.

When HDMI TX and RX are independent and HDMI TX is in TMDS mode, 8T49N241 operates in free running mode and generates a reference clock for the HDMI TX subsystem. When the HDMI subsystem is in passthrough and TMDS mode, 8T49N241 generates a jitter-attenuated reference clock to drive the HDMI TX subsystem to phase-align with of the RX subsystem.

A 400MHz reference clock is needed by the HDMI TX/RX subsystem to run in FRL mode. When in passthrough, FRL mode, HDMI does not use 8T49N241.

More information on the TI TMDS1204 is available on the TI website.

The series capacitor-connected HDMI TX and RX data signals from TMDS1204 are routed to the 2VE3858 GTYP Bank 207.

HDMI Control I2C Bus

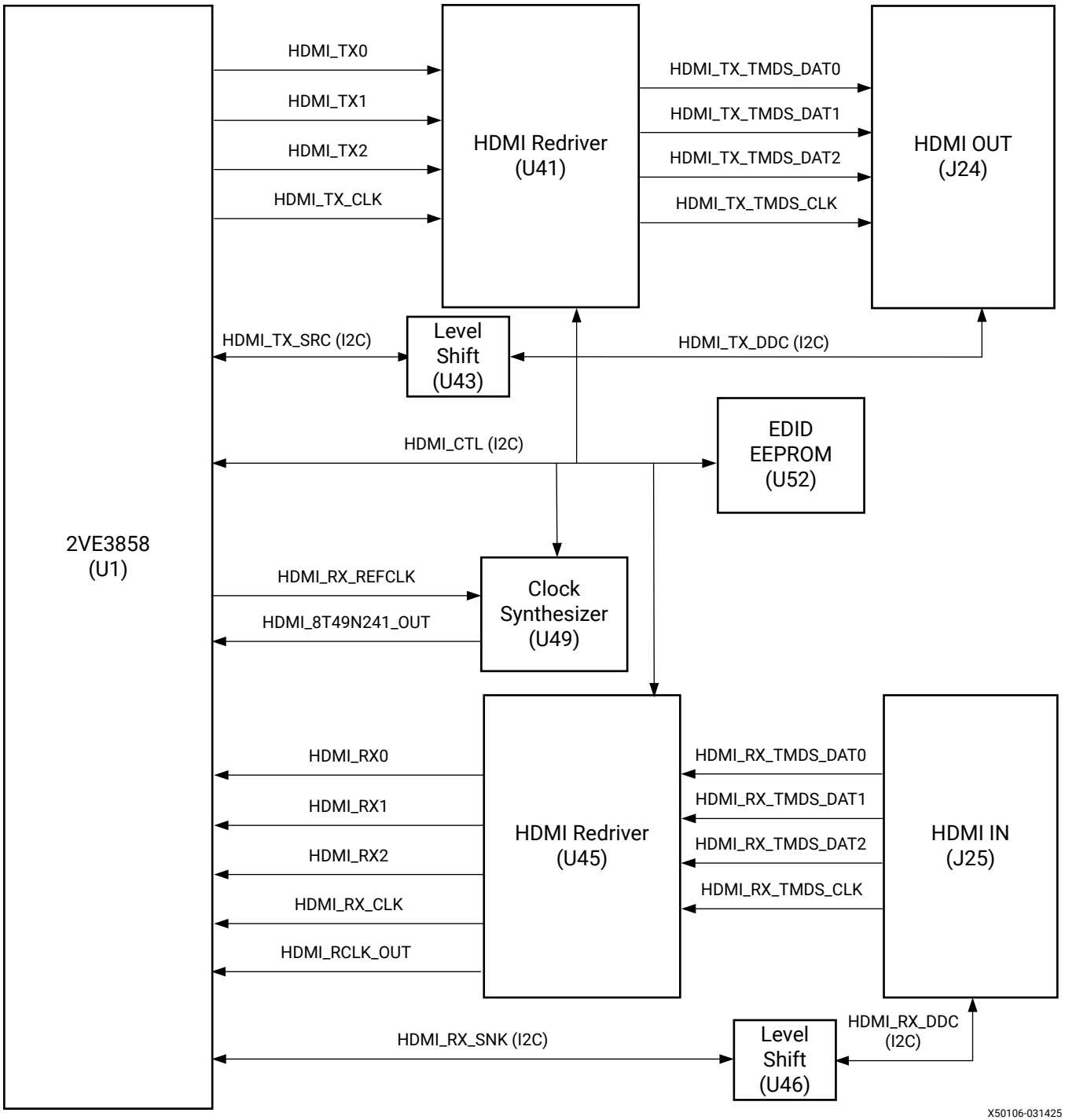
The HDMI_CTL I2C bus connects the 2VE3858 U1 bank 702 to two HDMI TDMS1204 redrivers (U41, U45), a M24128 128-Kbit EDID Serial EEPROM (U52), and a Renesas 8T49N241 FemtoClock NG Universal Frequency Translator (U49). See the VEK385 evaluation board schematic pages 8, 40, 41, and 42 for more information. The following table lists the control I2C bus devices and addresses.

Table 20: **HDMI Control I2C Bus**

Ref. Des.	I2C Devices	I2C Address
U41	TDMS1204 HDMI TX redriver	0x5E
U45	TDMS1204 HDMI RX redriver	0x5B
U49	8T49N241-994 FemtoClock	0x6C
U52	M24128 EEPROM	0x50

The HDMI video and control I/O block diagram is shown in the following figure.

Figure 26: **HDMI Video and Control I/O Block Diagram**



HDMI Clocking

HDMI Source Clock

The VEK385 evaluation board includes a SiTime SiT95314AI (U164). This chip is used to source the 400 MHz FRL/DRU clock (CLK95314_OUT2_B206_REFCLK1) used as the reference for driving the Versal device (U1) logic and related circuitry for HDMI.

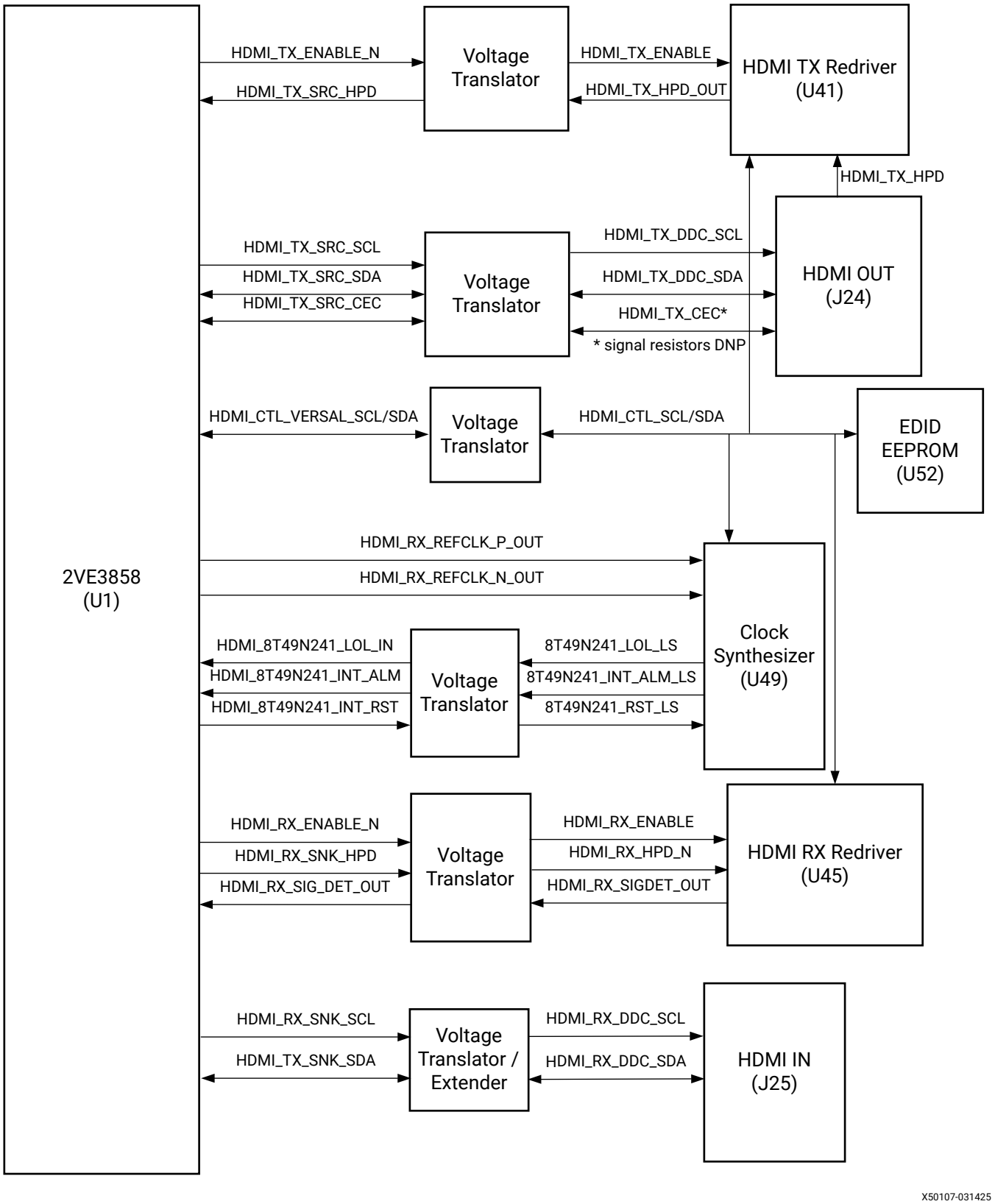
HDMI Clock Recovery

The HDMI circuitry includes a Renesas 8T49N241 (U49) frequency translator as a jitter attenuator. The jitter-attenuated clock (HDMI_8T49N241_OUT) is routed as a reference clock to GTYP Bank 207. The 8T49N241 (U49) is used to generate the reference clock for the HDMI transmitter subsystem. When the HDMI transmitter is used standalone mode (FRL/TMDS) or pass-through mode (FRL), the 8T49N241 clock synthesizer (U49) operates in free running mode and uses an external oscillator as the reference. When the HDMI operation is in pass-through mode (TDMS), the 8T49N241 generates a jitter-attenuated reference clock to drive the HDMI transmitter subsystem with a phase-aligned version of the HDMI RX subsystem TMDS clock. The 8T49N241 (U49) is controlled by the HDMI 2.1 IP via I2C bus, HDMI_I2C_CTL.

HDMI I/O Interface

The HDMI TX and RX I/O signals are assigned to 2VE3858 X5IO Bank 706. Some of these signals such as I2C buses, HDMI_TX_SRC, and HDMI_RX_SNK have voltage translation to 5V connected to the HDMI receptacle. The block diagram in the following figure shows the I/O signal connections for HDMI TX and RX. A 128-Kbit EEPROM is provided for storing HDMI EDID metadata in the circuitry.

Figure 27: **HDMI SRC and SNK Control I/O Block Diagram**



High-speed Debug Port

The PS includes an integrated Aurora 64B/66B block that is dedicated for accessing the debug packet controller (DPC) via a high-speed GT-based interface. This protocol to access the DPC is the high-speed debug port (HSDP) protocol. The HSDP provides bidirectional access to the device from an external host debug/trace module, allowing for high-speed debug and trace operations. The SmartLynq+ module can be connected to the Aurora interface to access the HSDP in Versal AI Edge Series Gen 2 devices. For more information, see the *SmartLynq+ Module User Guide* (UG1514). For information on the HSDP quad availability, see the *Versal AI Edge Series Gen 2 and Prime Series Gen 2 Technical Reference Manual* (AM026).

***Note*:** The VEK385 evaluation board has additional HSDP lanes provided for future system controller use.

***Note*:** The integrated HSDP Aurora interface is not available in all Versal AI Edge Series Gen 2 devices, which might support HSDP using a soft Aurora solution. This interface requires additional configuration in the Control, Interfaces, and Processing (CIPS) IP, a PL aurora implementation, and the use of additional gigabit transceivers.

User I/O

See Table 5 for default values.

The following table lists the net names, and reference designators for the user I/O. Refer to schematic page 65 for more information.

Table 21: **User I/O**

Net Name	Ref. Designator
GPIO_PB0	SW7
GPIO_PB1	SW6
GPIO_DIP_0	SW5
GPIO_DIP_1	SW5
GPIO_DIP_2	SW5
GPIO_DIP_3	SW5
GPIO_LED0	DS7
GPIO_LED1	DS6
GPIO_LED2	DS5
GPIO_LED3	DS4

Power and Status LEDs

The following figure shows the power and status LEDs.

Figure 28: **Power and Status LEDs**

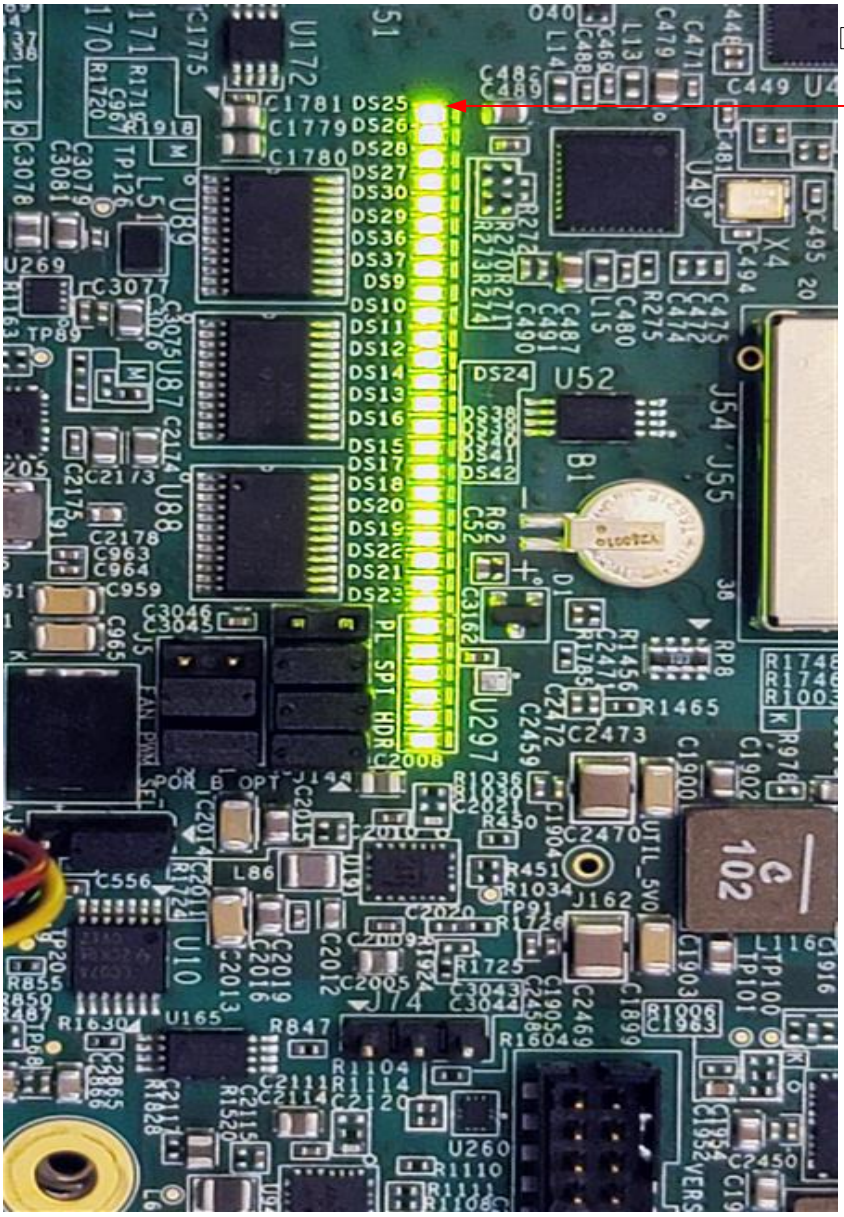


Figure 29: **AMD Kria™ K24 SOM Power Rail Good**

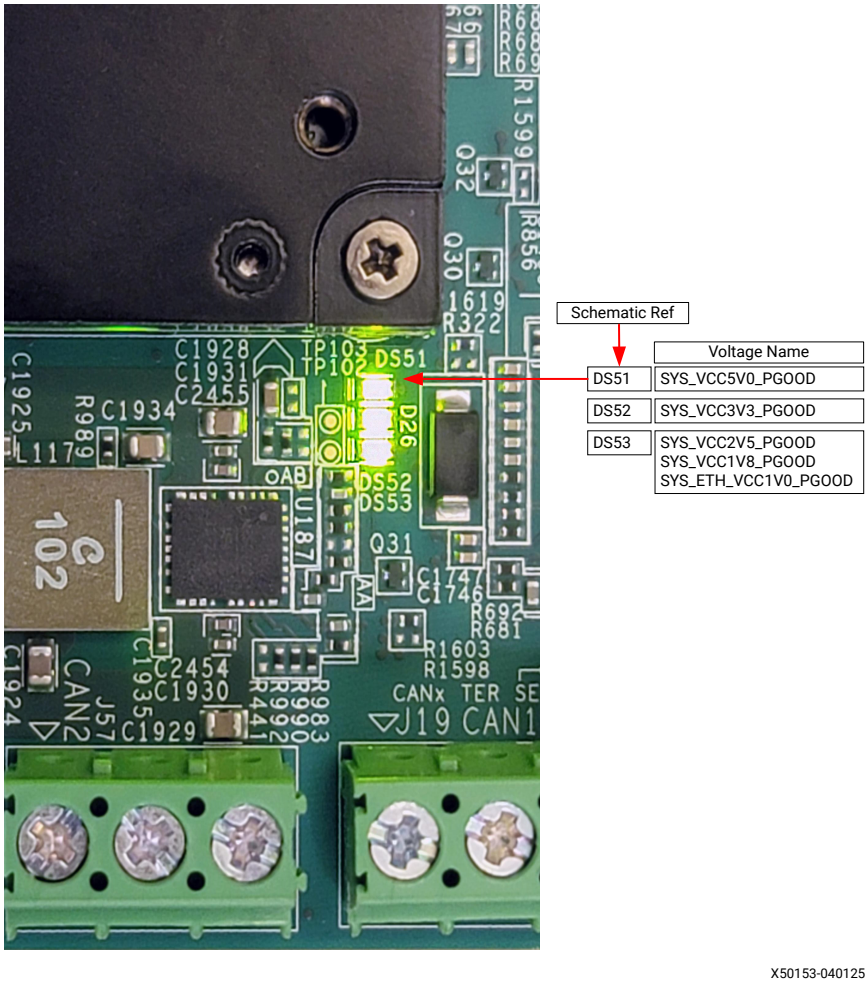


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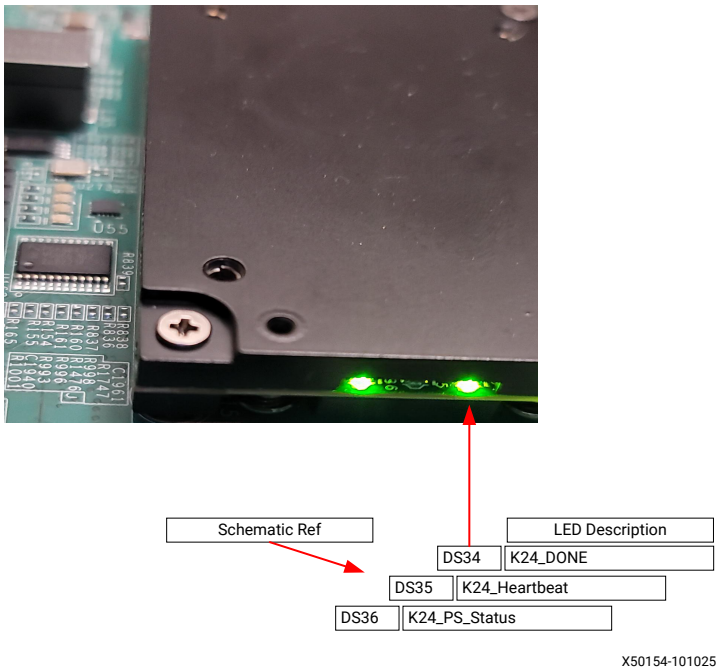
Figure 30: **Kria K24 SOM onboard LEDs**

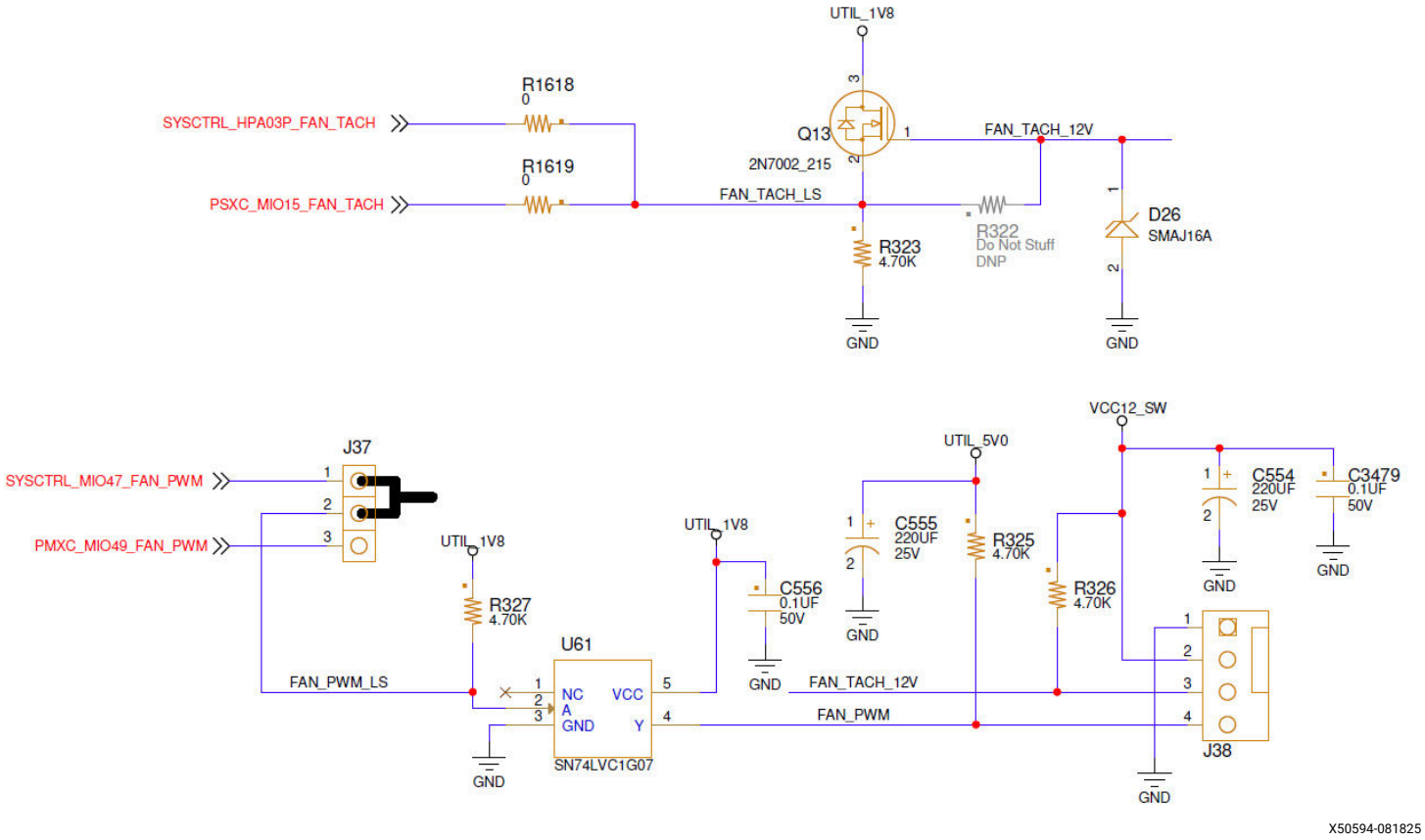


Cooling Fan Connector

The VEK385 cooling fan connector is shown in the following figure. The VEK385 uses the system controller to autonomously control the fan speed by controlling the pulse width modulation (PWM) signal to the fan. The fan rotates slowly (acoustically quiet) when the Versal AI Edge Series Gen 2 device U1 is cool and rotates faster as the device heats up (acoustically noisy).

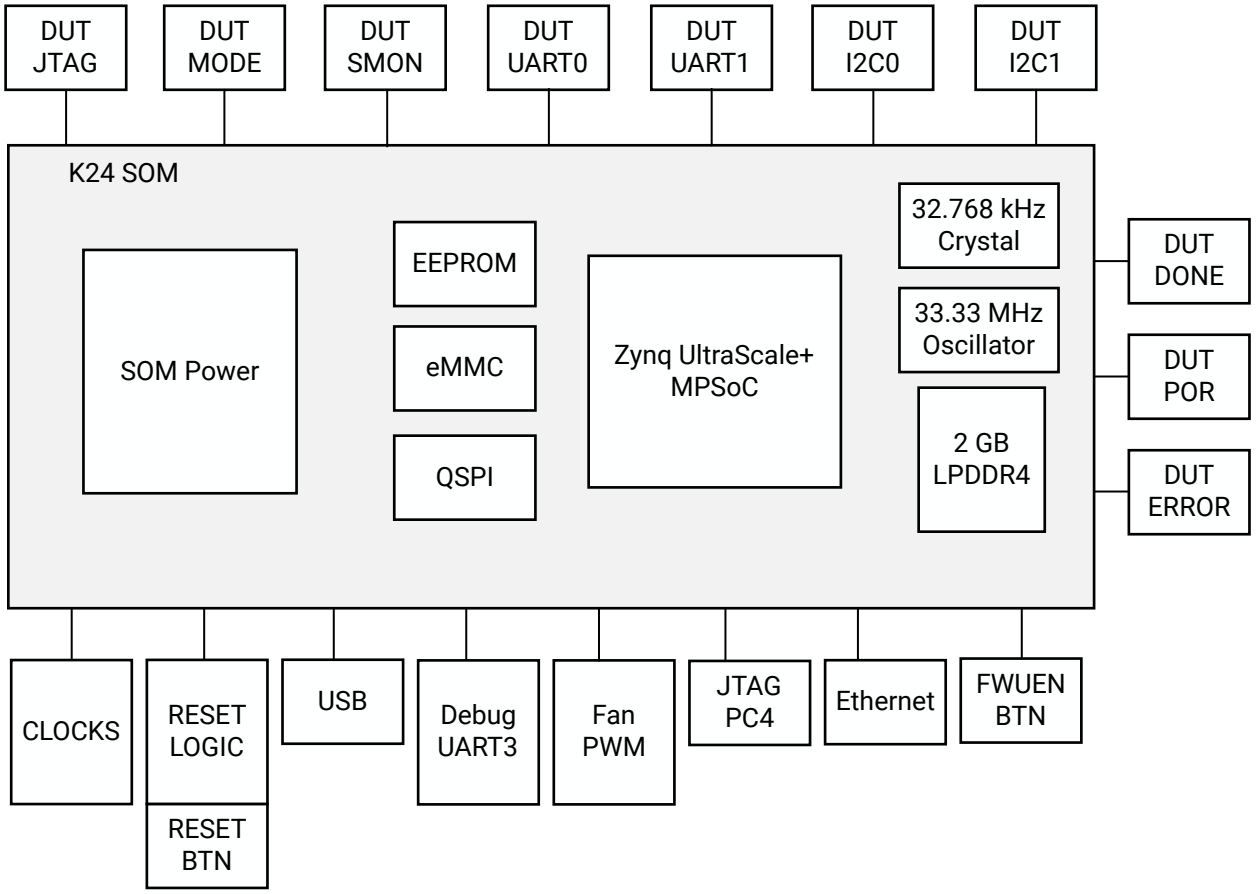
The VEK385 board provides a fan controller bypass header J37 to permit control by the Versal AI Edge Series Gen 2 device. See the Table 4 for more details.

Figure 31: **12V Fan Header**



System Controller

Figure 32: **System Controller Block Diagram**



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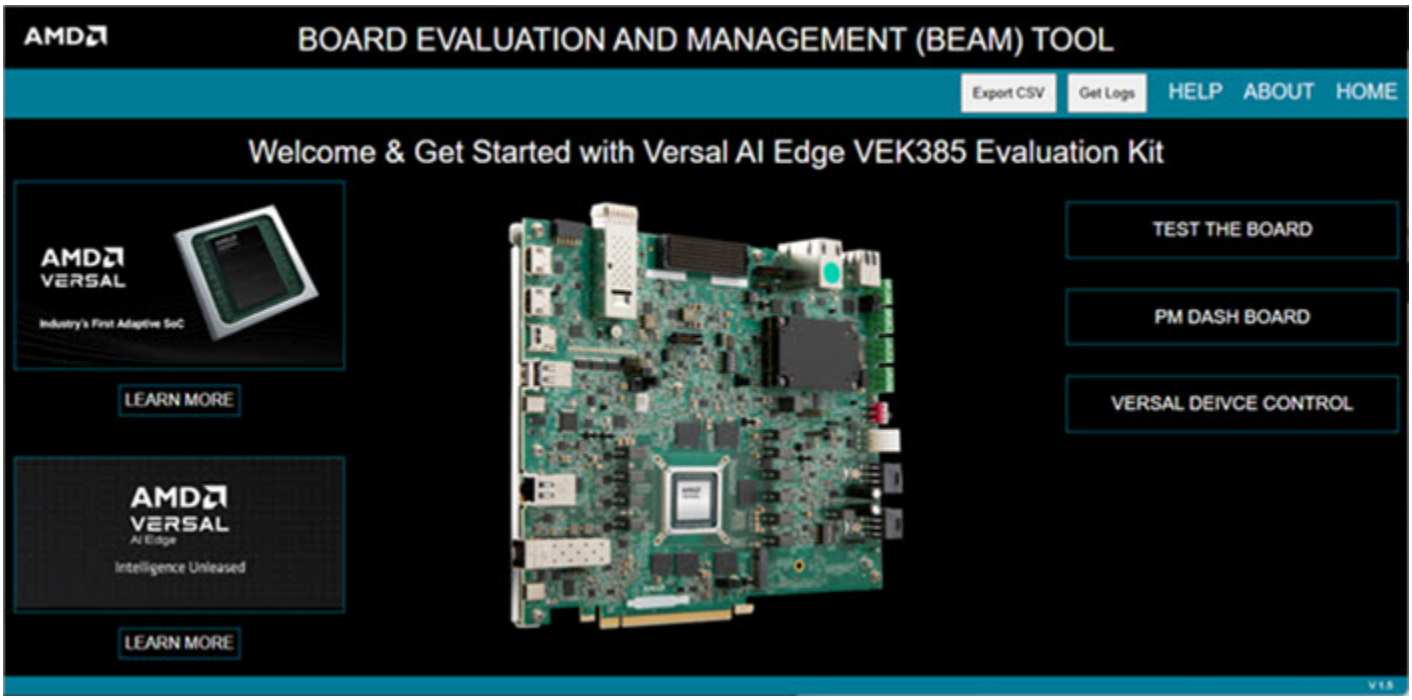
The VEK385 board includes an onboard system controller. The system controller consists of an AMD Kria™ K24, demonstrating the versatility of this System On Module (SOM). The system controller hosts a website that allows for various controls over aspects of the evaluation board. This web-based interface enables the query and control of select programmable features such as clocks, FMC functionality, and power system parameters (except for updates). Users should not change the default system controller image as that could potentially cause damage to the board if proper procedures are not followed. If this image needs to be updated and for more information on the system controller web interface, see the Versal Evaluation Board System Controller Wiki.

The web application is shown in the following figure.

Figure 33: **System Controller Web User Interface**



Power On/Off Slide Switch

The VEK385 board power switch is SW8. Sliding the switch actuator from the off to the on position applies 12 VDC power from the 2x3 6-pin mini-fit power input connector J28 (power from an external 120 VAC-to-12 VDC power adapter).

> **CAUTION!** *Do NOT plug a PC ATX power supply 6-pin connector into the VEK385 board power connector J16. The ATX 6-pin connector has a different pinout than J16. Connecting an ATX 6-pin connector into J16 damages the VEK385 board and voids the board warranty.*

The two 2x4 8-pin (6+2) ATX power supply PCIe-type connectors JP1 and JP2 are provided for higher power use cases.

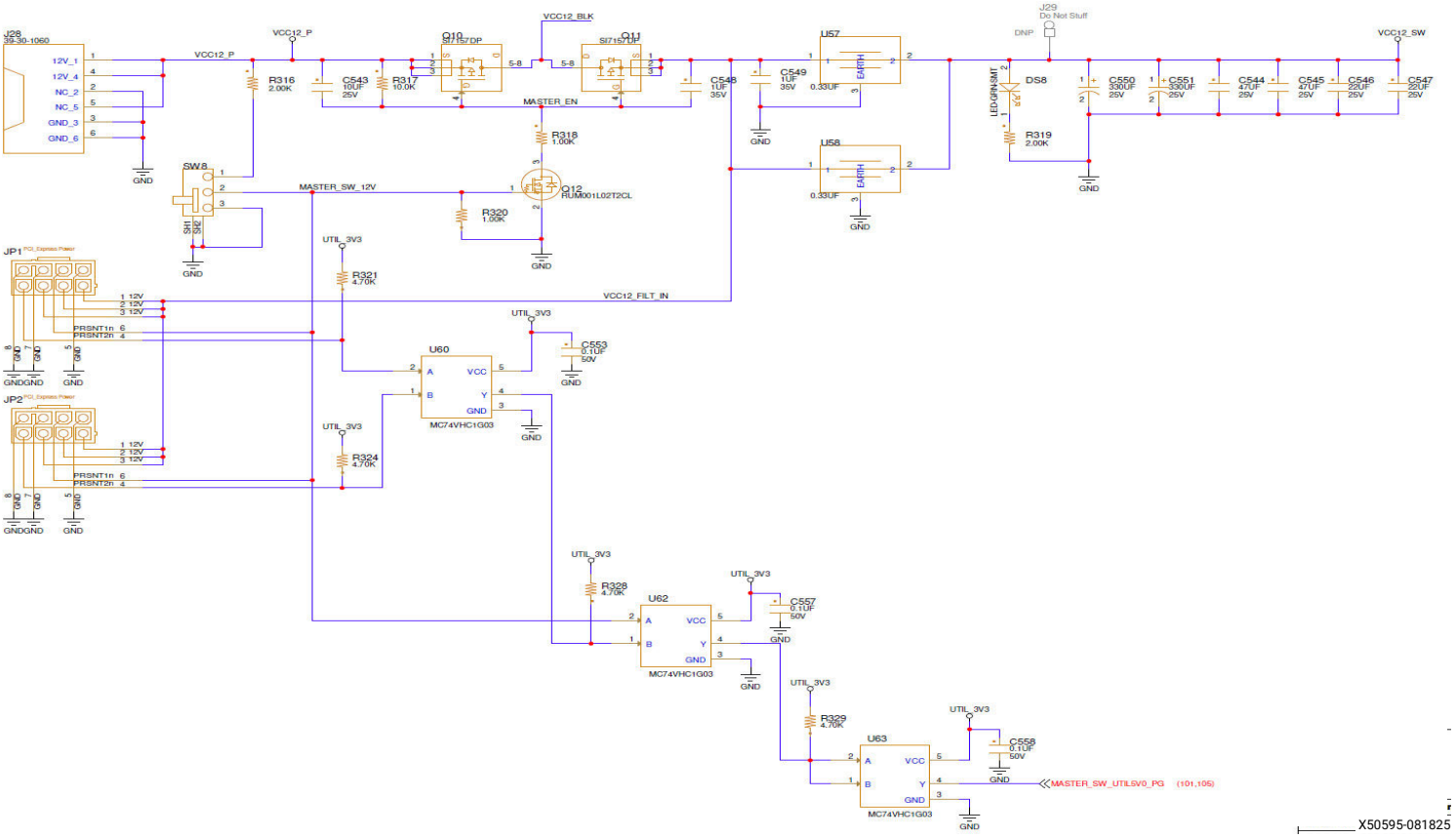
- The customer ATX supply chosen must support at least two PCIe (6+2) GPU connections to support powering the evaluation board.
- Only use a single ATX supply to support delivery of 12V to two PCIe GPU (6+2) connectors or damage might occur.
- When ATX PCIe GPU 6+2 connections are made, the 6 pin mini-fit Jr power brick connection and onboard on/off power switch is disabled.

The green LED DS8 illuminates when the VEK385 board power switch is on. See Board Power System for details on the onboard power system.

IMPORTANT! *Power to the VEK385 is mutually exclusive and only one of the two power connections should be powered. Either J28 or both JP1 and JP2 should be used to provide board power.*

The following figure shows the power connector J28, power switch SW8, and LED indicator DS8.

Figure 34: **Power Input**



Board Power System

The VEK385 evaluation board uses power management ICs (PMIC) and power regulators from MPS to supply the core and auxiliary voltages listed in the following tables. The detailed device connections for the feature described in this section are documented in the VEK385 board schematic.

Table 22: **Power System - PMBus Regulators and INA226 Map**

Domain	Rail Name	Nominal Voltage (V)	Max Current (A)	PMBUS Addr	PMIC Port	INA7xx Addr	Voltage Monitor Addr	Voltage Monitor Port
FPD	VCC_FPD	0.88	24	PMBUS1 0x23	8	PMBUS1_INA 0x40	PMBUS1 0x05	VIN2

Table 22: **Power System - PMBus Regulators and INA226 Map** *(cont'd)*

Domain	Rail Name	Nominal Voltage (V)	Max Current (A)	PMBUS Addr	PMIC Port	INA7xx Addr	Voltage Monitor Addr	Voltage Monitor Port
FPD	VCC_USB2_504	0.80	0.10	PMBUS1 0x12	N/A	N/A	N/A	N/A
FPD	VCC_PAUX_504	0.80	0.10	PMBUS2 0x13	N/A	N/A	N/A	N/A
FPD	VCC_USB3_504	0.80	0.20	PMBUS2 0x14	N/A	N/A	N/A	N/A
FPD	VCCIO_USB2_504	3.30	0.20	PMBUS2 0x15	N/A	N/A	N/A	N/A
FPD	VCCREG_USB2_504	3.30	0.20	PMBUS2 0x16	N/A	N/A	N/A	N/A
FPD	VCCIO_PAUX_504	1.80	0.10	PMBUS2 0x17	N/A	N/A	N/A	N/A
FPD	VCCIO_USB3_504	1.20	0.50	PMBUS2 0x18	N/A	N/A	N/A	N/A
LPD	VCC_LPD	0.88	6	PMBUS1 0x23	9	PMBUS1_INA 0x44	PMBUS1 0x05	VIN3
LPD	VCCAUX_LPD	1.50	2	PMBUS2 0x19	N/A	PMBUS1_INA 0x45	PMBUS1 0x05	VIN4
LPD	VCCO_50X	1.80	3	PMBUS1 0x1A	N/A	PMBUS1_INA 0x46	PMBUS1 0x05	VIN5
LPD	VCC_MIPI_507	0.80	0.50	PMBUS2 0x1E	N/A	PMBUS1_INA 0x47	N/A	N/A
LPD	VCCIO_MIPI_507	1.20	0.50	PMBUS2 0x1F	N/A	PMBUS2_INA 0x44	N/A	N/A
SoC	VCC_SOC_IO	0.80	30	PMBUS1 0x22	1-2	PMBUS1_INA 0x41	PMBUS1 0x05	VIN1PN
SoC	VCCAUX	1.50	5	PMBUS2 0x01	N/A	PMBUS2_INA 0x46	PMBUS1 0x06	VIN3
SoC	VCC_MMD	0.80	6	PMBUS1 0x22	9	PMBUS4_INA 0x44	PMBUS1 0x06	VIN5
SoC	VCCO_7xx_LP5	1.00	10	PMBUS1 0x22	8	PMBUS3_INA 0x47	PMBUS1 0x06	VIN4
SoC	VADJ_FMC	1.20	6	PMBUS2 0x02	N/A	PMBUS2_INA 0x47	N/A	N/A
PL	VCCINT	0.80	90	PMBUS1 0x23	1-4	PMBUS1_INA 0x48, 0x49, 0x4A, 0x4B	PMBUS1 0x07	VIN1PN
PL	VCC_RAM	0.80	2	PMBUS1 0x24	9	PMBUS4_INA 0x45	PMBUS1 0x07	VIN6
PL	VCCO_40X	3.30	2	PMBUS2 0x1B	N/A	PMBUS3_INA 0x44	N/A	N/A
PL	GTYP_AVCC	0.92	4	PMBUS1 0x24	8	PMBUS4_INA 0x46	PMBUS1 0x07	VIN3

Table 22: **Power System - PMBus Regulators and INA226 Map** *(cont'd)*

Domain	Rail Name	Nominal Voltage (V)	Max Current (A)	PMBUS Addr	PMIC Port	INA7xx Addr	Voltage Monitor Addr	Voltage Monitor Port
PL	GTYP_AVCCAUX	1.50	0.50	PMBUS1 0x1C	N/A	PMBUS3_INA 0x45	PMBUS1 0x07	VIN4
PL	GTYP_AVTT	1.20	4	PMBUS1 0x1D	N/A	PMBUS3_INA 0x46	PMBUS1 0x07	VIN5
AIE	VCC_AIE	0.80	90	PMBUS1 0x24	1-4	PMBUS2_INA 0x48, 0x49, 0x4A, 0x4B	PMBUS1 0x06	VIN1PN
UTIL0	UTIL_5V0	5.00	20	N/A	N/A	PMBUS2_INA 0x45 (Bank 504 only)	PMBUS1 0x07	N/A
UTIL0	UTIL_3V3	3.30	20	N/A	N/A	N/A	N/A	N/A
UTIL1	LP5_VDDH_1V05	1.05	5	PMBUS2 0x03	N/A	N/A	N/A	N/A
UTIL1	LP5_VDDQ_0V5	0.50	0.5	PMBUS2 0x04	N/A	N/A	N/A	N/A
UTIL1	UTIL_1V8	1.80	5	N/A	N/A	N/A	N/A	N/A
UTIL1	UTIL_2V5	2.50	5	N/A	N/A	N/A	N/A	N/A
UTIL1	UTIL_1V2	1.20	5	N/A	N/A	N/A	N/A	N/A
UTIL1	UTIL_ETH_VCC1V0	1.00	1	N/A	N/A	N/A	N/A	N/A
SYSCTRL0	SYS_VCC5V0	5.00	8	N/A	N/A	N/A	N/A	N/A
SYSCTRL1	SYS_VCC1V8	1.80	2	N/A	N/A	N/A	N/A	N/A
SYSCTRL1	SYS_VCC3V3	3.30	2	N/A	N/A	N/A	N/A	N/A
SYSCTRL1	SYS_VCC2V5	2.50	0.5	N/A	N/A	N/A	N/A	N/A
SYSCTRL1	SYS_ETH_VCC1V0	1.00	0.5	N/A	N/A	N/A	N/A	N/A

The FMCP HSPC (J13) VADJ pins are wired to the programmable rail VADJ_FMC. The VADJ_FMC rail is programmed to 1.20V by default, only 1.20V is supported. The VADJ_FMC rail also powers the 2VE3858 FMCP interface banks 705, 706, 707, 712, and 713. Documentation describing PMBus programming for the MPS power controllers is available on the MPS website. The PCB layout and power system design meet the recommended criteria described in the *Versal Adaptive SoC PCB Design User Guide* (UG863).

***Note*:** VCC12_SW is disabled when using ATX 12V (6+2) input.

More information about the power system regulator components can be found at the MPS website.

Monitoring Voltage and Current

Many power rails have a TI INA7xx PMBus power monitor circuit with connections to the rail series current sense resistor. This arrangement permits the INA7xx to report the sensed parameters separately on the PMBus. The rails equipped with the INA7xx power monitors are shown in the power system table in Board Power System. As described in PMXC_MIO[44:45] I2C1 Bus, the I2C1 bus provides access to the PMBus power controllers and the INA7xx power monitors via the U162 I2C multiplexor. All PMBus controlled regulators are tied to the various PMbus I2C PMBus interfaces, while the INA7xx power monitors are split across dedicated PMBus I2C PMBus interfaces. This is shown in the power system table in Table 22 and described in PMXC_MIO[44:45] I2C1 Bus.

These power system components are also accessible to the Kria K24 (JA) system controller web interface.

Appendix A

Xilinx Design Constraints

Overview

The Xilinx design constraints (XDC) file template for the board provides for designs targeting the evaluation board. Net names in the constraints listed correlate with net names on the latest evaluation board schematic. Identify the appropriate pins and replace the net names with net names in the user RTL.

See the *Vivado Design Suite User Guide: Using Constraints* (UG903) for more information.

The HSPC FMCP connector J13 is connected to the AMD Versal™ AI Edge Series Gen 2 adaptive SoC device U1 banks powered by the variable voltage VADJ_FMC. Because different FMC cards implement different circuitry, the FMC bank I/O standards must be uniquely defined by each customer.

IMPORTANT! *See the board documentation ("Board Files" check box) for the XDC file.*

Appendix B

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

For Technical Support, open a Support Service Request.

CE Information

CE Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

CE Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

CE Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

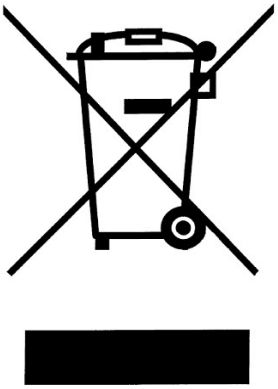
This is a Class A product. In a domestic environment, this product can cause radio interference, in which case the user might be required to take adequate measures.

CE Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Compliance Markings



In August of 2005, the European Union (EU) implemented the EU Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC and later the WEEE Recast Directive 2012/19/EU. These directives require Producers of electronic and electrical equipment (EEE) to manage and finance the collection, reuse, recycling and to appropriately treat WEEE that the Producer places on the EU market after August 13, 2005. The goal of this directive is to minimize the volume of electrical and electronic waste disposal and to encourage re-use and recycling at the end of life.

AMD has met its national obligations to the EU WEEE Directive by registering in those countries to which AMD is an importer. AMD has also elected to join WEEE Compliance Schemes in some countries to help manage customer returns at end-of-life.

If you have purchased AMD-branded electrical or electronic products in the EU and are intending to discard these products at the end of their useful life, please do not dispose of them with your other household or municipal waste. AMD has labeled its branded electronic products with the WEEE Symbol to alert our customers that products bearing this label should not be disposed of in a landfill or with municipal or household waste in the EU.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*.

Appendix C

Additional Resources and Legal Notices

Finding Additional Documentation

Technical Information Portal

The AMD Technical Information Portal is an online tool that provides robust search and navigation for documentation using your web browser. To access the Technical Information Portal, go to https://docs.amd.com.

Documentation Navigator

Documentation Navigator (DocNav) is an installed tool that provides access to AMD Adaptive Computing documents, videos, and support resources, which you can filter and search to find information. To open DocNav, do the following:

- From the AMD Vivado™ IDE, select **Help → Documentation and Tutorials**.
- On Windows, click the **Start** button and select **AMD Adaptive SoC and FPGA Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

***Note*:** For more information on DocNav, refer to the *Documentation Navigator User Guide* (UG968).

Design Hubs

AMD Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs, do the following:

- In DocNav, click the **Design Hubs View** tab.
- Go to the Design Hubs web page.

Support Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Support.

References

The most up to date information related to the VEK385 board and its documentation is available on this website:

These documents provide supplemental material useful with this guide:

1. *Versal Adaptive SoC GTY and GTYP Transceivers Architecture Manual* (AM002)
2. *Versal AI Edge Series Gen 2 and Prime Series Gen 2 Technical Reference Manual* (AM026)
3. *Versal Adaptive SoC PCB Design User Guide* (UG863)
4. *Vivado Design Suite User Guide: Using Constraints* (UG903)
5. *Versal AI Edge Series Gen 2 Data Sheet: DC and AC Switching Characteristics* (DS1021)
6. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
7. *Versal Adaptive SoC Integrated Block for PCI Express LogiCORE IP Product Guide* (PG343)
8. *Versal Adaptive SoC DMA and Bridge Subsystem for PCI Express Product Guide* (PG344)
9. *Programmable Network on Chip (NoC2) LogiCORE IP Product Guide* (PG406)
10. *Integrated DDR5/LPDDR5/5X Memory Controller LogiCORE IP Product Guide* (PG456)
11. *SmartLynq+ Module User Guide* (UG1514)
12. MPS
13. Versal Evaluation Board - System Controller BEAM Wiki

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
02/18/2026 Version 1.0	
Initial release.	N/A

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