Power Management IC

Two-Resistor Model for Thermal Simulation

This application note explains the two-resistor model, which is the simplest model among thermal models used in thermal simulations. The thermal simulations mentioned here cover three-dimensional model thermal conduction and thermal fluid analysis tools.

Models for thermal simulations

As shown in Figure 1, the models for thermal simulations can be classified into two types: compact thermal model (CTM) and detailed model.

For the CTM, JEDEC Solid State Technology Association has standardized two types of thermal models. The two-resistor model is suitable for “discrete” and “LSI” devices. Since this simple model is structured only by vertically dividing a package at the junction, it is ideal for single function devices such as discrete products. In addition, although the analysis speed of simulations is fast thanks to the simplicity of the model, its precision is the lowest among the three models. The DELPHI model supports LSI as well. It represents a package with a multi-resistor network so that errors can uniformly be reduced in a variety of operating environments. This model achieves a relatively good balance between analysis speed and precision with a small number of elements. However, it does not support the transient thermal analysis.

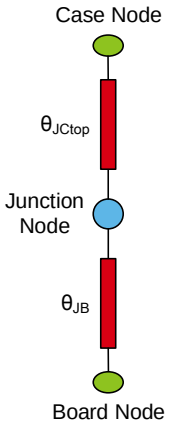
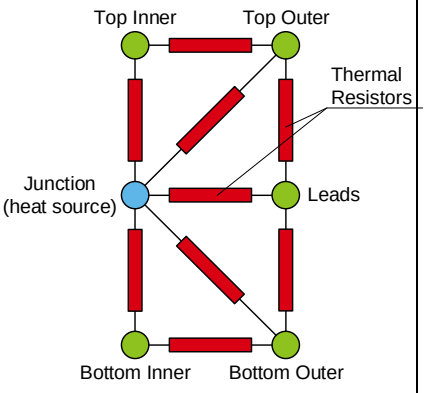
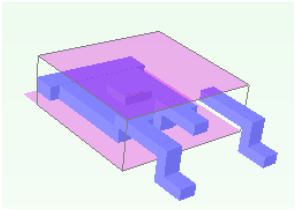
Type	Compact thermal model (CTM)		Detailed model
	Two-resistor model	DELPHI model	
Standard	JESD15-3	JESD15-4	N.A.
Shape			
Summary	• Simple model only dividing a package vertically at the junction • Ideal for single function devices such as discrete products	• Model representing a package with a multi-resistor network	• Detailed model including details of dimensions and physical properties of materials
Precision	Good	Better	Best
Shortcomings	• Least precise among the 3 models • Transient analysis not supported	• Transient analysis not supported	• Variation in quality without any standard • Long simulation time • No compatibility between tools

Figure 1. Models for thermal simulations

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In contrast, there is no standard for the detailed models and the quality of models varies with the companies that created them. Details of dimensions and physical properties of materials are needed to create a model. A non-disclosure agreement is normally required to obtain such information. Although the detailed model has the best precision, its simulation takes time. In addition, the thermal analysis tools are not compatible since there is no standard.

Description of two-resistor model

The physical arrangement of the two-resistor model is composed of three nodes as shown in Figure 2. The package includes a single integrated circuit. The temperature is represented with a single temperature node. The thermal flow path is represented using a thermal resistance network. Junction Node, Case Node, and Board Node represent the thermal source of the chip, the upper surface of the package, and the circuit board temperature at a position of 1 mm from the edge of the device, respectively. Two thermal resistors are connected between the junction and the case and between the junction and the board. The values of these thermal resistances are generated based on the thermal test of the JEDEC Standard. If no measurement value is available, the values extracted from the verified detailed model that simulates the test environment are used. For the extraction from the detailed model, three-dimensional thermal fluid analysis tools, such as Simcenter Flotherm™*1, are used.

The heating power occurs on Junction Node.

Case Node is considered to be in direct thermal contact with the environment immediately above the top part of the package (normally, air or thermal conducting material used together with the heat sink).

Board Node is considered to be in direct thermal contact with the environment immediately below the footprint of the package (normally, the printed circuit board).

The heat from the thermal source of the chip flows in two directions. One flows as radiation and convective heat transfer from the upper surface of the package to the surroundings, or into the heat sink mounted on the top of the package. The other flows into the PCB from the back surface of the package and the lead. Furthermore, no thermal flow is considered to be transferred from the side surfaces of the package to the surrounding fluid in this model.

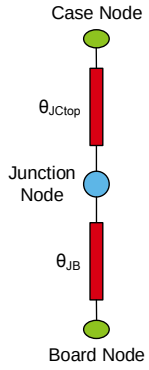

Figure 2. Physical arrangement of two-resistor thermal model

Overview of thermal resistance test environment

The methods of thermal resistance measurement are described for θ_{JB} in JEDEC Standard JESD51-8 and for θ_{JC} in JESD51-14. Here, an overview of the test environment for the two thermal resistors is explained. See JEDEC Standards for more details.

Test environment for θ_{JB}

For the measurement of θ_{JB}, an environment where the heat generated on Junction Node can be transferred to the board side is used. Figure 3 shows the schematic diagram of the test environment. The ring type cold plate is cooled with fluid (mainly water). The circuit board is clamped with the cold plate from both sides so that heat from the package flows radially in the inner surface of the circuit board. In addition, thermal insulation material is used for the package openings on the top and bottom of the cold plate to block the ambient temperature. The circuit board temperature is measured with the thermocouple. The temperature monitoring point is at the center of one side of the package, and within 1 mm from the periphery.

*1: Simcenter Flotherm™ is a trademark of Siemens Industry Software Inc.

After applying the power to the device, the junction temperature and the circuit board temperature are measured in a steady state. θ_{JB} is determined by Equation (1).

$$\theta_{JB} = \frac{T_J - T_B}{P} \quad [°C/W] \qquad (1)$$

T_J: Junction temperature when the device reaches the steady state after Power P is applied [°C]

T_B: Circuit board temperature in the steady state [°C]

P: Power consumption that causes the change in the junction temperature [W]

Test environment for θ_{JC}

As described in MIL-STD-883E, θ_{JC} had traditionally been determined by directly measuring the temperature difference between the junction and the surface of the case in contact with the water cooled copper heat sink using a thermocouple. Since the measurement of the case temperature with a thermocouple is prone to errors, these results had a poor reproducibility. This is because the contact between the thermocouple and the case may not be at the maximum case temperature due to the latent temperature distribution in the package case. In addition, the temperature may be lowered if the thermocouple is not adequately insulated from the cold plate.

In JESD51-14, the reproducibility of θ_{JC} measurement is significantly improved by eliminating the measurement of the case temperature using a thermocouple. Figure 4 shows the schematic diagram of the test environment. The cold plate is cooled with fluid (mainly water). The device to be tested is fixed on the cold plate. Pressure with a sufficient strength is applied from the top of the case to ensure a good thermal contact between the case surface and the cold plate. To minimize heat flow to the top of the device, the clamping parts should be heat-insulated using material with low thermal conductivity.

The junction temperature of the device is monitored and the following two types of transient thermal resistance $Z_{\theta JC}$ are measured: one is when thermal interface material (TIM), such as thermal conductive grease, oil, or sheeting, is used (wet) and the other is when TIM is not used (dry) between the device and the cold plate. θ_{JC} is determined from the branch point of the two types of transient thermal resistance measured.

Considerations for use

Since the two-resistor model is based on the thermal resistance measured in the JEDEC Standard environment, the model should be used after recognizing that an error will occur if the temperature is estimated by applying the model to other environments. θ_{JB} and θ_{JC} can be used as an index of the thermal performance to incorporate the device into thermal simulation models on the circuit board level. The way the information is used in the simulations on the circuit board level and the precision of their results vary with other errors in modeling of the environment, discretization errors, and the simulation software as well. Since θ_{JB} and θ_{JC} are mainly performance indices, the precision of the simulation results on the circuit board level is lower than the precision obtained with the detailed model. Therefore, care must be taken when using the two-resistor model to predict the absolute value of temperature. This model is suitable for roughly determining the circuit board size and the parts arrangement or checking relative differences between different packages during the initial designing.

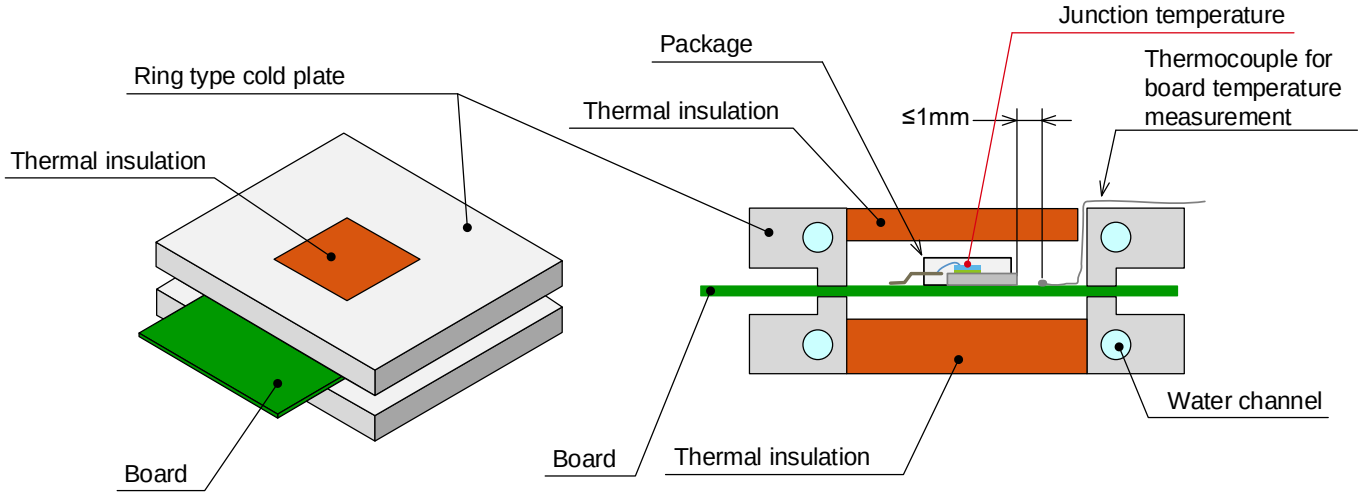

Figure 3. Schematic diagram of θ_{JB} test environment

Left: Overhead view, Right: Cross section of test fixture

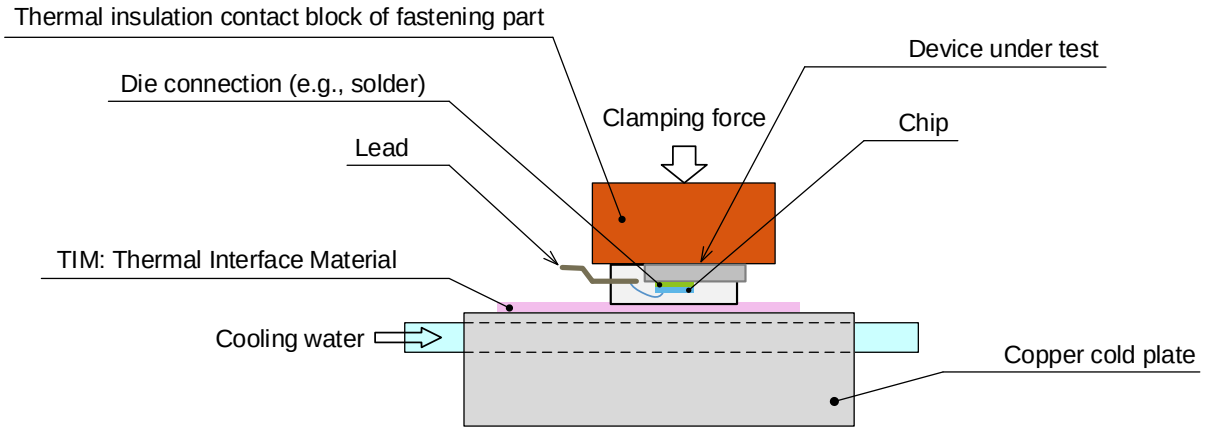

Figure 4. Schematic diagram of θ_{JC} test environment

References

[1] JESD51:1995, *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Devices)*

[2] JESD51-1:1995, *Integrated Circuit Thermal Measurement Method - Electrical Test Method*

[3] JESD51-3:1996, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

[4] JESD51-8:1999, *Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board*

[5] JESD51-12.01:2012, *Guidelines for Reporting and Using Electronic Package Thermal Information*

[6] JESD51-14:2010, *Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction to Case of Semiconductor Devices with Heat Flow Through a Single Path*

[7] JESD15-1:2008, *Compact Thermal Modeling Overview*

[8] JESD15-3:2008, *Two-Resistor Compact Thermal Model Guideline*

[9] MIL-STD-883E, METHOD 1012.1, *Thermal Characteristics*, 4 November 1980

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