USB 3.0 TO SATA BRIDGE

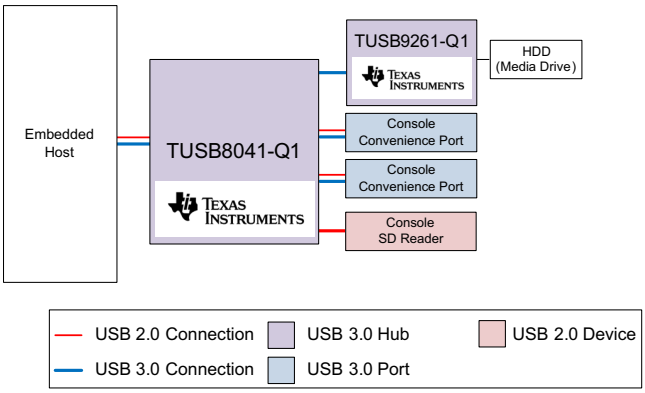
Check for Samples: TUSB9261-Q1

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Exceptions:
  - Device CDM ESD Classification Level C3
- Ideal for bridging Serial ATA (SATA) Devices, Such as Hard Disk Drives (HDD), Solid State Drives (SSD), or Optical Drives (OD) to Universal Serial Bus (USB)
- USB Interface
  - Integrated Transceiver Supports SS/HS/FS Signaling
  - Best in Class Adaptive Equalizer
    - Allows for Greater Jitter Tolerance in the Receiver
  - USB Class Support
    - USB Attached SCSI Protocol (UASP) for HDD and SSD
    - USB Mass Storage Class Bulk-Only Transport (BOT) Including Support for Error Conditions Per the 13 Cases (Defined in the BOT Specification)
    - USB Bootability Support
    - USB Human Interface Device (HID)
  - Supports Firmware Update Via USB Using a TI Provided Application
- SATA Interface
  - Serial ATA Specification Revision 2.6 Supporting gen1 and gen2 Data Rates
  - Supports hot plug
  - Supports Mass-Storage Devices Compatible with the ATA/ATAPI-8 Specification
- Integrated ARM Cortex M3 Core
  - Customizable Application Code Loaded From EEPROM Via SPI Interface
  - Two Additional SPI Port Chip Selects for Peripheral Connection
  - Up to 5 GPIOs for End-User Configuration via HID
  - Serial Communications Interface for Debug (UART)
- General Features
  - Integrated Spread Spectrum Clock Generation Enables Operation from a Single Low Cost Crystal or Clock Oscillator
    - Supports 20, 25, 30 or 40 MHz
  - JTAG Interface for IEEE1149.1 and IEEE1149.6 Boundary Scan
  - Available in a Fully RoHS Compliant Package (PAP)

APPLICATIONS

- Automotive
- External HDD/SSD
- External DVD
- HDD-Based Portable Media Player



DESCRIPTION

The TUSB9261-Q1 is an ARM cortex M3 microcontroller based Universal Serial Bus (USB) 3.0 to Serial ATA (SATA) bridge. It provides the necessary hardware and firmware to implement a USB Attached SCSI Protocol (UASP) compliant mass storage device suitable for bridging SATA compatible hard disk drives (HDD) and solid state disk drives (SSD) to a USB 3.0 bus. The firmware also implements the mass storage class bulk-only transport (BOT) for bridging optical drives and other compatible SATA devices to the USB bus. In addition to UASP and BOT support,a USB human interface device (HID) interfaces is supported for control of the general purpose input/ouput (GPIO). The SATA interface supports gen1 (1.5-Gbps) and gen2 (3.0-Gbps) for cable lengths up to 2 meters.

The device is available in a 64-pin HTQFP package and is designed for operation over the industrial temperature range of -40°C to 85°C.

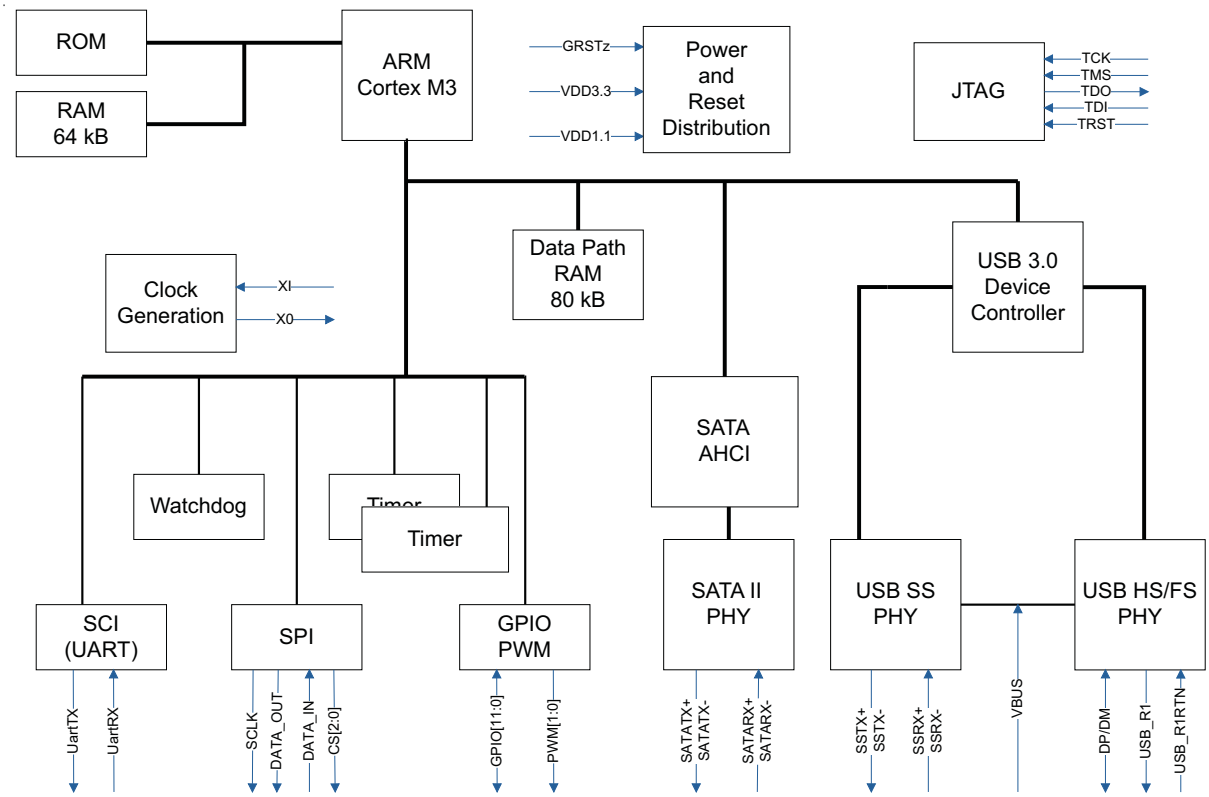


Figure 1. TUSB9261-Q1 Block Diagram

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN ASSIGNMENTS

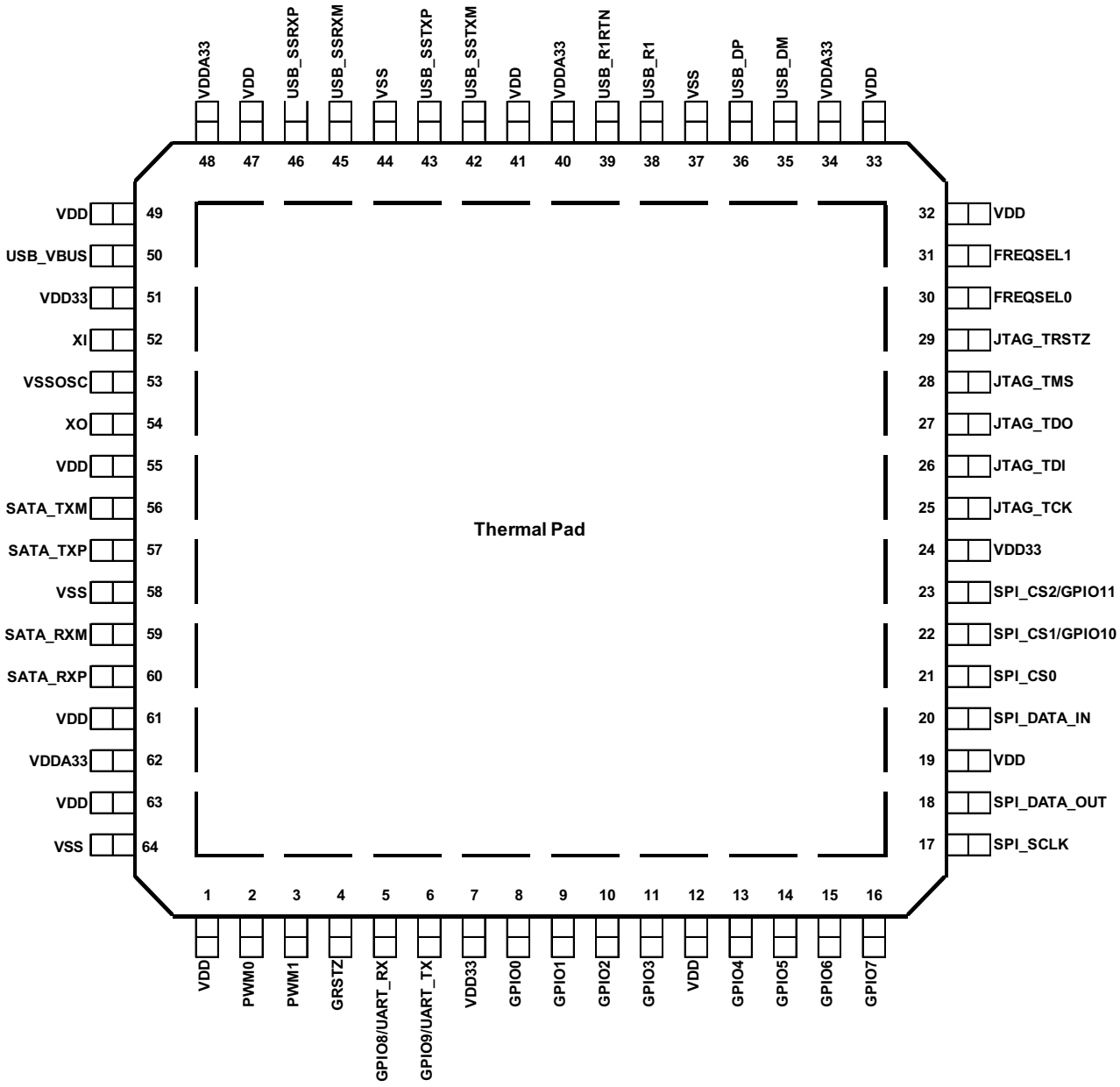


Figure 2. TUSB9261-Q1 Pin Diagram

Table 1. I/O Definitions

I/O TYPE	DESCRIPTION
I	Input
O	Output
I/O	Input - Output
PU	Internal pull-up resistor
PD	Internal pull-down resistor
PWR	Power signal

Table 2. Clock and Reset Signals

TERMINAL		I/O	DESCRIPTION		
NAME	PIN NO.				
GRSTz	4	I PU	Global power reset. This reset brings all of the TUSB9261-Q1 internal registers to their default states. When GRSTz is asserted, the device is completely nonfunctional.		
XI	52	I	Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal a 1-MΩ feedback resistor is required between X1 and XO.		
XO	54	O	Crystal output. This terminal is the crystal output for the internal oscillator. If XI is driven by an external oscillator this pin may be left unconnected. When using a crystal a 1-MΩ feedback resistor is required between X1 and XO.		
FREQSEL[1:0]	31, 30	I PU	Frequency select. These terminals indicate the oscillator input frequency and are used to configure the correct PLL multiplier. The field encoding is as follows:		
			FREQSEL[1]	FREQSEL[0]	INPUT CLOCK FREQUENCY
			0	0	20 MHz
			0	1	25 MHz
			1	0	30 MHz
			1	1	40 MHz

Table 3. SATA Interface Signals(1)

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
SATA_TXP	57	O	Serial ATA transmitter differential pair (positive)
SATA_TXM	56	O	Serial ATA transmitter differential pair (negative)
SATA_RXP	60	I	Serial ATA receiver differential pair (positive)
SATA_RXM	59	I	Serial ATA receiver differential pair (negative)

(1) Note that the default firmware and reference design for the TUSB9261-Q1 have the SATA TXP/TXM swapped for ease of routing in the reference design. If you plan to use the TI default firmware please review the reference design in the TUSB9261 DEMO User's Guide (SLLU139) for proper SATA connection.

Table 4. USB Interface Signals

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
USB_SSTXP	43	O	SuperSpeed USB transmitter differential pair (positive)
USB_SSTXM	42	O	SuperSpeed USB transmitter differential pair (negative)
USB_SSRXP	46	I	SuperSpeed USB receiver differential pair (positive)
USB_SSRXM	45	I	SuperSpeed USB receiver differential pair (negative)
USB_DP	36	I/O	USB High-speed differential transceiver (positive)
USB_DM	35	I/O	USB High-speed differential transceiver (negative)
USB_VBUS	50	I	USB Upstream port power monitor. The USB_VBUS input is a 1.2V I/O cell and requires a voltage divider to prevent damage to the input. The signal USB_VBUS must be connected to VBUS through a 90.9 kΩ ±1% resistor, and to signal ground through a 10 kΩ ±1% resistor. This allows the input to detect VBUS present from a minimum of 4V and sustain a maximum VBUS voltage up to 10V (applied to the voltage divider).
USB_R1	38	O	Precision resistor reference. A 10-kΩ ±1% resistor should be connected between R1 and R1RTN.
USB_R1RTN	39	I	Precision resistor reference return

Table 5. Serial Peripheral Interface (SPI) Signals

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
SPI_SCLK	17	O PU	SPI clock
SPI_DATA_OUT	18	O PU	SPI master data out
SPI_DATA_IN	20	I PU	SPI master data in
SPI_CS0	21	O PU	Primary SPI chip select for Flash RAM
SPI_CS2/ GPIO11	23	I/O PU	SPI chip select for additional peripherals. When not used for SPI chip select this pin may be used as general purpose I/O. SeeTable 8 for firmware configuration defaults.
SPI_CS1/ GPIO10	22	I/O PU	SPI chip select for additional peripherals. When not used for SPI chip select this pin may be used as general purpose I/O. SeeTable 8 for firmware configuration defaults.

Table 6. JTAG, GPIO, and PWM Signals

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
JTAG_TCK	25	I PD	JTAG test clock
JTAG_TDI	26	I PU	JTAG test data in
JTAG_TDO	27	O PD	JTAG test data out
JTAG_TMS	28	I PU	JTAG test mode select
JTAG_TRSTz	29	I PD	JTAG test reset
GPIO9/UART_TX	6	I/O PU	GPIO/UART transmitter. This terminal can be configured as a GPIO or as the transmitter for a UART channel. SeeTable 8 for firmware configuration defaults.
GPIO8/UART_RX	5	I/O PU	GPIO/UART receiver. This terminal can be configured as a GPIO or as the receiver for a UART channel. SeeTable 8 for firmware configuration defaults.
GPIO7	16	I/O PD	Configurable as general purpose input/outputs. SeeTable 8 for firmware configuration defaults.
GPIO6	15	I/O PD	
GPIO5	14	I/O PD	
GPIO4	13	I/O PD	
GPIO3	11	I/O PD	
GPIO2	10	I/O PD	
GPIO1	9	I/O PD	
GPIO0	8	I/O PD	
PWM0	2	O PD(1)	Pulse Width Modulation (PWM) which can be used to drive status LED's. SeeTable 8 for firmware configuration defaults.
PWM1	3	O PD(1)	

(1) PWM pull down resistors are disabled by default. A firmware modification is required to turn them on. All other internal pull up/down resistors are enabled by default.

Table 7. Power and Ground Signals

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO.		
VDD	1, 12, 19, 32, 33, 41, 47, 49, 55, 61, 63	PWR	1.1-V power rail
VDD33	7, 24, 51	PWR	3.3-V power rail
VDDA33	34, 40, 48, 62	PWR	3.3-V analog power rail
VSSOSC	53	PWR	Oscillator ground. If using a crystal, this should not be connected to PCB ground plane. If using an oscillator, this should be connected to PCB ground. See the Clock Source Requirements section for more details.
VSS	37, 44, 58, 64	PWR	Ground
VSS	65	PWR	Ground - Thermal Pad

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

				VALUE	UNIT
VDD	Steady-state supply voltage			–0.3 to 1.4	V
VDD33/ VDDA33	Steady-state supply voltage			–0.3 to 3.8	V
V_{IO}	USB 2.0 DP/DM			–0.3 to 3.8	V
	SuperSpeed USB TXP/M and RXP/M			–0.3 to 3.8	
	SATA TXP/M and RXP/M			–0.3 to 3.8	
	XI/XO			–0.3 to 1.98	
	3.3V Tolerant I/O			–0.3 to 3.8	
V_{USB_VBUS}	Voltage at USB_VBUS pad			–0.3 to 1.2	V
T_{STG}	Storage temperature range			-65 to 150	°C
T_J	Operating junction temperature range			-40 t o 105	°C
ESD rating	Human-body model (HBM) AEC-Q100 Classification Level H2			2	kV
	Charged-device model (CDM)	AEQ-Q100 Classification Level C4B	Corner pins	750	V
			Non-corner pins except USB_R1	500	
		AEQ-Q100 Classification Level C3	USB_R1	450	

THERMAL INFORMATION

THERMAL METRIC(1)		TUSB9261-Q1 PAP 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	30.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	11	
θ_{JB}	Junction-to-board thermal resistance(4)	6.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	.04	
ψ_{JB}	Junction-to-board characterization parameter(6)	6.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	0.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Digital 1.1 supply voltage	1.045	1.1	1.155	V
VDD33	Digital 3.3 supply voltage	3	3.3	3.6	V
VDDA33	Analog 3.3 supply voltage	3	3.3	3.6	V

RECOMMENDED OPERATING CONDITIONS (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IO}	USB 2.0 DM/DP	0		VDD33	V
	SuperSpeed USB TXM/P and RXM/P	0		VDD33	
	SATA TXM/P and RXM/P	0		VDD33	
	XI/XO	0		1.8	
	3.3V Tolerant I/O	0		VDD33	
V_{USB_VBUS}	Voltage at USB_VBUS PAD	0		1.155	V
T_A	Operating free-air temperature range	-40		85	°C
T_J	Operating junction temperature range	-40		105	°C

DC ELECTRICAL CHARACTERISTICS FOR 3.3-V DIGITAL I/O

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
T_R	Rise time	5 pF			1.5	ns
T_F	Fall time	5 pF			1.53	ns
I_{OL}	Low-level output current	VDD33 = 3.3 V, T_J = 25°C		6		mA
I_{OH}	High-level output current	VDD33 = 3.3 V, T_J = 25°C		–6		mA
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
V_{OH}	High-level output voltage	I_{OL} = –2 mA	2.4			V
V_O	Output voltage		0		VDD33	V
RECEIVER						
V_I	Input voltage		0		VDD33	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IH}	High-level input voltage		2			V
V_{hys}	Input hysteresis		200			mV
t_T	Input transition time (T_R and T_F)				10	ns
I_I	Input current	V_I = 0 V to VDD33			5	µA
C_I	Input capacitance	VDD33 = 3.3 V, T_J = 25°C		0.384		pF

SuperSpeed USB POWER CONSUMPTION

POWER RAIL	TYPICAL ACTIVE CURRENT (mA)(1)	TYPICAL SUSPEND CURRENT (mA)(2)
VDD11	291	153
VDD33(3)	65	28

(1) Transferring data via SS USB to a SSD SATA Gen II device. No SATA power management, U0 only.
(2) SATA Gen II SSD attached no active transfer. No SATA power management, U3 only.
(3) All 3.3-V power rails connected together.

HIGH SPEED USB POWER CONSUMPTION

POWER RAIL	TYPICAL ACTIVE CURRENT (mA)(1)	TYPICAL SUSPEND CURRENT (mA)(2)
VDD11	172	153
VDD33(3)	56	28

(1) Transferring data via HS USB to a SSD SATA Gen II device. No SATA power management.
(2) SATA Gen II SSD attached no active transfer. No SATA power management.
(3) All 3.3-V power rails connected together.

OPERATION

General Functionality

The TUSB9261-Q1 ROM contains boot code that executes after a global reset which performs the initial configuration required to load a firmware image from an attached SPI flash memory to local RAM. In the absence of an attached SPI flash memory or a valid image in the SPI flash memory, the firmware will idle and wait for a connection from a USB host through its HID interface which is also configured from the boot code. The latter can be accomplished using a custom application or driver to load the firmware from a file resident on the host system.

Once the firmware is loaded it configures the SATA advanced host controller interface host bus adapter (AHCI) and the USB device controller. In addition, the configuration of the AHCI includes a port reset which initiates an out of band (OOB) TX sequence from the AHCI link layer to determine if a device is connected, and if so negotiate the connection speed with the device (3.0 Gbps or 1.5 Gbps). Following speed negotiation, the firmware queries the attached device for capabilities and configures the device as appropriate for its interface and supported capabilities, for example a HDD that supports native command queuing (NCQ). If no SATA device is connected, the firmware will configure the USB interface as a removable media device which supports SATA hot plug events.

The configuration of the USB device controller includes creation of the descriptors, configuration of the device endpoints for support of UASP and USB mass storage class bulk-only transport, allocation of memory for the transmit request blocks (TRBs), and creation of the TRBs necessary to transmit and receive packet data over the USB. In addition, the firmware provides any other custom configuration required for application specific implementation, for example a HID interface for user initiated backup.

After USB device controller configuration is complete, the firmware connects the device to the USB bus when VBUS is detected. According to the USB 3.0 specification, the TUSB9261-Q1 will initially try to connect at SuperSpeed USB, if successful it will enter U0; otherwise, after the training time out it will enable the DP pull up and connect as a USB 2.0 high-speed or full-speed device depending on the speed supported by host or hub port.

When connected, the firmware presents the BOT interface as the primary interface and the UASP interface as the secondary interface. If the host stack is UASP aware, it can enable the UASP interface using a SET_INTERFACE request for alternate interface 1.

Firmware Support

Default firmware support is provided for the following:

- SuperSpeed USB and USB 2.0 High-Speed and Full-Speed
- USB Attached SCSI Protocol (UASP) for Hard Disk Drives (HDD) and Solid State Drives (SSD)
- USB Mass Storage Class (MSC) Bulk-Only Transport (BOT) for HDD, SSD, and Optical Drives
  - Including the 13 Error Cases
- USB Mass Storage Specification for Bootability
- USB Device Class Definition for Human Interface Devices (HID)
  - Firmware Update and Custom Functionality (e.g. One-Touch Backup)
- Serial ATA Advanced Host Controller Interface (AHCI)
- General Purpose Input/Output (GPIO)
  - LED Control and Custom Functions (e.g. One-Touch Backup Control)
- Pulse Width Modulation (PWM)
  - LED Dimming Control
- Serial Peripheral Interface (SPI)
  - Firmware storage and storing Custom Device Descriptors
- Serial Communications Interface (SCI)
  - Debug Output Only

GPIO/PWM LED Designations

The default firmware provided by TI drives the GPIO and PWM outputs as listed in the table below.

Table 8. GPIO/PWM LED Designations

GPIO0	Undefined. Defaults to input with integrated pull-down. Controllable as output via HID.	
GPIO1/GPIO5	Output indicating USB3 power state (U0-U3), if U1/U2 is enabled. Otherwise, defaults to an input with pull-down and may be driven low or high as an output via HID.	00: U3 state or default 01: U2 state 10: U1 state 11: U0 state
GPIO2	Output indicating HS/FS suspend when connected as USB 2.0. High indicates the USB 2.0 HS/FS bus is suspended.	
GPIO3	Input with integrated pull-down for momentary push button input to signal remote wake.	
GPIO4	Input to identify bus or self-powered status. Input should be high to indicate self-powered.	
GPIO6	Undefined. Defaults to input with pull-down. Controllable as output via HID.	
GPIO7	Output indicating SuperSpeed USB connection status. High indicates a SuperSpeed USB connection.	
GPIO8	UART Rx	
GPIO9	UART Tx	
GPIO10	Undefined. Defaults to input with integrated pull-up. Controllable as output via HID.	
GPIO11	Input with integrated pull-up to indicate a power fault condition. Low indicates a power fault.	
PWM0	Output indicating disk activity.	
PWM1	Output indicating software heartbeat.	

The LED's on the TUSB9261 Product Development Kit (PDK) board are connected as in the table above. Please see the TUSB9261 PDK Guide for more information on GPIO LED connection and usage. This EVM is available for purchase, contact TI for ordering information.

Power Up and Reset Sequence

The TUSB9261-Q1 does not have specific power sequencing requirements with respect to the core power (VDD), I/O power (VDD33), or analog power (VDDA33) for reliability reasons. The core power (VDD) or IO power (VDD33) may be powered up for an indefinite period of time while others are not powered up if all of these constraints are met:

- All maximum ratings and recommended operating conditions are observed.
- All warnings about exposure to maximum rated and recommended conditions are observed, particularly junction temperature. These apply to power transitions as well as normal operation.
- Bus contention while VDD33 is powered up must be limited to 100 hours over the projected life-time of the device.
- Bus contention while VDD33 is powered down may violate the absolute maximum ratings.

A supply bus is powered up when the voltage is within the recommended operating range. It is powered down when it is below that range, either stable or in transition.

A minimum reset duration of 1 ms is required. This is defined as the time when the power supplies are in the recommended operating range to the de-assertion of GRSTz. If a passive reset circuit is used to provide GRSTz it is recommended that core power (VDD) be ramped prior to or at the same time as I/O power (VDD33). If this is not practical it is recommended to use a power good output from the core voltage regulator or voltage supervisory circuit to ensure a good reset input. The recommended duration of the GRSTz input is greater than 2 ms but less than 100 ms.

CLOCK CONNECTIONS

Clock Source Requirements

The TUSB9261-Q1 supports an external oscillator source or a crystal unit. If a clock is provided to XI instead of a crystal, XO is left open and VSSOSC should be connected to the PCB ground plane. Otherwise, if a crystal is used, the connection needs to follow the guidelines below.

Since XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. It is also recommended to minimize the capacitance be-tween XI and XO. This can be accomplished by connecting the VSSOSC lead to the two external capaci-tors CL1 and CL2 and shielding them with the clean ground lines. The VSSOSC should not be connected to PCB ground when using a crystal.

Load capacitance (C_{load}) of the crystal varying with the crystal vendors is the total capacitance value of the entire oscillation circuit system as seen from the crystal. It includes two external capacitors CL1 and CL2 in Figure 3. The trace length between the decoupling capacitors and the corresponding power pins on the TUSB9261 needs to be minimized. It is also recommended that the trace length from the capacitor pad to the power or ground plane be minimized.

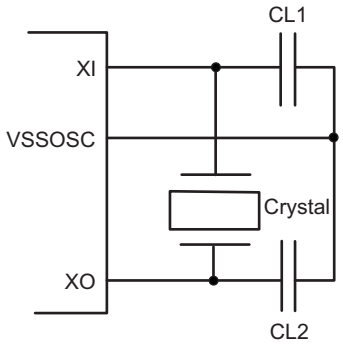


Figure 3. Typical Crystal Connections

Clock Source Selection Guide

Reference clock jitter is an important parameter. Jitter on the reference clock will degrade both the trans-mit eye and receiver jitter tolerance no matter how clean the rest of the PLL is, thereby impairing system performance. Additionally, a particularly jittery reference clock may interfere with PLL lock detection mechanism, forcing the Lock Detector to issue an Unlock signal. A good quality, low jitter reference clock is required to achieve compliance with supported USB3.0 standards. For example, USB3.0 specification requires the random jitter (RJ) component of either RX or TX to be 2.42 ps (random phase jitter calculated after applying jitter transfer function - JTF). As the PLL typically has a number of additional jitter components, the Reference Clock jitter must be considerably below the overall jitter budget.

Oscillator

XI should be tied to the 1.8-V clock source and XO should be left floating.

VSSOSC should be connected to the PCB ground plane.

A 20-, 25-, 30- or 40-MHz clock can be used.

Table 9. Oscillator Specification

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
C_{XI}	XI input capacitance	T_J = 25°C		0.414		pF
V_{IL}	Low-level input voltage				0.7	V
V_{IH}	High-level input voltage		1.05			V
T_{tosc_i}	Frequency tolerance	Operational temperature	–50		50	ppm
T_{duty}	Duty cycle		45	50	55	%
T_R/T_F	Rise/Fall time	20% - 80 %			6	ns
R_J	Reference clock R_J	JTF (1 sigma)(1) (2)			0.8	ps
T_J	Reference clock T_J	JTF (total p-p)(2) (3)			25	ps
T_{p-p}	Reference clock jitter	(absolute p-p)(4)			50	ps

(1) Sigma value assuming Gaussian distribution
(2) After application of JTF
(3) Calculated as 14.1 x R_J + D_J
(4) Absolute phase jitter (p-p)

Crystal

A parallel, 20-pF load capacitor should be used if a crystal source is used.

VSSOSC should not be connected to the PCB ground plane.

A 20-, 25-, 30- or 40-MHz crystal can be used.

Table 10. Crystal Specification

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
	Oscillation mode		Fundamental			
f_O	Oscillation frequency			20		MHz
				25		
				30		
				40		
ESR	Equivalent series resistance	20 MHz and 25 MHz			50	Ω
		30 MHz			40	
		40 MHz			30	
T_{tosc_i}	Frequency tolerance	Operational temperature			±50	ppm
	Frequency stability	1 year aging			±50	ppm
C_L	Load capacitance		12	20	24	pF
C_{SHUNT}	Crystal and board stray capacitance				4.5	pF
	Drive level (max)				0.8	mW

REVISION HISTORY

Changes from Original (January 2014) to Revision A	Page
• Deleted ORDERING INFORMATION table	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB9261IPAPQ1	ACTIVE	HTQFP	PAP	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB9261IQ1	Samples
TUSB9261IPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TUSB9261IQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TUSB9261-Q1 :

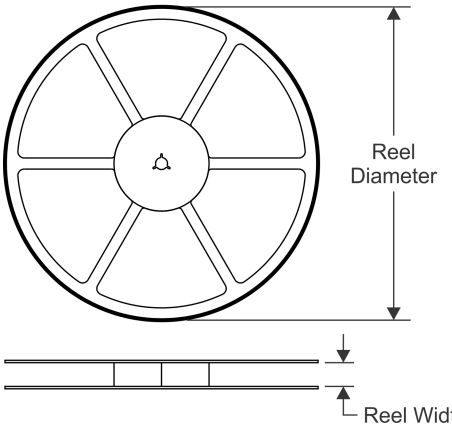
- Catalog: TUSB9261

NOTE: Qualified Version Definitions:

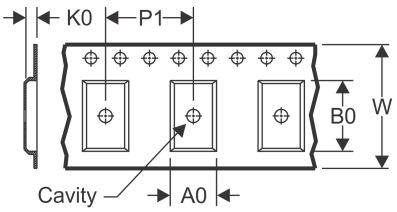
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

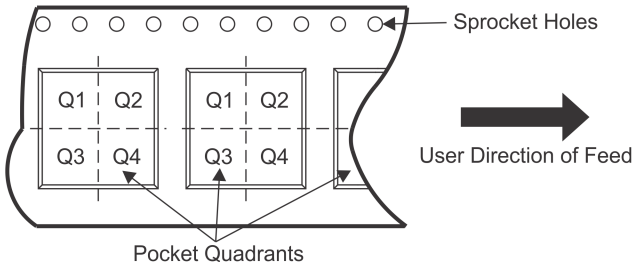


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

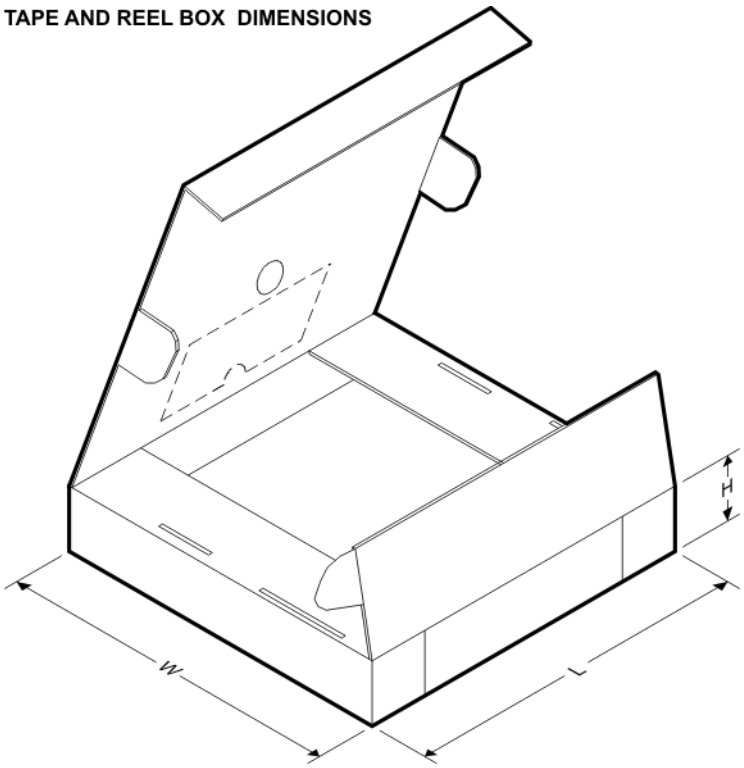
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB9261IPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

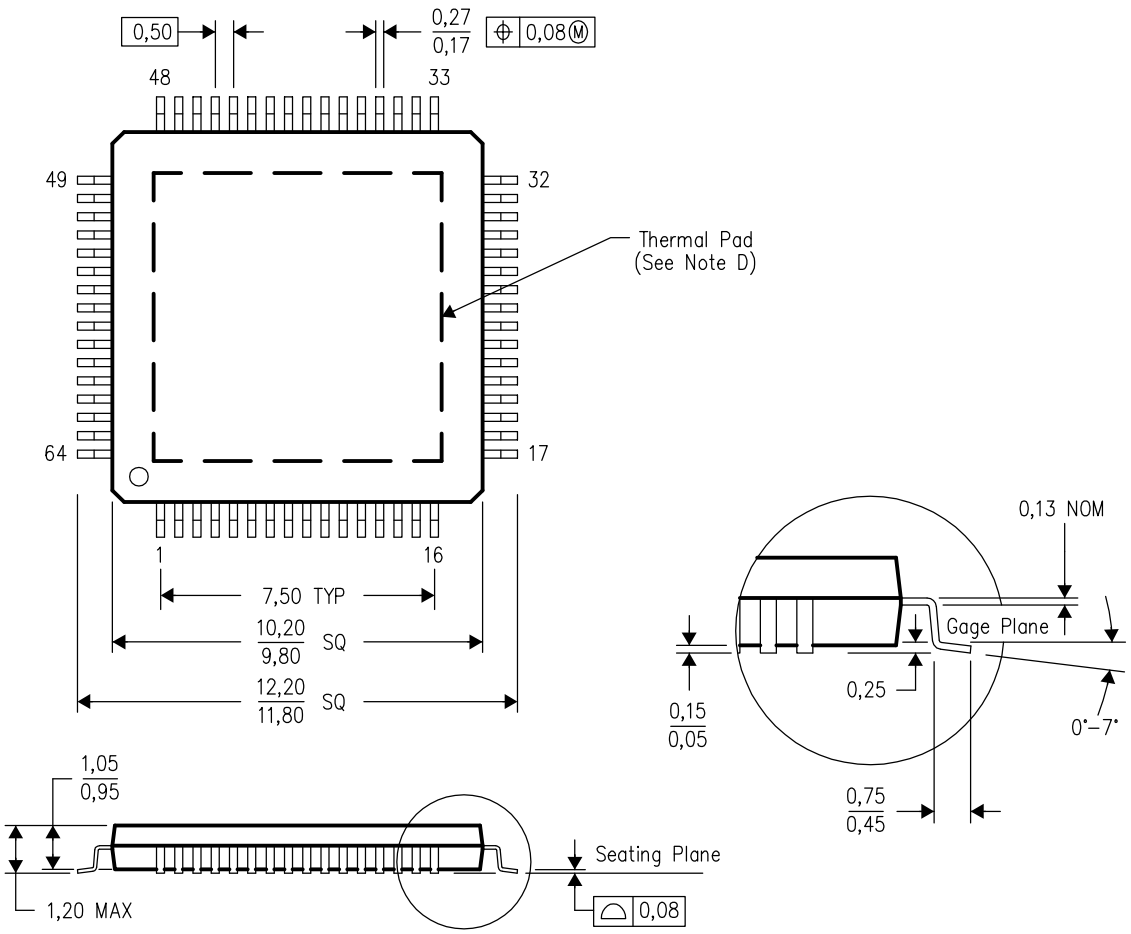
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB9261IPAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	55.0

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

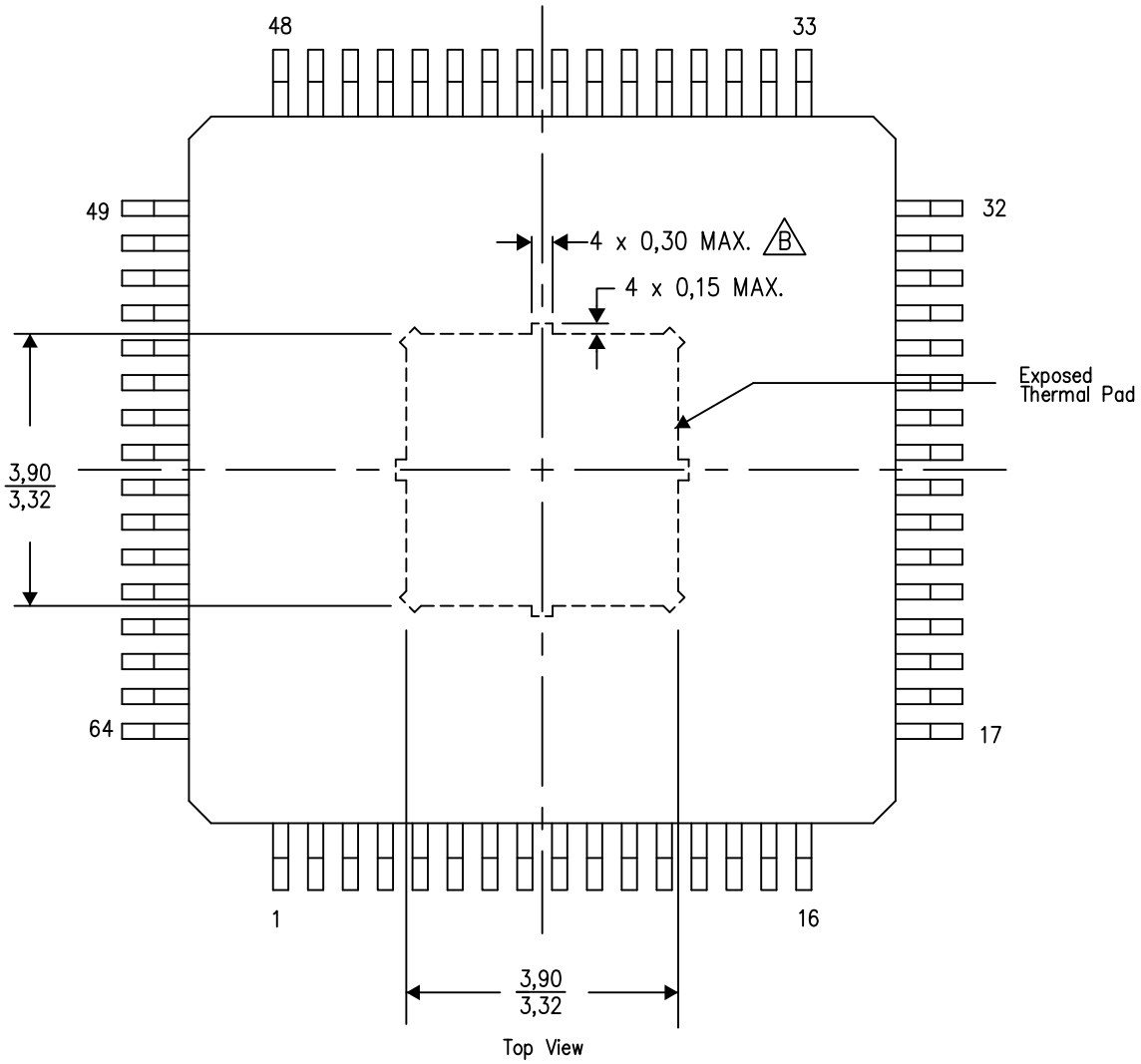
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

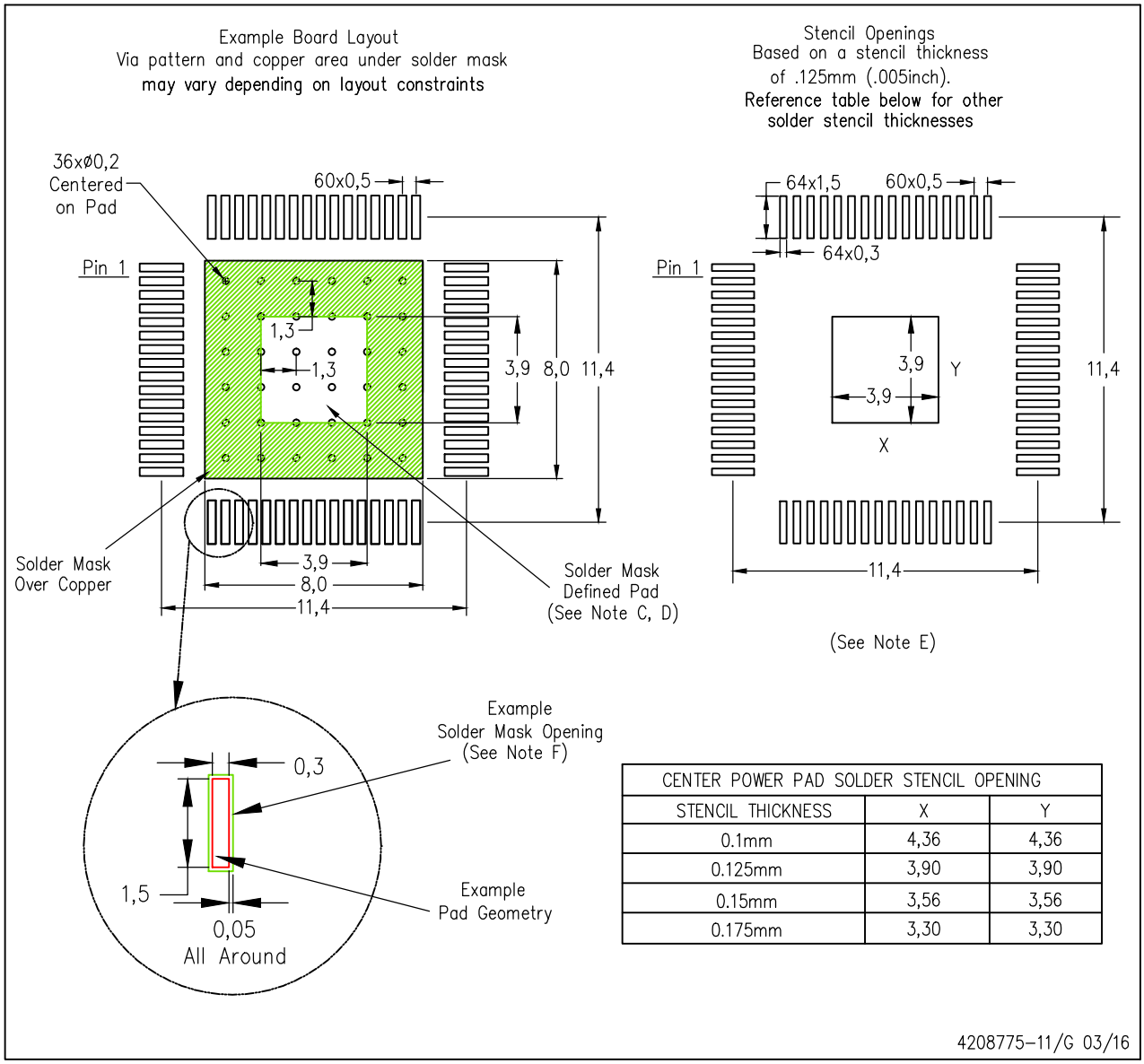
4206326–12/P 05/14

NOTES: A. All linear dimensions are in millimeters

B. Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	4,36	4,36
0.125mm	3,90	3,90
0.15mm	3,56	3,56
0.175mm	3,30	3,30

4208775–11/G 03/16

PowerPAD is a trademark of Texas Instruments

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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