

TPS92411x Floating Switch for Offline AC Linear Direct Drive of LEDs with Low Ripple Current

1 Features

- High-Performance Solution for Driving LEDs from AC Mains
- Simplifies Design of Phase Dimmable LED Driver with High Power Factor, Low Total Harmonic Distortion, and Low Current Ripple
- Suitable for LED Luminaires up to 70+ W
- Input Voltage Range: 7.5 V to 100 V
- Stackable 100 V, 2-Ω MOSFET Building Block
- Controlled Switch Open and Close Transitions Minimize EMI
- Designed for use with the [TPS92410](#) or with a Discrete Linear Regulator
- Input Undervoltage Protection
- Output Overvoltage Protection (TPS92411P)
- Low I_Q : 200 μ A (typ)

2 Applications

- LED Lamps and Light Bulbs
- LED Luminaires
- Downlights

3 Description

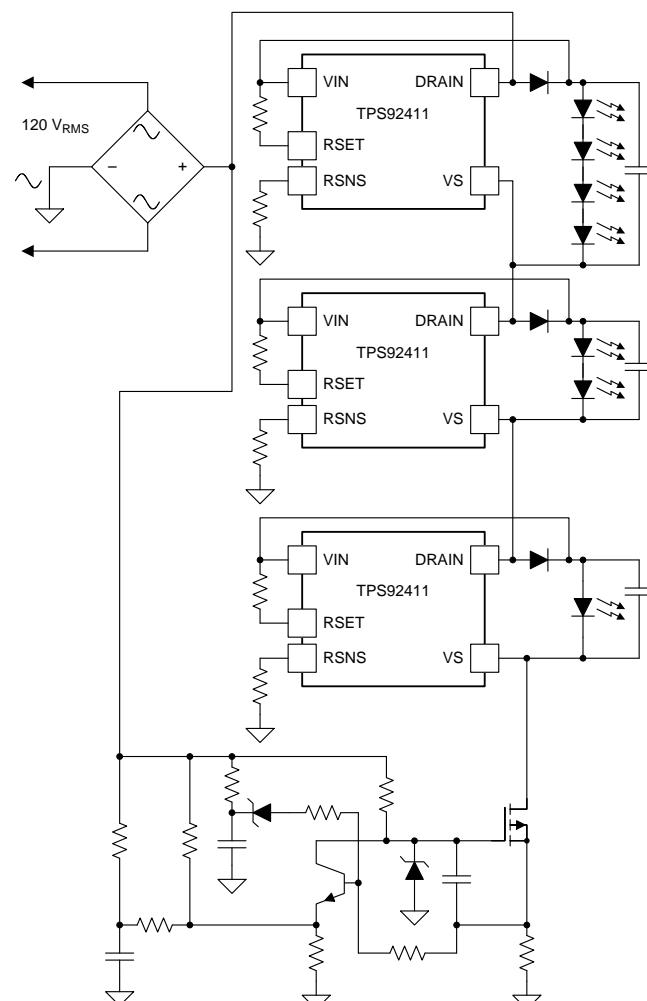
The TPS92411 is a 100-V floating MOSFET switch for use in offline LED lighting applications. The device is used in conjunction with a current regulator that can achieve a power factor greater than 0.9 to create a LED drive solution with low-ripple current. When properly designed, solution performance is comparable to traditional flyback, buck or boost-based AC/DC LED drivers. The approach requires no inductive components, thus saving size and cost. Slew-controlled low-frequency operation of the TPS92411 switches creates very little EMI. Detailed operation is described in the [Application Information](#) section.

Package options include SOT23-5 and PSOP-8 allowing the user to optimize for small size or scale for high power. Using the PSOP-8 package, design of LED luminaires up to 70 W or more is possible. Other features include a UVLO circuit to monitor when the device has sufficient voltage to operate properly and over-voltage protection (TPS92411P).

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS92411, TPS92411P	SOT-23 (5)	2.90 mm x 1.60 mm
	SO PowerPAD (8)	4.89 mm x 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



An **IMPORTANT NOTICE** at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. **PRODUCTION DATA**.

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4 Revision History

Changes from Revision A (May 2014) to Revision B	Page
<ul style="list-style-type: none"> Added <i>Pin Configuration and Functions</i> section, <i>Handling Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 	1

Changes from Original (October 2013) to Revision A	Page
Deleted preview designation for DDA package.....	3
Added availability information for DDA package	3

5 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	DDA	DBV		
DRAIN	8	4	O	Drain of the internal switch.
N/C	2			Not internally connected.
N/C	6	—	—	
N/C	7			
VIN	1	3	I	Positive power supply for the device.
VS	4	2	I/O	Source of the internal switch. This pin is also the device floating ground.
RSET	3	1	I/O	A resistor connected between the RSET pin and the VIN pin sets the rising threshold to open the switch.
RSNS	5	5	I/O	A resistor connected between the RSNS pin to system ground senses the VS voltage relative to system ground.
Exposed Thermal Pad				Connect to VS pin directly beneath the device.

6 Specifications

6.1 Absolute Maximum Ratings

All voltages are with respect to VS, $-40^{\circ}\text{C} < T_J = T_A \leq 150^{\circ}\text{C}$. All currents are positive into and negative out of the specified terminal (unless otherwise noted).

		MIN	MAX	UNIT
Supply voltage	VIN	-0.3	105	V
Switch voltage	DRAIN	-0.3	105	
Junction temperature	T _J	-40	165	°C

6.2 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature range	-65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾		1
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾		250

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
VIN	Input voltage	TPS92411P	7.5	94		V
		TPS92411	7.5	100		
T _J	Operating junction temperature		-40	25	150	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	TPS92411		UNIT
	DBV	DDA	
	5 PINS	8 PINS	
θ _{JA} Junction-to-ambient thermal resistance ⁽²⁾	209.8	58.6	°C/W
θ _{JCtop} Junction-to-case (top) thermal resistance ⁽³⁾	125.2	72	
θ _{JB} Junction-to-board thermal resistance ⁽⁴⁾	38	39.1	
Ψ _{JT} Junction-to-top characterization parameter ⁽⁵⁾	15.6	21.6	
Ψ _{JB} Junction-to-board characterization parameter ⁽⁶⁾	37.1	39.1	
θ _{JCbot} Junction-to-case (bottom) thermal resistance ⁽⁷⁾	N/A	15	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specified JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, θ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, θ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics

Unless otherwise specified $-40^{\circ}\text{C} \leq T_J = T_A \leq 150^{\circ}\text{C}$, $(V_{\text{VIN}} - V_{\text{VS}}) = 30\text{ V}$, $R_{\text{RSET}} = R_{\text{RSNS}} = \text{Open}$, all voltages are with respect to VS.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VIN)						
V _{IN(ovp)}	Input overvoltage protection	Rising threshold	95	100		V
		Falling threshold		96		
		Hysteresis		4		
I _Q	Bias current		200	400		µA
V _{IN(uvlo)}	Input undervoltage lockout	Rising threshold	6.5	7		V
V _{IN(hys)}	Input UVLO hysteresis		370			mV
SWITCH CONTROL (RSNS, RSET)						
I _{RSNS}	RSNS threshold current		-3.3	-4	-4.9	µA
V _{RSNS_OS}	RSNS offset voltage		165	210	255	mV
V _{RSET}	RSET threshold voltage		1.2	1.25	1.3	V
I _{RSET}	RSET current	I _{RSNS} = -20 µA, $(V_{\text{RSET}} - V_{\text{VS}}) = 1.5\text{ V}$	-9.3	-10	-10.7	µA
		I _{RSNS} = -40 µA, $(V_{\text{RSET}} - V_{\text{VS}}) = 1.5\text{ V}$	-19	-20	-21	
		I _{RSNS} = -100 µA, $(V_{\text{RSET}} - V_{\text{VS}}) = 1.5\text{ V}$	-47.9	-50	-52.1	
SWITCH (DRAIN, VS)						
R _{DS(on)}	On-resistance	I _{DRAIN} = 100 mA, T _J = 25°C	1	2	2.5	Ω

Electrical Characteristics (continued)

Unless otherwise specified $-40^{\circ}\text{C} \leq T_J = T_A \leq 150^{\circ}\text{C}$, $(V_{\text{VIN}} - V_{\text{VS}}) = 30\text{ V}$, $R_{\text{RSET}} = R_{\text{RSNS}} = \text{Open}$, all voltages are with respect to V_{S} .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$dv/dt_{(\text{ON})}$	$(V_{\text{DRAIN}} - V_{\text{VS}})$ falling 36 V to 4 V, $I_{\text{SW}} = 100\text{ mA}$		1		$\text{V}/\mu\text{s}$
$dv/dt_{(\text{OFF})}$	$(V_{\text{DRAIN}} - V_{\text{VS}})$ rising 4 V to 36 V, $I_{\text{SW}} = 100\text{ mA}$		0.5		

6.6 Typical Characteristics

Unless otherwise stated, $-40^{\circ}\text{C} \leq T_A = T_J \leq 150^{\circ}\text{C}$, $(V_{\text{VIN}} - V_{\text{VS}}) = 30\text{ V}$, all voltages are with respect to VS.

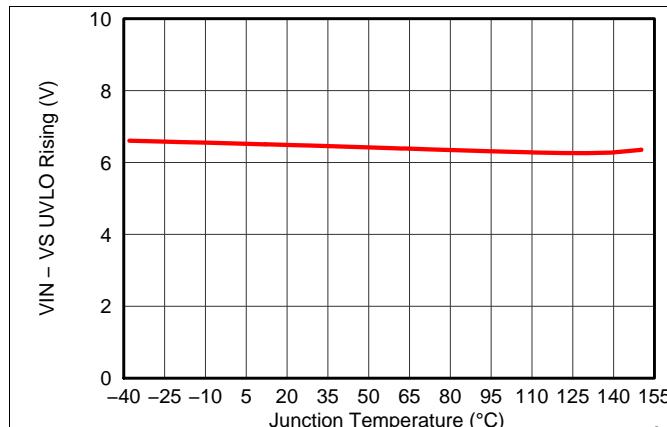


Figure 1. UVLO vs. Temperature

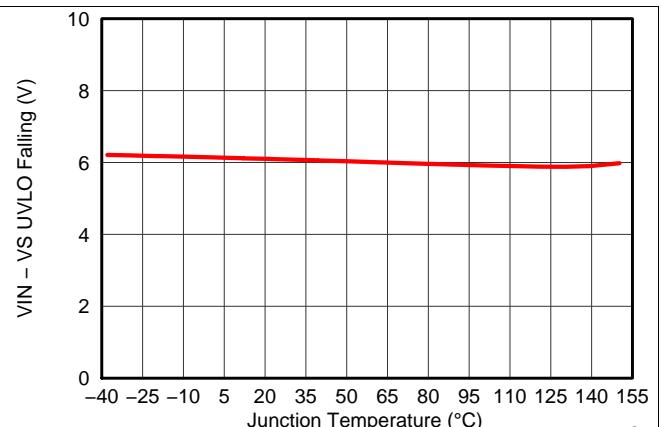


Figure 2. UVLO vs. Temperature

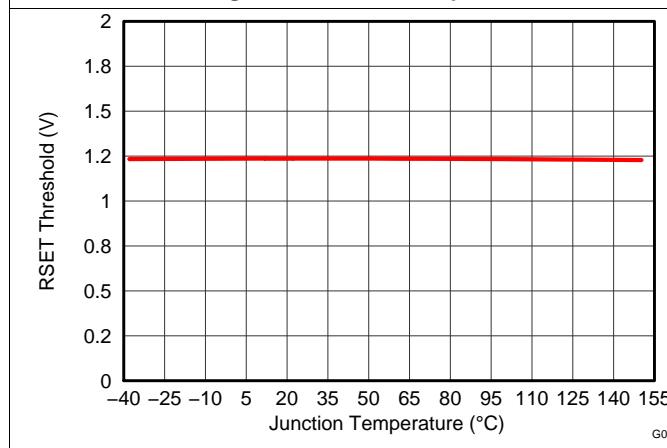


Figure 3. RSET Threshold vs. Temperature

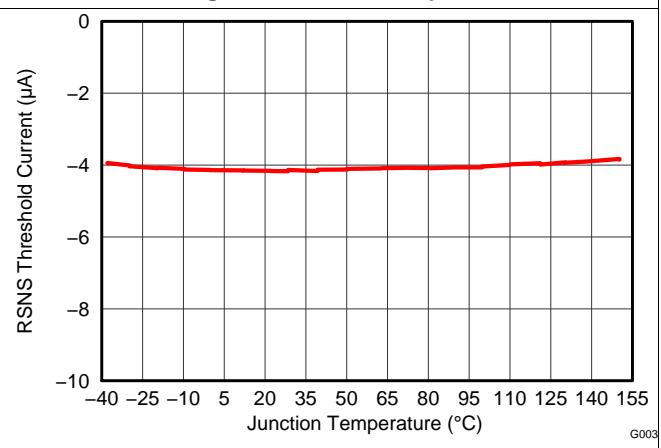


Figure 4. RSNS Threshold Current vs. Temperature

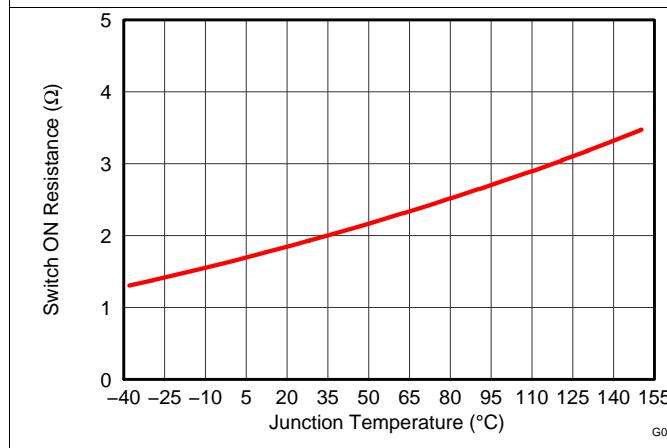
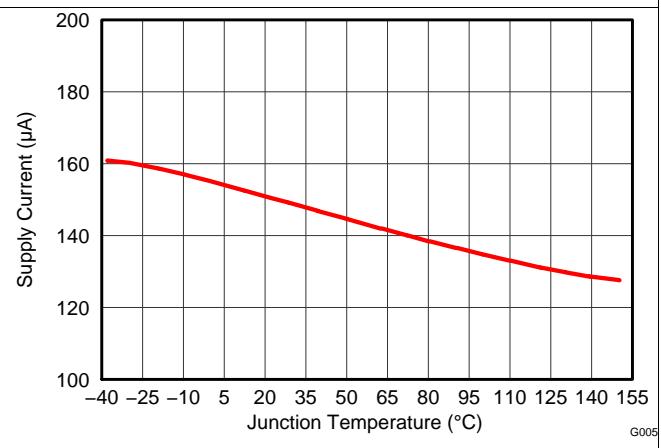
Figure 5. Switch On-Resistance (R_{DS(on)}) vs. Temperature

Figure 6. Input Voltage Quiescent Current vs. Temperature

Typical Characteristics (continued)

Unless otherwise stated, $-40^{\circ}\text{C} \leq T_A = T_J \leq 150^{\circ}\text{C}$, $(V_{\text{VIN}} - V_{\text{VS}}) = 30\text{ V}$, all voltages are with respect to VS .

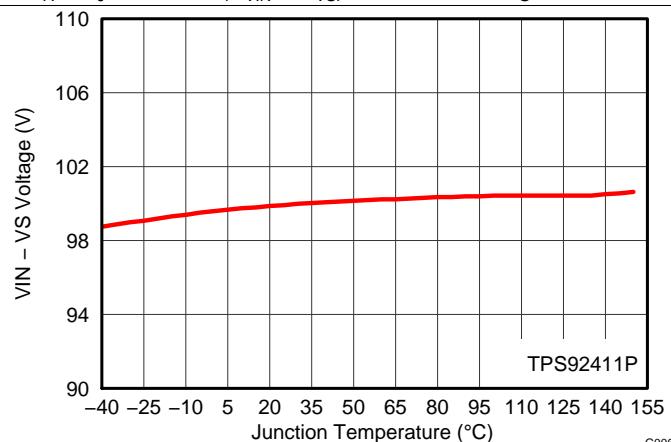


Figure 7. $(V_{\text{VIN}} - V_{\text{VS}})$ Overvoltage Threshold vs. Temperature

7 Detailed Description

7.1 Overview

The TPS92411 is an advanced, floating driver specifically designed for use with a linear regulator in low-power offline LED lighting applications. It integrates an on-board 100-V MOSFET switch to shunt LED current as the line transitions. As the line transitions through the cycle, the device monitors critical nodes for zero cross at which time the internal switch is either opened or shorted to steer the current through or away from the LED stack. The TPS92411 does not directly control output power or LED current, it just directs current to the LED stack or bypasses the LED stack.

7.2 Functional Block Diagram

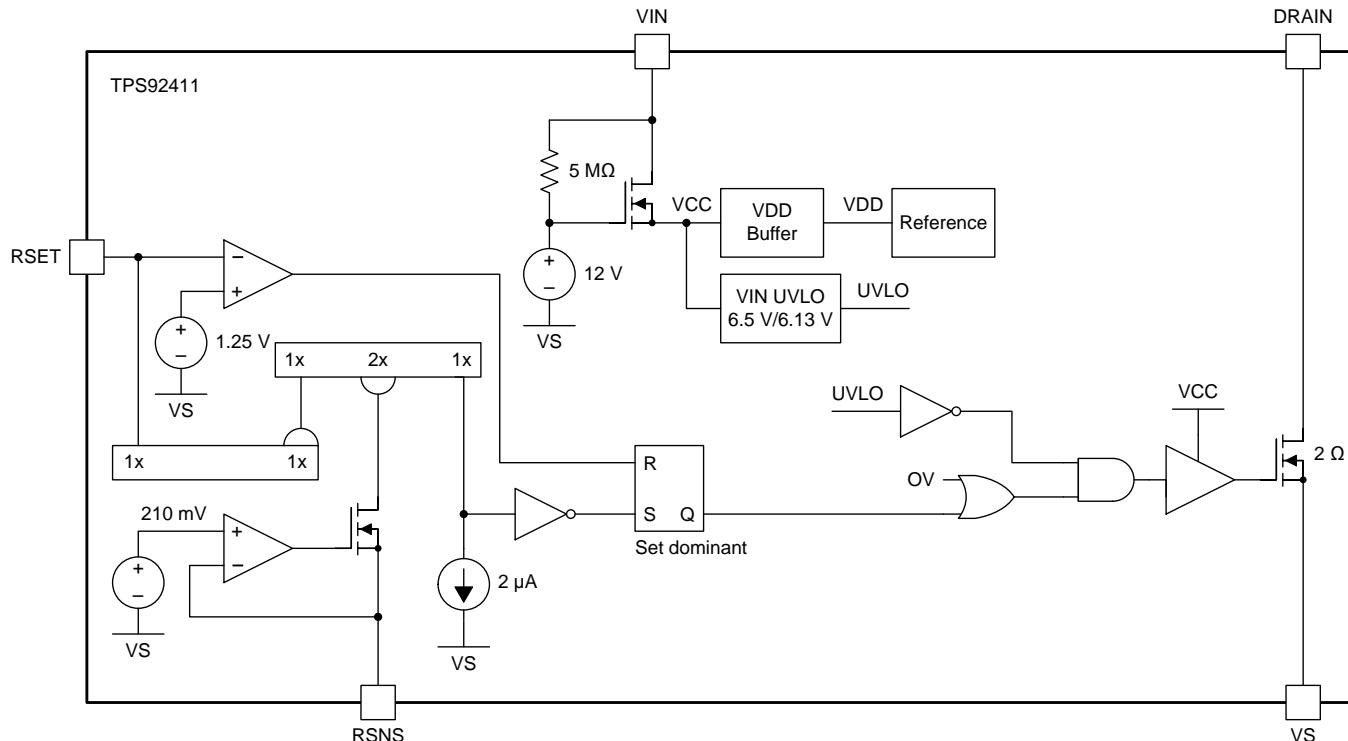


Figure 8. TPS92411 Block Diagram

Functional Block Diagram (continued)

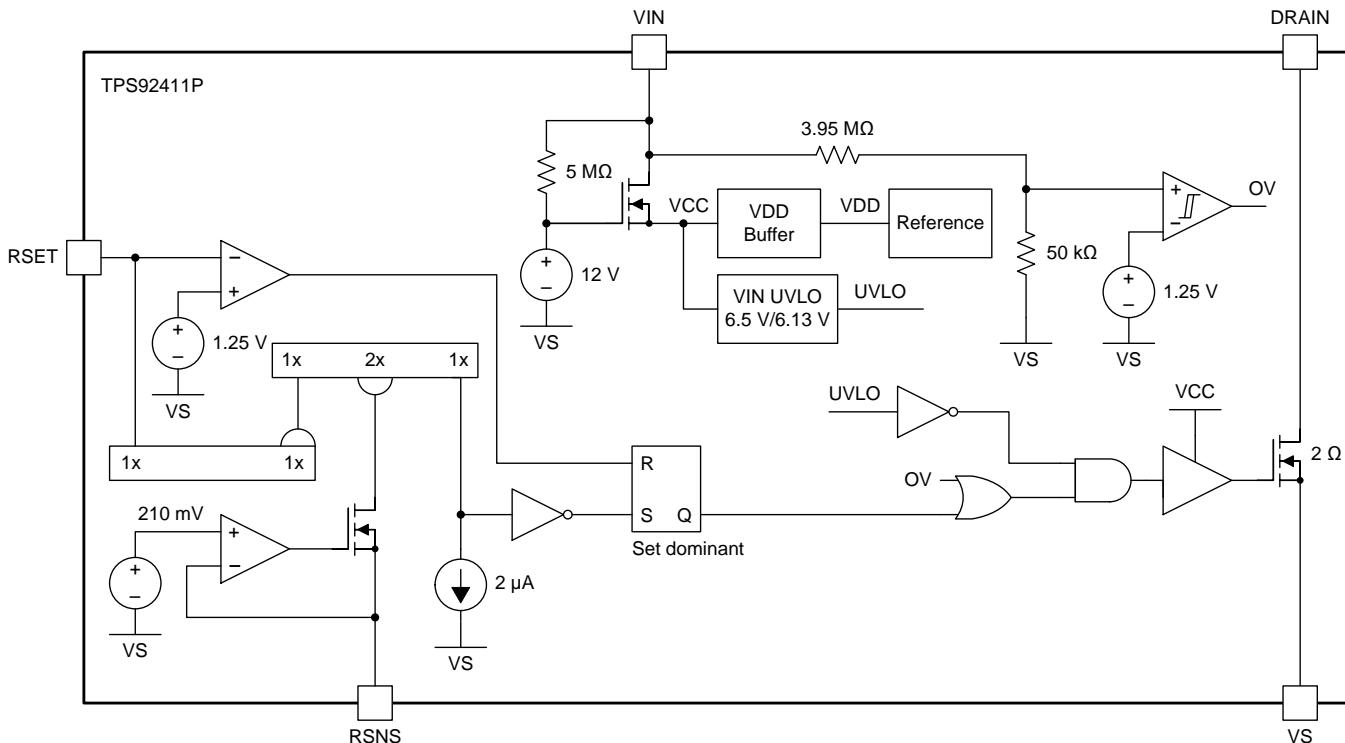


Figure 9. TPS92411P Block Diagram

7.3 Feature Description

7.3.1 Overvoltage Protection (OVP)

Overvoltage protection (OVP) in the TPS92411P version protects the device as well as the LEDs and storage capacitor. The OVP is set at approximately 100 V ($V_{VIN} - V_{VS}$) and closes the internal switch when the threshold voltage is reached. For this reason LED stack voltages of 94 V or less are recommended. Higher voltages can be used with the TPS92411 version but tolerances must be considered to ensure that the 105 V absolute maximum rating is not exceeded.

7.3.2 Input Undervoltage Lockout (UVLO)

The TPS92411 includes input UVLO. The UVLO prevents the device from operation until the VIN pin voltage with respect to VS exceeds 6.5 V and ensures the device behaves properly when enabled.

7.3.3 LED Capacitor

A capacitor is required across each LED stack to provide current to the LEDs during the switch ON time. Refer to the available calculator software (SLVC516 for 120-V applications or SLVC517 for 230-V applications) for calculating the minimum value required for any particular application. The software calculates the minimum value required for a particular application, but best performance is achieved by using as much capacitance as possible given size and cost constraints. These design tools also calculate a minimum value for any given current ripple percent or flicker index desired for the particular application.

7.3.4 Blocking Diode

A blocking diode is required between the drain of the switch (DRAIN) and the anode of the LED stack. This prevents the LED capacitor from discharging through the switch during the switch ON time instead allowing it to discharge through the LED stack. This diode should be rated for 200 V reverse voltage and capable of forward currents as high as the average linear regulator current setting.

7.4 Device Functional Modes

The TPS92411P has 4 functional modes while the TPS92411 has 3:

7.4.1 Input UVLO

As described in the previous section the device and internal switch will remain off until VIN is 6.5V or greater with respect to VS.

7.4.2 Operating with Internal Switch ON

After the device crosses the UVLO threshold the internal switch will turn on and remain on until the voltage at the VIN pin exceeds the threshold voltage set by the RSET resistor.

7.4.3 Operating with Internal Switch OFF

When the RSET threshold voltage is exceeded on the VIN pin the internal switch will turn off forcing all the current to flow through the LEDs and charge the LED capacitor. The switch will remain off until the VS pin drops below the threshold voltage set by RSNS or an overvoltage event occurs (TPS92411P only).

7.4.4 Overvoltage Operation (TPS92411P)

If an LED fails open or a string voltage exceeding the OVP level is used the device will enter OVP operation. The internal switch will close and remain closed until the VIN voltage with respect to the VS pin drops low enough to engage normal operation again.

8 Application and Implementation

8.1 Application Information

The TPS92411 is an advanced, floating driver specifically designed for use with a linear regulator in low-power offline LED lighting applications. It integrates an on-board 100-V MOSFET switch to shunt LED current as the line transitions. As the line transitions through the cycle, the device monitors critical nodes for zero cross at which time the internal switch is either opened or shorted to steer the current through or away from the LED stack. Use the following design procedure to select components for the TPS92411. The following calculators may also be used to select components for the TPS92411:

- [SLVC579](#) for 120-V applications using the TPS92410
- [SLVC580](#) for 230-V applications using the TPS92410
- [SLVC516](#) for 120-V applications using a discrete linear regulator
- [SLVC517](#) for 230-V applications using a discrete linear regulator

PSpice and TINA-TI models are also available. The following are typical applications using the TPS92411 for both 120-V and 230-V applications using a discrete linear regulator.

8.2 Typical Application

8.2.1 120-VAC, Phase Dimmable 11.5-W Input with Discrete Linear Regulator

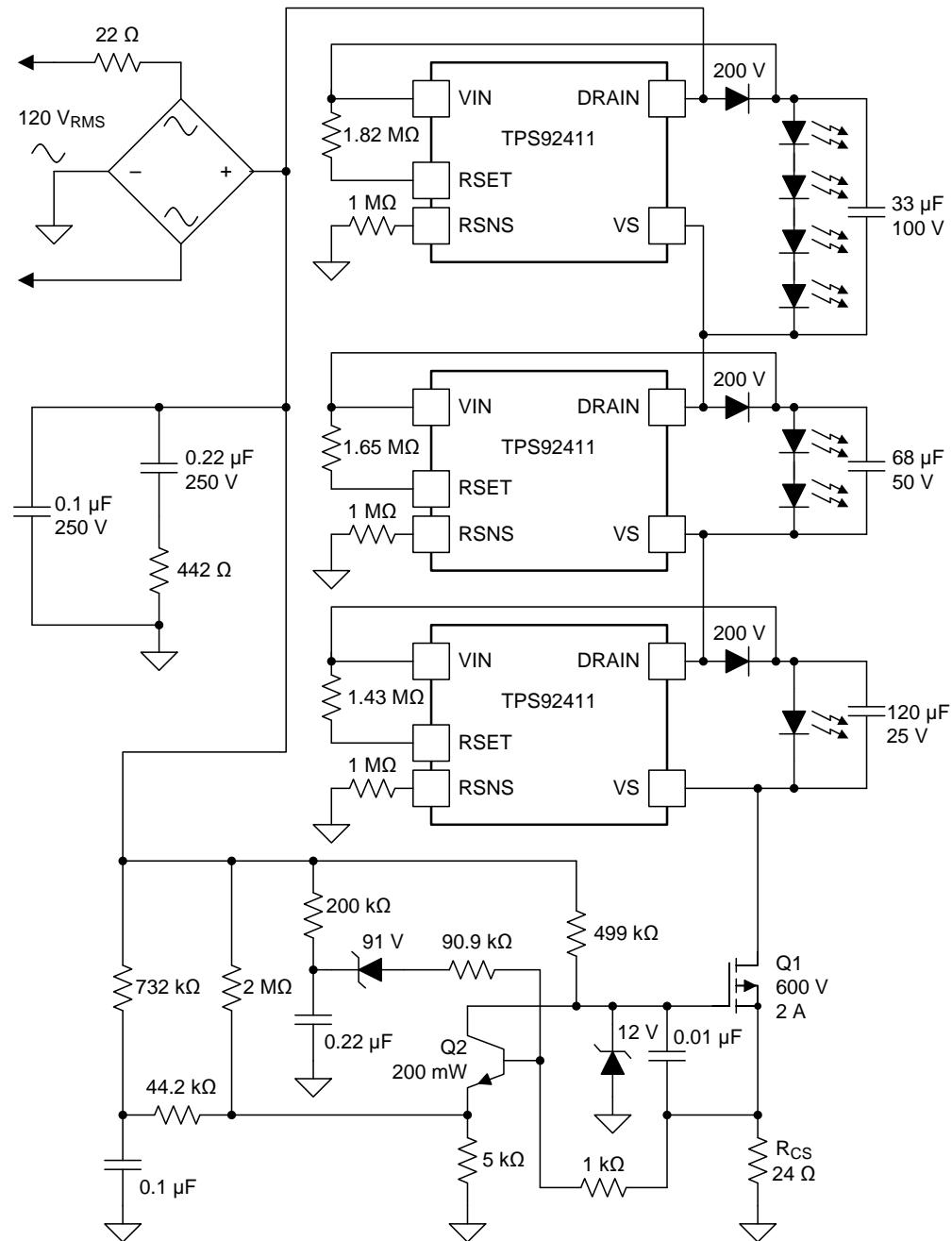


Figure 10. 120-VAC, Phase Dimmable 11.5-W Input with Discrete Linear Regulator

8.2.1.1 Design Requirements

For the 120-V application shown in Figure 10 the highest efficiency is obtained by using a high-voltage total LED stack to reduce losses in the linear regulator FET. The best current sharing efficiency between stacks can be achieved by using the lowest voltage stack at the bottom and making each stack voltage above 2 times the voltage of the stack below it. In this example 20-V LEDs are used. This effectively gives the lowest stack a total of 20 V, the middle stack a total of 40 V, and the upper stack a total of 80 V. The RSNS resistor is used to set a

Typical Application (continued)

low voltage point so that when the VS pin voltage falls below this threshold (either from the AC line falling or a higher voltage stack switch above it turning OFF) the TPS92411 switch turns ON and bypasses the LEDs. During the ON-time, the LEDs are supplied current from the capacitor. The RSET voltage is used to set a threshold to detect when the input voltage crosses this threshold it turns OFF the switch and allows the LEDs to conduct current from the line and charge the bypass capacitor.

8.2.1.2 Detailed Design Procedure

- Set V_{RSNS} for all three TPS92411 devices at 4 V
- Set V_{RSET} for the bottom stack at 26 V (20 V stack plus 6 V headroom)
- Set V_{RSET} for the middle stack at 46 V (40 V stack plus 6 V headroom)
- Set V_{RSET} for the top stack at 86 V (80 V stack plus 6 V headroom)

Switching order as the rectified AC line voltage increases is shown in [Table 1](#). [Figure 11](#) illustrates when each switch turns ON or OFF.

8.2.1.2.1 Setting the Switching Thresholds (RSNS, RSET)

The TPS92411 features two threshold settings to allow for proper LED control. The first setting determines when the internal switch turns off and allows current to charge the capacitor and flow through the LEDs. The second setting determines when the switch turns on to shunt the LEDs and allow the capacitor to supply current. The lower switch turn-on threshold (V_{SNS}) should be set first using a resistor (R_{RSNS}) from the RSNS pin to system ground. For best efficiency set this threshold between 4 V and 6 V. Then the upper switch turn-off threshold (V_{VS}) can be set using a resistor (R_{RSET}) from the RSET pin to the VIN pin. Set this threshold approximately 6 V to 10 V above the LED stack voltage (V_{LED}). The RSET threshold should be greater than the LED stack voltage plus the value of the RSNS threshold to prevent errant switching. These thresholds can be set with resistance calculated using [Equation 1](#) and [Equation 2](#).

$$R_{RSNS} = \frac{V_{SNS} + 0.21V}{|I_{RSNS}|} \quad (1)$$

$$R_{RSET} = \frac{(V_{LED} - 1.24V) \times 2 \times R_{RSNS}}{V_{VS} + 0.21V} \quad (2)$$

Table 1. Switching Order on Rising Edge of Rectified 120-VAC ⁽¹⁾⁽²⁾

STACK		
TOP 80-V	MIDDLE 40-V	BOTTOM 20-V
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

(1) 0 denotes switch ON and LEDs bypassed and supplied by the capacitor.

(2) 1 denotes switch OFF and LEDs conducting from the line, capacitor charging up.

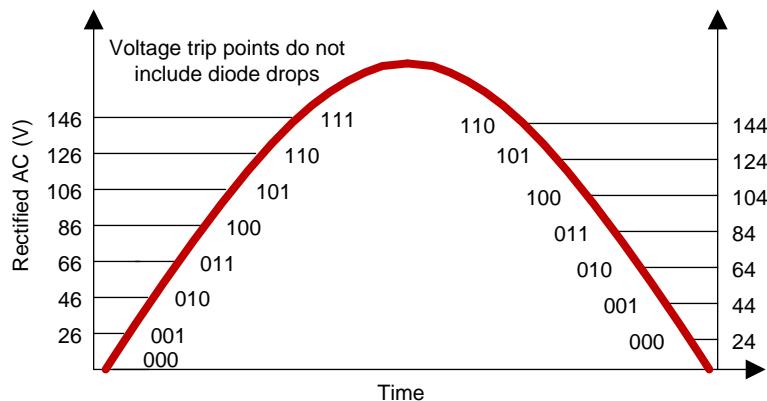


Figure 11. Switching Order on Rectified 120-VAC Waveform

The linear regulator in Figure 11 generates a current sense RMS voltage of approximately 2.3 V. The linear regulator RMS current is equal to the input current drawn from the AC line. For example, for a 11.5-W input power system the input current should be approximately 0.095 A and a 24- Ω resistor should be chosen for RCS. Other input power levels (P_{IN}) can be obtained using Equation 3.

$$R_{CS} = \frac{120 V_{RMS} \times 2.3 V_{RMS}}{P_{IN}} \quad (3)$$

8.2.1.3 Application Curve

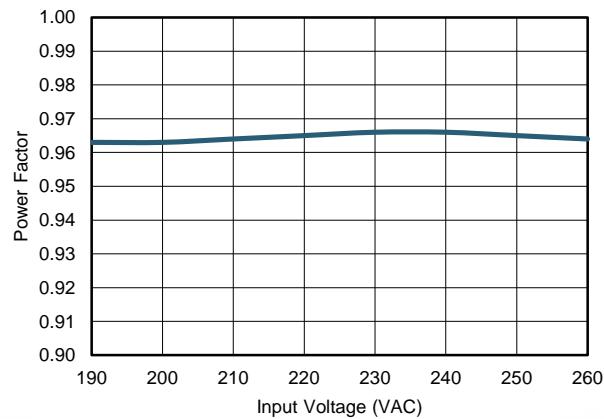


Figure 12. Power Factor vs. Input Voltage

8.2.2 230-VAC, Phase Dimmable 16-W Input with Discrete Linear Regulator

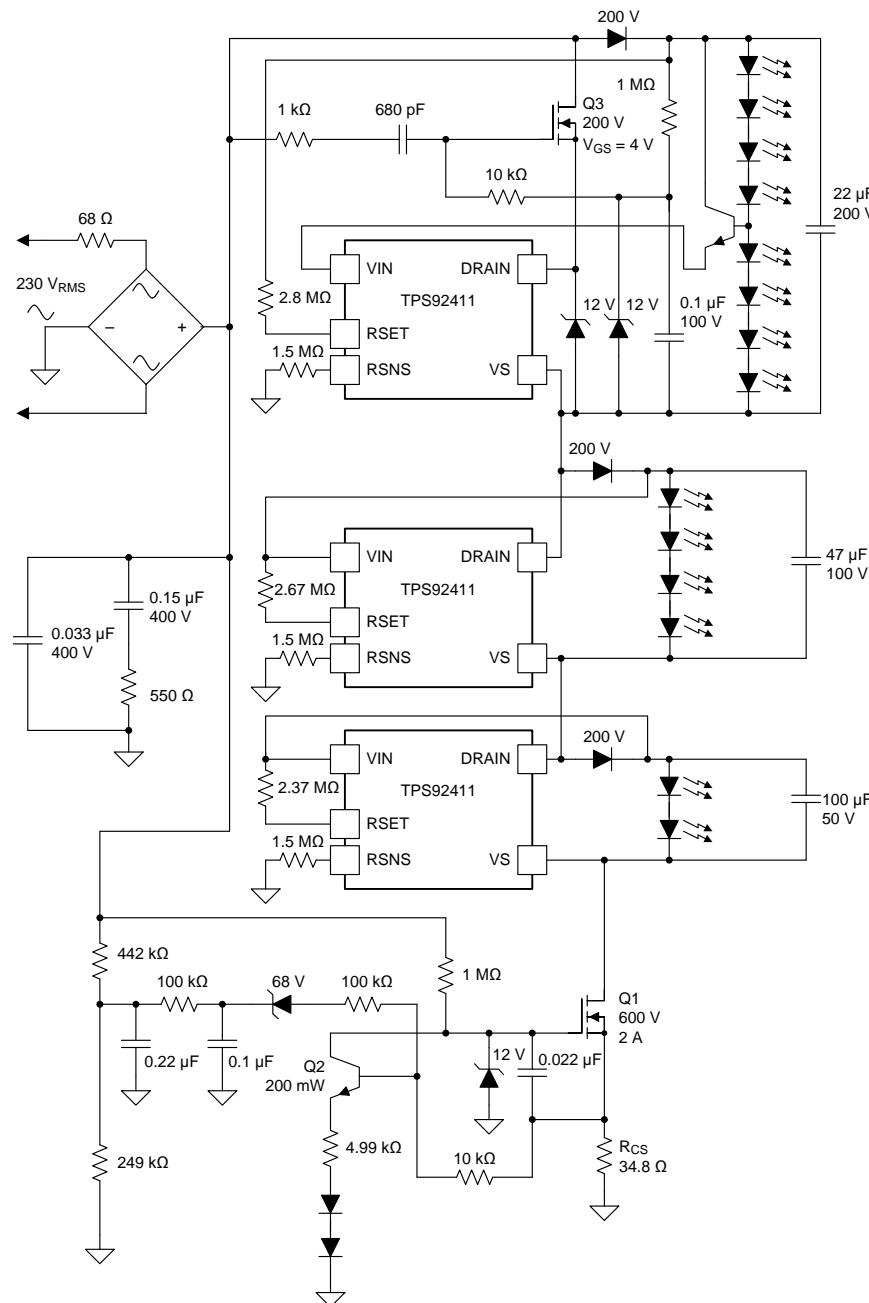


Figure 13. 230-VAC, Phase Dimmable 16-W Input with Discrete Linear Regulator

8.2.2.1 Design Requirements

In the 230-V application shown in [Figure 13](#), the highest efficiency can be obtained by using a high-voltage total LED stack to reduce losses in the linear regulator FET. The best current sharing between stacks can be achieved by using the lowest voltage stack at the bottom and making each stack voltage above that two times that of the stack below it (as in described in the 120-V application). In this example, very good results can be obtained by setting the lowest stack at 40 V, the middle stack at 80 V, and adding a high-voltage cascode FET with the top stack and using 160 V. Use the RSNS pin to set a low voltage point so that when the VS pin of the

device falls below this threshold (either from the AC line falling or a higher voltage stack switch above it turning OFF) the TPS92411 switch turns ON and bypasses the LEDs. During the ON-time, the capacitor supplies current to the LEDs. The RSET voltage threshold for a 230-V application is generally set to approximately 8 V to 12 V above the LED stack voltage connected across the TPS92411 (for an RSNS voltage of 6 V). This threshold is higher than in the typical 120-V application to allow more headroom.

8.2.2.2 Detailed Design Procedure

- Set V_{RSNS} for all three TPS92411 devices at 6 V
- Set V_{RSET} for the bottom stack at 49 V (40 V stack plus 9 V headroom)
- Set V_{RSET} for the middle stack at 89 V (80 V stack plus 9 V headroom)
- Set V_{RSET} for the top stack at 169 V (160 V stack plus 9 V headroom)

Switching order as the rectified AC line voltage increases is shown in [Table 2](#). [Figure 14](#) illustrates when each switch turns ON or OFF.

Table 2. Switching Order on Rising Edge of the Rectified 230-VAC Waveform⁽¹⁾⁽²⁾

STACK		
TOP 160-V	MIDDLE 80-V	BOTTOM 40-V
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

(1) 0 denotes switch ON and LEDs bypassed and supplied by the capacitor.

(2) 1 denotes switch OFF and LEDs conducting from the line, capacitor charging up.

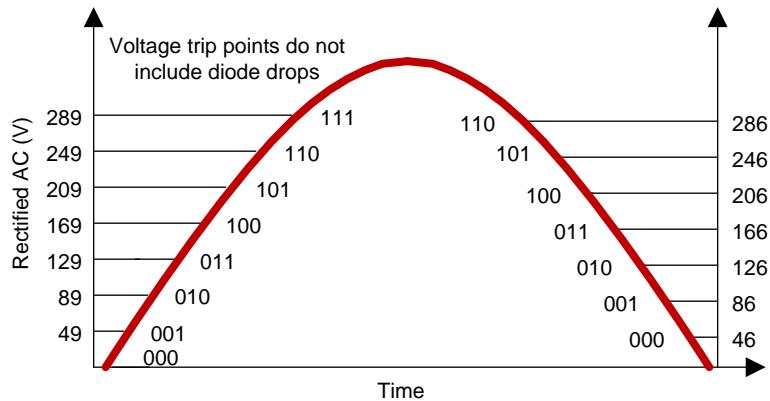


Figure 14. Switching Order on Rising Edge of the Rectified 230-VAC Waveform

The linear regulator in [Figure 14](#) generates a current sense RMS voltage of 2.44 V. The linear regulator RMS current is equal to the input current drawn from the AC line. For example, for a 16-W input power system the input current should be approximately 0.07 A and a 34.8- Ω resistor should be chosen for R_{CS} . Other input power levels (P_{IN}) can be calculated using [Equation 4](#).

$$R_{CS} = \frac{230 V_{RMS} \times 2.44 V_{RMS}}{P_{IN}} \quad (4)$$

8.2.2.3 Application Curve

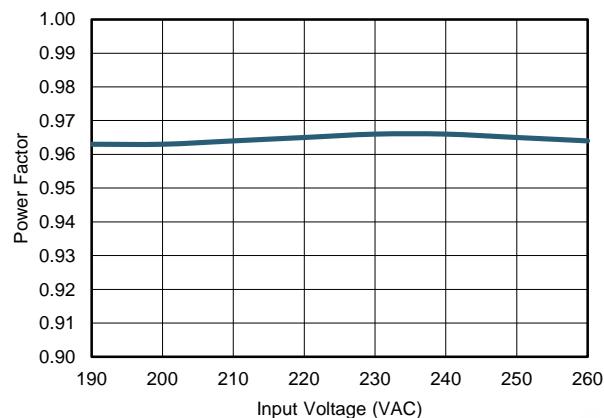


Figure 15. Power Factor Input Voltage

9 Power Supply Recommendations

For testing purposes any benchtop adjustable AC power supply with a power rating higher than what is required by the circuit is suitable. An example would be an Hewlett Packard 6811B or equivalent. An isolated supply is recommended for safety purposes.

10 Layout

10.1 Layout Guidelines

The TPS92411 allows for a simple layout, however some considerations should be taken. The RSET resistor should be connected directly between the RSET pin and VIN pin as close to the device as possible. The trace between the resistor and the RSET pin should be as short as possible. The trace from the RSNS pin to the RSNS resistor should also be as short as possible to minimize parasitic capacitances. The blocking diode should be placed between the DRAIN pin and the VIN pin and also located close to the device. Placement of the LED capacitor may depend on the physical design of the application, however it should be placed as close to the TPS92411 as the design allows to minimize parasitic inductances.

10.2 Layout Example

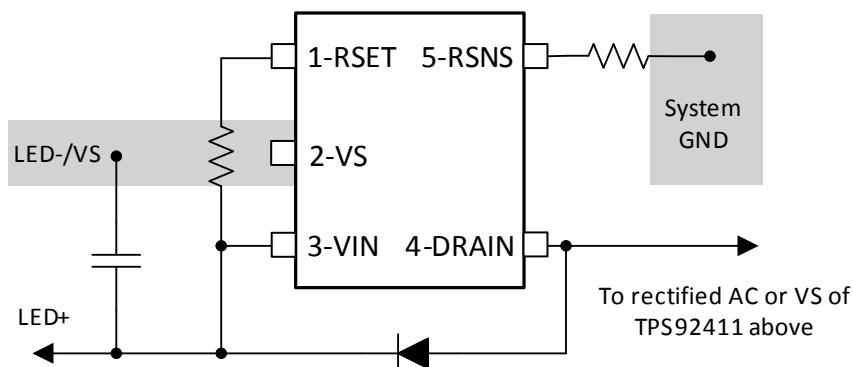


Figure 16. Recommended Component Placement (DBV)

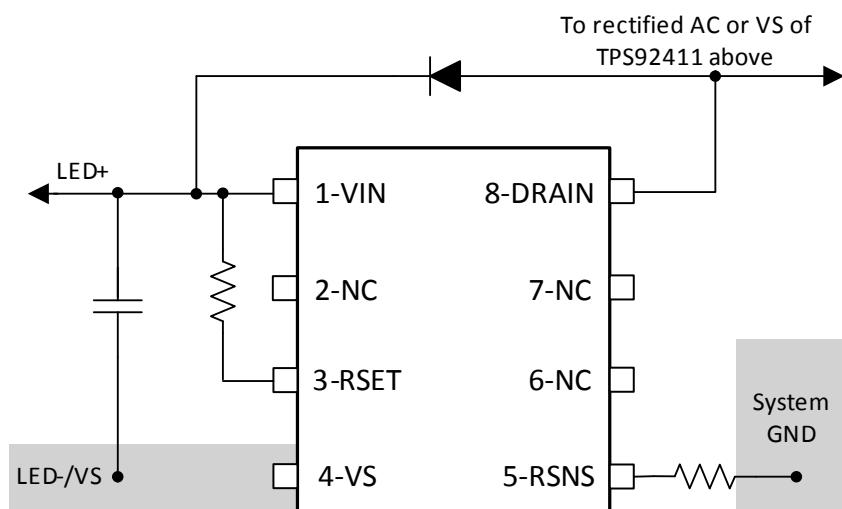


Figure 17. Recommended Component Placement (DDA)

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS92411	Click here				
TPS92411P	Click here				

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022 — TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92411DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	PB9Q	Samples
TPS92411DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	PB9Q	Samples
TPS92411DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	92411	Samples
TPS92411DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	92411	Samples
TPS92411PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	PB8Q	Samples
TPS92411PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 150	PB8Q	Samples
TPS92411PDAA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	92411P	Samples
TPS92411PDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 150	92411P	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

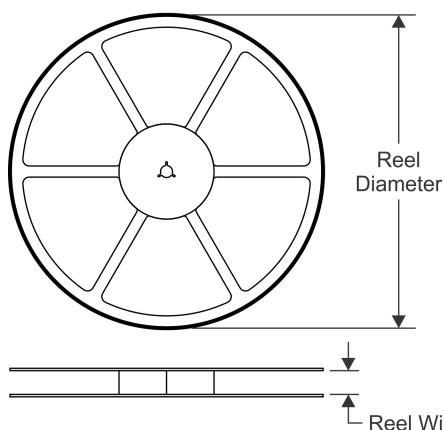
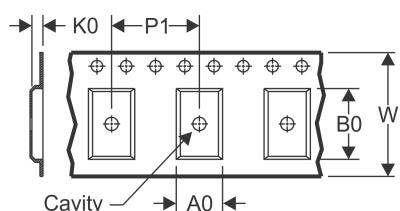
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

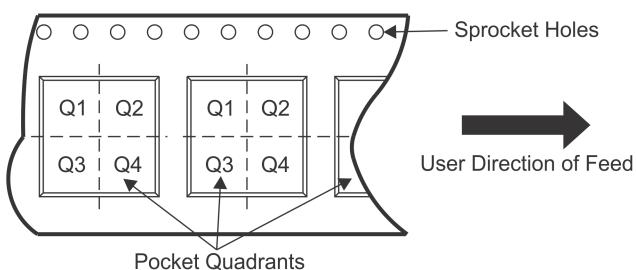
-
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
 - (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
 - (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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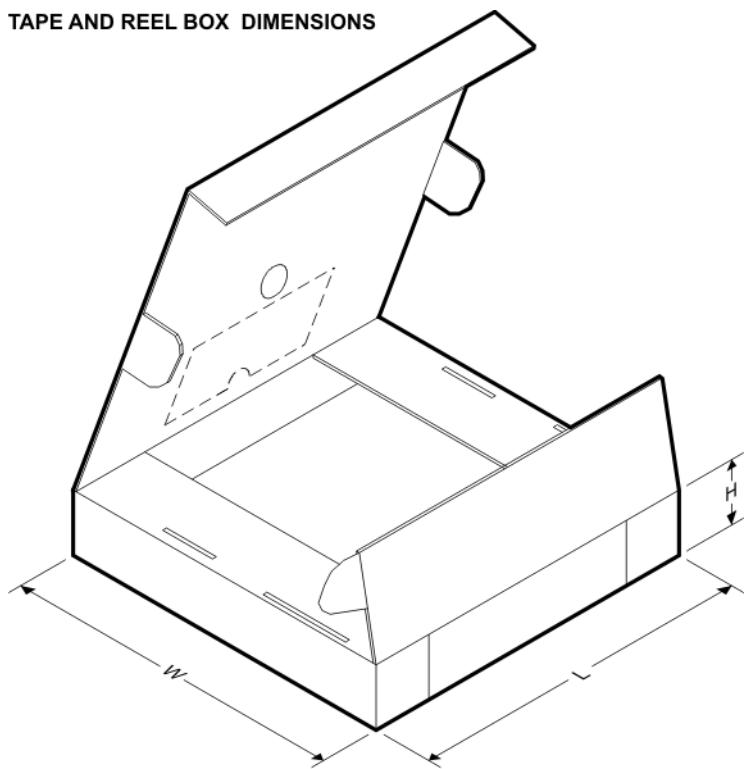
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92411DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS92411DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS92411DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TPS92411PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS92411PDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS92411PDDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92411DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS92411DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS92411DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TPS92411PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS92411PDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS92411PDDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

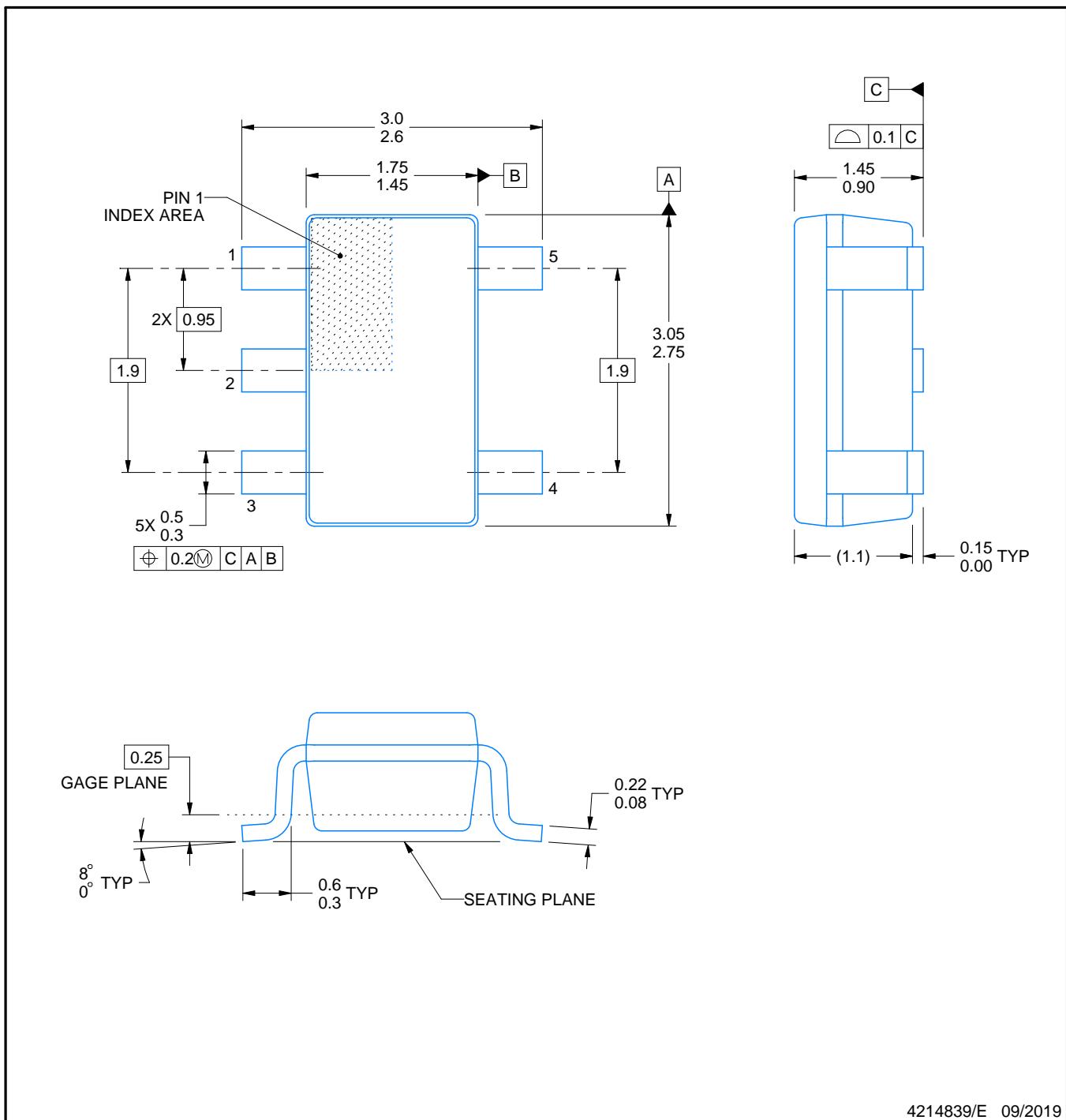
PACKAGE OUTLINE

DBV0005A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/E 09/2019

NOTES:

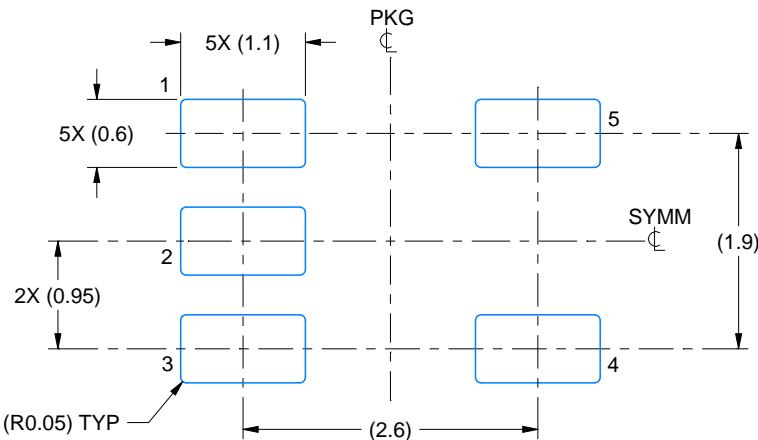
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

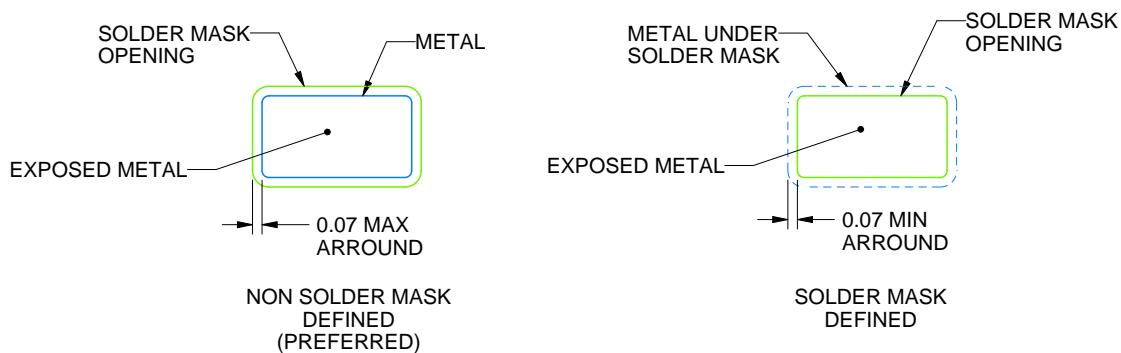
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

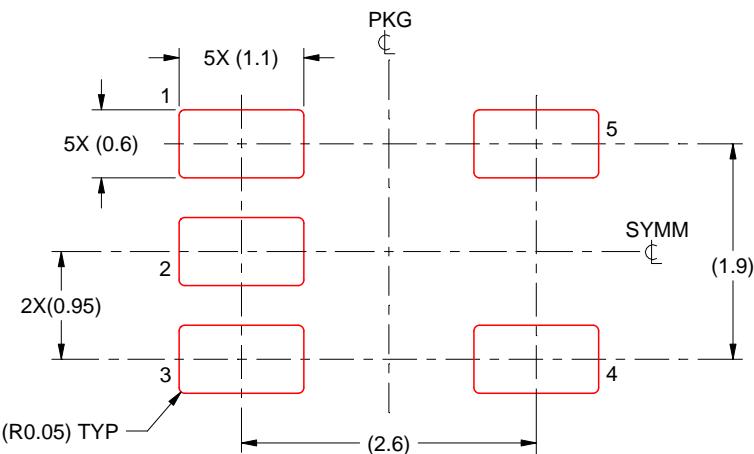
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

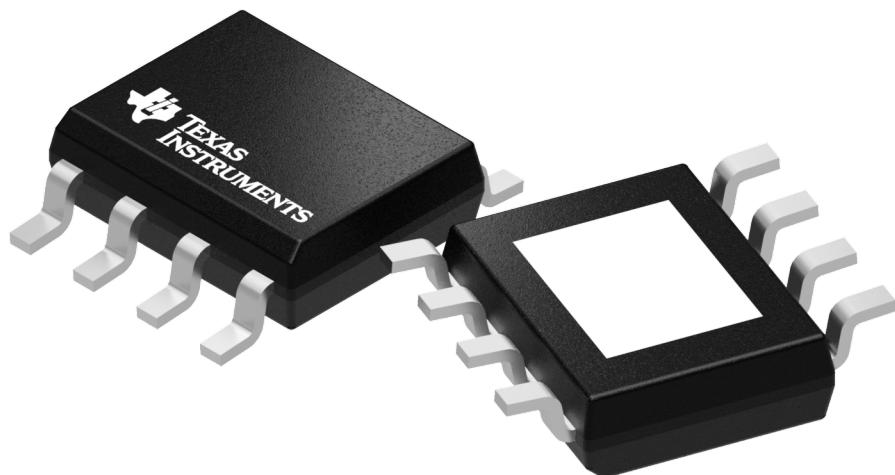
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DDA 8

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE

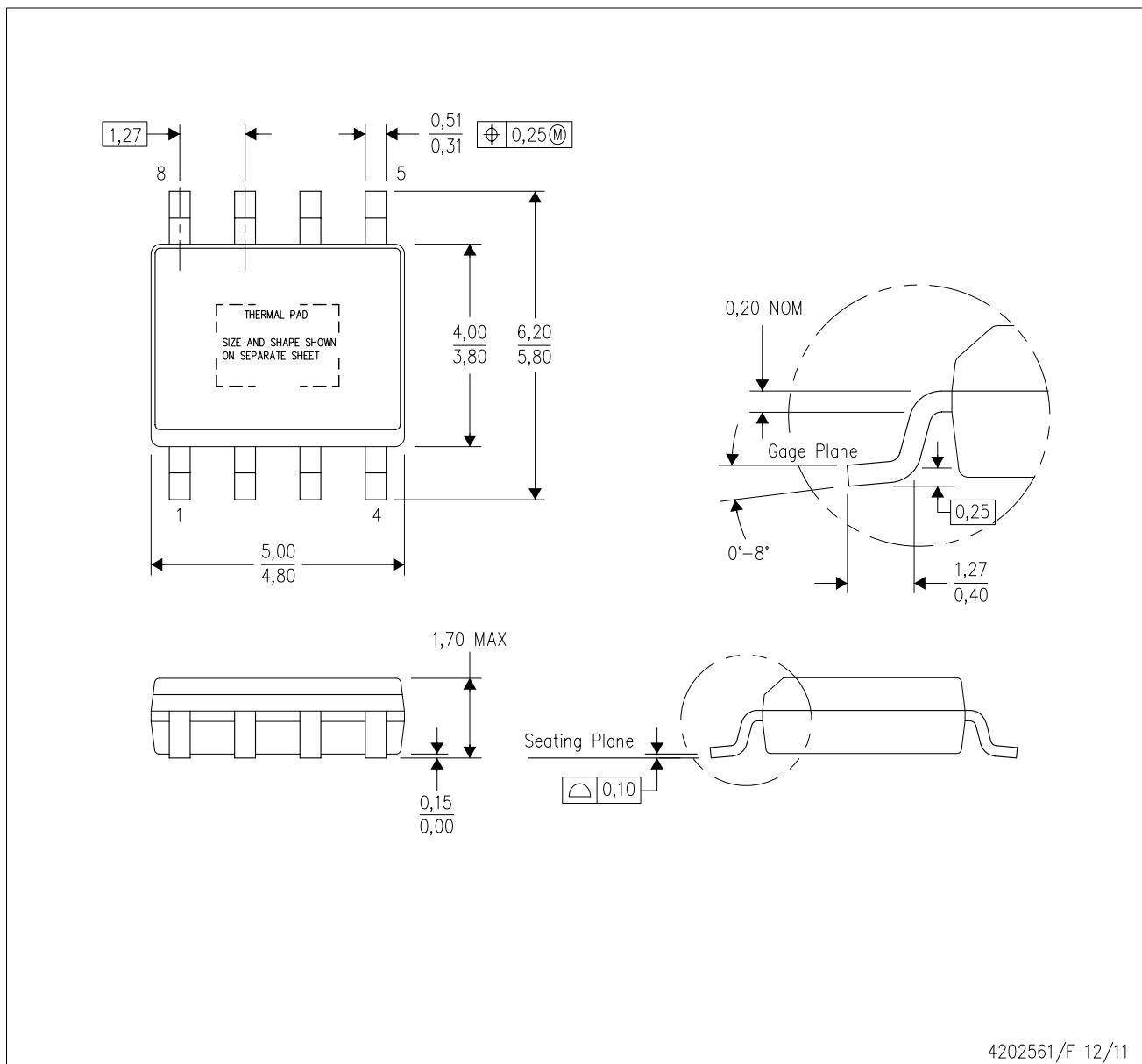


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4202561/G

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



4202561/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R-PDSO-G8)

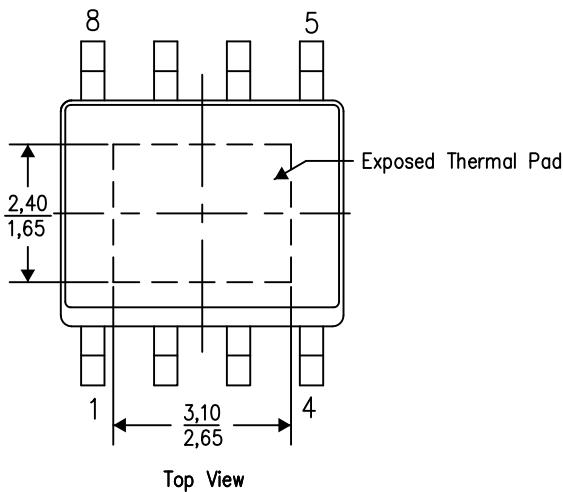
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322-6/L 05/12

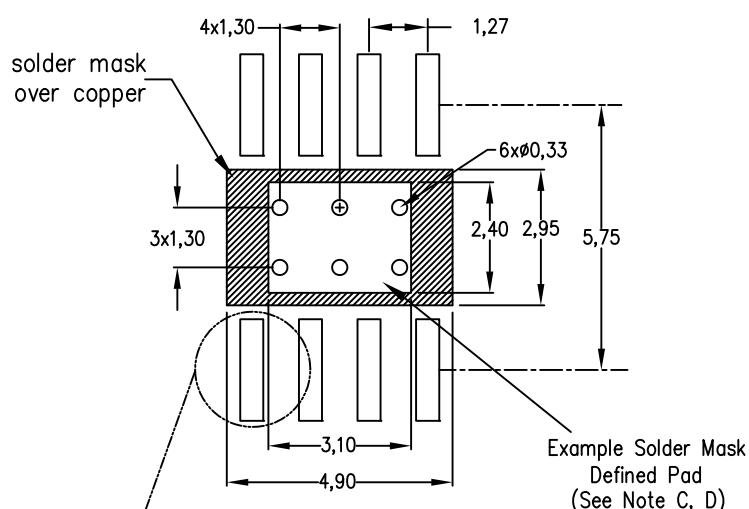
NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

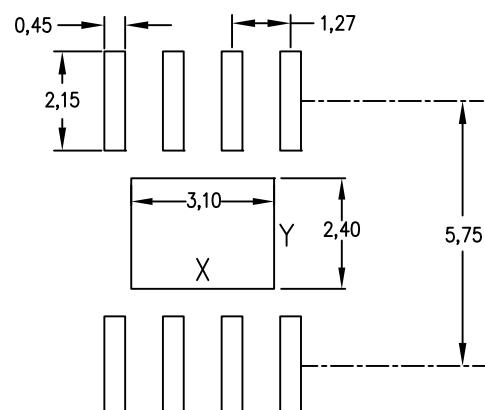
DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE

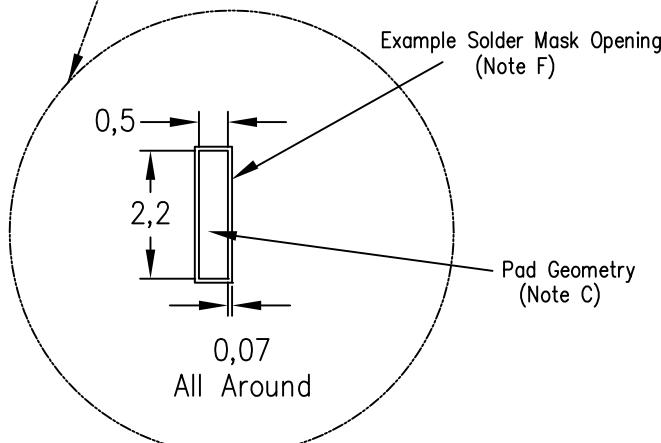
Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints



0,127mm Thick Stencil Design Example
Reference table below for other
solder stencil thicknesses
(Note E)



Non Solder Mask Defined Pad



Example Solder Mask Opening (Note F)

Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0,1mm	3,3	2,6
0,127mm	3,1	2,4
0,152mm	2,9	2,2
0,178mm	2,8	2,1

4208951-6/D 04/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

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