Fully integrated controller for USB-PD 3.1 EPR chargers

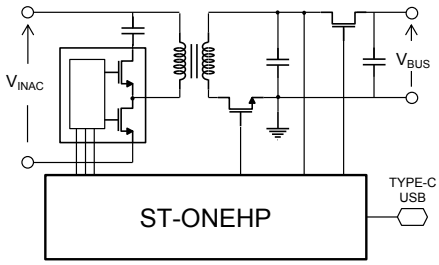
Product status link

ST-ONEHP

Product label

SUSTAINABLE TECHNOLOGY

Figure 1. Typical system block diagram



Features

- ZVS non-complementary active clamp flyback controller with synchronous rectification and USB-PD 3.1 EPR interface
- ARM® 32-bit Cortex®-M0+ MCU with 64 kB flash memory for digital power control and USB protocol
  - FW programmable secondary side MCU controls both synchronous rectifier and ZVS Active Clamp flyback on the primary side to improve system efficiency in every condition
  - High switching frequency operations in companion with MasterGaN power stage allow to use small size magnetic components, including planar transformers
- Reinforced galvanically isolated dual communication channel compliant with IEC 62368:
  - 4 kV pk transient voltage
  - 9.6 kV pk 1min hipot type testing
  - 6.4 kV pk 1s hipot production testing
- 800 V high voltage startup with integrated input voltage sensing and Brown-in/out functions
- Active input filter capacitor discharge circuitry for reduced standby power compliant with IEC 62368-1
- Fully Integrated USB-PD PHY with 24 V tolerant protection, and integrated load switch driver

Application

- USB-PD 3.1 EPR chargers and adapters up to 140W and over for smartphones, tablets, laptops and other handheld equipment
- High power charger for power tools and appliances

Description

The ST-ONEHP is the world's first digital controller embedding ARM Cortex M0+ core, an offline programmable controller with synchronous rectification, and USB PD PHY in a single package. Such a system is specifically designed to control ZVS non-complementary active clamp flyback converters to create high power density chargers and adapters with USB-PD 3.1 EPR interface.

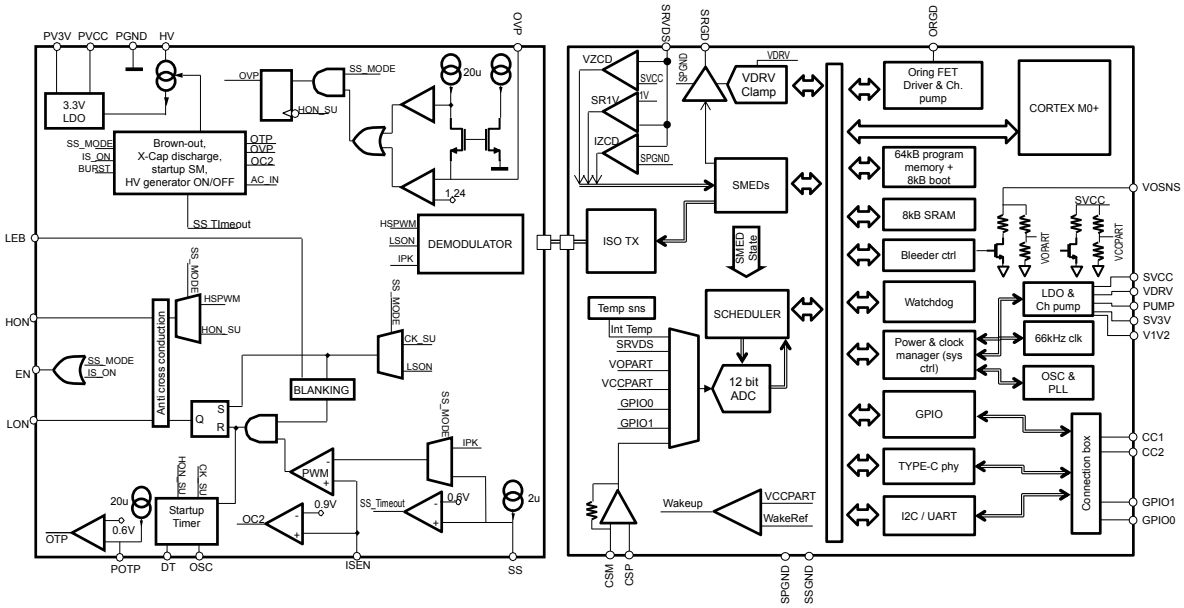
The device includes an active clamp flyback controller and its HV startup on the primary side, a microcontroller and all the peripherals required to control the conversion and the USB-PD communication on the secondary side. The two sides are connected through an embedded galvanically isolated dual communication channel. By using a novel non-complementary control technique and specifically designed power modes the device allows to reach both high efficiency and low no load power consumption

The device is delivered with a pre-loaded firmware which handles both the power conversion and the communication protocols for USB-PD 3.1 including EPR, optional PPS and electronically marked cable management.

A dedicated memory stores a default device configuration during factory process. The user can change or adapt this memory area to fit the final product specifications.

1 ST-ONEHP block diagram

Figure 2. ST-ONEHP block diagram



2 Pin connections and description

Figure 3. **Pin connection (top view)**

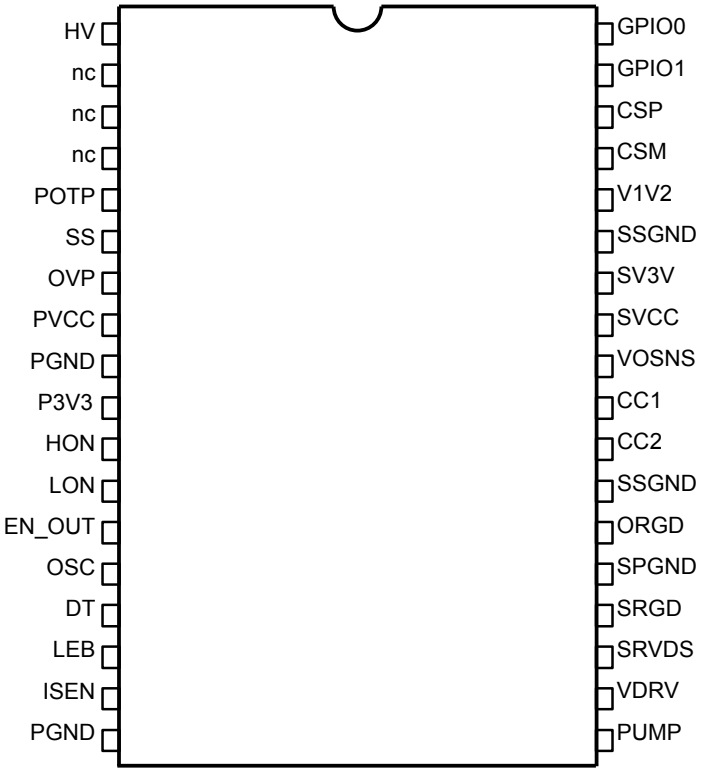


Table 1. **Pin functions**

Pin	Name	Function
1	HV	High voltage start-up generator / ac voltage sensing input. The pin, able to withstand 800 V, must be connected to the ac side of the input bridge via a pair of diodes to sense the ac input voltage. When the voltage on the pin is higher than $V_{HVStart}$, an internal pull-up circuit charges the capacitor connected between the pin PVCC and PGND. The pin is used also to sense the ac voltage, which is used by ac brown-out and X-cap discharge functions.
2,3,4	nc	High voltage spacer. The pin is not connected internally to increase spacing between the high-voltage pin and the other pins.
5	POTP	Primary side overtemperature protection. Pulling this pin below V_{POVTH} shuts down the IC.
6	SS	Soft-start setting. Connect a capacitor to PGND to set the soft-start duration.
7	OVP	Aux winding sense for overvoltage protection.
8	PVCC	Primary side supply voltage pin. The internal high voltage generator allows to charge an external capacitor connected between this pin and PGND before the converter starts up. A small bypass capacitor (0.1 µF typ.) to PGND must be placed close to the pins to get a clean bias voltage.
9	PGND	Primary side ground. Reference for I/Os.
10	P3V3	Primary side internal supply regulator bypass capacitor.
11	HON	High-side gate-drive control signal.
12	LON	Low-side gate-drive control signal.
13	EN_OUT	Enable signal for an external driver. Improves efficiency during bursts in case the driver supports this functionality.

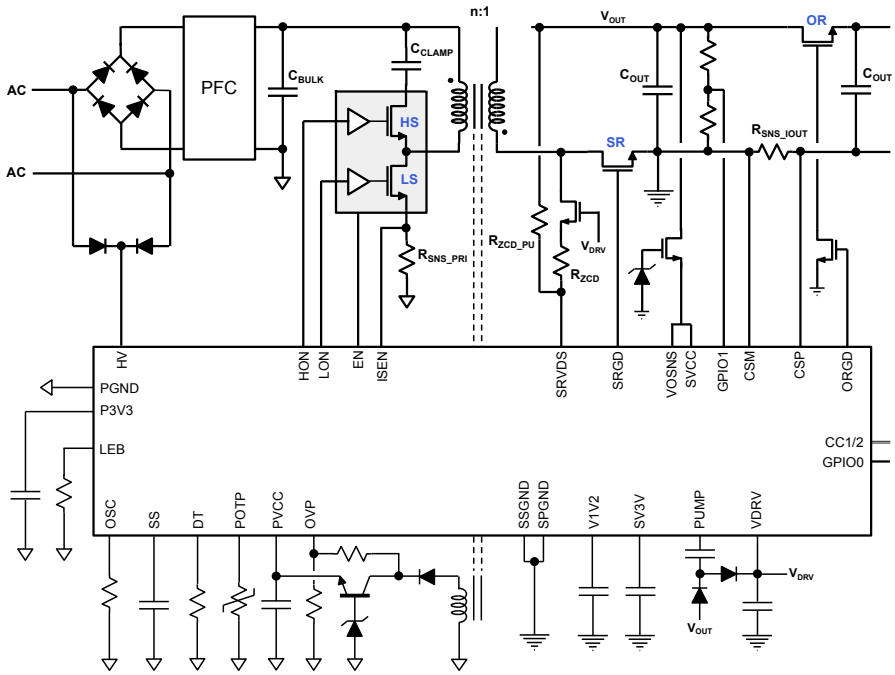
Pin	Name	Function
14	OSC	Oscillator pin. A resistor from the pin to PGND defines the switching frequency during the initial soft-start.
15	DT	Deadtime programming. A resistor from this pin to PGND sets the deadtime during soft-start and minimum deadtime during functional mode.
16	LEB	Leading edge blanking time programming. A resistor from this pin to ground sets the leading edge blanking time for the ISEN comparator.
17	ISEN	Current sense (PWM comparator) input. The voltage on this pin is compared with an internal reference to turn off LON.
18	PGND	Primary side signal ground. Reference for analog signals.
19	PUMP	Charge pump pin 1. Used to power the sync FET driver input VDRV when the voltage on SVCC is low.
20	VDRV	Sync FET driver supply.
21	SRVDS	Output winding voltage sense. Connect to sync FET drain through a clamping MOSFET.
22	SRGD	Synchronous rectifier gate driver.
23	SPGND	Secondary side power ground. Current return for the sync FET gate-drive current.
24	ORGD	Load switch control pin. Connect an external circuit to control a P type MOSFET.
25	SSGND	Secondary side signal ground.
26	CC2	USB Type-C CC2 pin. Used for USB-PD compliant communication or alternate function as DN / GPIO3 / I2C-SCL / UART-TX.(1) Add an external clamp if tolerance to voltage above 21V is required
27	CC1	USB Type-C CC1 pin. Used for USB-PD compliant communication or alternate function as DP / GPIO2 / I2C-SDA / UART-RX.(1) Add an external clamp if tolerance to voltage above 21V is required
28	VOSNS	Unused pin, connect to SVCC.
29	SVCC	Secondary side VCC. The device senses and controls the converter output through this pin when the programmed output voltage is below 15V.
30	SV3V	3.3 V Regulated supply for the IC. Connect a 1µF capacitor from this pin to SSGND.
31	SSGND	Secondary side signal ground.
32	V1V2	1.2 V regulated supply for the IC. Connect a 4.7µF capacitor from this pin to SSGND.
33	CSM	Output current sense pin. Connect to the negative side of sense resistor on the ground path.
34	CSP	Output current sense pin. Connect to the positive side of sense resistor on the ground path to sense the current drawn by the load.
35	GPIO1	Feedback input for output regulation when target voltage is above or equal to 15V. Connect a resistor divider from the converter output voltage to this pin. Can be reprogrammed as general purpose digital I/O, digital interface, analog input or alternate function as SWD-CLK / UART-TX / I2C-SCL.
36	GPIO0	General purpose digital I/O, digital interface, analog input or alternate function as SWDIO-TMS / UART-RX / I2C-SDA. The pin is also used to enter in programming/boot mode at IC startup. Connect a 100kΩ pullup to SV3V to avoid unwanted entry in boot mode at startup, unless this function is configured as disabled.

1. *The firmware loaded on ST-ONE configures the pins as either USB-PD or programming interface, depending on parameter setup. The default configuration is programming interface*

3 Typical application schematic

The following image is a simplified schematic for the typical application

Figure 4. Typical configuration



The ST-ONEHP is a very integrrated IC, which needs a few external components to build a complete system. On the primary side:

- An AC full wave power rectifier connected to a bulk capacitor.
- Two rectifier diodes to provide HV voltage to ST-ONE IC both for high voltage startup and AC brownout and disconnection detection.
- An integrated half bridge power stage (e.g ST MasterGaN) or Gate driver + FETs connected to the transformer primary winding.
- A clamp capacitor to store the residual energy in the transformer leakage inductance.
- An auxiliary winding power supply for the IC PVCC, also used to perform overvoltage function during the soft-start.

On the secondary side:

- A synchronous rectifier FET is connected to the SRGD pin.
- A cascode FET connected to the SRVDS pin to provide synchronous rectifier drain voltage sense while limiting the voltage on the pin below its AMR.
- A cascode FET connected to the SVCC and VOSNS pins to provide IC power supply and output voltage sense while limiting the voltage on the pin below its AMR.
- A resistor divider to provide output voltage sense when the target regulation voltage is 15V or above
- A P-channel MOSFET connected to ORGD pin through a N-channel signal MOSFET used as load switch to disconnect the output voltage as required by USB-PD power supplies.
- A sense resistor is connected to CSM/CSP pins to read the output current.
- A capacitor and two diodes connected to the PUMP pin to implement a charge pump providing the driving voltage to the synchronous rectifier.
- Two optional N-channel signal mosfets with gate connected to VDRV to provide tolerance on the CC pins higher than 21V

4 Package drawings

Figure 5. **Package drawings**

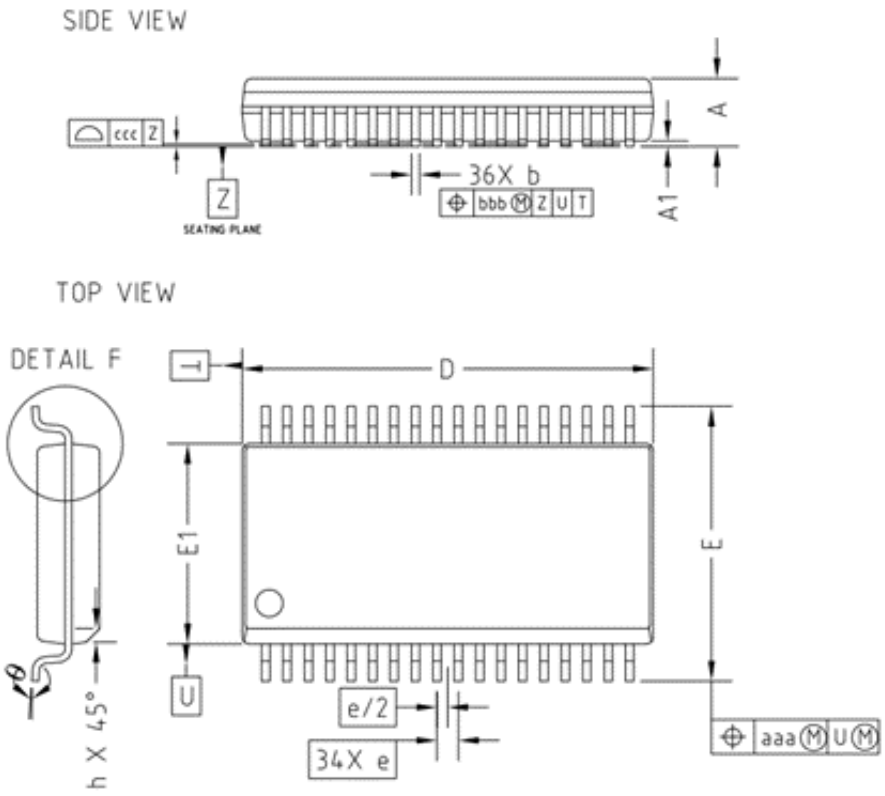


Figure 6. **Package dimensions**

DATABOOK				
SYMBOL	MIN.	NOM.	MAX.	NOTE
A			2.65	
A1	0.1		0.30	
b	0.25		0.35	
c	0.20		0.33	
D	15.20		15.60	
E1	7.40		7.60	
E	10.05		10.55	
e		0.80 BSC		
L	0.61		0.91	
h	0.25		0.75	
θ	0°		8°	

SYMBOL	TOLERANCE OF FORM AND POSITION DATABOOK	
aaa	0.25	
bbb	0.25	
ccc	0.10	

Note: All dimensions are in millimeters and angles in degrees.

Revision history

Table 2. **Document revision history**

Date	Version	Changes
05-Dec-2022	1	Initial release.

Contents

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