INTRODUCING

SLIVER DIRECT TO LEAD FRAME (DLF) INTERCONNECTS FOR SFF-TA-1002

- Standardized designs
- Supports high speed and density for next-gen silicon
- Design flexibility

Our new high performing Sliver DLF interconnects for the SFF-TA-1002 standard can help improve system performance, enable system modular design while also helping to reduce system design complexity and costs.

APPLICATIONS

- Internal Cabled Solutions
  - Chip to Chip
  - Chip to I/O
  - Chip to Backplane
  - Board to Board
- PCB Card Edge
- Supports Ethernet, PCIe, SAS, SATA, InfiniBand and Other Custom Protocols

ELECTRICAL

- **Voltage rating:** 20mV
- **Current rating:** 100mA DC Max

MECHANICAL

- **Operating temperature:** -55 to 105 °C
- **Mating and un-mating force:** Max rate 25.4mm/Min

MATERIALS

- **Housing:** LCP UL 94-V0
- **Contact:** Gold plated copper alloy

KEY BENEFITS

- Enables design flexibility by cable assemblies being available in flexible mounting options: vertical and horizontal mounting ear design
- Standardized designs enable ease of design in and multi-sourcing by consolidating fragmented pinouts and speeds. They reduce mother board size/costs and may eliminate re-timers
- Supports high speed and density for next-gen silicon though PCIe Gen 5, with a roadmap to 128 Gbps for PCIe Gen 7. Supports next gen silicon PCIe lane counts where current products in the market begin to max out. Eliminates the need for a separate power cable while providing high power rates of (150W) peripheral(s)

STANDARDS AND SPECIFICATIONS

- SFF-TA-1002
- EDSFF
- OCP NIC
- PCIe

LEARN MORE

- Landing Page
- Brochure
- eCatalog