6 A, 33 mΩ, 2.8 V to 23 V, eFuse With Programmable Current Limit and OVP

DESCRIPTION

The SIP32434A and SIP32434B are single-channel eFuses that integrate multiple control and protection features, which provide increased controllability and reliability, with simplified designs and minimal external components.

The SIP32434A and SIP32434B protect both power sources and downstream circuitry connected to the switch from overloads, short circuits, voltage surges, and excessive inrush currents.

The output current limit can be set by a single external resistor. V_{IN} overvoltage protection and undervoltage lockout threshold levels can be set with an external resistor network. V_{IN} inrush current requirements can be set with a single external soft start capacitor.

Upon switch-off due to latchable faults, the SIP32434A will latch the power switch off and the PGD will remain low. The switch can restart by resetting the EN or V_{IN}. The SIP32434B will auto retry if there is no OTP or OVP fault. The retry delay time is 32 times the soft start time set by the CSS.

The switch is characterized for operation over a junction temperature range of -40 °C to +125 °C.

APPLICATIONS

- Industrial
- IoT and smart home
- Medical and healthcare equipment
- Network and telecom equipment
- Data storage, solid state drives
- Computing
- PLC
- Lighting
- Gaming consoles

FEATURES

- 2.8 V to 23 V operation voltage
- 28 V max. voltage rating with 24 V internal OVP
- 33 mΩ typical switch resistance
- 0.5 A to 6 A current limit setting range
- Current limit accuracy of ± 7 %
- Fast short circuit protection response
- OCP triggering without overhead current
- Programmable turn-on slew rate
- Turn-on delay: 190 µs
- Adjustable OVP (and fixed 24 V OVP at V_{IN})
- Adjustable UVLO
- Over-temperature protection
- ESD / HBM: > 2 kV
- ESD / CDM: > 750 V
- PGD: power good indicator output
- Compact TDFN10 3 mm x 3 mm package (for AEC-Q100 qualified automotive applications, please refer to SIPQ32434)
- Active reverse blocking feature available with SIP32433
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

TYPICAL APPLICATION CIRCUIT

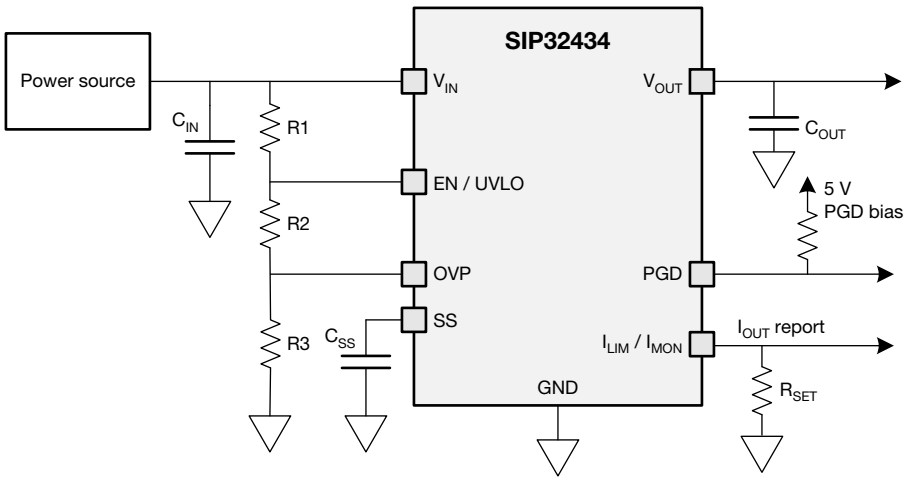


Fig. 1 - Application Circuit

ORDERING INFORMATION

PART NUMBER	OCP RESPONSE	$R_{DS(on)}$ (mΩ)	TRUE REVERSE CURRENT BLOCKING	REPORT	MARKING CODE	PACKAGE
SIP32434ADN-T1E4	Latch	33	No	PG	2434A	DFN10 3 mm x 3 mm
SIP32434BDN-T1E4	Auto-retry	33	No	PG	2434B	DFN10 3 mm x 3 mm
SIP32434AEVB	Evaluation board					
SIP32434BEVB	Evaluation board					

Note

- For AEC-Q100 qualified automotive applications, please refer to SIPQ32434ADN-T1E4 and SIPQ32434BDN-T1E4

ABSOLUTE MAXIMUM RATINGS

PARAMETER	CONDITION	LIMIT	UNIT
Input voltage (V_{IN})	Reference to GND	-0.3 to +28	V
Output voltage (V_{OUT})	Reference to GND	-0.3 to (V_{IN} + 0.3) or 28, whichever comes first	
		-5 V for +5 µs	
EN voltage	Reference to GND	-0.3 to +28	
OVP	Reference to GND	-0.3 to +6.0	
SS	Reference to GND	-0.3 to +6.0	
I_{LIM}		-0.3 to +6.0	
PGD		-0.3 to +6.0	
Maximum continuous switch current	SIP32434	6	A
Thermal resistance ($_{thJA}$)		44.8	°C/W
ESD rating	HBM	± 2	kV
ESD rating	CDM	± 0.75	
Latch up current (V_{IN} and V_{OUT})		200	mA
Temperature			
Operating junction temperature		-40 to 150	°C
Maximum operating junction temperature		+150	
Storage temperature		-65 to +150	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

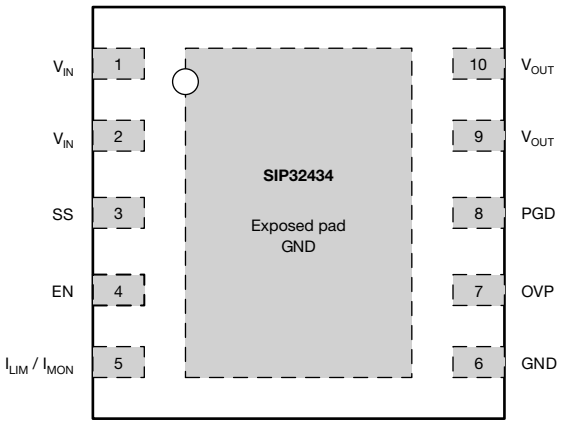
ELECTRICAL	LIMIT	UNIT
Input voltage (V_{IN})	3 to 23	V
Operating junction temperature	-40 to +125	°C

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V_{IN} = 12 V, T_J = -40 °C to +125 °C, $V_{EN(H)}$ = 2.4 V, C_{OUT} = 0.1 µF, R_{LIM} = 4.1 kΩ	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Power Supply						
Power input voltage	V_{IN}	Operating input voltage range	2.8	-	28	V
Quiescent current	$I_{Q(ON)}$	EN = 1.8 V, V_{IN} = 2.8 V to 28 V, V_{OUT} open	-	230	340	µA
Shutdown current	$I_{Q(SD)}$	V_{IN} = 2.8 V to 28 V, EN = 0 V, T_A = 25 °C	-	0.8	5	
OVP switch-off current	$I_{Q(OVP)}$	V_{IN} = 2.8 V to 28 V, EN = 2.4 V, OVP = 1.4 V	-	1	-	
V_{IN} ULVO						
Switch V_{OUT} leakage	I_{UVLO_OUT}		-500	-	+500	nA
Switch V_{IN} leakage	I_{UVLO_IN}	V_{IN} = 2.3 V	-	27	50	µA
Overvoltage Protection						
OVP threshold	V_{OVP}	V_{IN} = 12 V, OVP rising, T_A = 25 °C	1.14	1.2	1.26	V
OVP hysteresis	OVP_{HST}	T_A = 25 °C	60	105	140	mV
OVP leakage	I_{OVP}	V_{OVP} = 1.2 V on the pin, T_A = 25 °C	-	40	100	nA
IN pin internal fixed OVP	IN_{OVP}	T_A = 25 °C	23	24	25.6	V
EN / UVLO						
EN on threshold	V_{UVPR}	V_{EN} rising	-	1.25	-	V
EN off threshold	V_{UVPF}	V_{EN} falling	-	1.05	-	
EN / UVLO leakage		V_{EN} = 1.2 V	-0.25	-	+0.25	µA
Overcurrent Protection						
Current limit voltage threshold	V_{OCP}	Voltage that triggers the OCP shown on I_{LIM} pin	-	0.6	-	VCu
Current limit accuracy	I_{OCP}	V_{IN} - V_{OUT} = 1 V, R_{SET} = 2.06 kΩ	5.58	6	6.42	A
			3.22	3.5	3.78	
			1.32	1.5	1.68	
			0.43	0.5	0.58	
Current limit setting range		Minimum R_{SET} = 2 kΩ	0.5	-	6	
Current limit hold-up time	t_{ILIM}	Current limiting timeout, if no OTP	3	6	9	ms
Power Switch						
ON resistance	$R_{DS(ON)}$	V_{IN} = 5 V to 22 V, I_{OUT} = 1 A, T_J = 25 °C	-	33	41	mΩ
		V_{IN} = 5 V to 22 V, I_{OUT} = 1 A, T_J = 85 °C	-	-	48	
PGD, Power Good						
PGD pull-down resistance	R_{PG}	V_{IN} = 5 V, output pin = 0.1 V	-	5.2	10	Ω
PGD oll leakage	I_{PG}	Biased with 5 V_{DC}	-	0.01	1	µA
Switching Characteristics						
EN / UVLO						
Switch turn-on delay time	T_{ON_DLY}	From EN / UVLO voltage, V_{UVPR} to V_{OUT} reaches 10 % V_{IN}, R_L = 10 Ω, C_L = 10 µF, C_{SS} open	-	220	-	µs
Shutdown delay	T_{OFF_DLY}	From EN / UVLO low to V_{OUT} = 0.9 x V_{IN}, R_L = 10 Ω, C_L = 10 µF, C_{SS} open	-	10	-	
OVP Timing						
OVP off time	t_{OVP}	R_L = 100 Ω, C_L = 0 µF, OVP steps from 1 V to 1.4 V; measured from OVP pin voltage crossing 1.2 V threshold to V_{OUT} = 0.9 x V_{IN}	-	0.3	1	µs
Internal OVP off time	t_{OVP_INT}	R_L = 100 Ω, C_L = 0 µF, V_{IN} steps from 22 V to 26 V; measured from V_{IN} pin voltage crossing 24 V threshold to V_{OUT} = 0.9 x V_{IN}	-	1.5	-	
Flag reporting delay		PGD pull up to 5 V through a 100 kΩ; delay time from OVP pin voltage step to PGD is below 0.5 V	-	-	2	
Overcurrent protection						
Moderate overcurrent protection	t_{OCP}	Load current is 120 % of current limit threshold	-	1.1	-	µs

ELECTRICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS SPECIFIED V_{IN} = 12 V, T_J = -40 °C to +125 °C, $V_{EN(H)}$ = 2.4 V, C_{OUT} = 0.1 µF, R_{LIM} = 4.1 kΩ	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Soft Start Control						
Output rise up time	t_R	V_{IN} = 12 V, R_L = 10 Ω, C_L = 10 µF, V_{OUT} from 10 % to 90 % V_{IN}, C_{SS} open	-	560	-	µs
		V_{IN} = 12 V, R_L = 10 Ω, C_L = 10 µF, V_{OUT} from 10 % to 90 % V_{IN}, C_{SS} = 22 nF	-	4.7	-	ms
SS charge current			-	5	-	µA
Auto Retry						
Auto retry cycle	RTY_{cnt}	Delay time of restart after all faults are removed; this is defined as the number of cycles of soft start time set by C_{SS}	-	32	-	
Thermal Shutdown						
Thermal shutdown		Temperature increases	-	165	-	°C
Thermal shutdown hysteresis			-	45	-	°C

PACKAGE OUTLINE



DFN10, pin 1 dot marking is on top of the device

Fig. 2 - Pin Out Drawing (top view)

PIN DESCRIPTION		
PIN #	NAME	FUNCTION
1, 2	V_{IN}	Power switch input pins; two pins are fused inside the package
3	SS	A capacitor from this pin to GND sets output voltage slew rate
4	EN / UVLO	Active high switch control input; V_{THL} < 0.3 V, V_{THH} > 1.4 V
5	I_{LIM} / I_{MON}	A resistor from this pin to GND sets the overload and short-circuit current limit; the pin can be used for current reporting, referring to the voltage developed over the current limit setting resistor
6	GND	Ground
7	OVP	Input for setting the programmable overvoltage protection threshold. An overvoltage event turns-off the internal FET and asserts FLT to indicate the overvoltage fault
8	PGD	Open drain output, when V_{OUT} is ≥ 95 % V_{IN}, and none of the following faults are triggered: OT, OC, OV
9, 10	V_{OUT}	Power switch output pins; two pins are fused inside the package
Exposed pad	GND	The package's central exposed pad must be connected to the ground plane; optimal PCB thermal design will enhance device performance

FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE

TRUTH TABLE	
EN	**SWITCH**
1	ON
0	OFF

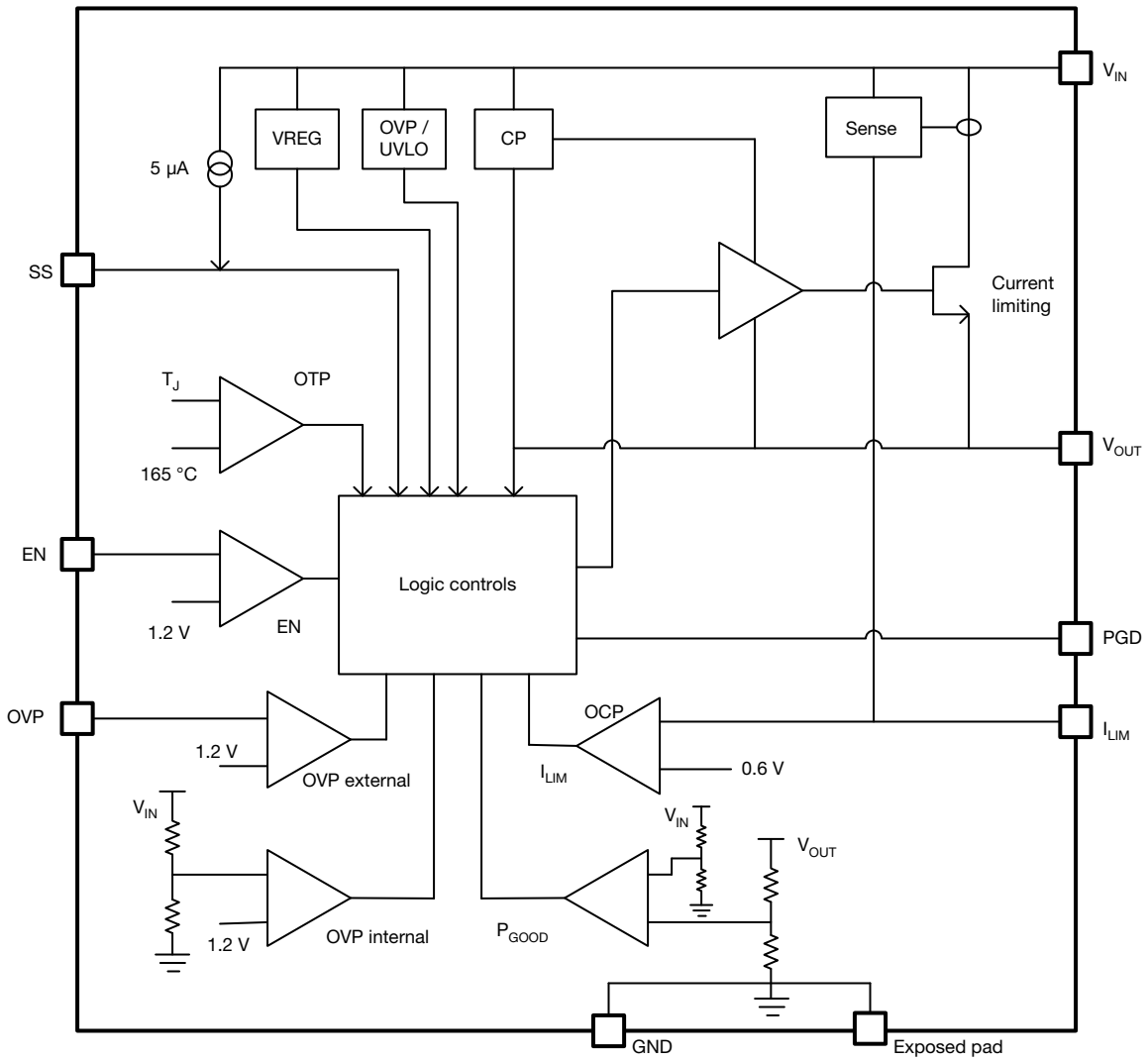


Fig. 3 - Device Block Diagram

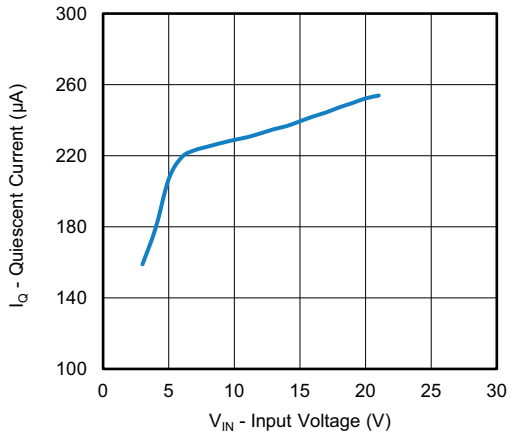


Fig. 4 - Quiescent Current vs. Input

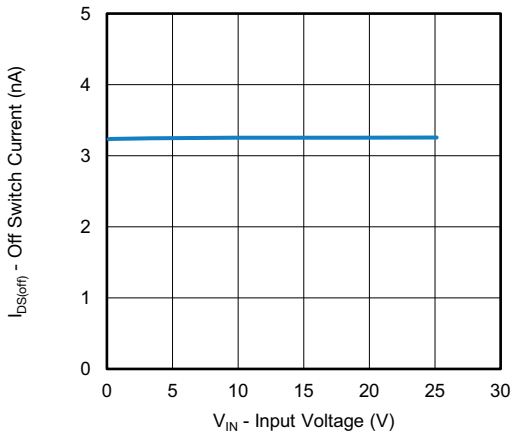


Fig. 7 - Switch Off Current vs. Input

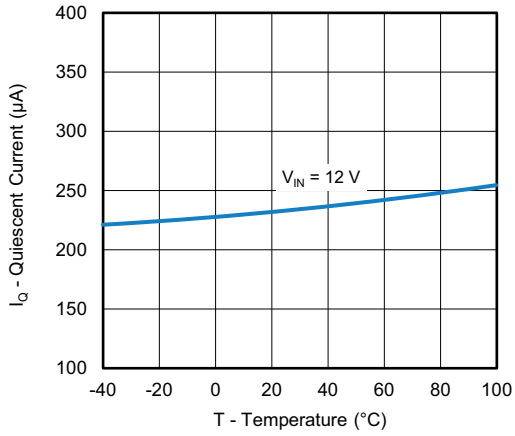


Fig. 5 - Quiescent Current vs. Temperature

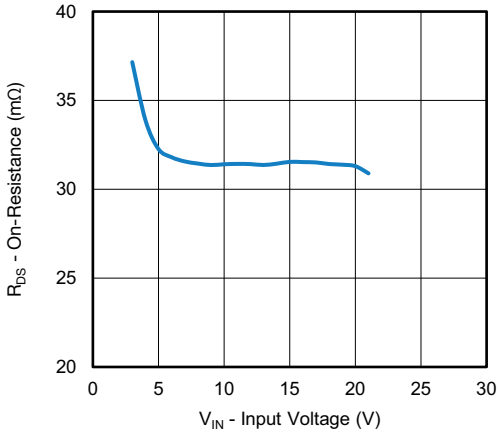


Fig. 8 - On Resistance vs. Input

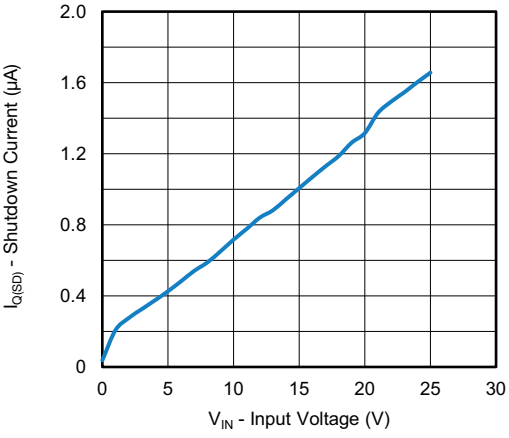


Fig. 6 - Shutdown Current vs. Input

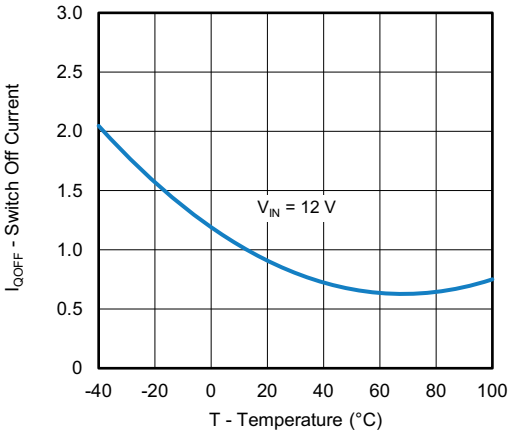


Fig. 9 - Shutdown Current vs. Temperature

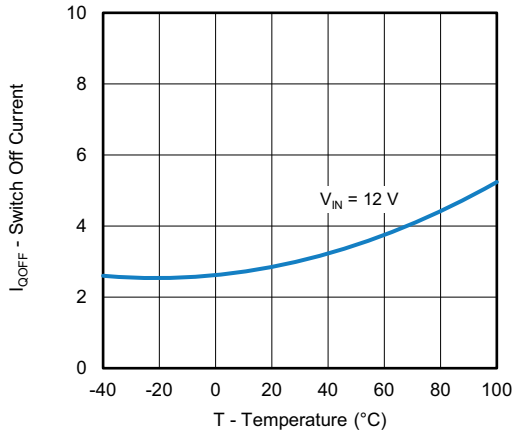


Fig. 10 - Switch Off Current vs. Temperature

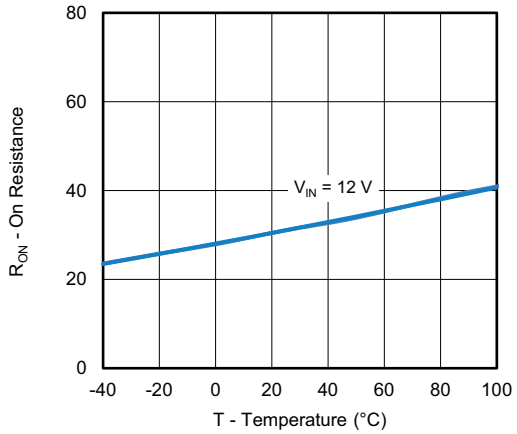


Fig. 11 - On Resistance vs. Temperature

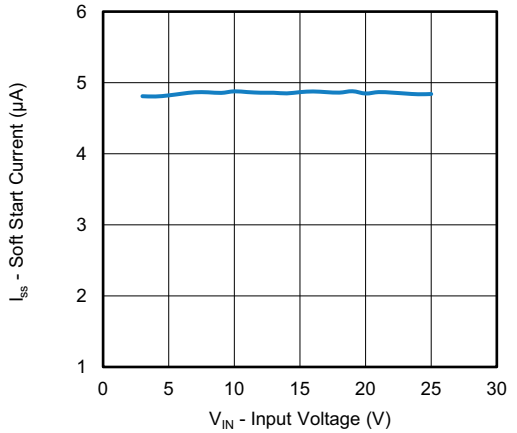


Fig. 12 - Soft Start Current vs. Input Voltage V_{IN}

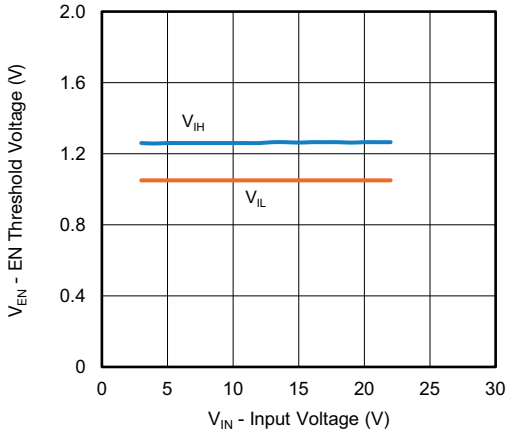


Fig. 13 - Threshold Voltage vs. Input Voltage V_{IN}

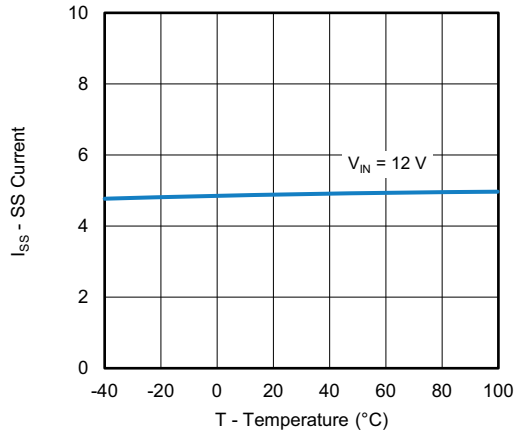


Fig. 14 - Soft Start Current vs. Temperature

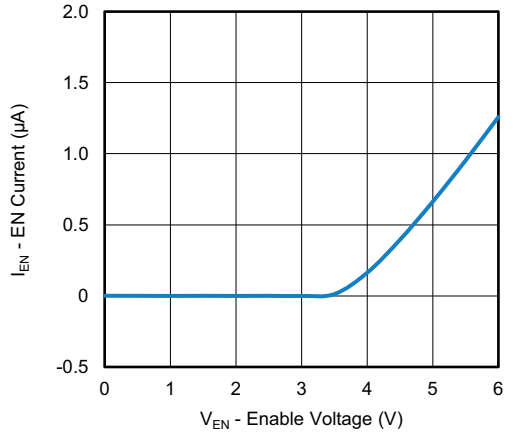


Fig. 15 - EN Current vs. EN Voltage

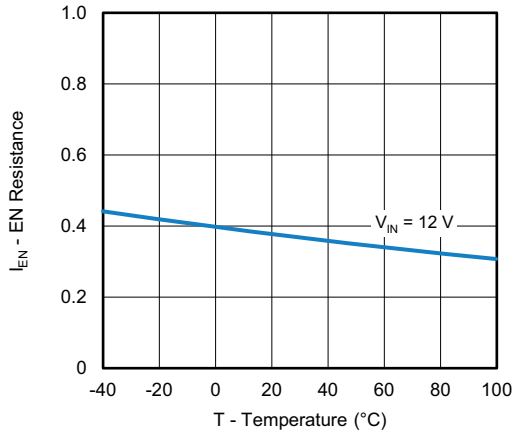


Fig. 16 - Enable Resistance vs. Temperature

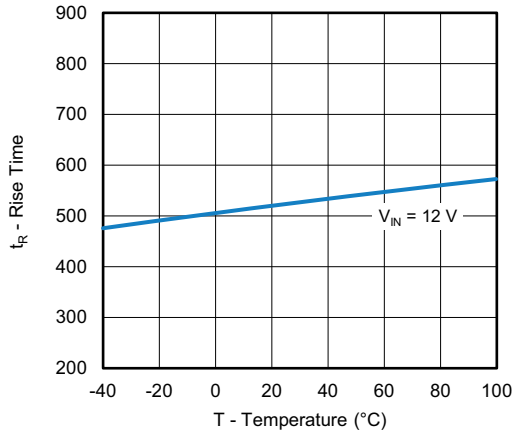


Fig. 17 - Rise Time vs. Temperature

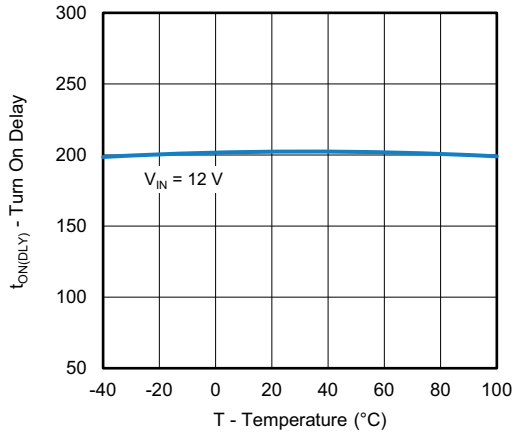


Fig. 18 - Turn On Delay Time vs. Temperature

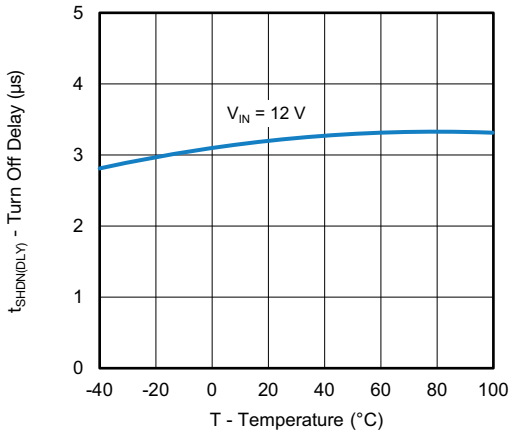


Fig. 19 - Turn Off Delay Time vs. Temperature

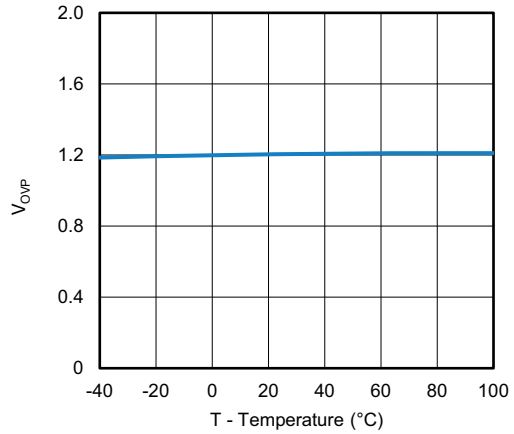


Fig. 20 - OVP Voltage vs. Temperature

TYPICAL CHARACTERISTICS

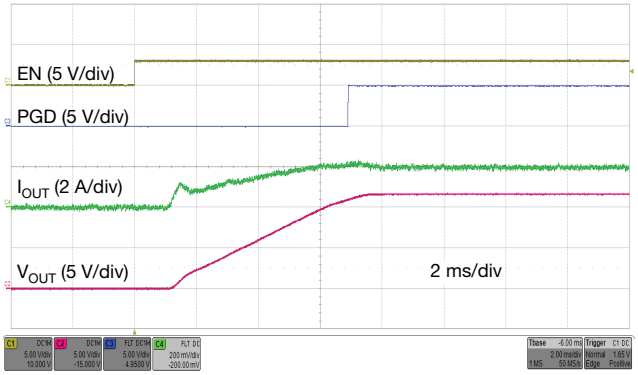


Fig. 21 - Turn On by EN
V_{IN} = 12 V, R_L = 6 Ω, C_L = 220 µF, C_{SS} = 22 nF, R_{LIM} = 1.74 kΩ

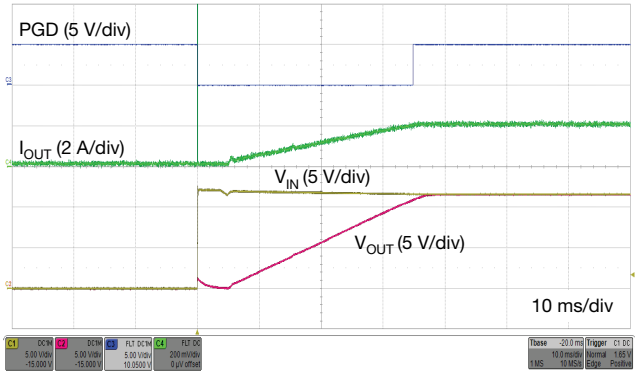


Fig. 24 - Turn On by Hot-Plug of V_{IN}
V_{IN} = 12 V, R_L = 6 Ω, C_L = 220 µF, C_{SS} = 133 nF, R_{LIM} = 1.74 kΩ
EN Voltage Divider Resistors, 1 MΩ and 127 kΩ

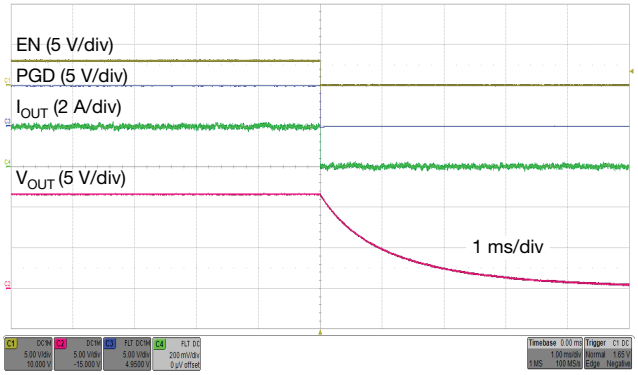


Fig. 22 - Turn Off by EN
V_{IN} = 12 V, R_L = 6 Ω, C_L = 220 µF, C_{SS} = 22 nF, R_{LIM} = 1.74 kΩ

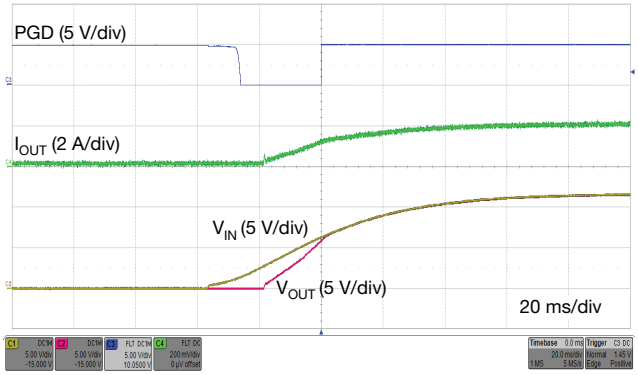


Fig. 25 - Turn On by V_{IN} When EN is 3 V
V_{IN} = 12 V, R_L = 6 Ω, C_L = 220 µF, C_{SS} = 133 nF, R_{LIM} = 1.74 kΩ

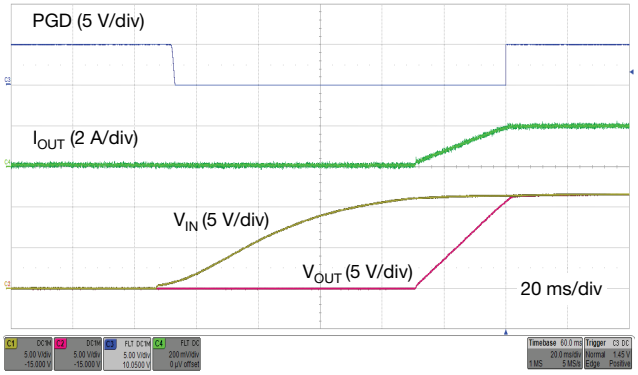


Fig. 23 - Turn On by V_{IN}
V_{IN} = 12 V, R_L = 6 Ω, C_L = 220 µF, C_{SS} = 133 nF, R_{LIM} = 1.74 kΩ
EN Voltage Divider Resistors, 1 MΩ and 127 kΩ

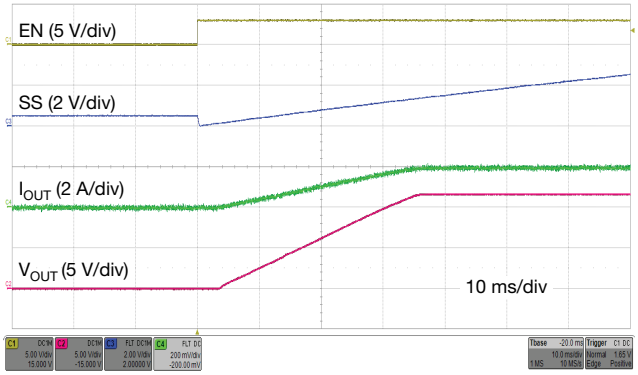


Fig. 26 - Turn On by EN Into Resistive Load
V_{IN} = 12 V, R_L = 6 Ω, C_{SS} = 133 nF, R_{LIM} = 1.74 kΩ

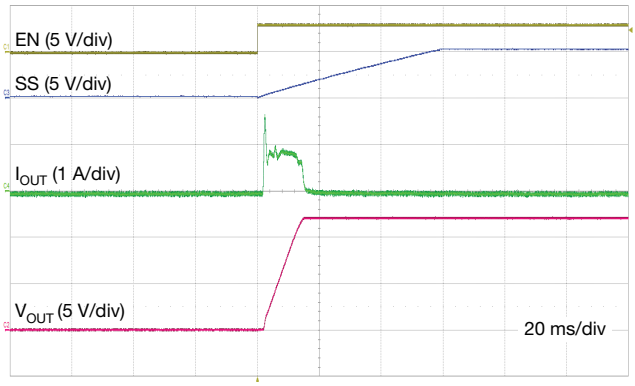


Fig. 27 - Turn On by EN Into Capacitive Load
V_{IN} = 12 V, C_L = 220 µF, C_{SS} = 47 nF, R_{LIM} = 1.74 kΩ

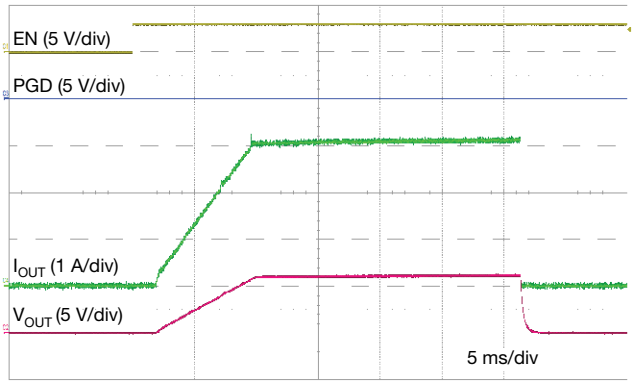


Fig. 30 - Turn On by EN Into OCP Load
V_{IN} = 12 V, R_L = 2 Ω, C_L = 220 µF, C_{SS} = 133 nF, R_{LIM} = 1.74 kΩ

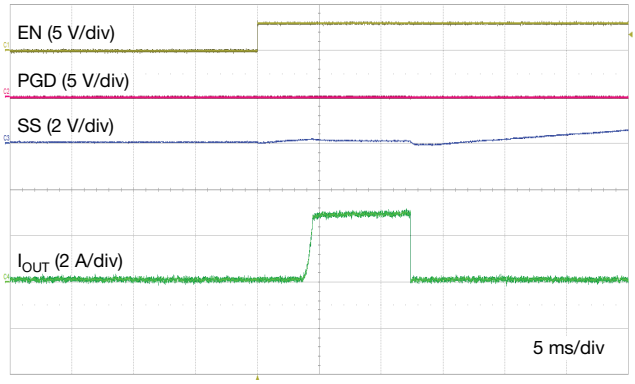


Fig. 28 - Turn On Into Output Short
V_{IN} = 12 V, C_{SS} = 133 nF, I_{LIM} = 1.74 kΩ

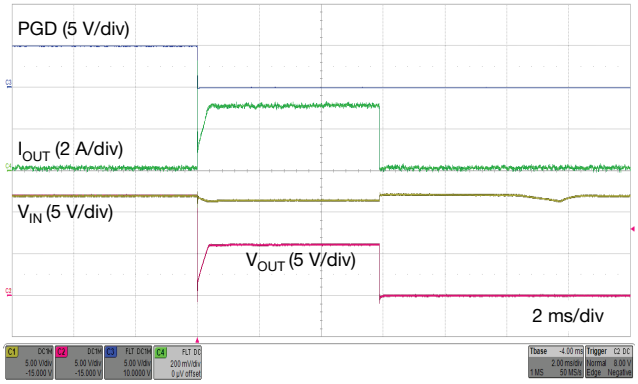


Fig. 31 - Output Short With a 2 Ω Load
V_{IN} = 12 V, R_L = 2 Ω, C_{SS} = 133 nF, R_{LIM} = 1.74 kΩ

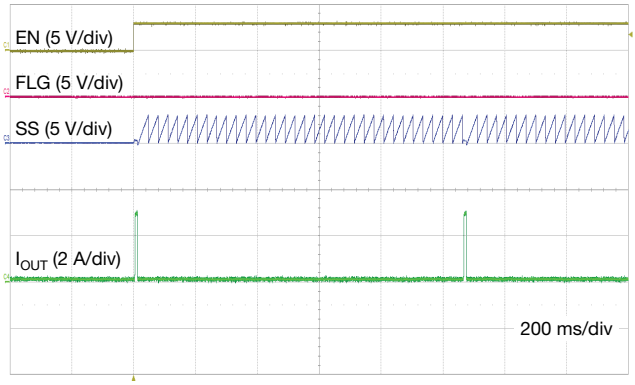


Fig. 29 - Turn On Into Output Short, Auto-Retry
V_{IN} = 12 V, C_{SS} = 133 µF, R_{LIM} = 1.74 kΩ

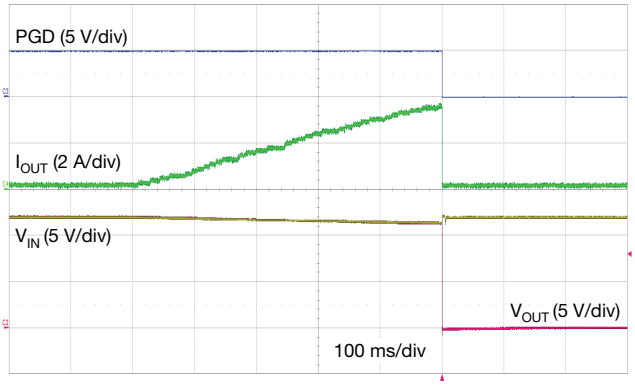


Fig. 32 - Over Current Protection
Increase Load Current Slowly
V_{IN} = 12 V, C_L = 220 µF, C_{SS} = 133 nF, R_{LIM} = 1.74 kΩ

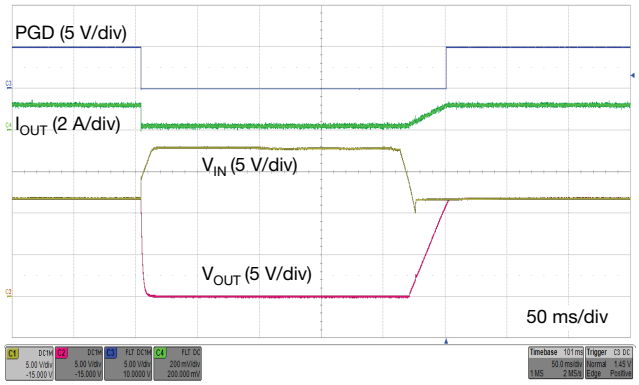


Fig. 33 - Over Voltage Protection
R_L = 12 Ω, C_L = 100 µF, C_{SS} = 27 nF, R_{LIM} = 1.74 kΩ, OVP Set to 15.6 V

OVERVIEW

The SIP32434A and SIP32434B are eFuses with comprehensive integrated control features that simplify the design and increase the reliability of the circuitry connected to the switch.

The 32 mΩ switches are designed to operate in the 2.8 V to 23 V range. An internally generated gate drive voltage ensures good R_{ON} linearity over the input voltage operating range.

The devices start their operation by checking the V_{IN}, V_{OUT}, OVP, and EN / UVLO pins. When the voltages are in the ranges without exceeding under- or over-voltage protection thresholds, the PGD open drain switch is off. A high level on the EN / UVLO pin enables the internal MOSFET to start conducting and allows current to flow from IN to OUT. When EN / UVLO is held low, the internal MOSFET is turned off.

After a successful turn-on sequence, the device now actively monitors its load current, input voltage, and protects the load from harmful over-current, and over-voltage conditions. A built-in thermal sense circuit will detect junction over temperature and shut down the switch for safety.

SWITCH ON / OFF, AND UNDER-VOLTAGE LOCK OFF PROTECTION - UVLO

EN / UVLO pin controls the on / off of the power switch. When EN / UVLO is at a logic high the switch is on. When EN / UVLO is at a logic low, the switch is off.

The SIP32434A and SIP32434B implement under-voltage protection on the EN / UVLO to turn off the output. It is a user-defined under-voltage protection setting to flexibly select the proper minimum applied voltage for the downstream load or the device's proper operation.

The diagram shows how a resistor divider from supply to GND can be used to set the UVLO set point for a given voltage supply level.

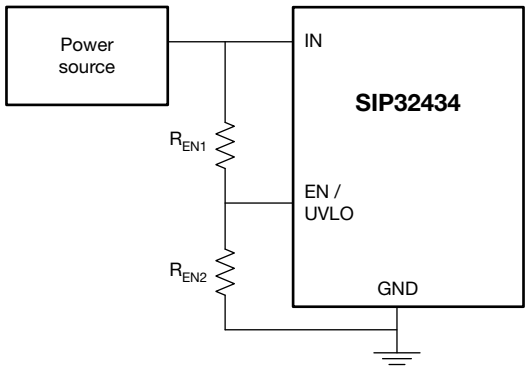


Fig. 34

The resistors must be sized large enough to minimize the constant leakage from supply to ground through the resistor divider network. At the same time, keep the current through the resistor network sufficiently larger than the leakage current on the EN / UVLO pin to minimize the error in the resistor divider ratio.

$$R_{EN1} = \frac{R_{EN2}(V_{IN} - V_{UVPR})}{V_{UVPR}}$$

Where V_{UVPR} is 1.25 V.

UVLO turn off delay (T_{OFF_DLY}) is typically 550 µs and turn on delay T_{ON_DLY} is typically 500 µs.

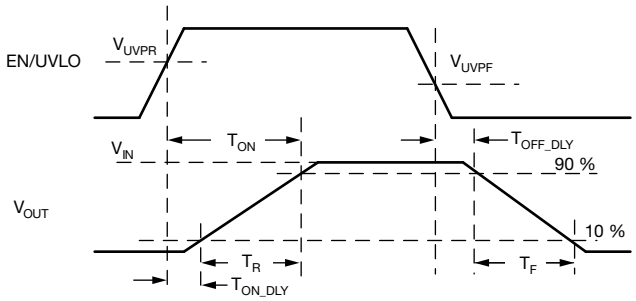


Fig. 35 - Switching Times

OVER-VOLTAGE PROTECTION (OVP)

The SIP32434A and SIP32434B implement overvoltage protection (OVP) on both the V_{IN} and OVP pins to protect the output load in the event of an input over-voltage. When the input exceeds the over-voltage protection thresholds $V_{OVP(R)}$ or the IN_{OVP}, which is typically 24 V, the device turns off the output within t_{OVP}, while the PGD asserts in the meantime. As long as an over-voltage condition is present on the input, the device stays disabled and the output will be turned off. Over-voltage is a non-latchable fault. Once the input voltage returns to the normal operating range, the device attempts to start up normally.

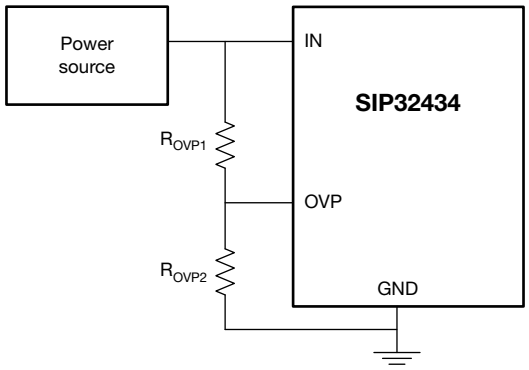


Fig. 36

$$\frac{R_{OVP1}}{R_{OVP2}} = \frac{V_{IN(OVP)} - 1.2\ V}{1.2\ V}$$

OVP voltage divider resistors total resistance should not be over 2.5 MΩ.

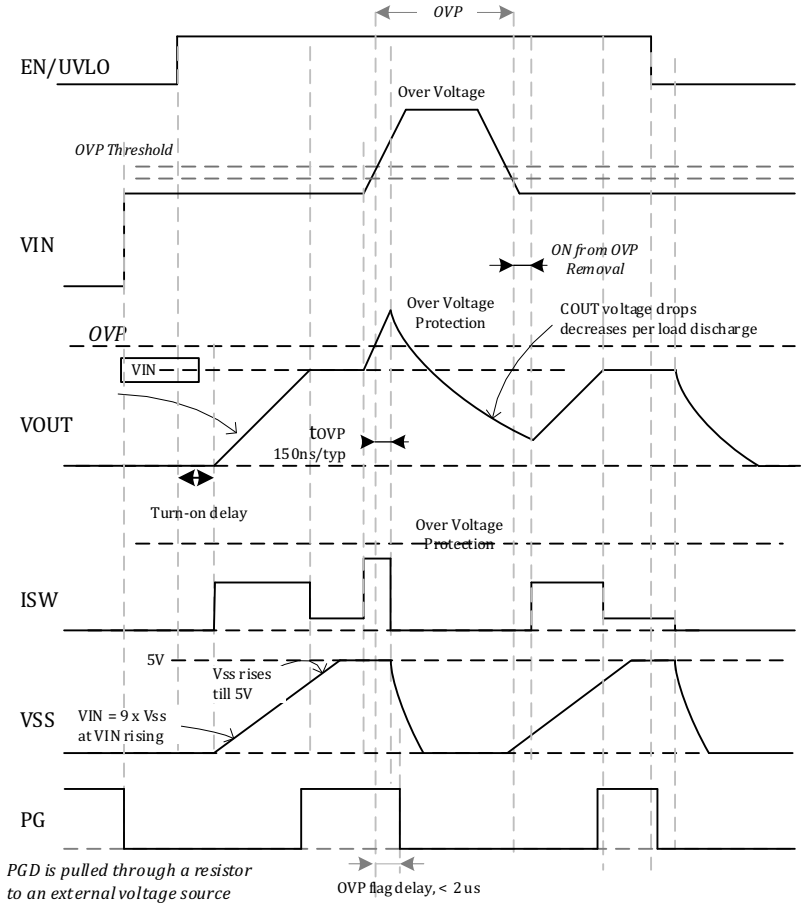


Fig. 37

INRUSH CURRENT, AND OVER-CURRENT PROTECTION

The SIP32434A and SIP32434B incorporate two protections against over-current:

- Adjustable slew rate (SR) for inrush current control
- Adjustable over-current protection / active current limit to protect against overload conditions

The over-current protection (OCP) is active also during soft start. The over-current protection circuit controls the switch impedance to limit the current to the level programmed by the R_{SET} resistor.

If the over-current condition persists for more than 6 ms (typ.), the switch shuts off and alert the drain FLG is asserted, pulling the pin to GND.

SLEW RATE CONTROL

An inrush current happens when the switch turns on into a large output capacitance. If the inrush current is not controlled, it can damage the input connectors and / or cause the system power supply to droop, leading to unexpected restarts elsewhere in the system.

The SIP32434A and SIP32434B provide integrated output slew rate control to manage the inrush current during start-up. This is achieved by forcing the V_{OUT} to follow the voltage on a soft start capacitor. A constant current source of 5 µA charges the C_{SS}, generating a linear ramp up voltage on C_{SS}.

The inrush current is proportional to the load capacitance and rising slew rate. The following equation can be used to calculate the slew rate required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

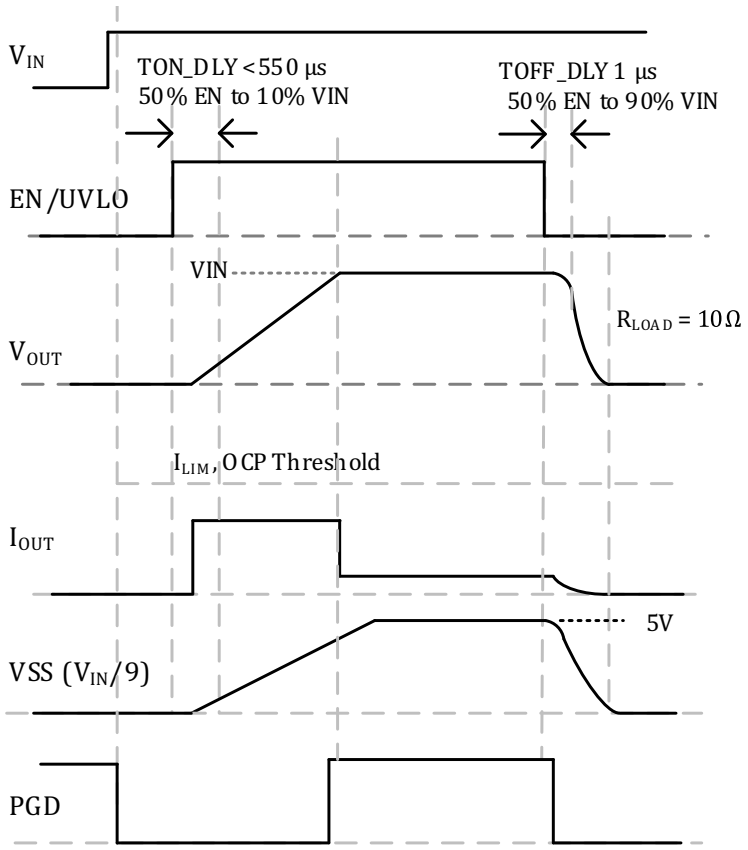
$$SR\ (V/ms) = \frac{I_{INRUSH}\ (mA)}{C_{OUT}\ (\mu F)}$$

$$T_{SS} = \frac{V_{IN}}{SR} = V_{IN} \times \frac{C_{OUT}\ (\mu F)}{I_{INRUSH}\ (mA)}$$

An external capacitor can be connected to the soft start (SS) pin to control the rising slew rate and lower the inrush current during turn-on. The output voltage follows the required C_{SS} capacitance to produce a given slew rate, which can be calculated using the following formula:

$$C_{SS} = \frac{(I_{SS} \times 9)}{SR}$$

The fastest output slew rate is achieved by leaving the soft start pin open.



PGD is pulled through a resistor to an external voltage source

Fig. 38

CURRENT LIMIT SETTING

The SIP32434A and SIP32434B actively monitor the current flow through the switch and provide a quick response to over-current conditions by actively regulating the current to a set limit. The current limit is set by connecting a resistor between the I_{LIM} pin and GND. R_{SET} can be calculated by the following formula for a desired current limit:

$$SR\ (V/ms) = \frac{I_{INRUSH}\ (mA)}{C_{OUT}\ (\mu F)}$$

$$R_{SET} = \frac{0.6\ V}{I_{LIM}} \times 20\ 600$$

When the load current exceeds the threshold (I_{LIM}), the parts respond within 1 µs (typ.) to turn off the switch and then regulate the switch gate voltage to limit the output current to the set I_{LIM} level. During this brief period before the over-current protection circuit is engaged, the parts will see a surge current, especially under a severe output short condition. The magnitude of the surge current developed during the period when the over-current protection is not engaged is determined by impedance in the loop from the input current source to ground and the response time. This impedance is the sum total of the current source impedance, the path resistance and inductance, and the load impedance.

If the over-current condition persists for more than 6 ms / typ., the switch shuts off. When V_{OUT} falls below 95 % of V_{IN}, the PGD is pulled low. The device will exit current limiting when the load current falls below I_{LIM} before the end of the current limit period. The control circuit will increase the gate drive in the same manner as the soft start when the switch exits from the current limit mode.

The current limit mode could result in excessive power on the switch, which increases the T_J quickly. The SIP32434A and SIP32434B have OTP, providing an enhanced level of production.

Once the device is off due to OCP or OTP faults, the SIP32434A stays in the latch-off state and the SIP32434B auto-retries after 32 times of the programmed soft start time. They can be reset by toggling V_{IN} or EN / UVLO.

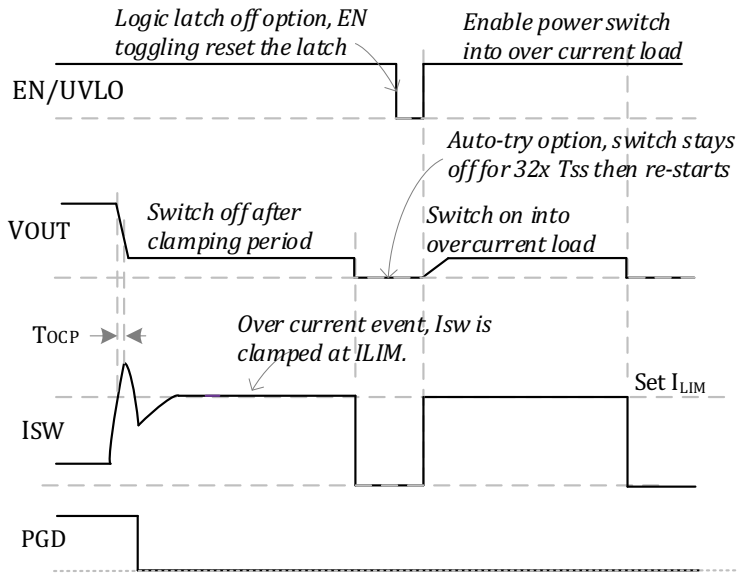


Fig. 39 - Over-Current Protection

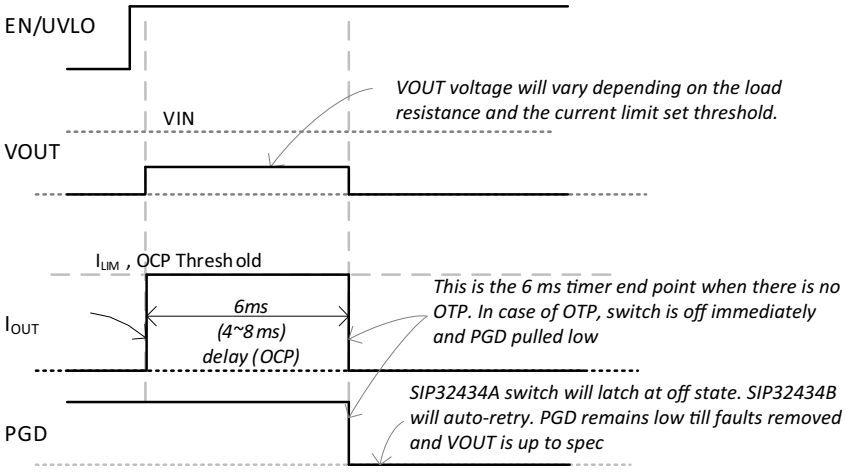


Fig. 40 - Turn On Into Over-Current Load

OTP, OVER-TEMPERATURE PROTECTION

Over-temperature protection turns off the power switch when the die temperature reaches the OTP threshold of 165 °C. The hysteresis is 45 °C. When the die temperature drops below 120 °C, it is allowed to turn on again.

PGD, POWER GOOD REPORTING

PGD is an open drain output. A pull-up resistor must be connected pulling to 3 V or 5 V. It is asserted low when V_{OUT} is below 95 % of V_{IN}, or an over-current, over-voltage, or over-temperature fault condition occurs.

INPUT CAPACITOR

While bypass capacitors at the input pins are not required, a 2.2 µF or larger capacitors for C_{IN} is recommended in almost all applications. The bypass capacitors should be placed as physically close to the device's input pins and ground to be effective to minimize transients on the input. Ceramic capacitors are recommended over tantalum because of their ability to withstand input current surges from low impedance sources such as batteries. For hot-plug applications, where input path inductance is negligible, this input capacitor can be minimized or eliminated.

OUTPUT CAPACITOR

The SIP32434A and SIP32434B do not require an output capacitor for proper operation. A proper value C_{OUT} is recommended to accommodate load transient per circuit design requirements. There are no ESR or capacitor type requirements.

Protection

LAYOUT GUIDELINES

The SIP32434A and SIP32434B are protection switches designed to maintain a constant output load current upon over-current fault. Optimized layout with efficient heat sinking is critical. It is recommended to put as much copper as possible to the devices' central exposed pad which is connected to ground. Connect all ground planes with all possible thermal VIAs.

The circuit setting components should be laid close to their connection pins. The components include current limit setting resistor, soft start setting capacitor, and resistors connected to EN / UVLO and OVP pins.

Protection devices such as input TVS or output Schottky diodes must be located close the pins to be protected and routed with short traces to reduce inductance.

Below is a layout example.

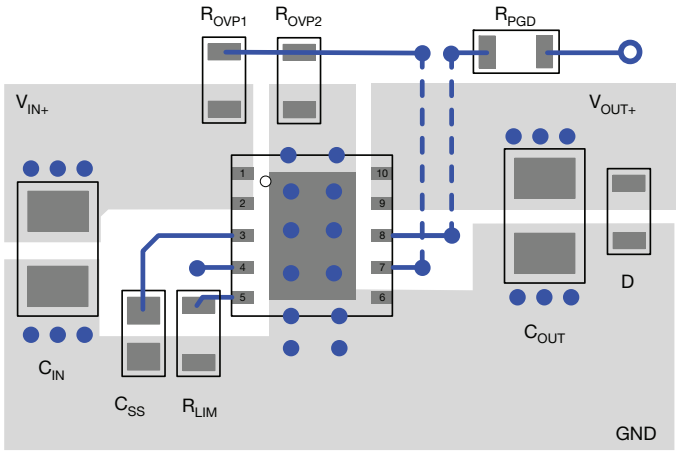


Fig. 41

PRODUCT SUMMARY		
Part number	SIP32434A	SIP32434B
Description	6 A, 33 mΩ, 2.8 V to 23 V, programmable OVP and current limit, latch-off on fault	6 A, 33 mΩ, 2.8 V to 23 V, programmable OVP and current limit, auto retry on fault
Configuration	Single	Single
Slew rate time (µs)	Adjustable	Adjustable
On delay time (µs)	190	190
Input voltage min. (V)	2.8	2.8
Input voltage max. (V)	28	28
On-resistance at input voltage min. (mΩ)	33	33
On-resistance at input voltage max. (mΩ)	33	33
Quiescent current at input voltage min. (µA)	180	180
Quiescent current at input voltage max. (µA)	250	250
Output discharge (yes / no)	N	N
Reverse blocking (yes / no)	N	N
Continuous current (A)	6	6
Package type	DFN33-10L	DFN33-10L
Package size (W, L, H) (mm)	3.0 x 3.0 x 0.9	3.0 x 3.0 x 0.9
Status code	Active	Active
Product type	Slew rate, current limit	Slew rate, current limit
Applications	Computers, consumer, industrial, healthcare, networking, portable	Computers, consumer, industrial, healthcare, networking, portable

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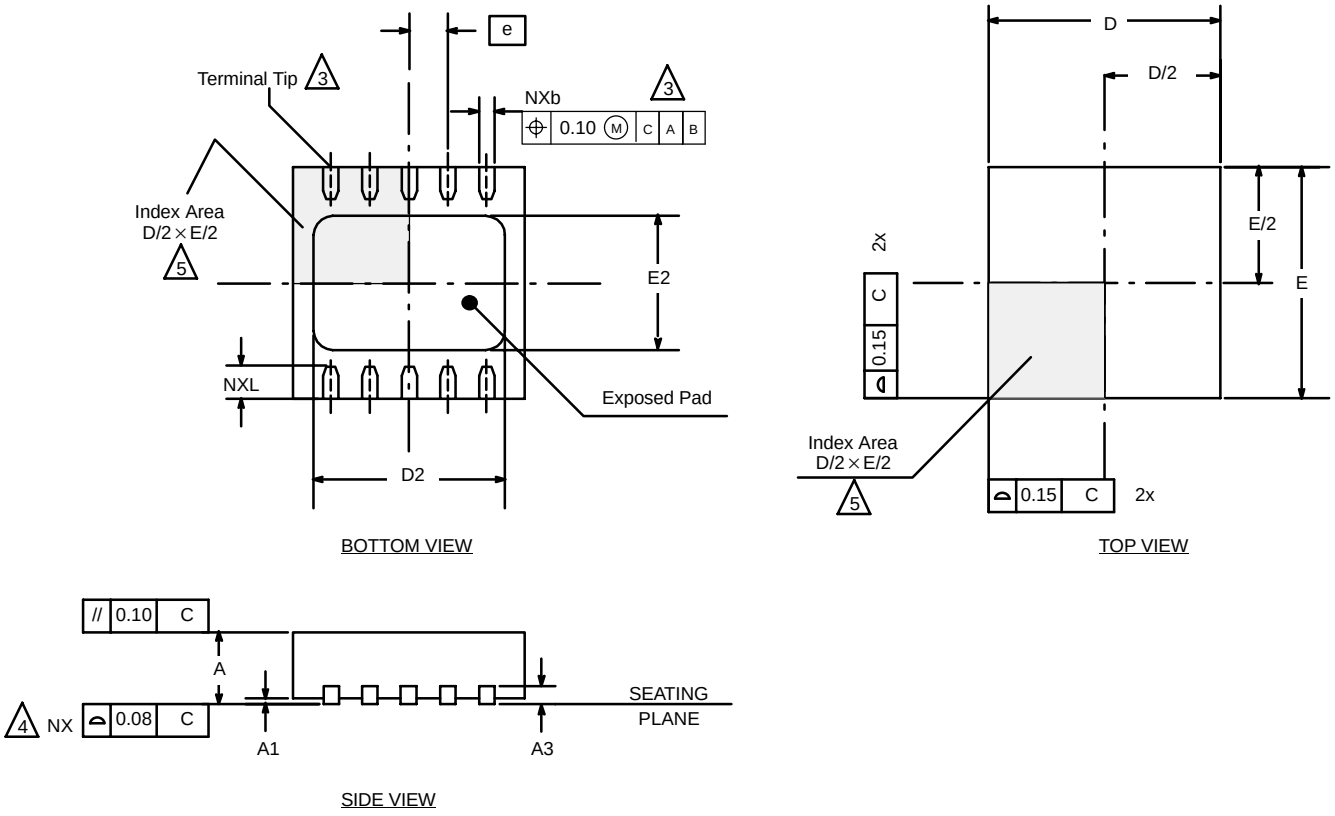
DFN-10 LEAD (3 X 3)



NOTES:

1. All dimensions are in millimeters and inches.
2. N is the total number of terminals.
3. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30 mm from terminal tip.
4. Coplanarity applies to the exposed heat sink slug as well as the terminal.
5. The pin #1 identifier may be either a mold or marked feature, it must be located within the zone iindicated.

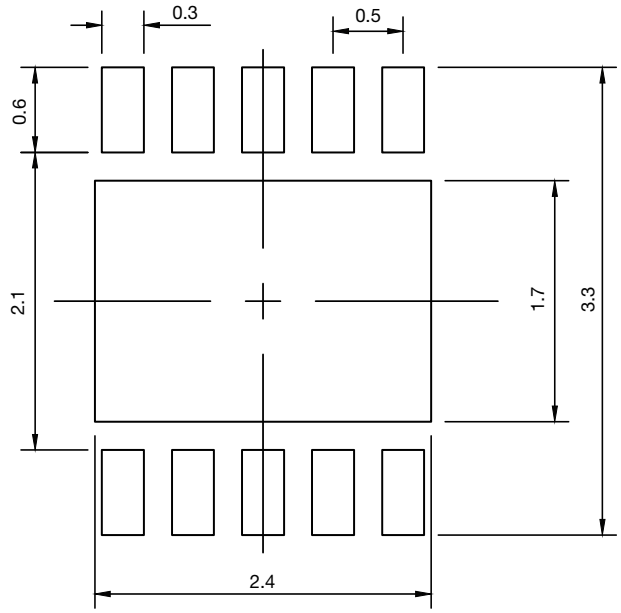
Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 BSC			0.008 BSC	
b	0.18	0.23	0.30	0.007	0.009	0.012
D		3.00 BSC			0.118 BSC	
D2	2.20	2.38	2.48	0.087	0.094	0.098
E		3.00 BSC			0.118 BSC	
E2	1.49	1.64	1.74	0.059	0.065	0.069
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

*Use millimeters as the primary measurement.

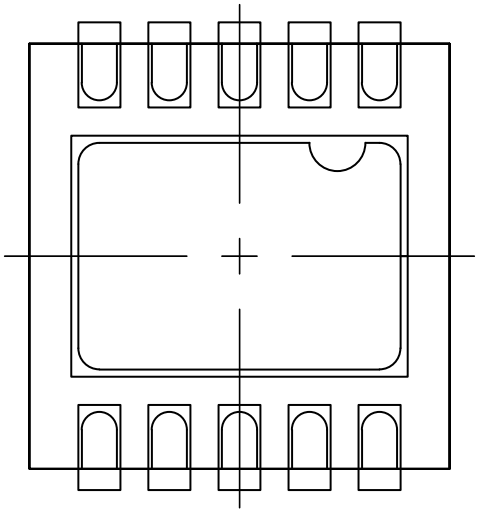
ECN: S-42134—Rev. A, 29-Nov-04
DWG: 5943

Recommended Minimum PAD for DFN10 3 mm x 3 mm

Recommended Land Pattern



Recommended Land Pattern vs. Case Outline



Note: Dimension are in millimeters

ECN: S22-0379-Rev. A, 02-May-2022
DWG: 3008

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