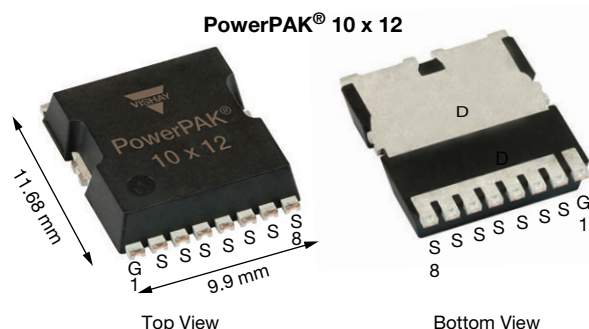


N-Channel 100 V (D-S) MOSFET



PRODUCT SUMMARY

V _{DS} (V)	100
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.0014
R _{DS(on)} max. (Ω) at V _{GS} = 7.5 V	0.0016
Q _g typ. (nC)	131
I _D (A) ^a	417
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK® 10 x 12
Lead (Pb)-free and halogen-free	SiJK5100E-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	100	V
Gate-source voltage		V _{GS}	± 20	
Continuous drain current (T _J = 175 °C)	T _C = 25 °C	I _D	417	A
	T _C = 100 °C		295	
	T _A = 25 °C		74 ^{b, c}	
	T _A = 100 °C		52 ^{b, c}	
Pulsed drain current (t = 100 μs)		I _{DM}	700	
Continuous source-drain diode current	T _C = 25 °C	I _S	487	
	T _A = 25 °C		15 ^{b, c}	
Single pulse avalanche current	L = 0.1 mH	I _{AS}	65	mJ
Single pulse avalanche energy		E _{AS}	214	
Maximum power dissipation	T _C = 25 °C	P _D	536	W
	T _C = 100 °C		268	
	T _A = 25 °C		17 ^{b, c}	
	T _A = 100 °C		8.3 ^{b, c}	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	$t \leq 10$ s	R_{thJA}	6.3	9	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	0.21	0.28	

Notes

- $T_C = 25\text{ }^\circ\text{C}$
- Surface mounted on 1" x 1" FR4 board
- $t = 10\text{ s}$
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 10 x 12 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is $39\text{ }^\circ\text{C/W}$

FEATURES

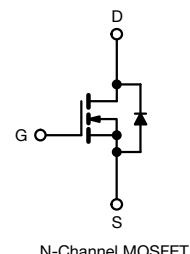
- TrenchFET® Gen V power MOSFET
- Leadership $R_{DS(on)}$ minimizes power loss from conduction
- 100 % R_g and UIS tested
- Standard level FET
- Enhance power dissipation and lower R_{thJC}
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- Automation
- OR-ing and hot swap switch
- Power supplies
- Motor drive control
- Battery management



N-Channel MOSFET



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	55	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-8	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2	-	4	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 80 A	-	0.00110	0.00140	Ω
		V _{GS} = 7.5 V, I _D = 80 A	-	0.00125	0.00160	
Forward transconductance ^a	g _{fs}	V _{DS} = 25 V, I _D = 100 A	-	245	-	S
Dynamic ^b						
Input capacitance	C _{iSS}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	-	11 480	-	pF
Output capacitance	C _{oss}		-	3210	-	
Reverse transfer capacitance	C _{rSS}		-	17	-	
Total gate charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 20 A	-	131	200	nC
Gate-source charge	Q _{gs}		-	53	-	
Gate-drain charge	Q _{gd}		-	5.3	-	
Total gate charge	Q _g	V _{DS} = 50 V, V _{GS} = 7.5 V, I _D = 20 A	-	97.4	146	
Output charge	Q _{oss}	V _{DS} = 50 V, V _{GS} = 0 V	-	330	-	Ω
Gate resistance	R _g	f = 1 MHz	0.2	0.8	1.6	
Turn-on delay time	t _{d(on)}	V _{DD} = 50 V, R _L = 5 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	32	65	ns
Rise time	t _r		-	15	30	
Turn-off delay time	t _{d(off)}		-	54	110	
Fall time	t _f		-	35	70	
Turn-on delay time	t _{d(on)}	V _{DD} = 20 V, R _L = 5 Ω, I _D ≅ 10 A, V _{GEN} = 7.5 V, R _g = 1 Ω	-	41	80	ns
Rise time	t _r		-	18	35	
Turn-off delay time	t _{d(off)}		-	47	95	
Fall time	t _f		-	35	70	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	487	A
Pulse diode forward current	I _{SM}		-	-	700	
Body diode voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V	-	0.7	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	140	280	ns
Body diode reverse recovery charge	Q _{rr}		-	360	720	nC
Reverse recovery fall time	t _a		-	61	-	ns
Reverse recovery rise time	t _b		-	79	-	

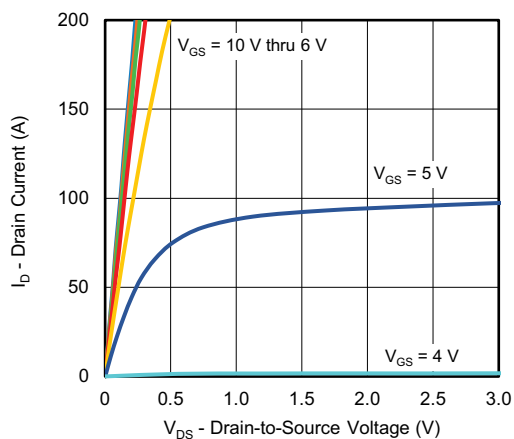
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

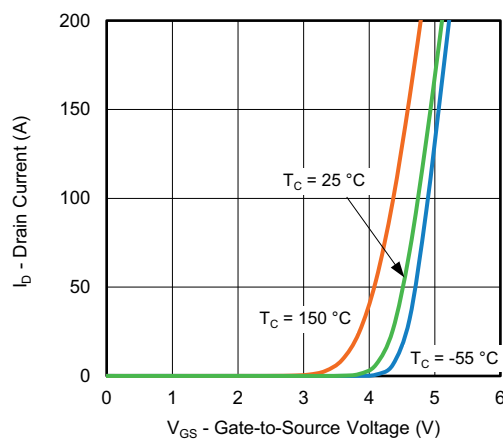
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



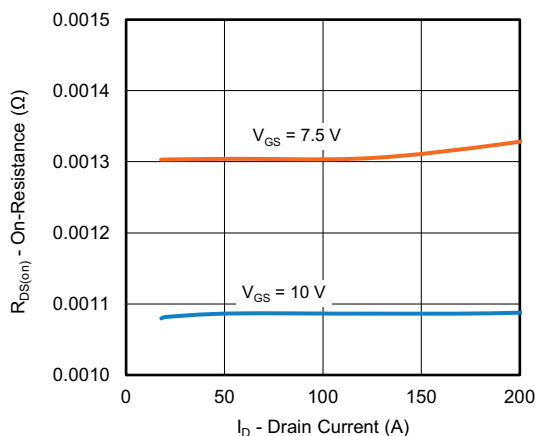
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



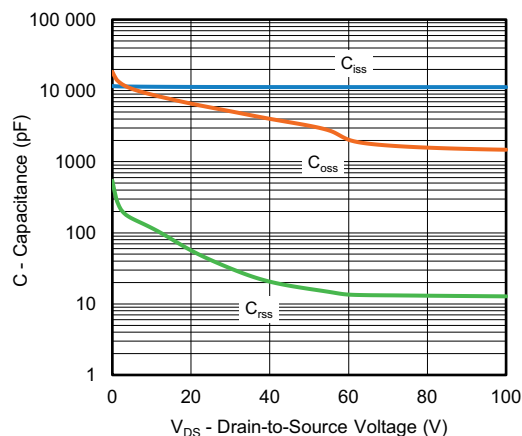
Output Characteristics



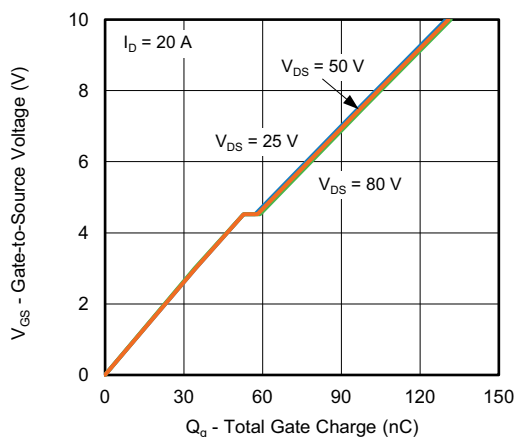
Transfer Characteristics



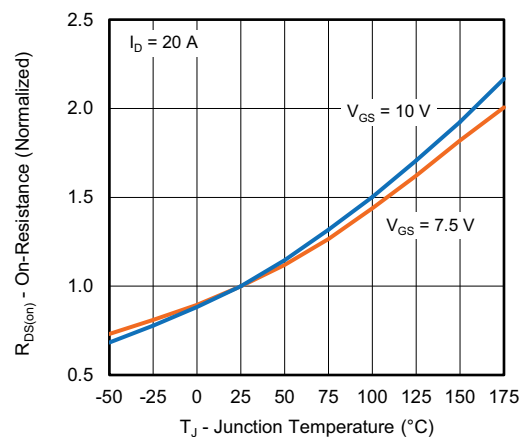
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



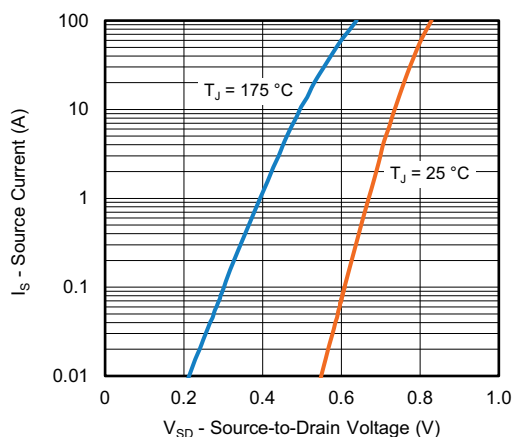
Gate Charge



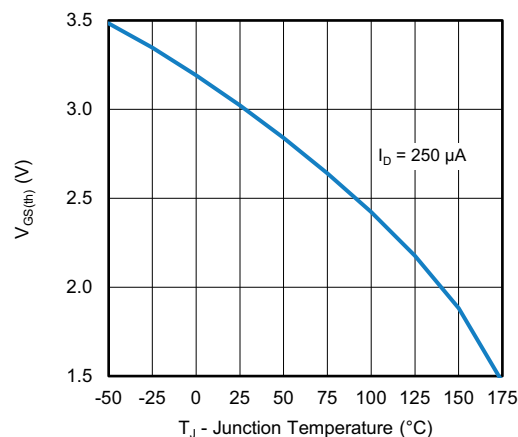
On-Resistance vs. Junction Temperature



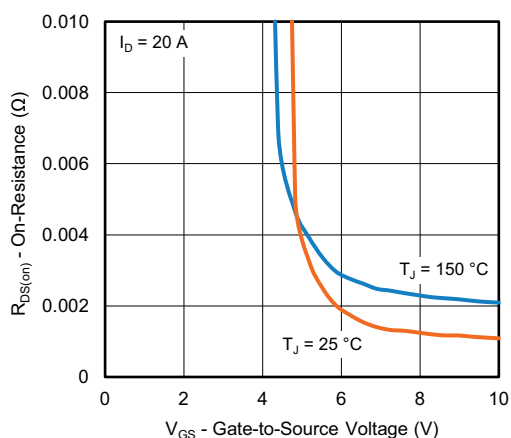
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



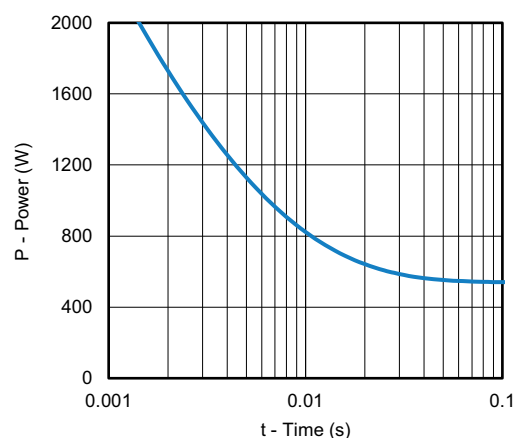
Source-Drain Diode Forward Voltage



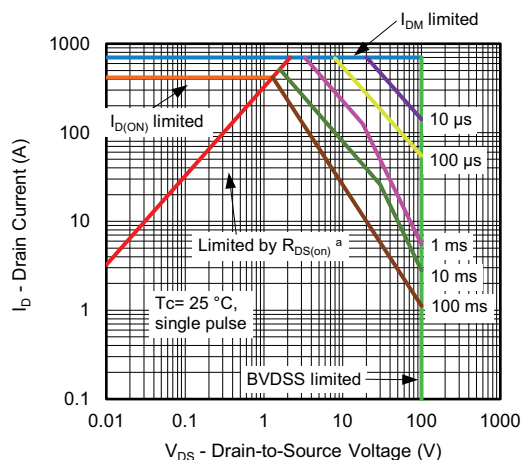
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Case



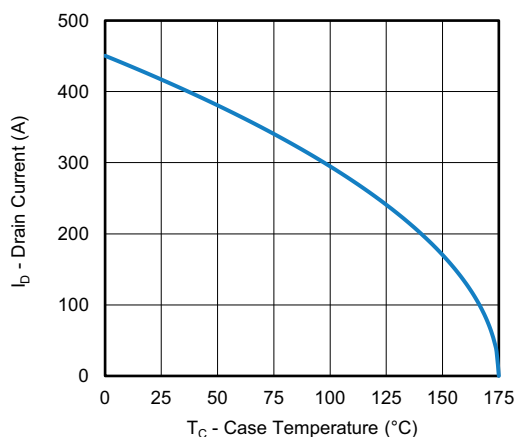
Safe Operating Area, Junction-to-Ambient

Note

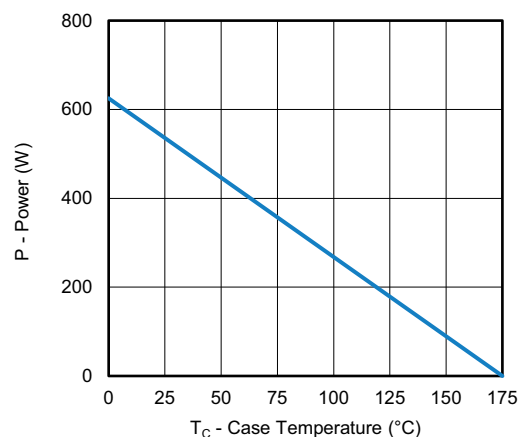
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



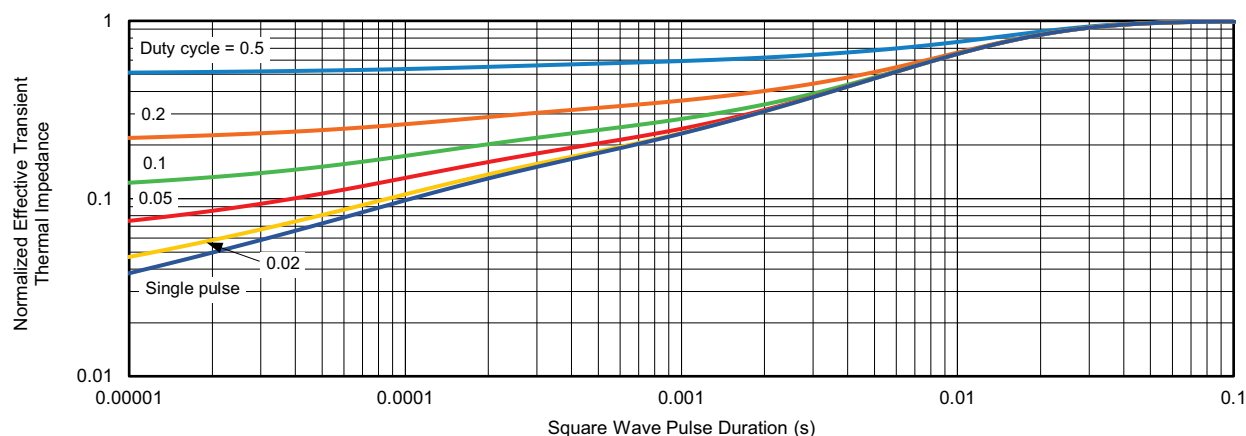
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Case

Note

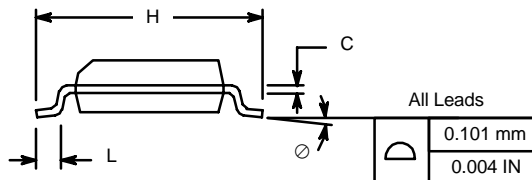
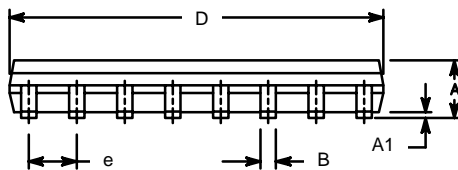
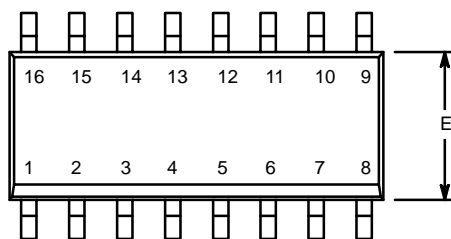
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

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SOIC (NARROW): 16-LEAD

JEDEC Part Number: MS-012

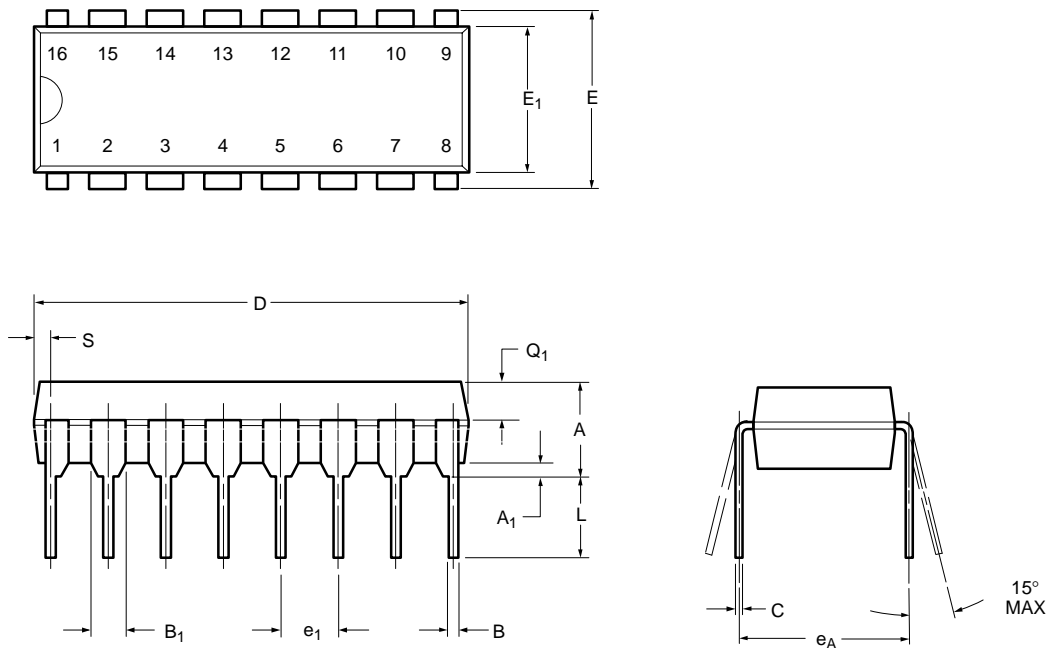


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⌀	0°	8°	0°	8°

ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



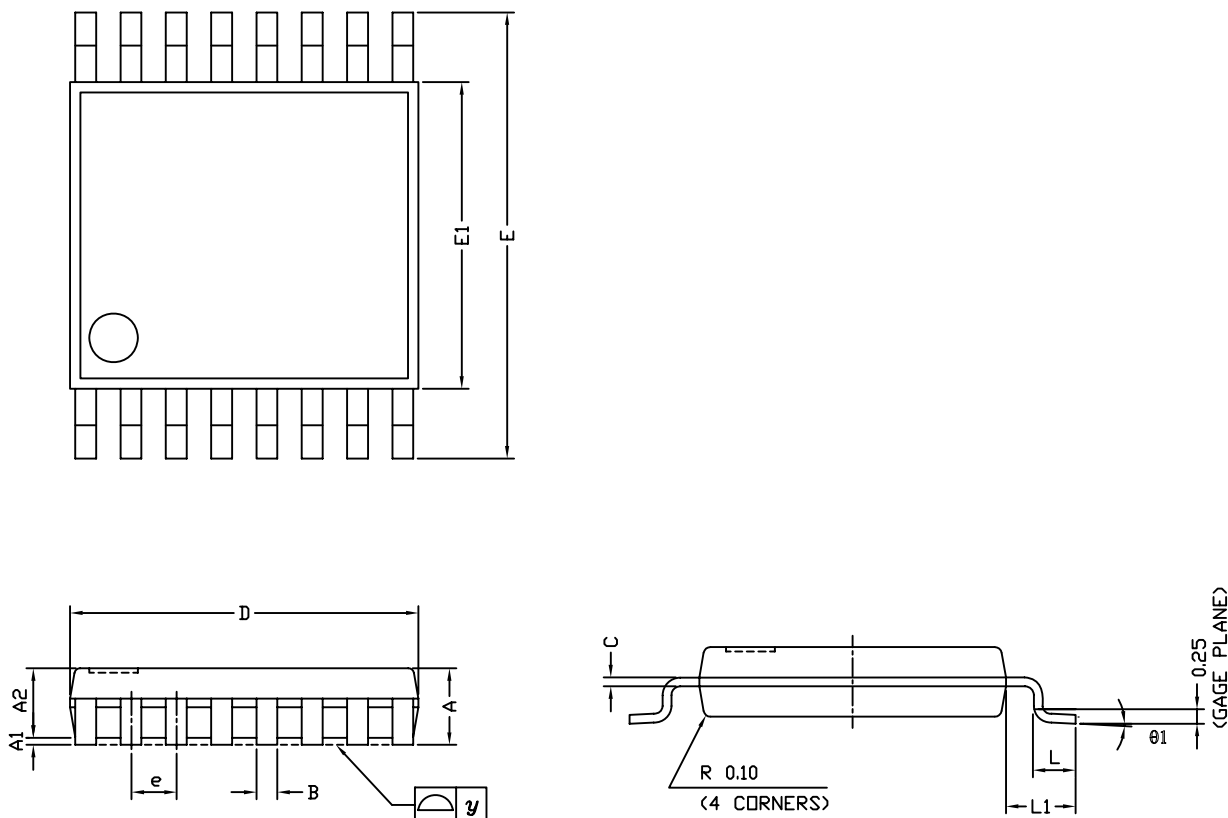
PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A ₁	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B ₁	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E ₁	5.59	7.11	0.220	0.280
e ₁	2.29	2.79	0.090	0.110
e _A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q ₁	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060

ECN: S-03946—Rev. D, 09-Jul-01
DWG: 5482

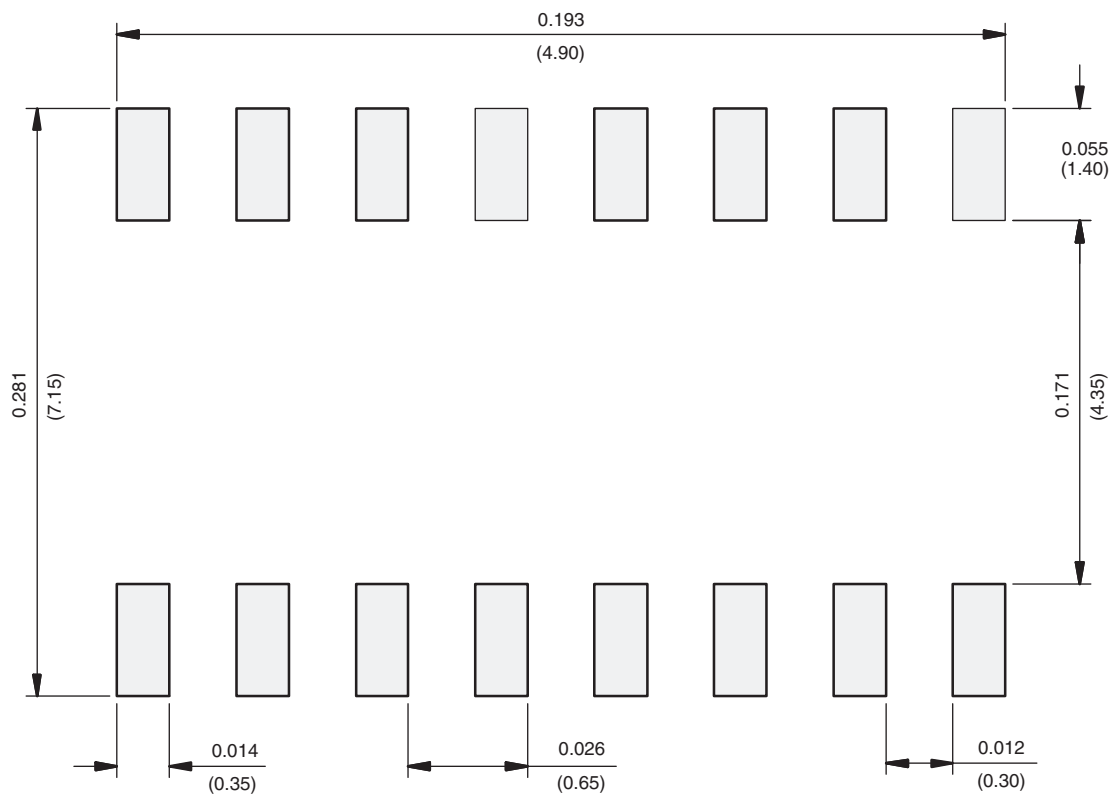
TSSOP: 16-LEAD



Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06			
DWG: 5624			

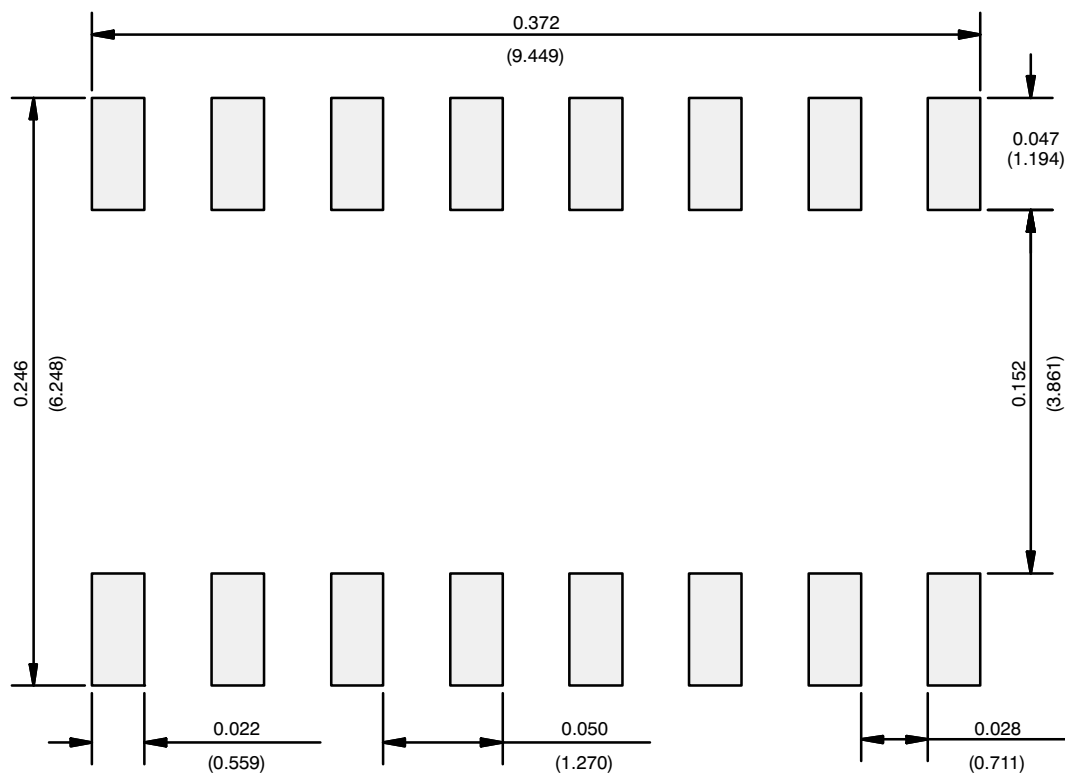


RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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