

## Power Switching Device

# Gate-source voltage behaviour in a bridge configuration

Power switching devices such as MOSFETs and IGBTs are used for various kinds of power supply applications, power supply line switching components, and other power applications. In addition, the circuit topologies used are diverse, parallel and series connections are widely used, not to mention single device use. Especially in bridge circuit configuration, in which the devices are connected in series, it is common to turn on and turn off each device alternately. Due to the current flowing and the voltage change in each device, the devices greatly affect one another. In this application note, we focus on Gate-Source voltage in MOSFET bridge configuration based on one of the simplest power circuits, a synchronous rectification boost converter to understand the switching operation in detail.

## A bridge configuration of MOSFETs

A synchronous rectification boost circuit, the simplest bridge structure consisting of MOSFETs, is shown in the schematic (Figure. 1)

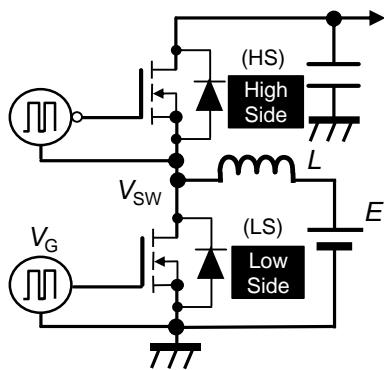


Figure 1: Synchronous rectification BOOST circuit

In this circuit, see Figure 1, the high-side (HS) and low-side (LS) MOSFETs turn on alternately. A dead time, where both transistors are in off-state, is set in order to avoid cross conduction where both devices are on. (Figure 2). This is so that you can later refer to HS and LS meaning the MOSFETs without having to say "the LS MOSFET" or "the HS MOSFET" every time later.

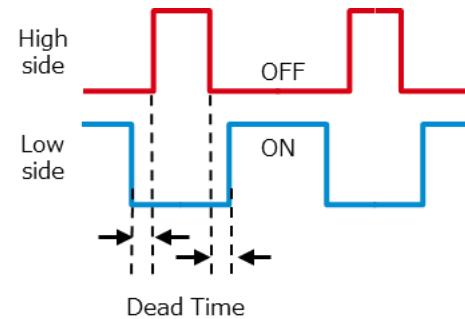


Figure 2: Gate signal ( $V_G$ ) sequence

In Figure 3, the waveforms of the drain-source voltage ( $V_{ds}$ ) and drain current ( $I_d$ ) are sketched respectively for the HS and LS transistors shown in Figure 1. This is an example of hard-switching, where the current flowing through the inductor  $L$  is continuous.

The horizontal axis denotes time, and the time periods  $T_k$  ( $k=1 \sim 8$ ) are defined as follows:

- T1: LS is ON, and  $I_d$  of the MOSFETs varies
- T2: LS is ON, and  $V_{ds}$  of the MOSFETs varies
- T3: LS is ON, and  $I_d$  and  $V_{ds}$  are nearly stable
- T4: LS is OFF, and  $V_{ds}$  of the MOSFETs varies
- T5: LS is OFF, and  $I_d$  of the MOSFETs varies
- T4-T6: Dead time, LS is OFF until HS turns ON

T7: HS is ON (synchronous rectification)

T8: Dead time, HS is OFF until LS turns ON

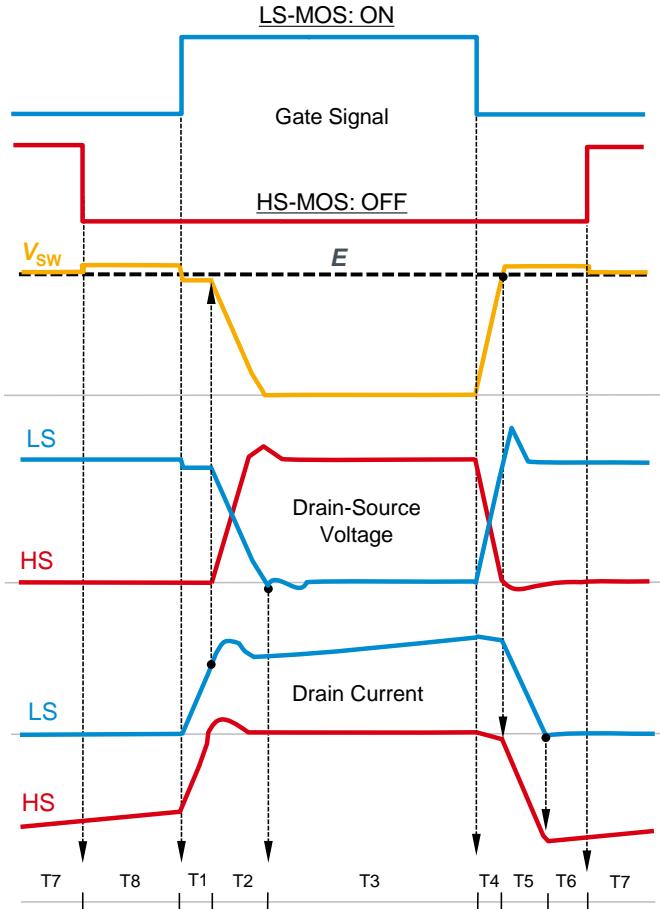


Figure 3: Voltage and current waveforms of HS and LS MOSFET.

## Gate driver

In order to analyze how the changes of  $V_{ds}$  and  $I_d$  affect the gate-source voltage ( $V_{gs}$ ) of transistors, an equivalent circuit for the gate drive has been provided in Figure 4.

The equivalent circuit includes: a gate signal ( $V_G$ ), a gate resistance internally embedded in the MOSFET ( $R_{g,int}$ ), the source inductance of the device package ( $L_{source}$ ), the inductance of the gate-driver circuit layout ( $L_{trace}$ ), and an external gate resistance ( $R_{g,ext}$ ). Selected voltage polarities and current directions have been indicated in the diagram.

The inductance generated by the internal wiring of a transistor should also be taken into account, but this value is negligible in

comparison to  $L_{trace}$ . Thus this inductance is ignored here.

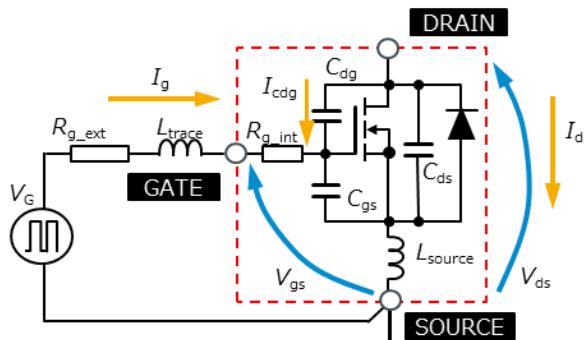


Figure 4: The equivalent circuit of a gate-drive circuit and a MOSFET.

## Turn-on and -off operation

The following paragraphs describe each waveform segment as sketched in Figure 3.

When a positive supply,  $V_G$  is applied to the gate of LS to turn it on, the gate-source capacitance ( $C_{gs}$ ) of LS starts to charge and  $V_{gs}$  increases. When  $V_{gs}$  goes over the threshold voltage,  $V_{gs(th)}$ , the drain current  $I_d$  of LS starts to flow and simultaneously the drain current  $I_d$  of HS starts to decrease (Figure 3-T1).

Finally, the HS  $I_d$  reaches zero and its body diode turns off, reducing the voltage between the HS source and the LS drain ( $V_{sw}$ ). Simultaneously, the drain-source capacitance ( $C_{ds}$ ) and the drain-gate capacitance ( $C_{dg}$ ) of HS begins to change (Figure 3-T2). When this charging process is completed (the counterpart capacitances of LS discharge) and the  $V_{gs}$  of LS reaches  $V_G$ , the turn-on process of LS has been finished.

The  $V_G$  of LS going into the off-state initiates the turn-off of LS (figure 3-T4). The charge stored in  $C_{gs}$  of LS is then discharged and  $V_{gs}$  of LS reaches the plateau voltage (Miller-effect domain). Then the  $V_{ds}$  of LS begins to go up, and  $V_{sw}$  rises at the same time. At this point, most of the load current still flows through LS (see Figure 3-T4). The body diode of HS is not active yet. When the charging of  $C_{ds} + C_{dg}$  of LS is completed,  $V_{sw}$  goes over the supplied voltage ( $E$ ), the body diode of HS turns on, and  $I_d$  of LS starts to flow through HS (see Figure 3-T5). After  $I_d$  of LS finally reaches zero, the circuit goes into the effective dead time period

(see Figure 3-T6). The positive  $V_G$  is applied to the gate of HS, turning HS on and the synchronous operation begins (see Figure 3-T7).

In this sequence of the switching operation, the changes in  $V_{ds}$  and  $I_d$  of both HS and LS create various kinds of gate currents, making  $V_{gs}$  behaviour differ from the original  $V_G$  signal. Figure 5 shows what types of gate currents arise in a boost bridge configuration. Each label of (I), (I'), (II), and (III) represents an individual phenomenon that leads to a change in  $V_{gs}$ .

The resulting  $V_{gs}$  waveform is depicted in Figure 6. The numbers therein correspond to the same phenomena as those indicated in Figure 5. The dotted line in  $V_{gs}$  is an ideal waveform of the gate-source voltage signal.

The details are given in the following paragraphs.

### Gate current generated by $dV_{ds}/dt$

As shown in Figure 4, a change in  $V_{ds}$  causes a current ( $I_{cdg}$ ) to flow through  $C_{dg}$ . This current, as shown in Figure 5, divides into one current charging  $C_{gs}$  ( $I_{cdg1}:(II)-1$ ) and the other current flowing into the gate-drive circuit ( $I_{cdg2}:(II)-2$ ). At the early stage of  $V_{ds}$  change, the impedance of the gate-drive circuit is large, and thereby  $I_{cdg}$  mainly flows into  $C_{gs}$ . At this point,  $I_{cdg1}$  is mathematically expressed as:

$$I_{cdg} \approx I_{cdg1} = \frac{C_{dg}}{1+C_{dg}/C_{gs}} \cdot \frac{dV_{ds}}{dt} \quad (1)$$

This equation reveals that large  $C_{dg}$  and/or small  $C_{dg}/C_{gs}$  ratio increase  $I_{cdg1}$ .

### $V_{gs}$ generated by $dI_d/dt$

The time-derivative of  $I_d$ ,  $dI_d/dt$ , generates the voltage expressed as:

$$V_{Lsource} = L_{source} \cdot \frac{dI_d}{dt} \quad (2)$$

This is the event (I) and the associated current (I') flows as shown in Figure 5.

$dV_{ds}/dt$  and  $dI_d/dt$  can take either a positive or a negative value, and thereby their consequent currents and voltages change polarity and direction, depending on whether turn-on or turn-off takes place. As shown in Figure 5, this voltage is seen by the measurement probes, but not by the device itself.

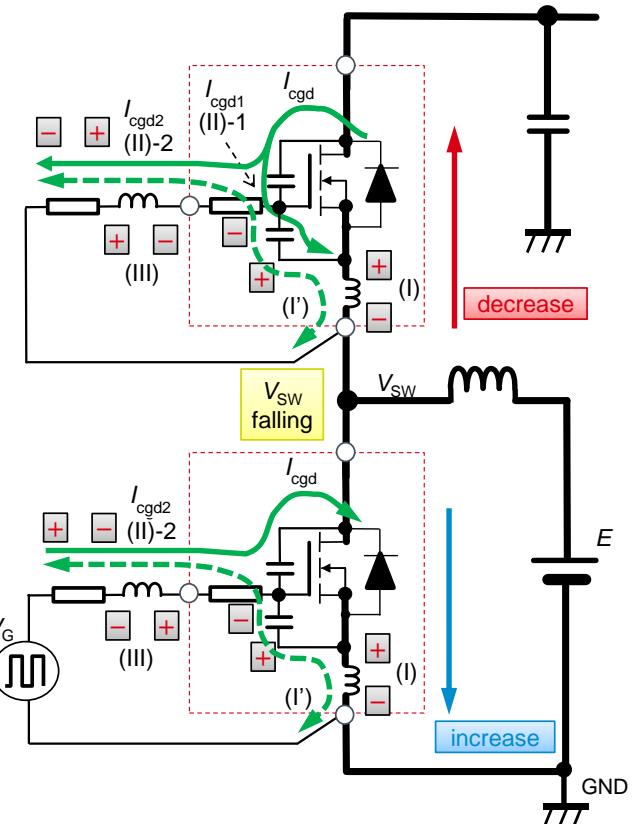


Figure 5: Gate current behaviour when LS turns on.

### $V_{gs}$ behaviour during turn-on

When LS turns on,  $I_d$  varies first, (see Figure 3-T1), and  $dI_d/dt > 0$  for both LS and HS. Thus the event (I) occurs and the electromotive force expressed by equation (2) arises in the parasitic source inductance with the polarity shown in Figure 5. This generates a current charging  $C_{gs}$  with its source side being a positive voltage. This charging polarity forces down  $V_{gs}$  of LS, and also pulls  $V_{gs}$  of HS into negative bias, observed as negative surge voltage.

When the LS  $I_d$  of LS settles, LS  $V_{ds}$  decrease (see Figure 3-T2). Thus the current, as expressed in equation (1), flows as indicated by (II)-1, and (II)-2 in Figure 5, making  $V_{gs}$  of HS go up as theoretically described by:

$$V_{surge2-1} = \frac{1}{C_{gs}} \int (I_{cdg1}) dt \\ = \frac{1}{1+C_{gs}/C_{dg}} \cdot \Delta V_{ds} \quad (3)$$

$$V_{surge2-2} = I_{cdg2} \cdot R_{g\_ext} + L_{trace} \cdot \frac{dI_{cdg2}}{dt} \quad (4)$$

The increase in  $V_{gs}$  described in equation (3) is the major event just after  $V_{ds}$  begins to change, but the increase in  $V_{gs}$ , predicted by equation (4) may be observed with time. This shows that the behaviour of  $V_{gs}$  is affected by the ratio  $C_{dg}/C_{gs}$  of the MOSFET, the  $R_{g\_ext}$  of the drive circuit, and the parasitic inductance  $L_{trace}$  due to the layout of the gate-drive circuit.

As can be seen in Figure 5,  $I_{cdg2}$  in the HS-side ((II)-2) forces up  $V_{gs}$ . If the  $V_{gs}$  value goes over the threshold value it causes the so-called self-turn-on of the HS MOSFET. If this happens, both LS and HS are in on-state, generating a short-circuit current through HS and LS.

$I_{cdg2}$  continues to flow until the turn-on of LS is completed, and the electromagnetic energy accumulates in  $L_{trace}$ . However, this current vanishes when the change of  $V_{sw}$  is finally completed, and thus  $L_{trace}$  generates a voltage as shown in Figure 5. This is event (III). This voltage can be larger than expected, because  $I_{cdg2}$  reaches several amperes in some cases, depending on the switching conditions, including  $R_{g\_ext}$ .

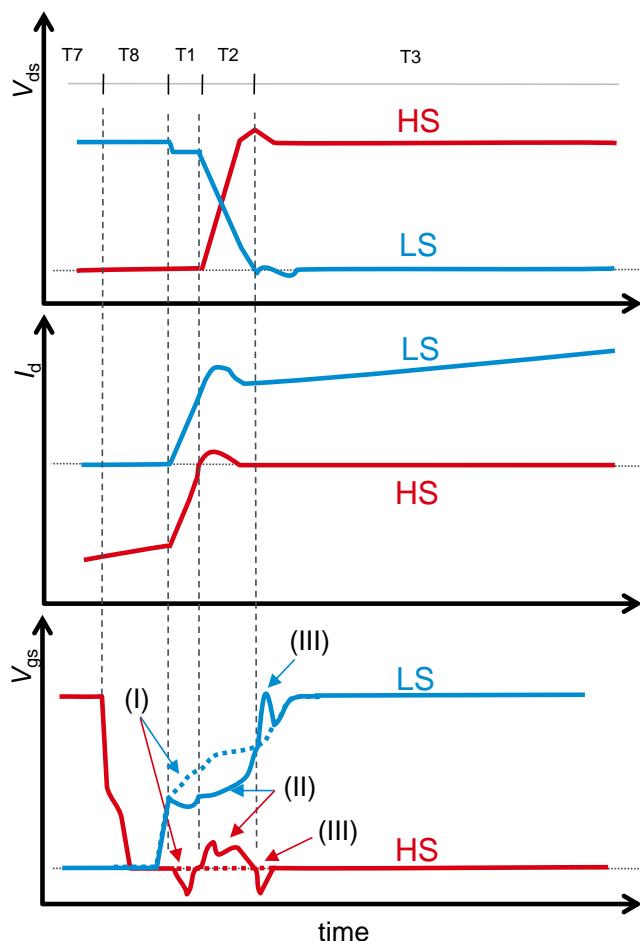


Figure 6:  $V_{ds}$ ,  $I_d$ , and  $V_{gs}$  waveforms when LS turns on.

Figure 7 shows the double-pulse test results for a bridge circuit comprising ROHM devices with the LS turning on.  $R_{g\_ext}$  is  $0\Omega$  for Figure 7(a) and  $10\Omega$  for Figure 7(b).

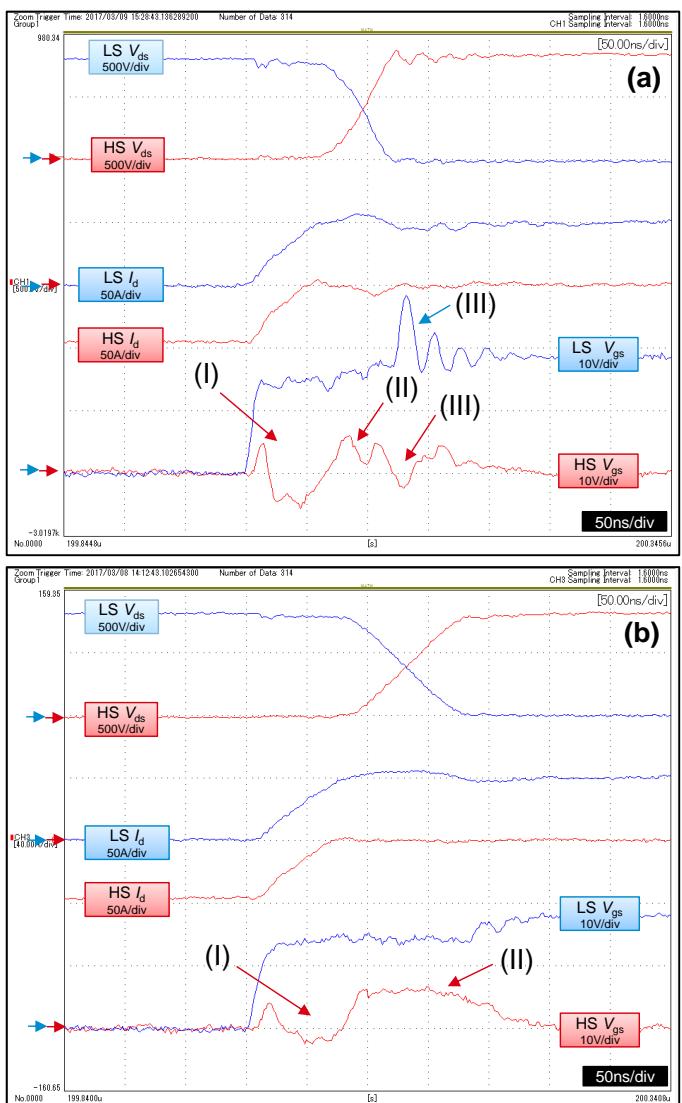


Figure 7: turn-on waveforms.

(a)  $R_{g\_ext}=0\Omega$ , (b)  $R_{g\_ext}=10\Omega$

Small  $R_{g\_ext}$ , as shown in Figure 7(a), enhances the reduction in  $V_{gs}$  caused by event (I). Event (III) can be clearly recognized due to very high speed switching.  $0\Omega$  of  $R_{g\_ext}$  makes event (II) less significant, but on the other hand the unintentional increase in  $V_{gs}$ , due to event (II)-2, is seen in Figure 7(b).

These results show that a small  $R_{g\_ext}$  at HS turning off is generally recommended to inhibit the raising of  $V_{gs}$  (related to event (II)-2) inducing the self-turn-on of HS when LS is in

on-state. However,  $R_{g\_ext}$  for HS and LS are usually equal. Due to this, small  $R_{g\_ext}$  enhances the increase in  $dV_{ds}/dt$  of LS, and consequently  $I_{cdg}$  in HS rises as shown in equation (1). This increases event (II) surge of HS, as can be easily understood by use of equation (4). In order to avoid this, it is recommended that you separately set  $R_{g\_ext}$  for turn-on and turn-off. A diode as shown in Figure 8 is one of the common methods to realize this.

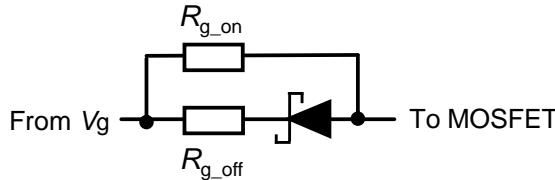


Figure 8: Adapted  $R_{g\_ext}$  circuit for different turn-on and turn-off gate resistance values

Here is another useful comment on the behaviour of  $V_{gs}$  : In Figure 7, HS  $V_{gs}$  goes positive for a moment before event-(I) occurs. This is conducted through  $C_{gs}$  by the voltage in  $L_{source}$  generated at the moment that the current relating to event (I) begins to flow.

### $V_{gs}$ behaviour during turn-off

Figure 9 shows how gate current flows when LS turns off. As we do for turn-on, each event is labelled as (IV), (V), and (VI). The fundamentals are the same for turn-off and turn-on, and the only difference is that  $V_{ds}$  and  $I_d$  change first. Each event has an equivalent one at turn-on:

<u>turn-off</u>	<u>turn-on</u>
event (IV)	→ event (II)
event (V)	→ event (III)
event (VI)	→ event (I)

Event (IV) is related to an unintentional increase in  $V_{gs}$  of LS caused by  $dV_{ds}/dt$  and a negative surge in  $V_{gs}$  of HS (see Figure 3-T4). After T4 ends, event (V) occurs because the voltage surge is caused by the energy due to  $I_{cdg1}$  as expressed in equation (1). After this,  $I_d$  starts to vary (see Figure 3-T6), and this time-derivative creates a voltage in  $L_{source}$  (equation (2)), which drives the current related to event (VI) as shown in Figure 9.

This current charges  $C_{gs}$  positively, and hence  $V_{gs}$  is raised up in HS and LS. This phenomenon opposes the decrease of

$V_{gs}$  in LS. All these events are summarized in the  $V_{gs}$  waveforms shown in Figure 10. The dotted line in  $V_{gs}$  represents an ideal gate-source voltage waveform.

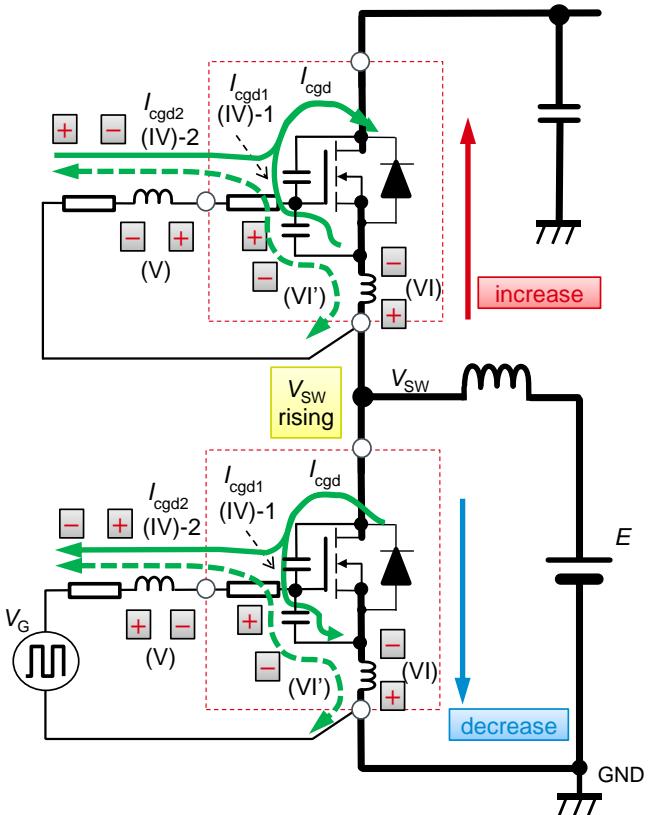


Figure 9: Gate current flow when LS turns off.

Figure 11 shows the double-pulse test results for a bridge circuit comprising ROHM devices with LS turning off.  $R_{g\_ext}$  is  $0\Omega$  for Figure 11(a) and  $10\Omega$  for Figure 11(b).

One can easily observe an event-(V) surge. The effects of event (IV) by  $dV_{ds}/dt$  are not generally significant, but the negative surge voltage in HS caused by this is often larger than the negative  $V_{gs}$  rating of SiC-MOSFETs. It is therefore necessary to prepare countermeasure circuitry. A small  $R_{g\_ext}$  is generally effective to reduce the negative surge voltage in HS during turn off. However, the common  $R_{g\_ext}$  circuit as shown in Figure 8 makes event (IV) worse because  $R_{g\_on}$  is usually a highly resistive. Care should be taken to ensure that  $R_{g\_on}$  is not too big. (An example of the countermeasure circuit is provided in another application note.)

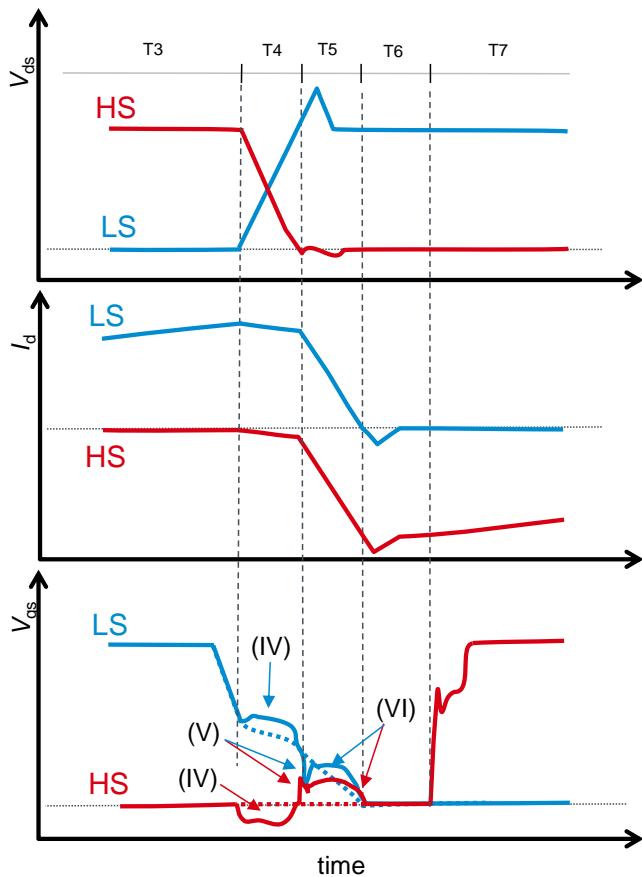


Figure 10:  $V_{ds}$ ,  $I_d$ , and  $V_{gs}$  waveforms when LS turns off.

The voltage hump in  $V_{gs}$  related to event (VI) occurs a moment before the turn-off operation completes. Therefore, if HS begins to turn on, it is not serious because LS is already turned off.

## Summary

As has been described, the behaviour of  $V_{gs}$  in a bridge configuration is not trivial, because the MOSFETs interact with each other, and the gate-drive part plays an important role in determining the switching behaviour of the MOSFETs. It is therefore necessary to observe very different behaviours for different circuit board layouts even given the same circuit topology. Firstly, one should understand the fundamentals MOSFET behaviour as provided in this explanation, in order to optimise circuit performance. In this example a boost circuit with LS switching was used but a similar approach may be used for

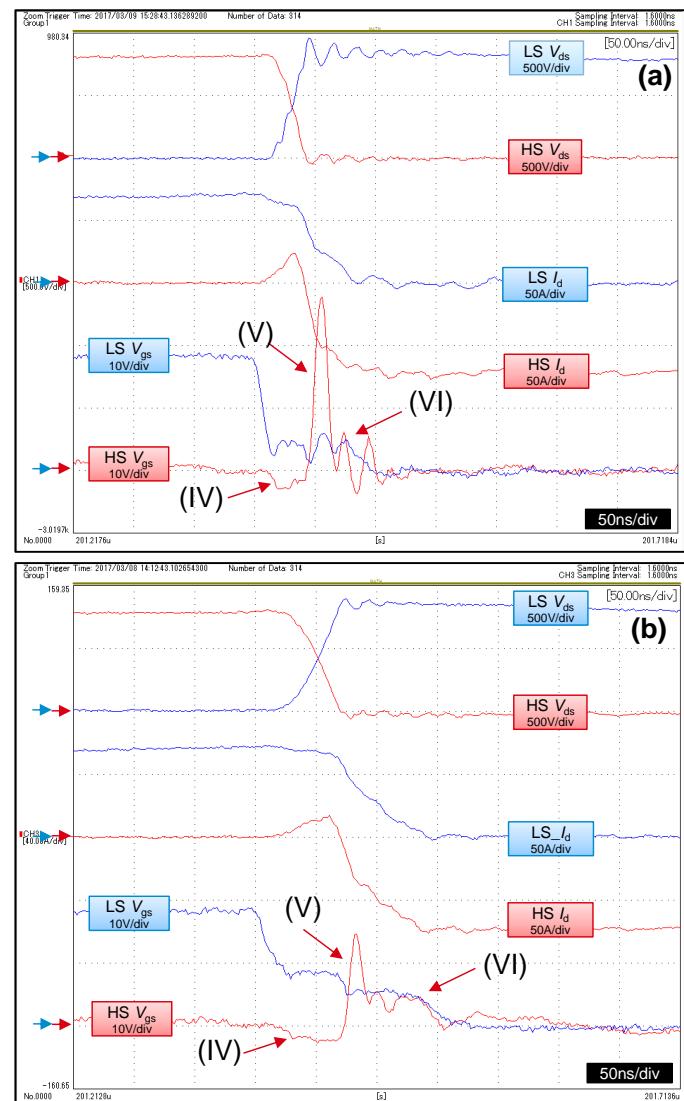


Figure 11. turn-off waveforms.

(a)  $R_{g\_ext}=0\Omega$ , (b)  $R_{g\_ext}=10\Omega$

a buck converter with HS switching by replacing the function of LS and HS. These principles may in fact be applied to various circuit topologies which use hard switching.

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