RAA2S4252B

Automotive Sensor Signal Conditioner with Analog Output

Description

The RAA2S4252B is a member of Renesas' family of CMOS integrated circuits for highly accurate amplification and sensor-specific correction of differential bridge sensor signals. Featuring a maximum analog pre-amplification of 900 with analog sensor offset correction (XSOC), the RAA2S4252B is adjustable to nearly all resistive bridges.

Conditioning calculation is accomplished via a 16-bit RISC microcontroller. Calibration coefficients and configuration data are stored in the nonvolatile memory (NVM), which is reliable in automotive applications.

Measured values are provided via a ratio-metric analog output signal. End-of-line calibration is also supported through this output pin via a One-Wire Interface (OWI). Digital calibration helps keep assembly cost low as no trimming by external devices or lasers is needed.

The RAA2S4252B is optimized for harsh automotive environments by over-voltage and reverse polarity protection circuitry, excellent electromagnetic compatibility, and multiple diagnostic features.

Typical Applications

- Pressure sensing in hydraulic and pneumatic systems
- HVAC pressure measurement
- Differential and single ended bridge sensor readout

Available Support

- Evaluation Kit
- Application Notes
- Calculation Tools

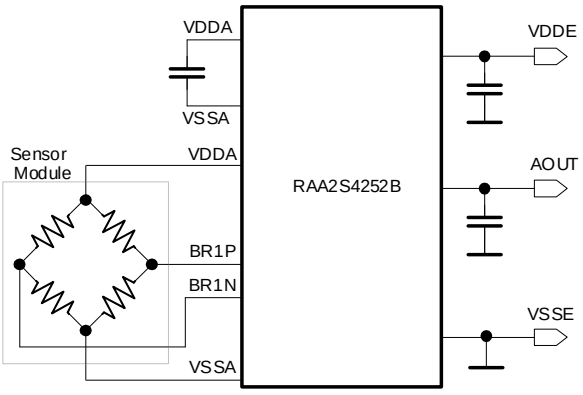
Features

- Differential bridge sensor input with selectable on-chip or external PN-junction temperature sensor
- 0.5mV/V to 800mV/V sensor span with 13 to 18bit resolution; supported sensor offset/span ratio of 10
- Digital compensation for offset, gain, and higher order nonlinearity as well as for temperature coefficients of measured bridge sensor input signal
- Accuracy: 1%FS at -40°C to 150°C
- Output update rate of 100µs in fastest mode; comparable analog bandwidth in 3kHz region
- Higher order digital LPF with cut-off frequency of 10Hz to 1000Hz, and configurable transfer characteristic
- One-pass, end-of-line calibration algorithm minimizes production costs: fast in calibration. Statistical based temperature calibration point minimization is supported.
- Minimum amount of external components enables design of sensor modules with best-in-class form factor
- Qualified according to AEC-Q100 Grade 0; operating temperature range: -40°C to 150°C

Physical Characteristics

- Operation supply: 4.5V to 5.5V
- Protection up to ±40V; robust in automotive
- Output resolution: 12-bit analog output; signed 16-bit readout for raw data acquisition
- Package: 8-SOIC (4.9mm × 3.9mm; wettable flanks)

RAA2S4252B Basic Circuit



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1. Pin Assignments

The RAA2S4252B is available in an 8-SOIC (4.9mm × 3.9mm) RoHS-conformant package.

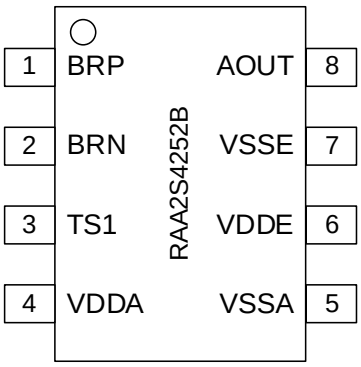

Figure 1. Pin Assignments for 4.9mm × 3.9mm 8-SOIC – Top View

2. Pin Descriptions

Table 1. Pin Description

8-SOIC Pin #	Pin Name	Type	Description
1	BRP	Analog	Positive bridge sensor input
2	BRN	Analog	Negative bridge sensor input
3	TS1	Analog	External temperature sensor input 1
4	VDDA	Supply	Internal supply and positive bridge supply voltage
5	VSSA	Ground	Internal ground and negative bridge supply voltage
6	VDDE	Supply	External supply
7	VSSE	Analog	External ground
8	AOUT	Analog	Analog output and One-Wire Interface (OWI) input/output

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RAA2S4252B at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability. In addition, extended exposure to stresses above the operating conditions given in section 4 might affect device reliability.

See section 7.9 for information about over-voltage protection, reverse-polarity, and short-circuit protection.

Table 2. Absolute Maximum Ratings

Requirement	Parameter	Symbol	Conditions	Min	Max	Unit
DS_001	Supply voltage	V_{DDE_MAX}	$V_{DDE} = V_{VDDE} – V_{VSSE}$	-40	40	V
DS_002	Voltage at AOUT pin	V_{AOUT_MAX}	To VSSE	-40	40	V
DS_003	Pin voltage difference	V_{PIN_MAX}	Voltage between any two of these pins: VDDE, AOUT and VSSE	-40	40	V
DS_004	Analog supply voltage	V_{DDA_MAX}	$V_{DDA} = V_{VDDA} – V_{VSSA}$; on-chip controlled voltage; do not supply externally	-0.3	6.0	V
DS_005	Voltage at all other pins	V_{PIN}	Maximum voltage is V_{VDDA} + 0.3V	-0.3	6.0	V
DS_006	Junction temperature	T_J		-40	160	°C
DS_007	Storage temperature	T_{STG}	Time < 1000 hours	-55	165	°C

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4. Operating Conditions

The operation conditions in Table 3 specify the conditions that the application circuit must provide to the device in operation for proper function. Unless otherwise stated, the parameter limits in this section are applied as test conditions for the electrical parameters specified in sections 5.

Table 3. Operating Conditions

Requirement	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DS_050	Supply voltage	V_{DDE}	$V_{DDE} = V_{VDDE} – V_{VSSE}$	4.5	5	5.5	V
DS_051	Ambient temperature [3] [7][8]	T_{AMB_TQE}	Extended Temperature Range (TQE)	-40		150	°C
		T_{AMB_TQA}	Advanced-Performance Temperature Range (TQA)	-40		125	°C
Informational	Thermal resistance SOIC8 [1] [4] [5]	R_{th_SOIC8}	According to JESD 51		93		K/W
DS_052	Bridge resistance [1] [2] [6]	R_{BR}	Output range 5% to 95%	2		15	kΩ
		R_{BR_10-90}	Output range 10% to 90%	1		15	kΩ

[1] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[2] R_{BR} up to 22kΩ is allowed but may result in higher noise

[3] Temperature stress over lifetime is restricted to temperature profiles that are equivalent to the HTOL qualification described in section 11.

[4] Assuming application conditions according to test board design as per JESD51-7 and natural convection test conditions as per JESD51-2.

[5] Package-related parameter.

[6] Symmetric behavior and identical electrical properties (including the low-pass characteristic) of the differential bridge sensor inputs are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins can generate a failure in signal operation.

[7] Definition of ambient temperature according to JESD 402-1.

[8] The end user of RAA2S4252B determines the exact worst case condition of the junction temperature in the field of operation. It is recommended to perform a thermal simulation of the module integrating the RAA2S4252B if the effective context of use is significantly different than the ones stated in this datasheet.

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5. Electrical Parameters

All parameter values are valid under the operating conditions specified in section 4 (unless otherwise stated). This means that all parameters are valid for the ambient temperature range T_{AMB_TQE} (DS_051) and for the supply voltage range V_{DDE} (DS_050). Unless otherwise defined, the parameters are related to the device itself. All internal voltages are referenced to VSSA.

The following parameters are specified based on a RAA2S4252B main channel configuration setup using a PGA gain of 200 and assuming a resulting ADC input range usage of ≥ 50%FS. Further preconditions are an ADC resolution of 14 bits, a 2-step A/D conversion scheme using an MSB-to-LSB ratio of 8/6 bit, and an ADC clock frequency of nominal 1MHz (first step) / 2MHz (second step).

Table 4. Electrical Parameters

Note: See important table notes at the end of the table.

Requirement	Parameter	Symbol	Descriptions/Conditions	Min	Typ	Max	Unit
Supply Current and System Operation Conditions							
DS_100	Supply current [1]	I_S	Oscillator adjusted f_{OSC}=8MHz		5	7	mA
DS_102	Oscillator frequency	f_{OSC}	Calibrated, adjusted to 8MHz, recommended	7.2	8.0	8.8	MHz
DS_104	Bridge sensor supply voltage	V_{SENS}	$V_{SENS} = V_{TOP} - V_{BOT}$ where: V_{TOP}: voltage at internal TOP pin V_{BOT}: voltage at internal BOT pin TOP and BOT are internally connected to VDDA and VSSA.	0.9		1	V_{DDA}
Informational	Analog supply voltage	V_{DDA}	Do not supply V_{DDA} externally. Note: V_{DDA} is limited if V_{DDE} exceeds the threshold of $V_{OV\_LIM\_TH}$	0.925			V_{DDE}
Analog Front-End Characteristics							
DS_120	Differential input span	V_{IN_SPAN}	Analog gain: 1…912	0.5		800	mV/V
DS_121	Differential input offset cancellation range	$V_{IN\_OFFS\_XSOC}$	Including Extended Sensor Offset Compensation (XSOC); Depends on gain adjust; see section 7.4.5 .	-1000		1000	% V_{IN_SPAN}
DS_122	Input voltage range	V_{IN_RNG1}	Analog gain = 1; corresponds to V_{ADC_IN}	0.05		0.95	V_{SENS}
DS_123		V_{IN_RNG2}	Analog gain = 3 to 912	0.3		0.65	V_{SENS}
DS_124	Time constant at input pins [2]	LTC	Capacitance either between pins BRP, BRN to VSSA or between BRP and BRN Calculation: $C_{IN} \leq$ LTC / (7 × RBR) Time constant can be extended by configuration.			75	µs
A/D Conversion Refer to section 7.4.6.							
DS_130	ADC resolution [2]	r_{ADC}		12		18	Bit
DS_131	ADC input range [2]	V_{ADC_IN}		0.05		0.95	V_{SENS}
DS_132	DNL [2]	DNL_{ADC}	Best fit; overall AFE; V_{ADC_IN} according to DS_131			0.95	LSB
DS_133	INL	INL_{ADC_TQA}	Best fit, temperature range TQA [2]			5	LSB_{14}
DS_134		INL_{ADC_TQE}	Best fit, temperature range TQE			8	LSB_{14}
Temperature Measurement Refer to section 7.3.2.							

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Requirement	Parameter	Symbol	Descriptions/Conditions	Min	Typ	Max	Unit
Informational	On-chip PTAT measurement range [2]	OPR_{TS}	Important: This range exceeds operating conditions for junction temperature T_{J_ABS}.	-60		200	°C
DS_140	On-chip PTAT measurement sensitivity	ST_{TSI}		20			LSB /K
DS_141	External temperature diode gain	A_{TSE_D}		25			LSB /mV
DS_142	External temperature diode bias current	I_{TSE_D}	Selectable nominal values: 20µA and 100µA	10		150	µA
DS_143	External temperature diode input range [2]	V_{TSE_D}	Related to VDDA	-1		-0.2	V
Bridge Sensor Diagnostic Tasks							
DS_151	Sensor connection loss detection threshold [2]	R_{SCC}	Covered by fault check BRSC2. Threshold can be adjusted.	40		1000	kΩ
DS_152	Sensor short detection threshold [2]	R_{SSC}	Covered by fault check BRSC. Threshold can be adjusted.	50		1000	Ω
DAC and Analog Output (Pin AOUT)							
DS_160	Analog Output Range	$AOUT_{RNG}$	R_{LOAD} ≥ 2kΩ R_{LOAD} ≥ 1kΩ	5 10		95 90	%VDDE
DS_161	DAC resolution [2]	r_{DAC}	Analog output		12		Bit
DS_162	Output current sink/source	$\lvert I_{OUT\_SRC/SINK} \rvert$	V_{AOUT}: 5-95%, R_{LOAD} ≥ 2kΩ			2.75	mA
DS_163			V_{AOUT}: 10-90%, R_{LOAD} ≥ 1kΩ			5.5	mA
DS_164	Absolute output current driving capability [2] [3]	I_{OUT_LIM}		6			mA
DS_165	Absolute short-circuit current [3]	$\lvert I_{OUT\_SHRT} \rvert$	AOUT short to VSSE or VDDE with maximum output current limit adjustment			25	mA
DS_170	Output slew rate [2]	SR_{OUT}	C_{LOAD} < 50nF	0.1			V/µs
DS_171	Output resistance in Diagnostic Mode [2]	R_{OUT_DIA}	Diagnostic Range: < 4%V_{DDE} OR > 96%V_{DDE} for R_{LOAD} ≥ 2kΩ < 8%V_{DDE} OR > 92%V_{DDE} for R_{LOAD} ≥ 1kΩ			80	Ω
DS_172	DNL	DNL_{OUT}	r_{DAC} =12bit (in Analog Output Range $AOUT_{RNG}$)			0.99	LSB
DS_173	INL @ TQA [2]	INL_{OUT}	Best fit, r_{DAC} = 12bit (in Analog Output Range $AOUT_{RNG}$)			5	LSB
DS_174	INL @ TQE	INL_{OUT}	Best fit, r_{DAC} = 12bit (in Analog Output Range $AOUT_{RNG}$)			8	LSB
DS_175	Absolute AOUT leakage current in TQA [2]	$I_{OutLeak\_TQA}$	At ground loss with R_{LOAD} connected to VSSE. At power loss with R_{LOAD} connected to VDDE.			15	µA
DS_176	Absolute AOUT leakage current in TQE	$I_{LEAK\_OUT\_GND\_TQE}$	At ground loss with R_{LOAD} connected to VSSE. At power loss with R_{LOAD} connected to VDDE.			20	µA
System Response							
DS_180	Startup time [2]	$t_{STARTUP}$	Time to first valid output after power-on; V_{DDE} slew rate > 0.1V/µs			5	ms
DS_181	Output update rate [2]	OUR	depends on configuration		1.25	10	kHz
DS_182	Bandwidth [2]	BW	66% step response			3	kHz

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Requirement	Parameter	Symbol	Descriptions/Conditions	Min	Typ	Max	Unit
DS_184	Failure messaging time [2]	FMT	Time between occurrence of a failure event and reporting on analog output assuming one failure confirmation, main-to-auxiliary measurement ratio equal to one. Depends on configuration			20	ms
		FMT_FOUR	As described above plus FOUR option. Depends on configuration.			5	ms
DS_185	Analog output noise peak-to-peak [2]	$V_{NOISE,PP}$	DAC and output buffer only; bandwidth ≤ 10kHz			10	mV
DS_186	Analog output noise RMS [2]	$V_{NOISE,RMS}$	DAC and output buffer only; bandwidth ≤ 10kHz			3	mV
DS_187	Ratiometricity error [2]	$RE_{OUT\_0.5}$	Maximum error (@ V_{DDE} = 5V +/- 0.5V)	-1000		1000	ppm
DS_188	Ratiometricity error [2]	$RE_{OUT\_0.25}$	Maximum error (@ V_{DDE} = 5V +/- 0.25V)	-500		500	ppm
DS_189	Overall failure bridge sensor measurement; deviation from ideal line including INL, gain, offset, and temperature impacts [2] [4]	F_{ALL}	Temperature range TQA			0.5	% FSO
			Temperature range TQE			1.0	
Power Management							
DS_210	Power-on threshold	V_{PWR_ON}		3.3		3.9	V
DS_211	Power-off threshold	V_{PWR_OFF}		3.0		3.6	V
DS_212	Power-on reset hysteresis [2]	V_{POR_HYST}			0.4		V
DS_213	Over-voltage switch-off threshold [2]	V_{OV_DISC}		8		15	V
DS_214	Over-voltage switch-off delay [2]	t_{OV_DISC}				10	ms
DS_215	Over-voltage limitation threshold	$V_{OV\_LIM\_TH}$	Limitation threshold of internal supply voltage in case of over-voltage	5.55	5.8	6.0	V
DS_216	Over-voltage power consumption [1] [2]	P_{OV}	5.5V < V_{DDE} < 40V			250	mW

[1] Excluding bridge supply current and excluding output current at AOUT pin.

[2] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[3] Analog output current limitation is adjustable between 7mA and 20mA.

[4] Full-scale output (FSO). No sensor-caused effects included in overall error. ADC input range from 10% to 90% of V_{SENS}; DAC from 5% to 95% of output range.

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6. Interface Characteristics and Non-volatile Memory

Table 5. Interface Characteristics and Non-volatile Memory

Requirement	Parameter	Symbol	Descriptions/Conditions	Min	Typ	Max	Unit
ZACwire™ One-Wire Interface (OWI)							
DS_220	Start window [1]	$t_{OWI\_STARTWIN}$	V_{DDE} slew rate > 0.1V/µs	100	225	350	ms
DS_221	Communication start time [1]	t_{COMM_STRT}	V_{DDE} slew rate > 0.1V/µs; time to be ready for communication after power-on	4			ms
DS_222	Bit time [1]	$t_{OWI\_BIT\_NL}$	No output load	0.02		4	ms
		t_{OWI_BIT}	10nF ≤ C_{LOAD} ≤ 100nF	1		4	ms
DS_223	OWI voltage level HIGH [1]	$V_{OWI\_IN\_H}$	Master to slave	0.8			V_{DDE}
DS_224	OWI voltage level LOW [1]	$V_{OWI\_IN\_L}$	Master to slave			0.2	V_{DDE}
DS_225	Slave output level LOW [1]	$V_{OWI\_OUT\_L}$	Open drain, I_{OL} ≤ 2mA			0.1	V_{DDE}
Non-volatile Memory (NVM)							
DS_230	Ambient temperature for NVM programming [1] [2]	T_{AMB_NVM}		-40		150	°C
DS_231	Re-write cycles [a]	N_{NVM}		100			cycle
DS_233	Data retention [1]	t_{NVM_RET}	Operation conditions over lifetime must comply with the temperature profile [3]	15			a
DS_234	Programming time [1]	t_{NVM_WRI}	Per programmed data word		3	6	ms

[1] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[2] Consider additional package and temperature range restrictions.

[3] Over lifetime and valid for the dice. Note that package can cause additional restrictions.

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7. Circuit Description

7.1 General Operation Description

The RAA2S4252B is a sensor signal conditioner (SSC) for highly accurate amplification and sensor-specific correction of resistive bridge sensors. Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity is accomplished via an internal 16-bit RISC microcontroller running a ROM based correction algorithm with calibration coefficients stored in an NVM.

The RAA2S4252B is adjustable to nearly all resistive sensor element types. Measured values are provided at the analog voltage output. The digital one-wire interface (OWI) can be used for a simple PC-controlled calibration procedure in order to program a set of calibration coefficients into an on-chip NVM. The specific sensor element and the RAA2S4252B can be quickly calibrated together. The RAA2S4252B and the calibration equipment communicate digitally, so the noise sensitivity is greatly reduced. Digital calibration helps keep assembly cost low as no trimming by external devices or lasers is needed.

The RAA2S4252B is optimized for automotive environments by over-voltage and reverse-polarity protection circuitry, excellent electromagnetic compatibility, full automotive temperature range, and multiple diagnostic features.

Figure 2 provides a block diagram of the RAA2S4252B. Refer to section 15 for definitions of abbreviations.

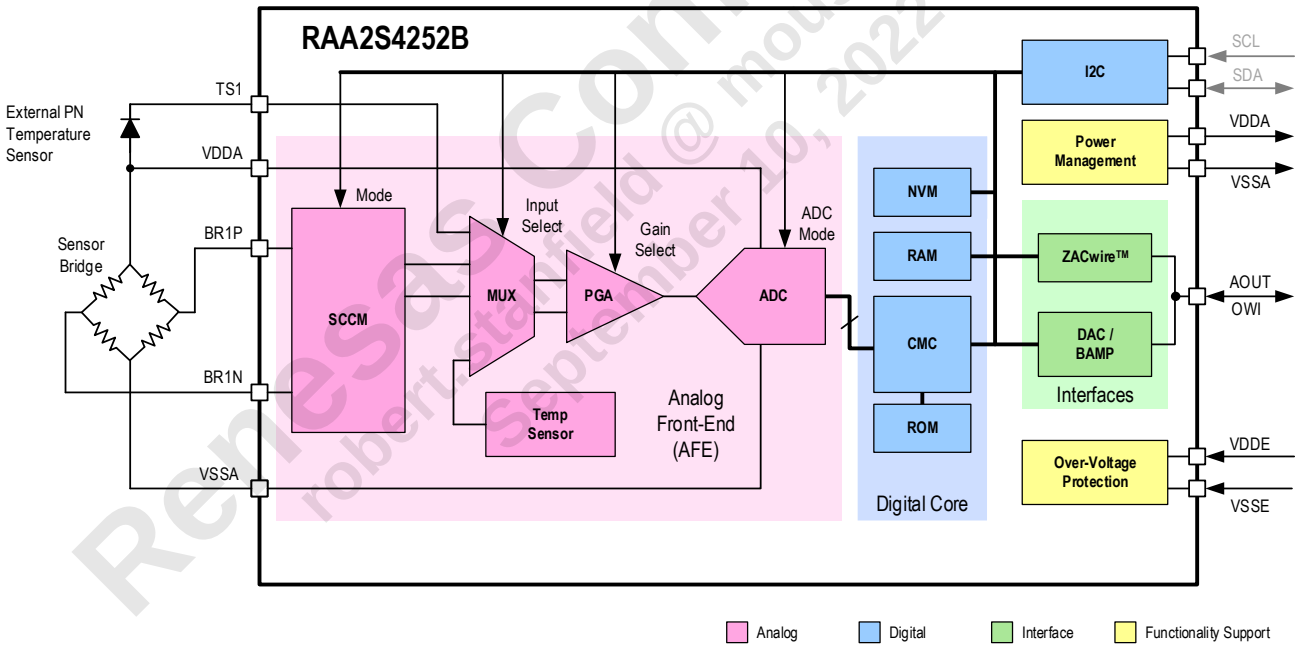

Figure 2. RAA2S4252B Block Diagram

7.2 Signal Path

The RAA2S4252B signal path consists of the analog front-end (AFE), the digital signal processing unit, and the analog output stage. In addition, this is supported by a serial digital one-wire interface (ZACwire™) for calibration purposes.

The resistive bridge sensor signal is input via the BRP and BRN and is handled as a fully differential signal. Both signal lines have a dynamic range symmetrical to the common mode potential (analog ground; equal to $V_{DDA}/2$) in order to process both positive and negative differential input signals. These differential signals are pre-

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amplified by the programmable gain amplifier (PGA) and are converted to digital values by the A/D converter (ADC).

A multiplexer (MUX) selects and transmits the signals from either the bridge sensor or the selected temperature sensor to the analog-to-digital converter (ADC) in a defined sequence. The temperature sensor can either be an external diode or an on-chip proportional-to-absolute-temperature (PTAT) source selected by NVM configuration.

The digital signal correction is processed in the calibration microcontroller (CMC) using ROM-resident correction formulas and sensor-specific coefficients stored in the NVM. The configuration data and the conditioning coefficients are programmed into the NVM during the calibration process by digital one-wire communication via the AOUT pin.

During the calibration process, raw measurement values can be requested via the digital interfaces.

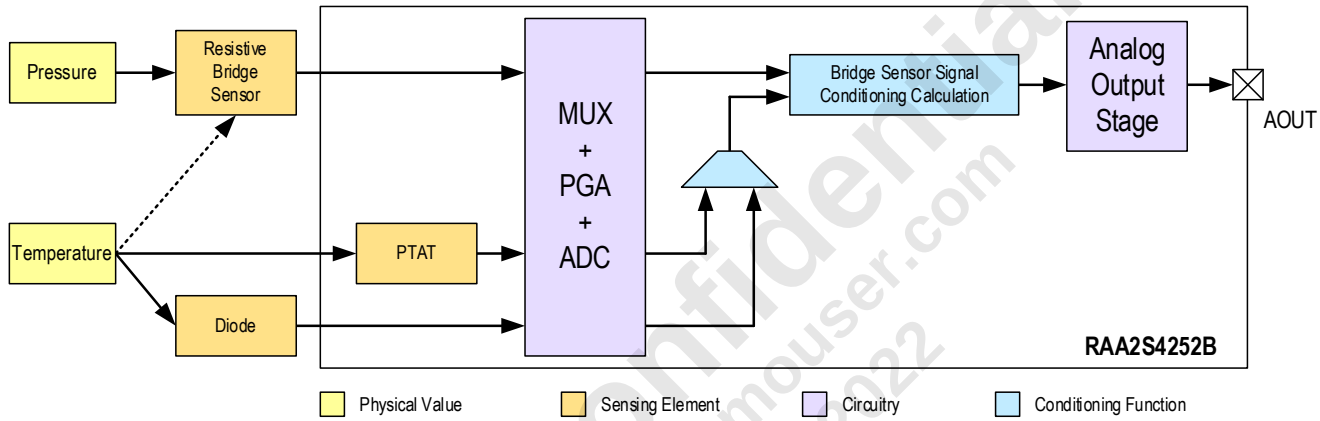

Figure 3. Main Signal Path

7.3 Signal Measurement

7.3.1. Full Bridge Sensor Measurement

The RAA2S4252B measures a differential bridge sensor element signal (BRP to BRN). The signal path is ratiometric and fully differential. The ratiometric reference voltage V_{REF} is equal to (V_{TOP} – V_{BOT}). V_{TOP} equals to V_{DDA} and VBOT equals to V_{SSA} since both voltage references are shorted internally.

7.3.2. Temperature Measurements

The RAA2S4252B supports different methods for acquiring temperature data needed for the conditioning of the sensor signal:

- An on-chip PTAT sensor.
- An external PN-junction temperature sensor connected to the TS1 pin and referenced to the sensor top potential (VDDA pin).

7.3.3. Measurement Cycle

The measurement cycle is the sequence of measurements processed during the Normal Operation Mode (NOM). It delivers the raw measurement results from all connected sensor elements and from the supervision functions. The measurements are processed sequentially, all using the same ADC to convert the analog input voltages to a digital value.

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7.4 Analog Front-End

7.4.1. Overview

The analog front-end (AFE) consists of the multiplexer (MUX), the programmable gain amplifier (PGA), and the analog-to-digital converter (ADC). The internal offset of the analog front-end is eliminated by an auto-zero compensation.

7.4.2. SCM

The sensor check module (SCM) implements the self-diagnostic features for the analog front-end. The SCM provides the sensor connection checks (short and open circuit) as well as several other diagnostic functions.

7.4.3. Input Multiplexer

The input multiplexer (MUX) selects one of the various inputs and connects it to the signal path utilizing a single ADC. It allows a very flexible signal routing between the connected sensor and the RAA2S4252B.

7.4.4. Programmable Gain Amplifier

The sensor signal can be amplified by the on-chip programmable amplifier (PGA) using a gain between 2 and 200. Alternatively, the PGA can be bypassed and the sensor signal is applied directly to the ADC. The gain is adjustable for every single bridge sensor measurement task individually in order to provide an ADC input signal span of greater than 50% FS.

Table 6 shows the adjustable gains of the PGA, the corresponding signal spans, and the common mode range limits.

Table 6. Adjustable PGA Gains and Resulting Sensor Signal Spans

Select Value PgaGainSel	PGA Gain a_{PGA}	Sensor Span V_{IN_SPAN} [mV/V]	PGA Gain with XSOC a_{PGA_XSOC}	Sensor Span with XSOC $V_{IN\_SPAN\_XSOC}$ [mV/V]
0	1.0	1000.0	n.a.	n.a.
1	3.0	338.7	24.00	41.667
2	3.5	285.2	28.50	35.088
3	4.2	237.1	34.29	29.167
4	5.0	199.7	40.71	24.561
5	5.9	169.4	48.00	20.833
6	7.0	142.6	57.00	17.544
7	8.4	118.5	68.57	14.583
8	10.0	99.8	81.43	12.281
9	11.8	84.7	96.00	10.417
10	14.0	71.3	114.00	8.772
11	16.9	59.3	137.14	7.292
12	20.0	49.9	162.86	6.140
13	23.6	42.3	192.00	5.208
14	28.0	35.7	228.00	4.386
15	33.7	29.6	274.29	3.646
16	40.1	25.0	325.71	3.070
17	47.2	21.2	384.00	2.604
18	56.1	17.8	456.00	2.193
19	67.5	14.8	548.57	1.823
20	80.1	12.5	651.43	1.535
21	94.5	10.6	768.00	1.302
22	112.2	8.9	912.00	1.096
23	137.1	7.3	n.a.	n.a.
24	162.9	6.1	n.a.	n.a.

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Select Value PgaGainSel	PGA Gain a_{PGA}	Sensor Span V_{IN_SPAN} [mV/V]	PGA Gain with XSOC a_{PGA_XSOC}	Sensor Span with XSOC $V_{IN\_SPAN\_XSOC}$ [mV/V]
25	192.0	5.2	n.a.	n.a.
26	228.0	4.4	n.a.	n.a.
27	274.3	3.6	n.a.	n.a.
28	325.7	3.1	n.a.	n.a.
29	384.0	2.6	n.a.	n.a.
30	456.0	2.2	n.a.	n.a.
31	548.6	1.8	n.a.	n.a.

Recommendation: To achieve the best stability and linearity performance of the AFE, operate the PGA in a differential output voltage range within 10% to 90% of the ratiometric reference voltage $V_{REF} = V_{SENS} = (V_{TOP} – V_{BOT})$. V_{TOP} equals to V_{DDA} and V_{BOT} equals to V_{SSA} since both voltage references are shorted internally. The gain must be selected to guarantee this constraint for the entire operating temperature range of the application and for the specified sensor bridge tolerances.

7.4.5. Compensation of Large Sensor Offsets

The RAA2S4252B supports both analog and digital sensor offset compensation:

- Analog sensor offset compensation (XSOC): supports the compensation of large sensor offset values up to 10 times higher than the span. An offset compensation voltage is added before analog amplification as otherwise the sensor signal would overdrive the analog frontend. XSOC is adjustable with 64 steps for every polarity.
- Digital sensor offset compensation (digital zooming): processed as part of the digital signal conditioning by the DSP unit. It is applicable for large sensor offsets up to three times higher than the span. It generates a loss of resolution of up to 3 bit and therefore requires measurement of the sensor signal with higher resolution.

Table 2: Extended Sensor Offset Compensation (XSOC) Adjustments

Select Value PgaGainSel	PGA Gain a_{PGA_XSOC}	Sensor Span $V_{IN\_SPAN\_XSOC}$ [mV/V]	Input Related XSOC Value [mV/V]		Absolute Compensable Sensor Offset [mV] @ VBR=5000mV	
			Min/Step	Maximum	Min/Step	Maximum
0	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.
1	24.00	41.667	0.0078	0.4922	39.1	2460.9
2	28.50	35.088	0.0078	0.4922	39.1	2460.9
3	34.29	29.167	0.0055	0.3445	27.3	1722.7
4	40.71	24.561	0.0055	0.3445	27.3	1722.7
5	48.00	20.833	0.0039	0.2461	19.5	1230.5
6	57.00	17.544	0.0039	0.2461	19.5	1230.5
7	68.57	14.583	0.0027	0.1723	13.7	861.3
8	81.43	12.281	0.0027	0.1723	13.7	861.3
9	96.00	10.417	0.0020	0.1230	9.8	615.2
10	114.00	8.772	0.0020	0.1230	9.8	615.2
11	137.14	7.292	0.0014	0.0861	6.8	430.7
12	162.86	6.140	0.0014	0.0861	6.8	430.7
13	192.00	5.208	0.0010	0.0615	4.9	307.6
14	228.00	4.386	0.0010	0.0615	4.9	307.6
15	274.29	3.646	0.0007	0.0431	3.4	215.3
16	325.71	3.070	0.0007	0.0431	3.4	215.3
17	384.00	2.604	0.0005	0.0308	2.4	153.8
18	456.00	2.193	0.0005	0.0308	2.4	153.8
19	548.57	1.823	0.0003	0.0215	1.7	107.7
20	651.43	1.535	0.0003	0.0215	1.7	107.7
21	768.00	1.302	0.0002	0.0154	1.2	76.9
22	912.00	1.096	0.0002	0.0154	1.2	76.9

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7.4.6. Analog-to-Digital Converter

The analog-to-digital converter is implemented using the full-differential switched-capacitor technique. The conversion is largely insensitive to short-term and long-term instabilities of the clock frequency. The ADC provides adjustability of the A/D conversion input voltage range shift.

7.5 Bridge Sensor Signal Conditioning

The bridge sensor signal conditioning is processed every time a new measurement value is available from the analog-to-digital conversion. The conditioning calculation provides compensation of the temperature dependent offset and gain, and of the non-linearity. Both the external temperature sensor signal and the on-chip PTAT signal can be selected for compensating the temperature dependency of the bridge sensor signal.

The conditioning coefficients are stored to the NVM during the calibration process.

The RAA2S4252B provides the following filter functions:

- averaging low-pass filter
- IIR filter of higher order
- non-linear noise cancelation filter.

The conditioning result for the bridge sensor signal is stored to the RAM Output Memory.

7.6 Output Modes

In Normal Operation Mode (NOM), the RAA2S4252B provides analog voltage output at the pin AOUT. The analog output is continuously updated with the bridge sensor signal conditioning result.

Two output modes are available, which only differ in the final transfer characteristics from the bridge-sensor conditioning result to the analog output value:

- Analog Output
- Switch Output

An unity gain output buffer drives the analog output potential. For the buffer the input signal is generated by a 12-bit resistor-string DAC. The output buffer, which is a rail-to-rail operation amplifier, is offset compensated and current limited. Therefore, a short-circuit of the analog output to ground or the power supply does not damage the RAA2S4252B.

7.7 Digital One-Wire Interface

For configuration and calibration purposes, the RAA2S4252B provides serial digital communication via a one-wire interface (OWI). It can also be used as a communication interface in Normal Operation Mode (NOM) to read the bridge sensor signal conditioning result on request.

7.8 NVM

Configuration and calibration data are stored in an on-chip non-volatile memory (NVM), which is using the floating gate storage principle. The NVM stores data based on differential bit cells.

The NVM supports:

- A write lock option avoid overwriting the configuration data.
  Releasing the write lock via OWI communication is not possible.
- Traceability Data

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7.9 Over-Voltage, Reverse-Polarity, and Short-Circuit Protection

RAA2S4252B is designed for a 5V supply provided by an electronic control unit (ECU).

RAA2S4252B and the connected sensor elements are protected from over-voltage and reverse-polarity damage by an internal supply voltage regulator with a current limitation function. The analog output pin AOUT is protected regarding short-circuit, over-voltage and reverse polarity with all voltages according to the absolute maximum ratings, see section 3.

RAA2S4252B protection applies when the device is operated in the application circuits shown in section 9. Protection voltage is ±40V as defined in absolute maximum ratings (see Table 2). When the over-voltage protection is active, the device has a higher power dissipation. Depending on the ambient temperature and on the external sensor characteristics, the higher power dissipation of the device may lead to a violation of the maximum junction temperature.

Table 7. Protection Features

No.	VSSE Pin	AOUT Pin	VDDE Pin	Comment
DS_300	0	0 to 5V	5V	Normal Mode
DS_301	0	Open	40V	VDDE to VSSE
DS_302	0	Open	-40V	Reverse voltage
DS_303	0	40V	Open	AOUT to VSSE
DS_304	0	-40V	Open	Reverse voltage
DS_305	Open	0	40V	VDDE to AOUT
DS_306	Open	0	-40V	Reverse voltage
DS_307	0	0	40V	VDDE to (AOUT+VSSE)
DS_308	0	0	-40V	Reverse voltage
DS_309	0	40V	40V	(VDDE+AOUT) to VSSE
DS_310	0	40V	5.0V	AOUT to VSSE
DS_311	0	-40V	-40V	Reverse voltage
DS_312	0	40V	0	AOUT to (VDDE+VSSE)
DS_313	0	-40V	0	Reverse voltage AOUT
DS_314	0	-35V	5V	Reverse voltage AOUT

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8. Fault-Safe Operation

8.1 Overview

Fault checks verify the operation of the RAA2S4252B and of the connected sensing element at power-on and during Normal Operation Mode (NOM). If a fault is detected, the Diagnostic Mode (DM) is activated and the fault status is messaged.

8.2 Fault Messaging

In diagnostic mode, the analog output is either high-ohmic or driven to lower diagnostic range (LDR).

The RAA2S4252B has two different diagnostic modes with different behavior:

Static Diagnostic Mode

- The measurement and conditioning cycle is stopped.
- The analog output is set to diagnostic range.
- The one-wire communication interface is enabled for reading detailed diagnostic status information.
- If enabled, the RAA2S4252B is reset, including a reset of all status registers.
- The RAA2S4252B can be restarted by a power-off/power-on sequence.

Temporary Diagnostic Mode

- The measurement and conditioning cycle keeps running.
- Fault checks are continuously processed, including update of fault status.
- The analog output is set to diagnostic range.
- The one-wire communication interface is enabled for reading detailed diagnostic status information.
- The RAA2S4252B returns to Normal Operation Mode, including analog output of sensor signal, if fault checks no longer detect errors.

8.3 Fault Checks

Table 8 lists the available fault checks.

Table 8. Fault Checks

Requirement	Identifier	Fault Check
Device Self-Supervision Fault Checks		
DS_400	VDDAPOR	Analog supply voltage (VDDA) under-voltage reset; power-on reset (POR)
DS_401	VDDDBOD	Digital supply voltage (VDDD) under-voltage reset; brownout detection (BOD)
DS_402	OSCFAIL	Oscillator fail check; reset after oscillator restart
DS_403	NVMCRC	NVM content CRC check
DS_405	CYCCRC	Measurement and conditioning cycle CRC check
DS_406	RAMPRTY	RAM content parity check
DS_407	ROMCRC	ROM content CRC check
DS_408	WWDG	Windowed watchdog; CMC alive supervision
DS_409	COMP	Computational check; CMC code processing and peripheral bus access check
DS_410	CHIPP	Chipping check
Sensing Element Fault Checks		
DS_420	BRSC	Bridge sensor short and connection check
Environment and Operation Condition Fault Checks		
DS_430	BRSRNG	Bridge sensor signal range check
DS_431	PTATRNG	On-chip temperature range check
DS_432	TRNG	Temperature range check

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9. Application Circuit and External Components

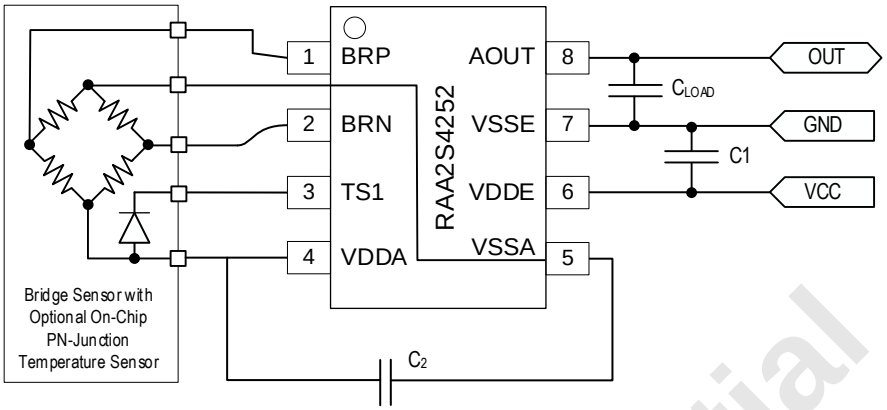

Figure 4. Application Circuit Example of a Pressure and Temperature Sensor with Analog Output

Table 9. Dimensioning of External Components for the Application Example

No.	Component	Symbol	Conditions	Min	Typical	Max	Unit
Informational	Capacitor	C1	V_{MAX} ≥ 60V, Low ESR type		100 ± 20%		nF
Informational	Capacitor	C2	V_{MAX} ≥ 10V, Low ESR type	47 ± 20%	100 ± 20%	220 ± 20%	nF
Informational	Capacitor	C_{LOAD}	V_{MAX} ≥ 60V, Low ESR type	10 ± 20%	47 ± 20%	470 ± 20%	nF

[1] The component values are examples and must be adapted to the requirements of the application, in particular to the EMC requirements.

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10. ESD Protection and EMC Specification

10.1 ESD Protection

All pins have an ESD protection of ≥ 2000V according to the Human Body Model (HBM with 1.5kOhm/100pF, based on MIL883, Method 3015.7). The VDDE, VSSE, and AOUT pins have an additional ESD protection of ≥ 4000V (HBM with 1.5kOhm/100pF, based on MIL883, Method 3015.7).

The level of ESD protection are tested with devices in SOIC 8 (4.9mm × 3.9mm) packages during the product qualification.

10.2 Latch-Up Immunity

All pins pass ±100mA latch-up test based on testing that conforms to the standard EIA/JESD 78.

10.3 Electromagnetic Emission

The wired emission of externally connected pins of the device is measured according to the following standard: *IEC 61967_4:2002 + A1:2006.*

Measurements must be performed with the application circuits described in section 9.

For the off-board pins, the spectral power measured with the 150Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN* in the >200kHz range. For the VSSE pin, the spectral power measured with the 1Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code 15KmO.*

10.4 Conducted Susceptibility

The conducted susceptibility of externally connected pins of the device is measured according to the IEC 62132-4 standard, which describes the direct power injection (DPI) test method.

Measurements must be performed with the application circuit described in the section 9.

Measurements are performed with an internal reference capacitor and internal temperature sensor. The sensing element is replaced by a resistive divider. Calibration is parameterized so that ~50% VDDA is output.

Table 10 gives the specifications for the DPI tests.

Table 10. Conducted Susceptibility (DPI) Tests

No.	Test	Frequency Range	Target (dBm)	Load Pins	Protocol	Error Band	Coupling Impedance
DS_350	DPI, direct coupled	1MHz to 300MHz	26	VDDE, AOUT	Analog out	±1%	5kΩ / 10nF
DS_351	DPI, direct coupled	300MHz to 1000MHz	32	VDDE, AOUT	Analog out	±1%	5kΩ / 10nF

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11. Reliability and RoHS Conformity

The RAA2S4252B is qualified according to the AEC-Q100 standard, operating temperature grade 0. A fit rate <20 FIT (junction temperature = 55°C, confidence level = 70%, activation energy = 0.7eV) is estimated.

A typical fit rate for TSMC's CV018BCD technology, which is used for the RAA2S4252B, is < 1 FIT (temperature = 55°C, confidence level = 60%, activation energy = 0.7eV).

The reliability calculation is based on the product qualification, 1000 hours high temperature operating life (HTOL) at an ambient temperature of 150°C under normal operating conditions.

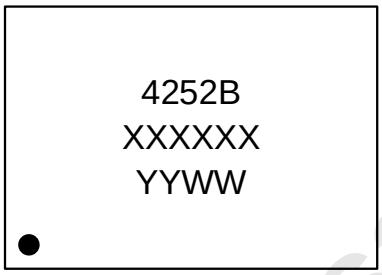
The RAA2S4252B complies with the RoHS directive and does not contain hazardous substances. The complete RoHS declaration update can be downloaded from https://www.renesas.com/eu/en/about/corporate-responsibility-citizenship.

12. Package Outline Drawings

The package outline drawings are accessible from the link below. The package information is the most current data available.

Package Outline Drawing Package Code:DCG8D4 8-SOIC 4.9 x 3.9 x 1.75 mm Body, 1.27mm Pitch (renesas.com)

13. Marking Diagram



1. "4252B" is the truncated part number.
2. "XXXXX" is the last digits of the lot number.
3. "YYWW" is the last digits of the year and week that the part was assembled.

14. Ordering Information

Part Number	Description and Package	MSL Rating	Shipping Packaging	Temperature
RAA2S4252B5HSP#JA0	8-Lead Small Outline (SOIC) Package	MSL1	Reel (13 inch)	-40°C to 150°C
RAA2S425XKIT	RAA2S425X SSC Evaluation Kit: Evaluation Board, 5 RAA2S4251B Samples.			
RAA2S4252EXT	RAA2S4252B adapter board with 5 RAA2S4252B samples			

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15. Glossary

Term	Description	Term	Description
ADC	Analog-to-Digital Converter	INL	Integral Nonlinearity
AEC	Automotive Electronics Council	LDR	Lower Diagnostic Range
AFE	Analog Front-End	LSB	Least Significant Bit
BOD	Brownout Detection	MUX	Multiplexer
BR	Bridge Sensor	NOM	Normal Operation Mode
CDM	Charged Device Model	NVM	Nonvolatile Memory
CM	Command Mode	OWI	One-Wire Interface
CMC	Calibration Microcontroller	PCB	Printed Circuit Board
CMOS	Complementary Metal-Oxide Semiconductor	PGA	Programmable Gain Amplifier
CRC	Cyclic Redundancy Check	PTAT	Proportional-to-Absolute Temperature
DAC	Digital-to-Analog Converter	PWR	Power Management and Protection Unit
DM	Diagnostic Mode	QFN	Quad-Flat No-Leads – IC package
DNL	Differential Nonlinearity	RAM	Random Access Memory
DPI	Direct Power Injection	RISC	Reduced Instruction Set Computing
DSP	Digital Signal Processing	RoHS	Restriction of Hazardous Substances
ECU	Electronic Control Unit	ROM	Read-Only Memory
EMC	Electromagnetic Compatibility	RMS	Root-Mean-Square
ESD	Electrostatic Discharge	SCM	Sensor Check Module
FIT	Failures in Time	sint	Signed integer value
FSO	Full Scale Output	SSC	Sensor Short Check (diagnostic feature) or Sensor Signal Conditioner
HBM	Human Body Model	TQA, TQE	Temperature range identifier. See DS_051 for definition.
HTOL	High Temperature Operating Life	uint	Unsigned integer value
HVAC	Heating, Ventilation and Air Conditioning	ZACwire™	RENESAS-specific One-Wire Interface
I2C	Inter-Integrated Circuit—serial two-wire data bus	XSOC	Analog Sensor Offset Correction
IIR	Infinite Impulse Response		

16. Revision History

Revision	Date	Description
1.0	Jun.17.22	Initial release.

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