Renesas RA Family

# Exception Handling

## Introduction

This application note explains how to handle exceptions on Renesas RA family MCUs with Arm® Cortex®-M cores for user applications using the Flexible Software Package (FSP). By properly managing the factors, location, and history of exception events that occur, you can increase debugging efficiency in the application development process and produce a robust system against exception events. This application note also describes a unique bus error monitoring system on Renesas devices with Arm® Cortex®-M33 cores that supports Arm® TrustZone® technology. The application project uses the Flexible Software Package (FSP) of the RA family, the GNU GCC compiler, and the integrated development environment e$^2$ studio IDE to demonstrate an exception handling flow for multiple possible faults.

## Prerequisites

- Experience using Renesas e$^2$ studio IDE
- Experience using Flexible Software Package (FSP) for the RA Family

Note: For developers who are new to the Renesas RA family of MCUs, we strongly recommend to start with Tutorial: Your First RA MCU Project – Blinky prior to trying out this application.

## Required Resources

Target Hardware:

- Renesas RA Kit EK-RA6M3 (for RA6M3 with Arm® Cortex®-M4)
- Renesas RA Kit EK-RA2E1 (for RA2E1 with Arm® Cortex®-M23)
- Renesas RA Kit EK-RA6M5 (for RA6M5 with Arm® Cortex®-M33)

Note: When applying this application note to other MCUs, be sure to change the settings according to the MCU specifications and evaluate it carefully.

Development Tools and Software:

- e$^2$ studio IDE version 2022-01 (22.1.0) or later
- Renesas Flexible Software Package (FSP) version 3.6.0 or later
- GCC ARM Embedded Toolchain version 10.3-2021.10 or later
- Segger J-Link RTT Viewer version 7.60e or later

## Using this Application Note

Section 1 covers the general overview of the exception model on Arm® Cortex®-M processor core.

Section 2 covers the Bus Error Monitoring System for Renesas implementation.

Section 3 covers the implementing method for user-defined exception handler on FSP-based projects.

Section 4 covers the debugging method of the occurred exception event

Section 5 covers the demonstration of the application attached to this application note.

## Notes on this document

In this document, the following names are used for Renesas devices equipped with ARM Cortex®-M core.

- **RA-CM4 devices**: RA family devices with a single Arm® Cortex®-M4 processor core based on Armv7-M architecture profile
  Examples of target devices: RA4M1, RA6M3
- **RA-CM23 devices**: RA family devices with a single Arm® Cortex®-M23 processor core based on Armv8-M architecture profile (without Security Extension)
  Examples of target devices: RA2A1, RA2E1
- **RA-CM33 devices**: RA family devices with a single Arm® Cortex®-M33 processor core based on Armv8-M architecture profile (with Security Extension)
  Examples of target devices: RA4M3, RA6M5, RA6E1, RA6T2

## Contents

# 1. Exception model on Arm® Cortex®-M processor core

The Arm® Cortex®-M processor core supports various fault detection and user notification methods. When the processor detects faults, exceptions, and interrupts, the processor transitions the processor mode. Available processor modes on Arm® Cortex®-M processor core are as follows (Figure 1.1. ).

- Thread mode
  Executes application software.
  The processor enters Thread mode on Reset, or as a result of an exception return.
- Handler mode
  Handles exceptions.
  The processor returns to Thread mode when it has finished all exception processing.

A processor with the Security Extension supports both Non-Secure and Secure states, which are orthogonal to traditional thread and handler modes. The four processor modes of operation are:

- Non-Secure Thread mode
- Non-Secure Handler mode
- Secure Thread mode
- Secure Handler mode

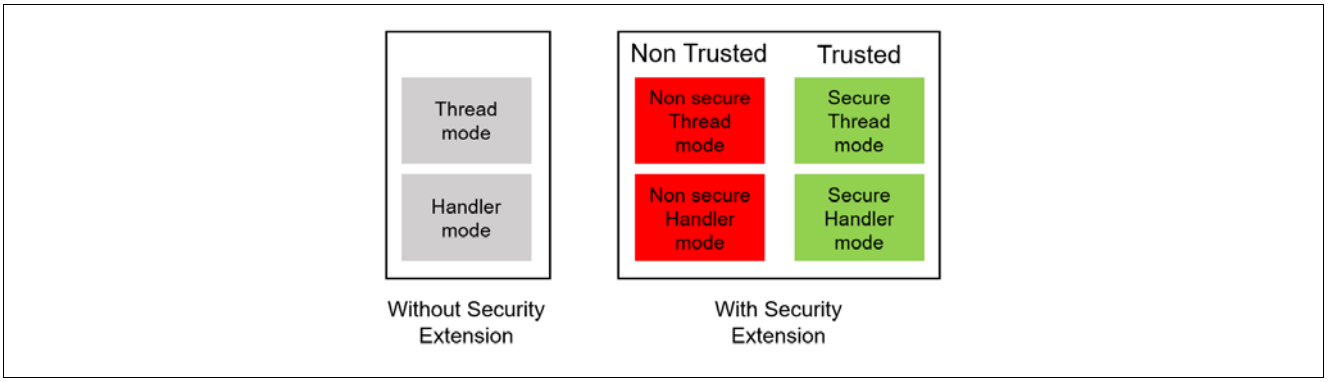



**Figure 1.1. Processor States**

When the processor takes an exception, the processor pushes information onto the current stack, and stores the information to status registers prior to exception entry.

Table 1.1 shows the available exception types and handlers, and fault status registers on each processor core. Please refer to Section: Exception model in the processor core's generic user guide for more details. These documents can be found in section 6 in this document.

## 1.1 Exception types and handlers

Table 1.1 shows the available exception types and handler types on each processor core.

**Table 1.1. Available exception types and handler types**

| Handler types | Exception types | | |
|---|---|---|---|
| | **Arm® Cortex®-M4** | **Arm® Cortex®-M23** | **Arm® Cortex®-M33** Note5 |
| Interrupt Service Routines (ISRs) Note1 | IRQ0 – IRQ239 | IRQ0 – IRQ239 | IRQ0 - IRQ479 |
| Fault handler Note4 | HardFault<br>MemManage Fault<br>BusFault<br>UsageFault | HardFault | HardFault Note2<br>MemManage Fault<br>BusFault Note2<br>UsageFault<br>SecureFault Note3 |
| System handler | NMI<br>PendSV<br>SVCall<br>SysTick | NMI<br>PendSV<br>SVCall<br>SysTick | NMI Note2<br>PendSV<br>SVCall<br>SysTick |

Note 1. Usable IRQ number depends on MCU device specification. Please refer to hardware user's manual of MCUs.

Note 2. The entry target state for HardFault, BusFault, NMI is controlled by a BFHFNMINS bit in AIRCR (Application Interrupt and Reset Control) register.

Note 3. SecureFault always targets Secure State.

Note 4. All faults can be treated as HardFault according to a fault enable bit in SHCSR (System Handler Control and State) register. This bit is set to 0 (Disabled) by default.

Note 5. With Security Extension.

## 1.2 Fault status registers

Table 1.2 shows the fault status registers on each fault. The processor core stores the information of fault status to these related registers when the fault occurs. By verifying these registers, we can recognize the factor and the location of faults that occurred. Please refer to processor core's generic user guide for more register details.

**Table 1.2 Fault status registers**

| Fault type | Status and Address register name Note2 | | |
|---|---|---|---|
| | **Arm® Cortex®-M4** | **Arm® Cortex®-M23** | **Arm® Cortex®-M33** |
| HardFault | SCB.HFSR | - | SCB.HFSR |
| MemManage Fault | SCB.MMFSR Note1<br>SCB.MMFAR | - | SCB.MMFSR Note1<br>SCB.MMFAR |
| BusFault | SCB.BFSR Note1<br>SCB.BFAR | - | SCB.BFSR Note1<br>SCB.BFAR |
| UsageFault | SCB.UFSR Note1 | - | SCB.UFSR Note1 |
| SecureFault | - | - | SAU.SFSR<br>SAU.SFAR |

Note 1. A subregister of the CFSR (Configurable Fault Status Register).

Note 2. Abbreviations used in this table are shown as follows.
SCB: System Control Block registers
SAU: Security Attribution Unit registers
HFSR: HardFault Status Register
MMFSR: MemManage Fault Status Register
MMFAR: MemManage Fault Status Address Register
BFSR: BusFault Status Register
BFAR: BusFault Address Register
UFSR: UsageFault Status Register
SFSR: Secure Fault Status Register
SFAR: Secure Fault Address Register

## 2. Bus Error on RA-CM33 devices

In addition to the faults specific to Arm® Cortex®-M33 CPU core, RA-CM33 devices provide some additional error detection capability supported by the bus error monitoring system. This chapter describes how to handle additional error information.

**Note on Section 2: This chapter describes the bus error monitoring system in case of RA-CM33 device RA6M5 MCU. Please refer to the MCU's hardware user's manual for other MCUs.**

### 2.1 Overview of Bus Error

The bus error monitoring system can detect the following types of bus errors:

- Illegal address access
- Bus master MPU error
- TrustZone Filter error
- Bus error transmitted from each slave IP

The TrustZone Filter (TZF) is special on RA-CM33 devices and can detect security access errors caused by peripheral modules below that are out of CPU core scope.

- Master TZF: For bus master (DMAC/DTC)
- Slave TZF: For bus slave (Memory, peripherals)

See Figure 2.1. for the TZF implementation on RA-CM33 devices.

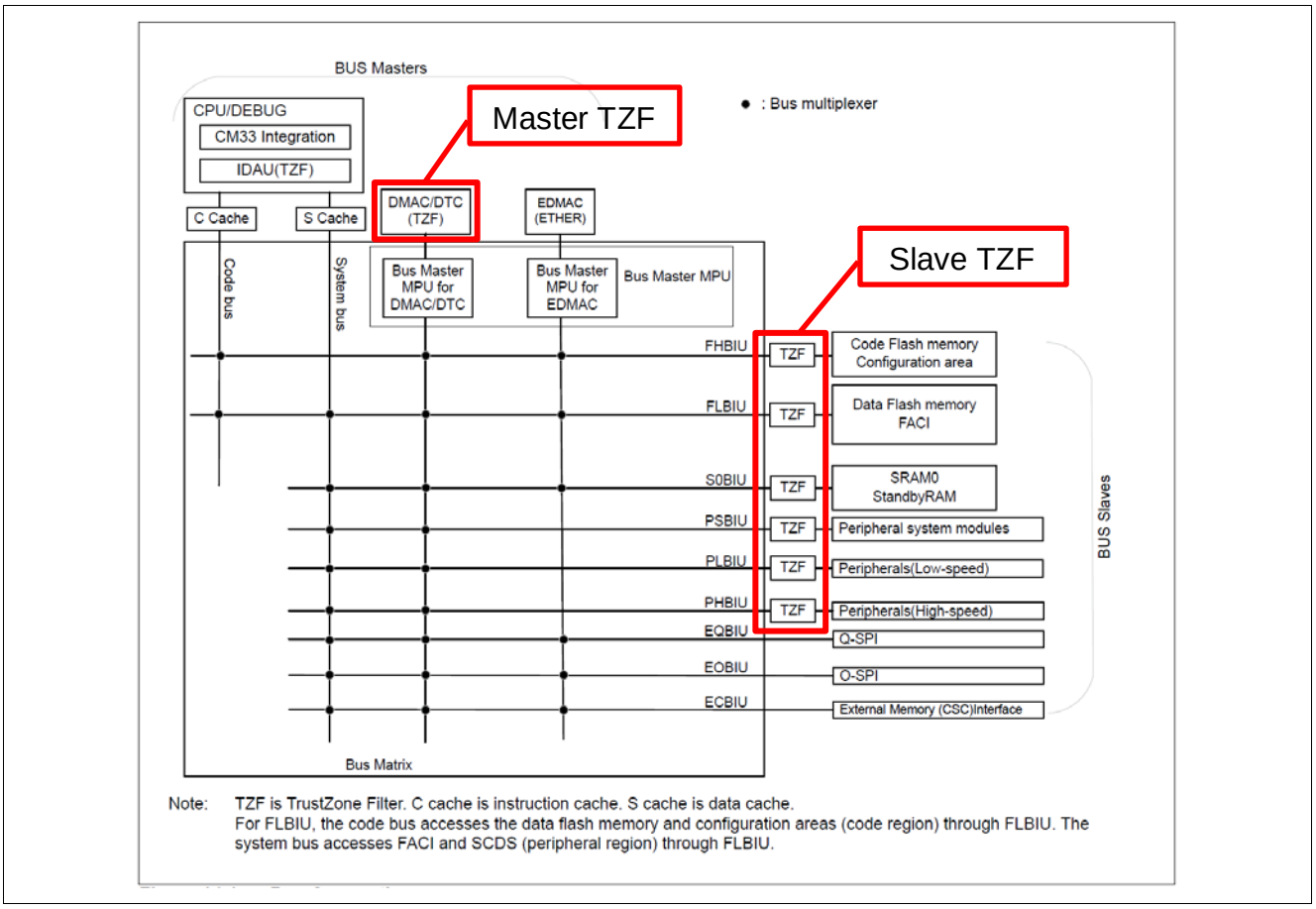



**Figure 2.1. TZF on RA-CM33 devices**

When TZF detects the access errors, the TZF error occurs. Table 2.1 shows the system behavior when the TZF error occurred. The behavior varies depending on the master or slave area to be accessed.

**Table 2.1. Behavior when the TZF error ocurred**

| Access to | Access from | |
|---|---|---|
| | **CPU** | **DMAC/DTC** |
| FHBIU (Code Flash)<br>FLBIU (Data Flash)<br>S0BIU (SRAM) | • SecureFault exception occurs | • Transfer does not start<br>• NMI or reset occurs Note1<br>• Interrupt occurs (DMA_TRANSERR) |
| PSBIU (System peripherals)<br>PHBIU (High-speed peripherals)<br>PLBIU (Low-speed peripherals) | • BusFault exception occurs Note2<br>• NMI or reset occurs Note1 | • Stop transfer Note3<br>• NMI or reset occurs Note1 Note3<br>• interrupt occurs Note3 (DMA_TRANSERR) |

Note 1: NMI or reset is selected with OAD (Operation after detection) bit in TZFOAD (TZF Operation After Detection) register.

Note 2: These error behaviors do not occur for write access to the PHBIU or PLBIU address space which memory attribute is set to "Early Write Acknowledgment" by the ARM® MPU.

Note 3: These error behaviors do not occur for write access from DMAC to the PHBIU or PLBIU address space when the bufferable write is enabled by DMBWR.BWE.

For information on the master TZF, please refer to the Bus Error Monitoring Section in the MCU hardware user's manual. The next section shows the error operations and the state clearing flow of the slave TZF.

### 2.1.1 Slave TrustZone Filter

The Slave TZF is applied to FHBIU (code flash), FLBIU (data flash), S0BIU (SRAM), PSBIU (System peripherals), PHBIU (high-speed peripherals) and PLBIU (low-speed peripherals).

When the slave TZF error is detected, the following steps are processed:

1. Store the address of the error in BTZFnERRADD (Bus Error Address) register.
2. Store the read/write information of the error in BTZFnERRRW (Bus Error Read Write) register.
3. Set 1 to STERRSTAT (Slave TZF Error Status) bit of BUSnERRSTAT (Bus Error Status Register) register.

Then an NMI request or reset request is generated depending on the OAD (Operation after Detection) bit setting in the TZFOAD (TZF Operation After Detection) register as shown in Figure 2.2.

Users can recognize the error status by verifying BTZFnERRADD, BTZFnERRRW and BUSnERRSTAT register in the NMI handler or after reset. These registers are kept until reset other than MPU- and TZF-related resets or being cleared by BUSnERRCLR (BUS Error Clear) register.

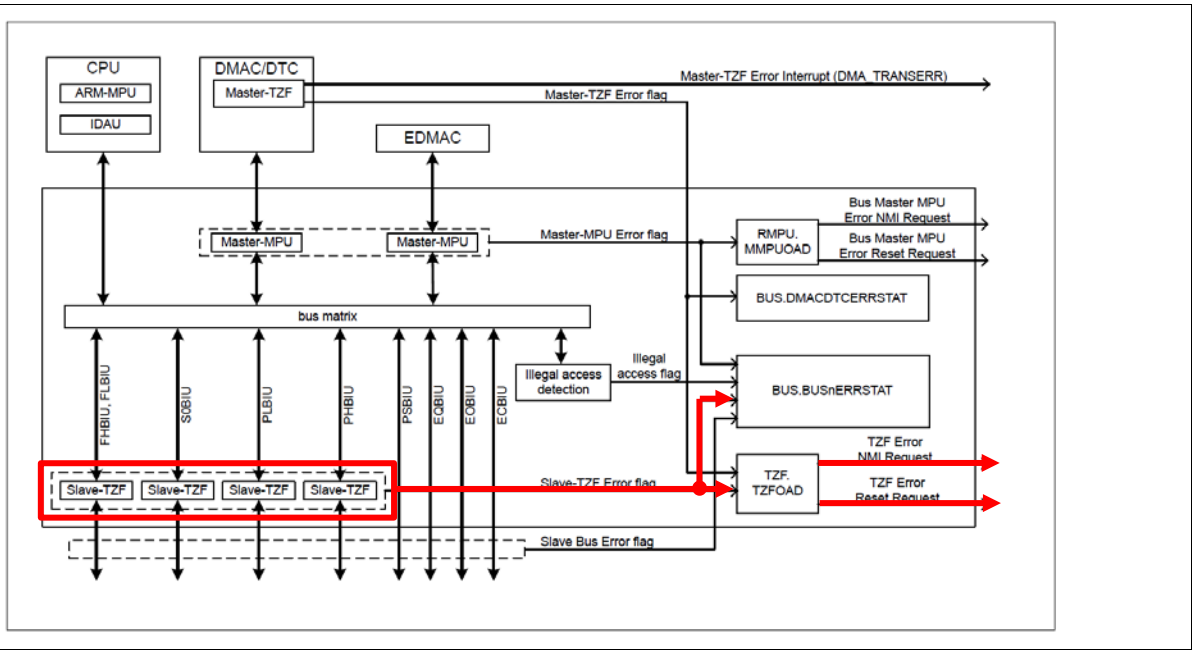



**Figure 2.2 Slave TZF error signal flow**

## 2.2 Bus error processing

To prevent unexpected operation, additional operations below should be added to the BusFault exception handler routine.

1. Verify the error information in the corresponding register
2. Clear the data in cache for the error address
3. Clear the Error Status register in the bus module

Figure 2.3. shows the recommended BusFault exception handling flowchart. For the RA-CM33 devices, one consideration is needed for the Slave TZF error if the TZFOAD register is configured to generate an NMI. In this case, NMI will occur first then the BusFault exception occurs next. The NMI handler should only clear the NMI status, and the bus error status should be cleared in the BusFault handler. Figure 2.4. shows the NMI handling flowchart.

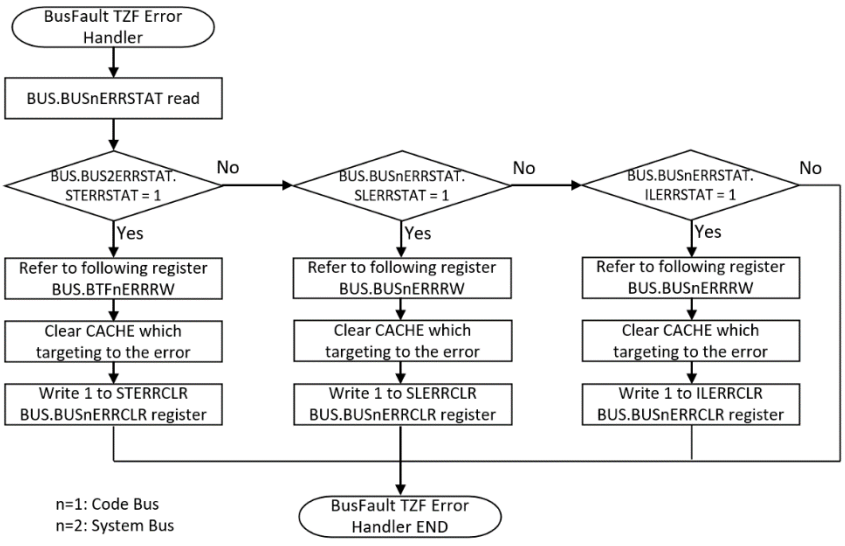



**Figure 2.3. BusFault interrupt handling flowchart**

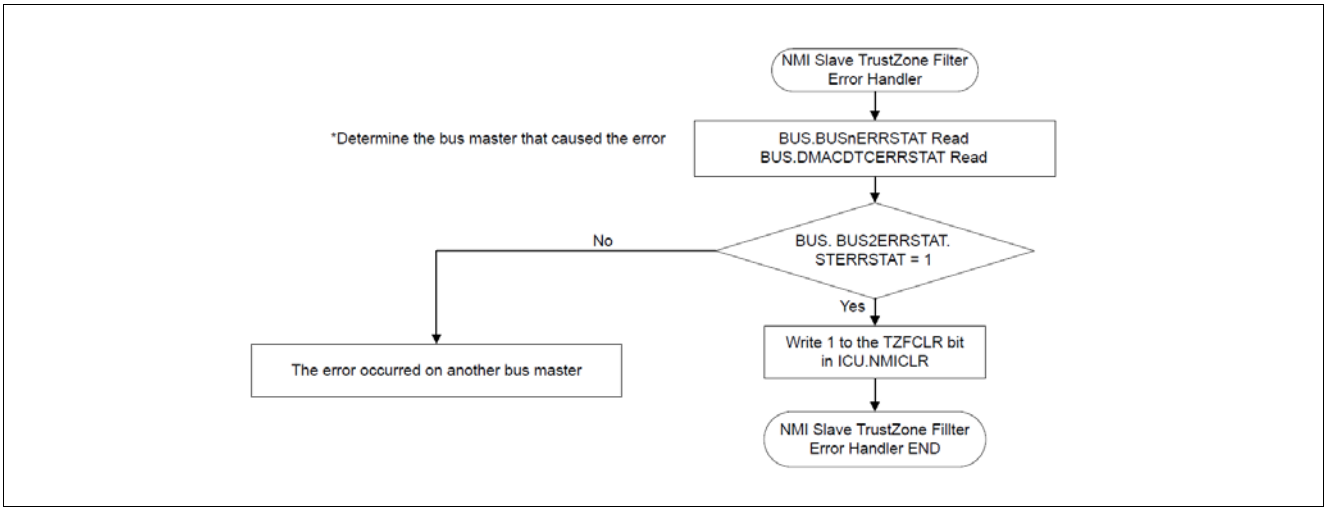



**Figure 2.4. NMI handling flowchart**

## 3. User-Defined Exception Handler

This chapter describes how to implement user-defined exception handlers in Flexible Software Package (FSP)-based projects.

### 3.1 Default implementation

The FSP of RA family MCUs provides Board Support Packages (BSP) to support startups, exception handlers, and so on that depend on the specifications of each device. BSP implements exception handlers in the following source files. These files are independent of the CPU core type and are applied to any devices in the RA family.

In `ra/fsp/src/bsp/cmsis/Device/RENESAS/Source/startup.c`:

- Vector table (Figure 3.1)
- Reset handler function (Figure 3.2)
- Prototype declaration of handler functions (Figure 3.3)
- Default handler function (Figure 3.4)

```
/* Vector table. */
BSP_DONT_REMOVE const exc_ptr_t __Vectors[BSP_CORTEX_VECTOR_TABLE_ENTRIES] BSP_PLACE_IN_SECTION(
    BSP_SECTION_FIXED_VECTORS) =
{
    (exc_ptr_t) (&g_main_stack[0] + BSP_CFG_STACK_MAIN_BYTES), /*      Initial Stack Pointer     */
    Reset_Handler,                                             /*      Reset Handler             */
    NMI_Handler,                                               /*      NMI Handler               */
    HardFault_Handler,                                         /*      Hard Fault Handler        */
    MemManage_Handler,                                         /*      MPU Fault Handler         */
    BusFault_Handler,                                          /*      Bus Fault Handler         */
    UsageFault_Handler,                                        /*      Usage Fault Handler       */
    SecureFault_Handler,                                       /*      Secure Fault Handler      */
    0,                                                         /*      Reserved                  */
    0,                                                         /*      Reserved                  */
    0,                                                         /*      Reserved                  */
    SVC_Handler,                                               /*      SVCall Handler            */
    DebugMon_Handler,                                          /*      Debug Monitor Handler     */
    0,                                                         /*      Reserved                  */
    PendSV_Handler,                                            /*      PendSV Handler            */
    SysTick_Handler,                                           /*      SysTick Handler           */
};
```

**Figure 3.1 Vector table**

```
/*******************************************************************************************************************//**
 * MCU starts executing here out of reset. Main stack pointer is set up already.
 **********************************************************************************************************************/
void Reset_Handler (void)
{
    /* Initialize system using BSP. */
    SystemInit();

    /* Call user application. */
    main();

    while (1)
    {
        /* Infinite Loop. */
    }
}
```

**Figure 3.2 Reset Handler function**

In `ra/fsp/src/bsp/mcu/all/bsp_group_irq.c`:

- NMI handler function (Figure 3.5)

### 3.1.1 Exception Handler Definition

FSP applies the default handler function to various exception handler functions to ensure they exist even if a user did not define each exception handler function. The method of implementation depends on the compiler (Figure 3.3).

```
/* All system exceptions in the vector table are weak references to Default_Handler. If the user wishes to handle
 * these exceptions in their code they should define their own function with the same name.
 */
#if defined(__ICCARM__)
 #define WEAK_REF_ATTRIBUTE

 #pragma weak HardFault_Handler                  = Default_Handler
 #pragma weak MemManage_Handler                  = Default_Handler
 #pragma weak BusFault_Handler                   = Default_Handler
 #pragma weak UsageFault_Handler                 = Default_Handler
 #pragma weak SecureFault_Handler                = Default_Handler
 #pragma weak SVC_Handler                        = Default_Handler
 #pragma weak DebugMon_Handler                   = Default_Handler
 #pragma weak PendSV_Handler                     = Default_Handler
 #pragma weak SysTick_Handler                    = Default_Handler
#elif defined(__GNUC__)

 #define WEAK_REF_ATTRIBUTE    __attribute__((weak, alias("Default_Handler")))
#endif

void NMI_Handler(void);                // NMI has many sources and is handled by BSP
void HardFault_Handler(void) WEAK_REF_ATTRIBUTE;
void MemManage_Handler(void) WEAK_REF_ATTRIBUTE;
void BusFault_Handler(void) WEAK_REF_ATTRIBUTE;
void UsageFault_Handler(void) WEAK_REF_ATTRIBUTE;
void SecureFault_Handler(void) WEAK_REF_ATTRIBUTE;
void SVC_Handler(void) WEAK_REF_ATTRIBUTE;
void DebugMon_Handler(void) WEAK_REF_ATTRIBUTE;
void PendSV_Handler(void) WEAK_REF_ATTRIBUTE;
void SysTick_Handler(void) WEAK_REF_ATTRIBUTE;
```

IAR compiler

GCC compiler
Arm compiler

**Figure 3.3 Definition of exception handlers**

#### 3.1.1.1 GCC compiler and Arm® compiler

The GCC and Arm® compilers use function attributes (weak symbols, alias functions) to apply the default handler function to exception handers, other than the reset handler. The user can overwrite these handlers to user-defined functions if the function is defined using the same name.

#### 3.1.1.2 IAR compiler

The IAR compiler uses pragma (weak symbols) to apply the default handler function to exception handlers, other than the reset handler. The user can overwrite these handlers to user-defined functions if the function is defined using the same name.

### 3.1.2 Default handler

The BSP defines the default handler function (`Default_Handler`) and the function applies identically to exception handlers other than NMI handlers. The default handler function executes a breakpoint instruction to stop the program.

```
/*******************************************************************************************************************//**
 * Default exception handler.
 **********************************************************************************************************************/
void Default_Handler (void)
{
    /** A error has occurred. The user will need to investigate the cause. Common problems are stack corruption
     *  or use of an invalid pointer. Use the Fault Status window in e2 studio or manually check the fault status
     *  registers for more information.
     */
    BSP_CFG_HANDLE_UNRECOVERABLE_ERROR(0);
}
```

**Figure 3.4 Default handler function**

### 3.1.3 NMI handler

The NMI handler function is defined in `bsp_group_irq.c`. When an NMI event occurs, the NMI handler calls a callback function that can be preset by the `R_BSP_GroupIrqWrite()` API. It then clears the status flag.

```
/*******************************************************************************************************************//**
 * Non-maskable interrupt handler. This exception is defined by the BSP, unlike other system exceptions, because
 * there are many sources that map to the NMI exception.
 **********************************************************************************************************************/
void NMI_Handler (void)
{
    uint16_t nmisr = R_ICU->NMISR;

    /* Loop over all NMI status flags */
    for (bsp_grp_irq_t irq = BSP_GRP_IRQ_IWDT_ERROR; irq <= BSP_GRP_IRQ_CACHE_PARITY; irq++)
    {
        /* If the current irq status register is set call the irq callback. */
        if (0U != (nmisr & (1U << irq)))
        {
            (void) bsp_group_irq_call(irq);
        }
    }

    /* Clear status flags that have been handled. */
    R_ICU->NMICLR = nmisr;
}
```

**Figure 3.5 NMI handler function**

## 3.2 How to add user-defined exception handler

### 3.2.1 How to configure NMI handler and faults

#### 3.2.1.1 Enable the additional exceptions

The additional exceptions can be enabled by the following bits. These bits are set 0 (Disable) after reset.

- SCB.SHCSR (System Handler Control and State Register)
  MEMFAULTENA: MemManage enable bit
  BUSFAULTENA: BusFault enable bit
  USGFAULTENA: UsageFault enable bit
  SECUREFAULTENA: SecureFault enable bit Note1

Note 1: Available for a processor with Security Extension

#### 3.2.1.2 Configure the exception for RA-CM33 devices

The target of HardFault, BusFault, and NMI are controlled by the BFHFNMINS (BusFault, HardFault, and NMI Non-Secure) bit in AIRCR (Application Interrupt and Reset Control) register. This register can be configured using the FSP configurator (Figure 3.6).

- **Properties of BSP tab > RAxxx Family > Security > Exceptions > BusFault, HardFault, and NMI Target**

Also, the secure exception prioritization can be controlled by the PRIS (Prioritize Secure exceptions) bit in AIRCR. If this bit is set to 1 (Enabled), Non-Secure exceptions are de-prioritized. In the FSP configurator, the configuration for this bit is:

- **Properties of BSP tab > RAxxx Family > Security > Exceptions > Prioritize Secure exceptions**

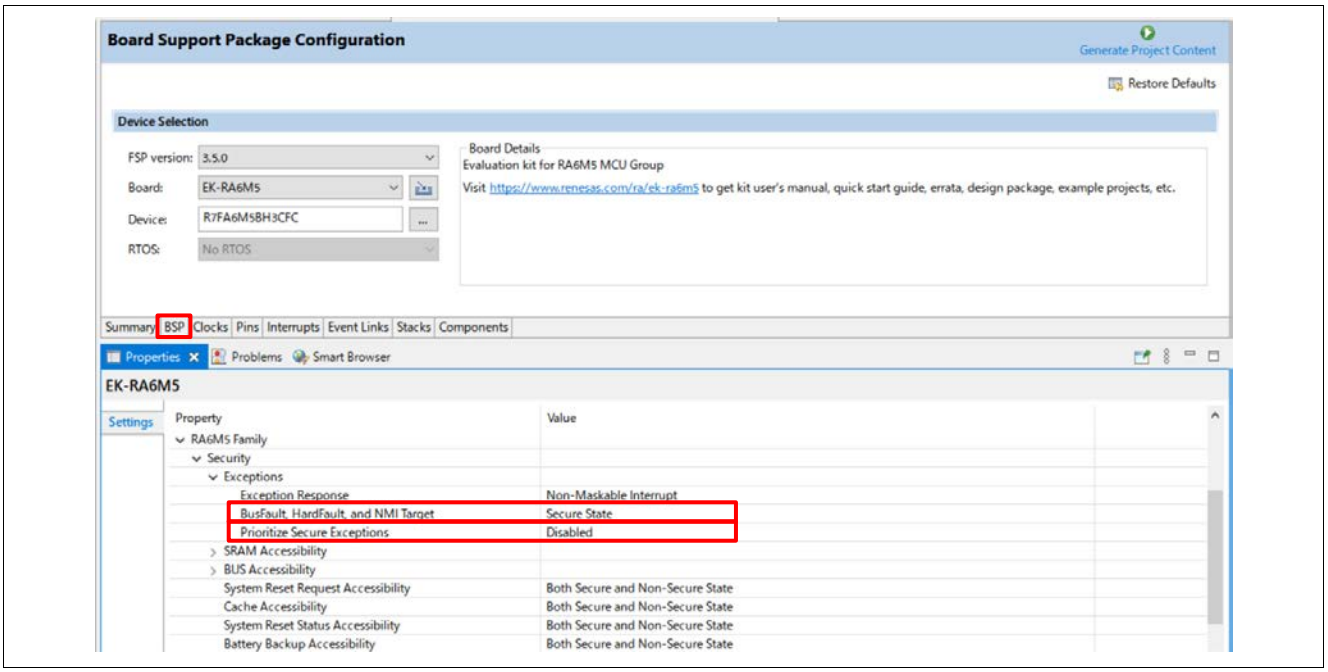



**Figure 3.6 Settings of exception for RA-CM33 devices**

### 3.2.1.3 Configure the Reset Interrupt Request for peripherals

TZF and some peripherals like WDT have options to cause Non-Maskable Interrupt request or Reset output when an exception occurs. For peripherals, most options can be configured in peripheral module driver properties in the **Stacks** tab. For TZF, this can be configured by the following settings in the **BSP** tab (Figure 3.7).

- **Properties of BSP tab > RAxxx Family > Security > Exceptions > Exception Response**

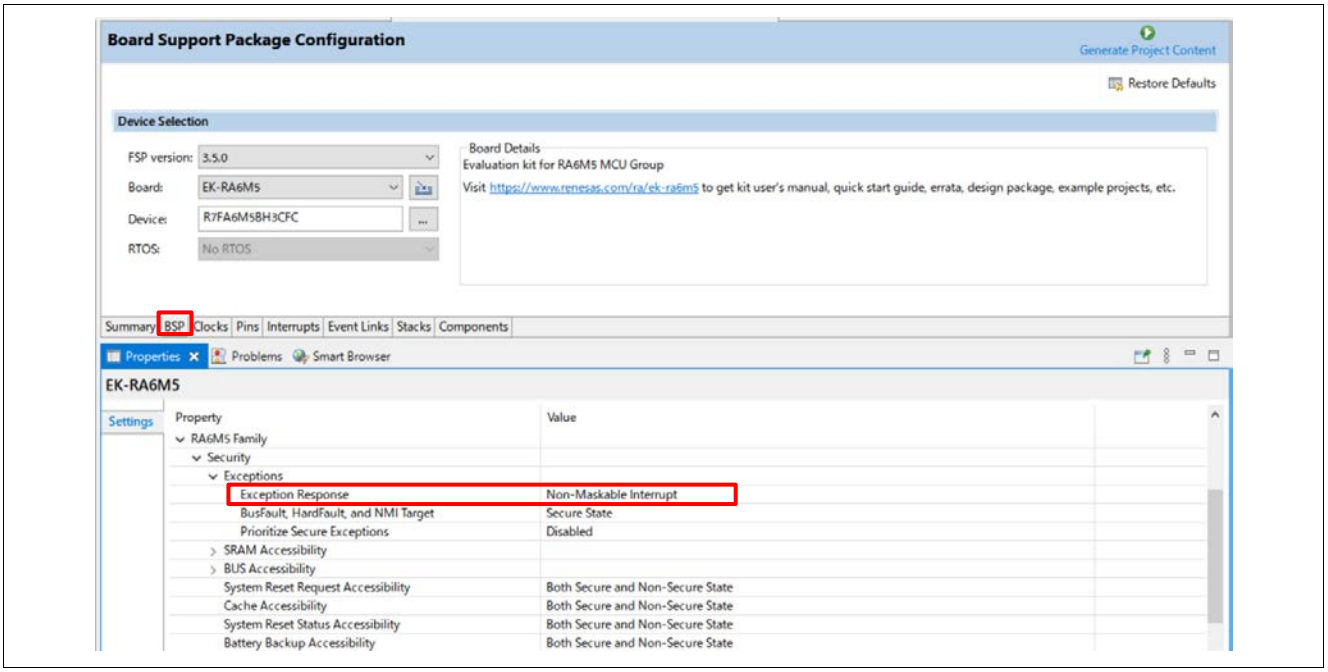



**Figure 3.7 Settings of exception response for TZF**

### 3.2.2 How to implement a user exception handler

As shown in Section 3.1.1, FSP's BSP applies the `Default_Handler()` function to each exception handler, other than the NMI handler, by using weak symbols. These exception handlers can be overwritten to a user-defined exception handler by non-weak definition.

The following shows the example of definition for user HardFault handler.

```
void HardFault_Handler(void);
void HardFault_Handler(void){
    …
}
```

## 3.3 Notes

RA-CM33 implements some security features such as a TrustZone® technology (Armv8-M Security Extension) and DLM (Device Lifecycle Management). These features enable a more secure application and allow for a more secure software development. When an exception occurs, the processor may call a secure exception handler depending on the security settings, but Non-Secure applications may not be able to detect the state. A Secure application may want to provide a user notification for a Non-Secure application.

### 3.3.1 TrustZone® technology

Arm® TrustZone® technology divides the system and the application into Secure and Non-Secure domains. Secure applications can access both Secure and Non-Secure memory and resources. Non-Secure code can access Non-Secure memory and resources, as well as Secure resources through a set of so-called veneers located in the Non-Secure Callable (NSC) region. When developing applications using DLM, you need to be aware of accessible areas by TrustZone® technology.

Note: For the application project with the FSP's Flat Project type, the entire project will be in the Secure domain except for the EDMAC RAM buffers.

### 3.3.2 Device Lifecycle Management

RA-CM33 devices provide Device Lifecycle Management (DLM) that allows users to limit the area that can be accessed from the debug interface and serial programming interfaces. By changing the level of this feature to the next stage, application developers can restrict program code reads from debug interface and serial programming interfaces. When developing an application using DLM, users need to be aware of how DLM works and the current status (Table 3.1). Please refer to MCU's Hardware User's Manual for more information.

**Table 3.1. DLM state in software development stage**

| Lifecycle | Debug level | Serial programming |
|---|---|---|
| SSD<br>(Secure Software Development) | Allows the debug connection<br>Can access all memories and peripherals | Available<br>Can program/erase/read all code/data flash area |
| NSECSD<br>(Non-Secure Software Development) | Allows the debug connection<br>Can access only Non-Secure memory regions and peripherals | Available<br>Can program/erase/read only Non-Secure code/data flash area |

# 4. Debugging exception events

This chapter provides debugging methods for exception events that have occurred. RA family devices provide a variety of debugging environments such as Renesas e$^2$ studio IDE and partner tools. You can use these debugging environments to improve debugging efficiency.

When an exception occurs, it is important to determine the factor, location, and history of the exception event to recognize that state. These can be acquired by checking the related registers and tracing the program execution.

- Confirm the fault related registers
  Determine the factors by checking the related fault state register, and the location of the root cause by checking the CPU general registers that have been retracted into current stack memory.
- Tracing the program execution
  Determine the history of the faults by tracing their execution.

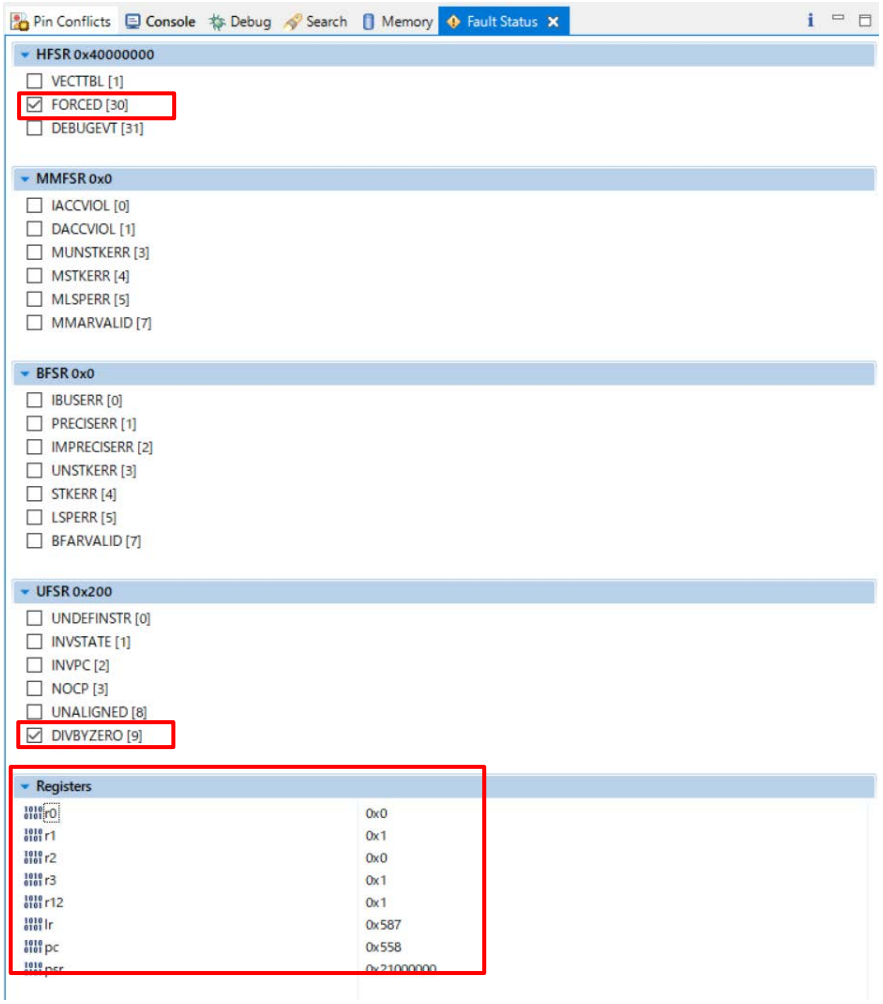
## 4.1 Confirming the fault status

Recognize the fault status using the e² studio view functions or partner tools.

### 4.1.1 View function on Renesas e² studio IDE

The e² studio IDE provides various view functions to visualize the state of the MCU. Refer to *Renesas e² studio 2021-04 or higher User's Manual: Quick Start Guide* (R20UT4989) for more details and usage instructions.

- **Fault Status** view
  The **Fault Status** view displays the related registers with the fault condition and the CPU general registers that have been retracted into stack memory (Figure 4.1. ).
- **Registers** view
  The **Registers** view displays information about the general registers in the CPU core.
- **Memory** view
  The **Memory** view allows users to display and edit the memory. That can be used to check stack memory.
- **Expressions** view
  The **Expressions** view allows users to monitor the value of global variables, static variables, or local variables that stored in the memory. That can be used to check the current value of the user buffer.



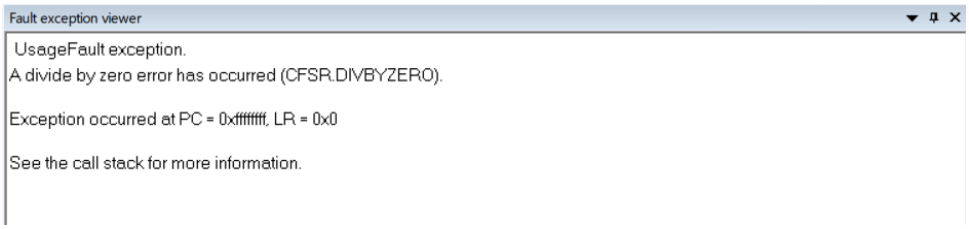

Note: This figure shows the fault status when a division-by-zero error occurs and the UsageFault is disabled.

**Figure 4.1. Fault Status view on e² studio IDE**

### 4.1.2 Partners tools

IAR Embedded Workbench for ARM and Arm® Keil® MDK provide visibility into fault-related status information for RA devices. Figure 4.2 shows an example of the **Fault exception viewer** window that

displays information on the most recent fault exception on the IAR EW for ARM. Please refer to partner tool documentation for more information.




Note: This figure shows the fault status when a dividion-by-zero error occurs.

**Figure 4.2 Fault exception viewer window on the IAR EW for ARM**

## 4.2 Tracing the exception

By tracing the program execution, the history of faults can be recognized.

- Tracing the program execution with Arm® CoreSight trace technology (ETM/SWV trace)
- Tracing the program execution without Processor Core Trace feature

### 4.2.1 Use of Arm® CoreSight trace

Arm® CoreSight technology provides hardware tracing feature such as ETM (Embedded Trace Macrocell) and SWV (Serial Wire Viewer). Using these tracing functions, we can understand the operation of a processor without affecting user program execution. These tracing functions are available for RA-CM4 and RA-CM33 devices.

- ETM
  ETM is a real-time trace module providing all the executed instructions and data tracing of a processor. It requires 4 wires and is an event -riven trace.
- SWV
  SWV provides trace capabilities such as display of reads, writes, exceptions, PC Samples, and printf. It is single wire and is a periodic polling trace.

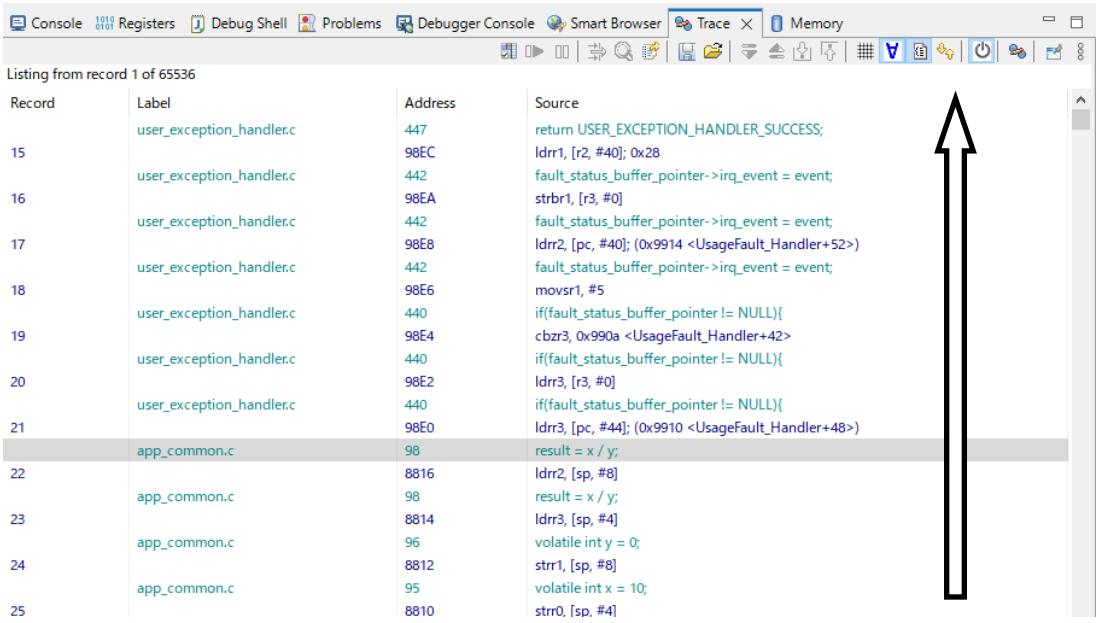
Note: Renesas e$^2$ studio IDE doesn't support ETM trace. We recommended that you use partner tools if you use the ETM trace.

Note: Renesas kits implement the ETM trace interface, but the on-board debugger doesn't support ETM trace. Additional hardware such as Segger J-Trace are required.

### 4.2.2 Use of e$^2$ studio Trace view

The e$^2$ studio IDE provides the program tracing function **Trace** view that can trace the program execution flow through the debugger. The function can be used without additional hardware and software. Therefore, the **Trace** view can be an effective tool for discovering root causes.

Refer to "*enesas e$^2$ studio 2021-04 or higher User's Manual: Quick Start Guide* (R20UT4989) for more details and usage instructions.




Note: This figure shows the fault status when a dividion-by-zero error occurs.

**Figure 4.3. Trace view on e² studio IDE**

# 5. Demonstration

This chapter explains the sample application that demonstrates an exception handling flow for multiple possible faults.

## 5.1 Functional specifications

The sample application implements the following functions.

- **Illegal operation attempt function**
  This function provides some options for attempting the illegal operation. Table 5.1 shows the available options. After the MCU starts, users can select the options by inputting the value on RTT Viewer.
- **Example exception handling function**
  This function implements the processing flow to identify and clear the slave TZF error as shown in section 2.2. When faults are occurred, this function **saves the fault status event**, **clears the status flag**, and **acquires the last execution program counter**. The fault status register values saved in this function are as shown in Table 1.2. The saved fault status will be output to RTT Viewer after system reset.
  Note: The software reset can be enabled by defining the ENABLED_SOFTWARE_RESET macro. If the macro is defined, the system executes software reset after exception operation, otherwise stop the program by breakpoint instruction.
  Note: For EK-RA6M5 projects that use Secure/Non-Secure project types, by default, the acquired fault status events are stored in a Non-Secure region memory buffer for both Secure and Non-Secure exceptions.
- **LED Blinky function (For confirming the CPU is running under no-fault)**
  This function toggles a LED for a test purpose. When LED blinks, that means the MCU is running fine. When it stopped, exception(s) have occurred.

**Table 5.1. Available input options on RTT Viewer**

| RTT Viewer Input | Action | Available exceptions on target MCU kits | | | |
|---|---|---|---|---|---|
| | | EK-RA6M3 (RA-CM4 device) Flat project | EK-RA2E1 (RA-CM23 device) Flat project | EK-RA6M5 (RA-CM33 device) Flat project | EK-RA6M5 (RA-CM33 device) Secure/Non-Secure project |
| “1” | WDT underflow | ✓ NMI | ✓ NMI | ✓ NMI | ✓ NMI |
| “2” | Stack overflow | ✓ NMI | ✓ NMI | ✓ UsageFault | ✓ UsageFault |
| “3” | Execute instruction from illegal region | ✓ MemManage | ✓ HardFault | ✓ MemManage | ✓ MemManage |
| “4” | Divide by zero | ✓ UsageFault | - | ✓ UsageFault | ✓ UsageFault |
| “5” | Access Secure attribute memory from Non-Secure code | - | - | – | ✓ SecureFault |
| “6” | Access Secure attribute peripheral register from Non-Secure code | - | - | – | ✓ NMI, BusFault |
| “7” | Access Secure attribute peripheral register from Non-Secure code via NSC | - | - | – | ✓ (No fault) |
| “10” | Clear the fault status buffer | ✓ | ✓ | ✓ | ✓ |

Note. “✓” : Available, “-”: Not available.

## 5.2 Description of the application project

Table 5.2 describes the sample applications in the application project (zip file). The projects can be downloaded from the Renesas web site.

**Table 5.2. Sample Projects**

| Project Name | Description |
|---|---|
| Exception_Handling_Example_EK_RA6M3_Flat | The sample application with Flat project type for EK-RA6M3 kit |
| Exception_Handling_Example_EK_RA2E1_Flat | The sample application with Flat project type for EK-RA2E1 kit |
| Exception_Handling_Example_EK_RA6M5_Flat | The sample application with Flat project type for EK-RA6M5 kit |
| Exception_Handling_Example_EK_RA6M5_NS<br>Exception_Handling_Example_EK_RA6M5_S | The sample applications with Secure/Non-Secure project type for EK-RA6M5 kit |

The files in Table 5.3 from this application project serve as a reference.

**Table 5.3. Files used in application project**

| File name | Purpose |
|---|---|
| src/hal_entry.c | Contains main application call |
| src/app_main.c | Contains data structures and functions used in main application |
| src/app_common.c | Contains functions used for the LED Blinky function and Illegal operation attempting function |
| src/app_common.h | Accompanying header for exposing functionality provided by app_common.c |
| src/app_message_data.h | Contains macros to output messages and register descriptions to RTT Viewer |
| src/user_exception_handler.c | Contains data structures and functions used in example exception handling function |
| src/user_exception_handler.h | Accompanying header for exposing functionality provided by user_exception_handler.c |
| src/user_nmi_handler.c | Contains functions used in exception handling function |
| src/user_nmi_handler.h | Accompanying header for exposing functionality provided by user_nmi_handler.c |
| src/SEGGER_RTT/* | Implementation of SEGGER real-time transfer (RTT) which allows real-time communication on targets which support debugger memory accesses while the CPU is running |
| src/rtt_common_utils.h | Contains macros, data structures, and functions commonly used across the project |

## 5.3 Used peripheral modules

This application uses the following peripheral modules.

- GPT (General PWM Timer) channel 0: Generate periodic interrupt for the LED toggling. For EK-RA6M5 Secure/Non-Secure projects, the GPT0's security attribute is set to Secure.
- WDT (WatchDog Timer): Generate NMI interrupt when underflow event has occurred.

## 5.4 User interface

Table 5.4 and Figure 5.1. show the pins used for user interfaces.

**Table 5.4. Used pins and connectors**

| User Interface | EK-RA6M3 Kit | EK-RA2E1 Kit | EK-RA6M5 Kit |
|---|---|---|---|
| LED1 | P403 | P915 | P006 |
| PC connector | J10 | J10 | J10 |

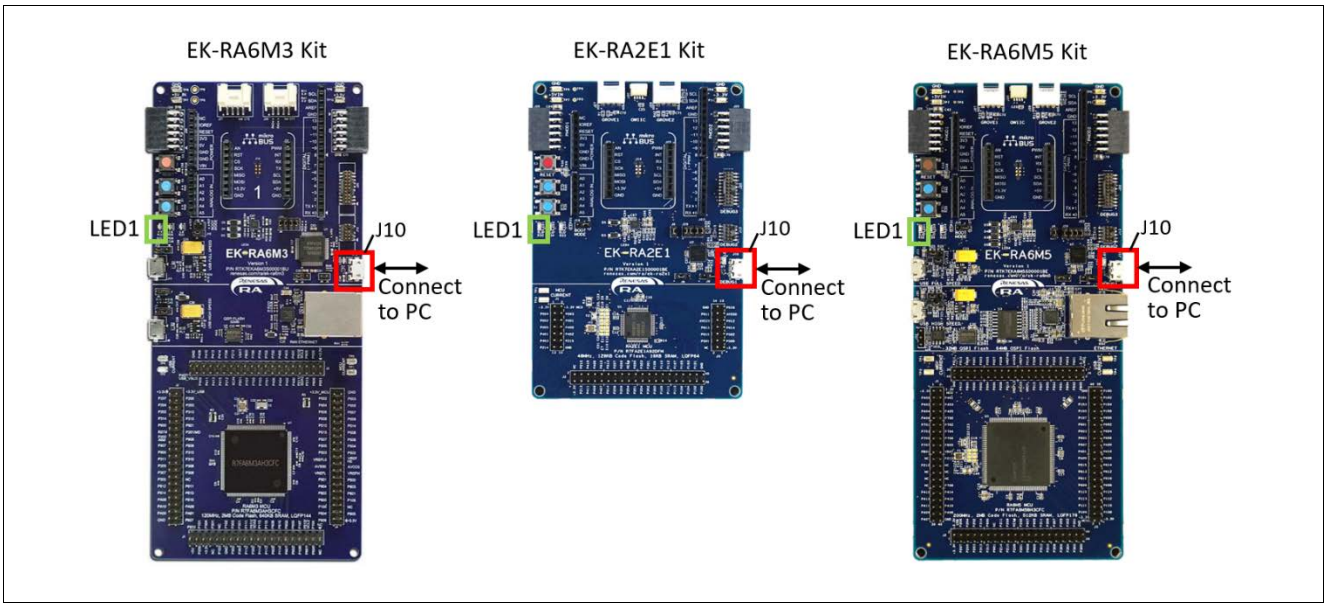



**Figure 5.1. The position of used LED and connector**

## 5.5 Overall algorithms

Figure 5.2 and Figure 5.3 shows the overall algorithms of the sample application.

For EK-RA6M3 Flat project, EK-RA2E1 Flat project and EK-RA6M5 Flat project, please refer to Figure 5.2.

For EK-RA6M5 Secure/Non-Secure project, please refer to Figure 5.3.

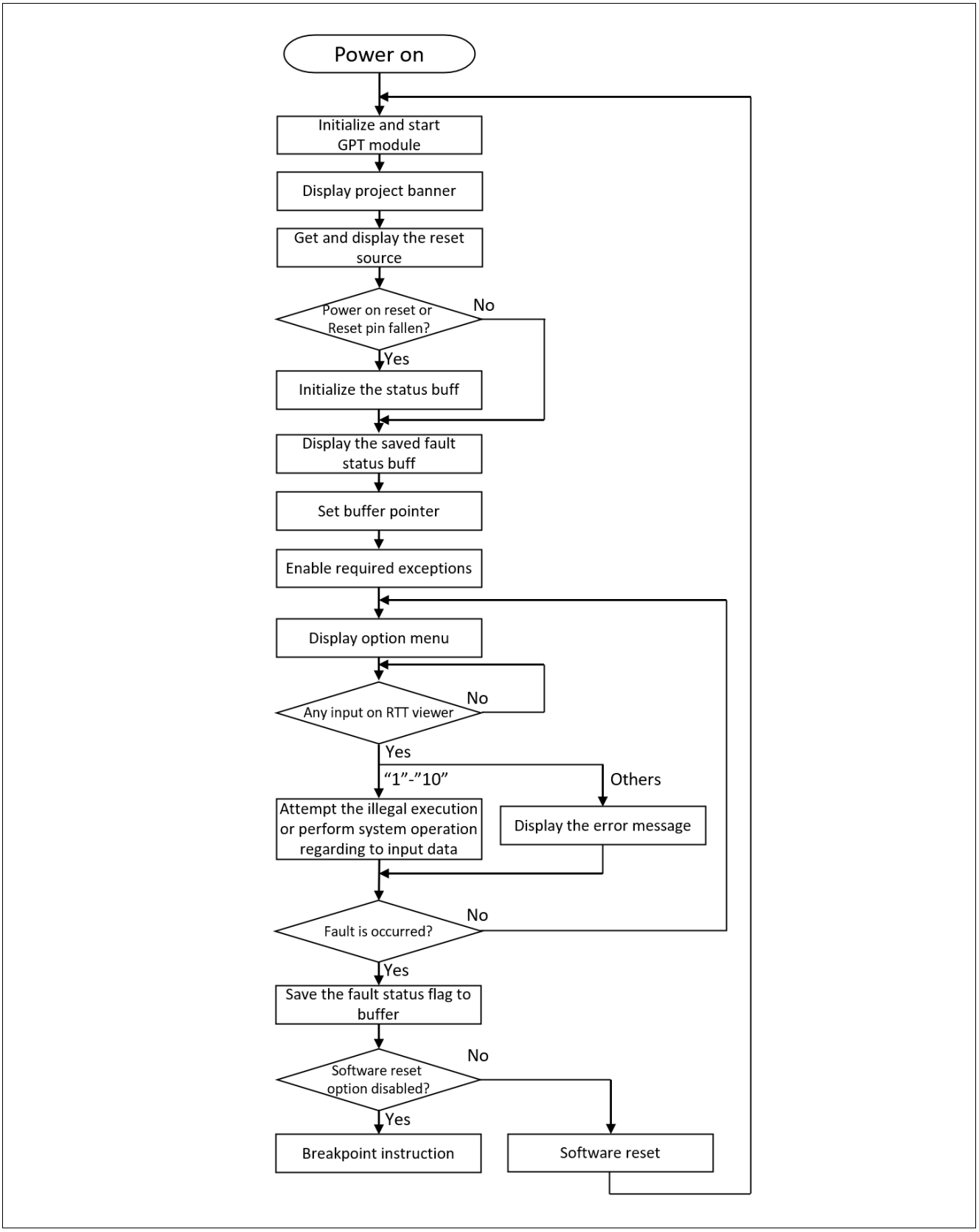



**Figure 5.2 Overall algorithm of sample application (EK-RA6M3 Flat project, EK-RA2E1 Flat project and EK-RA6M5 Flat project**

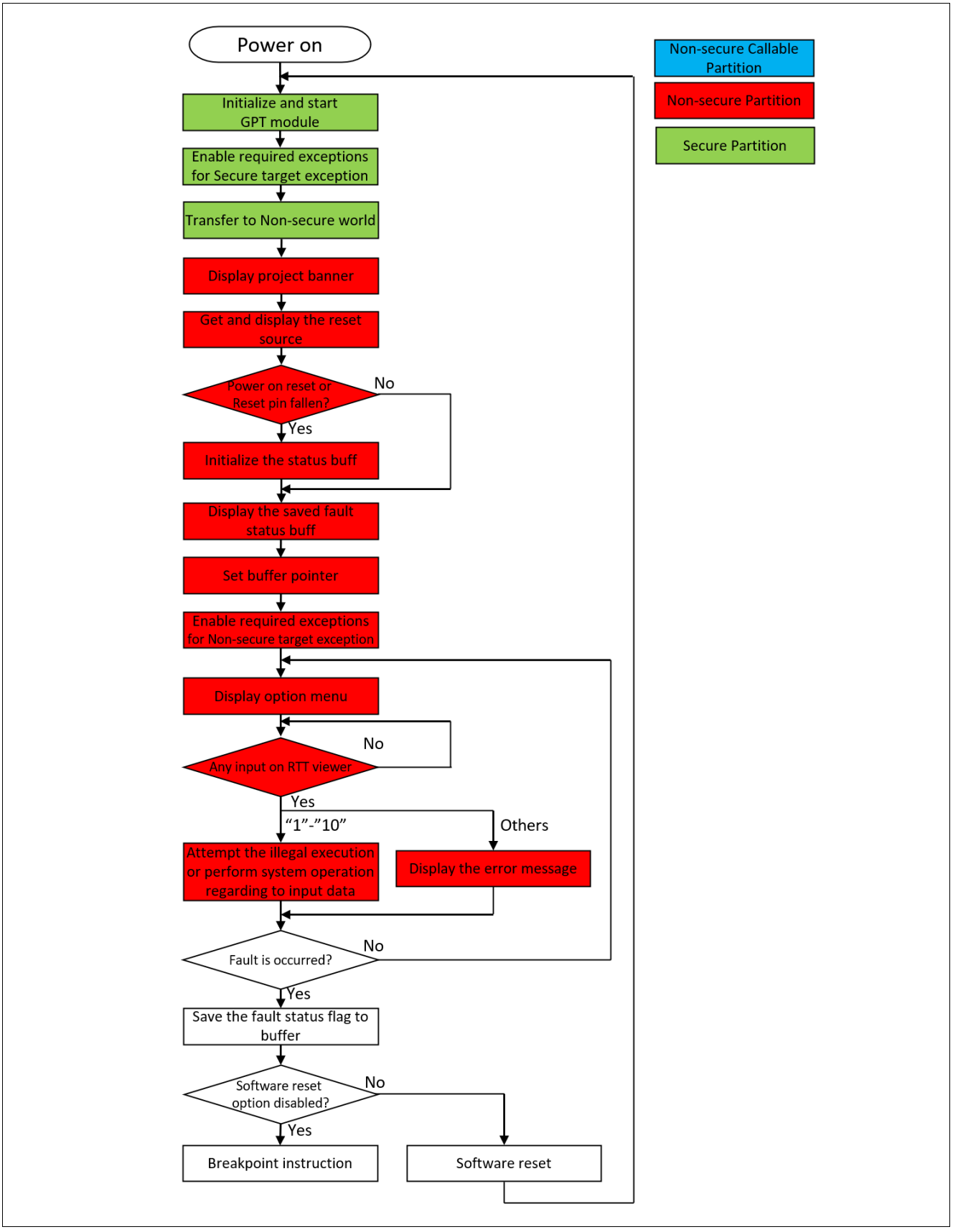



**Figure 5.3 Overall algorithm of sample application (EK-RA6M5 Secure/Non-Secure project)**

## 5.6 Checking procedure

The following steps show the checking procedure of the sample application.

1. Import and build a project. See section 5.6.1.
2. Download program and start debugging. See section 5.6.2.
3. Start the program tracing. See section 5.6.3
4. Press the **Resume** button twice in e$^2$ studio IDE.
5. Connect to the J-Link RTT Viewer. See section 5.6.4.
6. Enter the user selection to J-Link RTT Viewer and Check the behavior. See section 5.8 for more information on this demonstration.

### 5.6.1 Import and build a project

To build an application project with e$^2$ studio ISDE, proceed as follows:

1. Launch e$^2$ studio IDE.
2. Select any workspace in **Workspace launcher**.
3. Close **Welcome** window.
4. Select a **File** > **Import**.
5. Select **Existing Projects into Workspace** from the Import dialog box.
6. Select archive file.
7. Select the project you want to import and click **Finish**.
   Note: For the EK-RA6M5 Secure/Non-Secure projects, please import both the Non-Secure (NS) project and the Secure (S) project.
8. Clicking **Generate Project Content** in the Configurator window
9. Select **Project** > **Build Project**.
   Note: For the EK-RA6M5 Secure/Non-Secure projects, the Secure project (Exception_Handling_Example_EK_RA6M5_S) must be built at first. Then build the Non-secure project (Exception_Handling_Example_EK_RA6M5_NS).

### 5.6.2 Download program and debug

To download an application project and start debugging, proceed as follows.

1. Connect the J10 connector on each kit and PC with a micro-USB cable.
2. Right-click the project and open **Debug Configuration…** from **Debug As**
   Note: For EK-RA6M5 Secure/Non-Secure projects, open the **Debug Configuration** of the Non-Secure project (Exception_Handling_Example_EK_RA6M5_NS) and make sure that both the secure project program and the Non-Secure project program are set to be downloaded (Figure 5.4. )

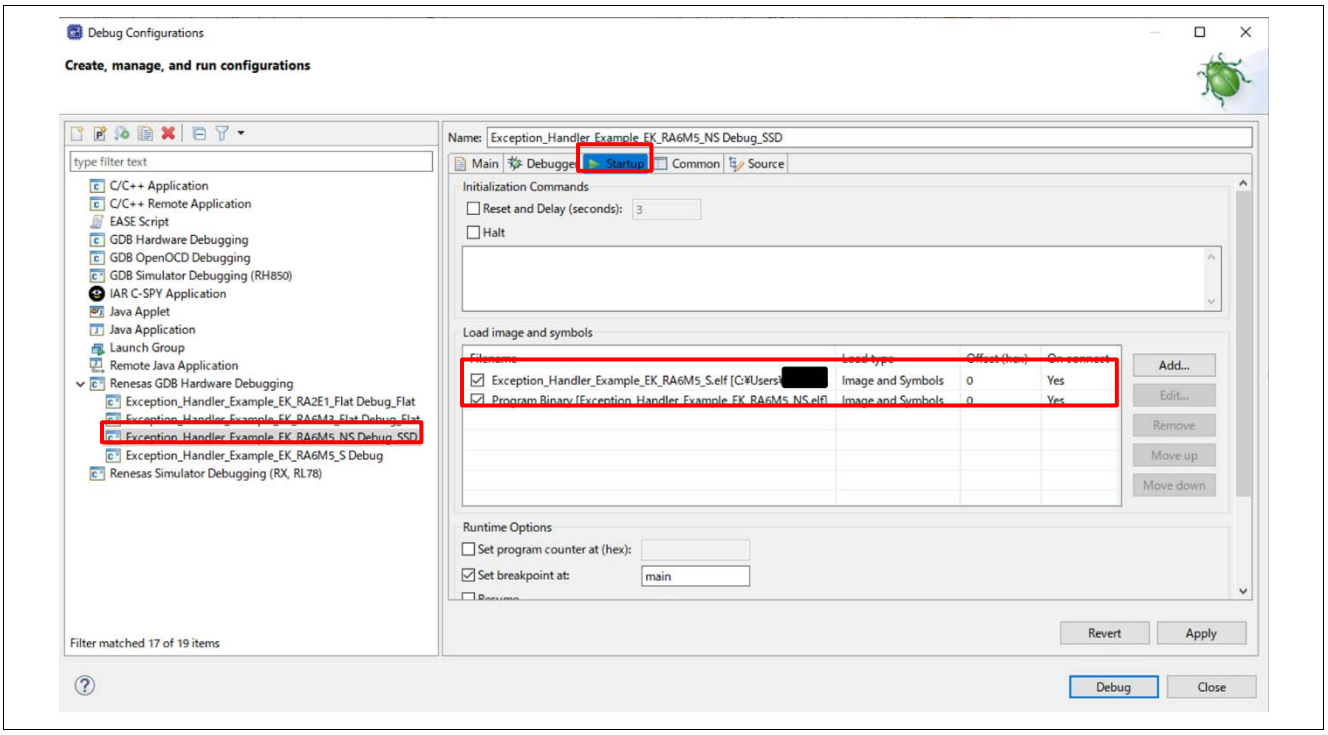



**Figure 5.4. Debug Configuration on EK-RA6M5 Secure/Non-Secure projects**

3. Click **Debug**.

### 5.6.3 Start the program tracing

To trace the program execution, this demonstration uses the **Trace** view function of e$^2$ studio IDE. The **Trace** view is turned off by default. It must be turned on before the target system starts. The **Trace** view can be turned on as follows.

1. Open the **Trace** view window.
2. Press the **Turn Trace On/Off** button at the right-top in the window.

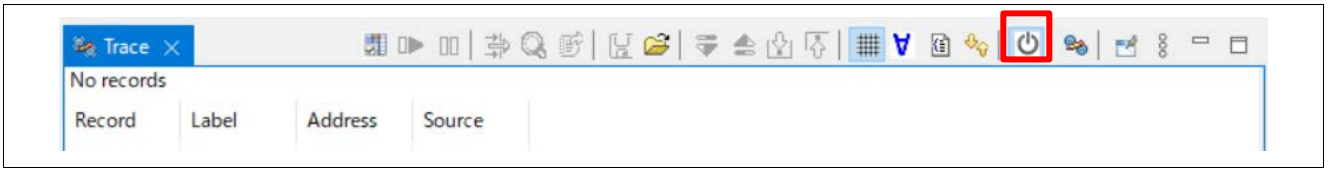



**Figure 5.5. Trace view window**

### 5.6.4 Connect to J-Link RTT Viewer

The sample application uses the Segger J-Link RTT Viewer for inputting/outputting data. The J-Link RTT Viewer can be connected as follows.

1. Launch J-Link RTT Viewer.
2. Configure the settings in Configuration page as follows.
   a. EK-RA6M3 Flat project:
      Specify Target Device：R7FA6M3AH
      RTT Control Block：Auto Detection
   b. EK-RA2E1 Flat project:
      Specify Target Device：R7FA2E1A9
      RTT Control Block：Auto Detection
   c. EK-RA6M5 Flat project and Secure/Non-Secure projects:
      Specify Target Device：R7FA6M5BH
      RTT Control Block：Search Range (Enter “0x20000000 0x10000” in input box)
3. Select **OK**.
4. Configure the Sending settings to **Send on Enter**.

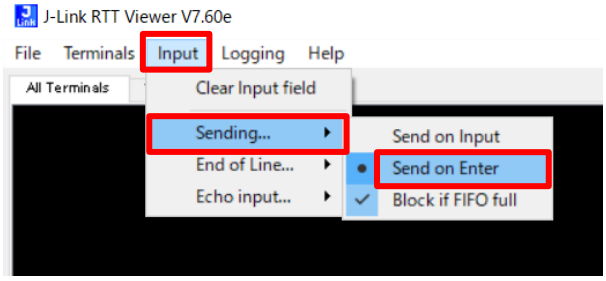



**Figure 5.6 The Sending function on RTT Viewer**

After the program starts, if the connection is successful, a startup message (project banner) can be shown as following Figure 5.7 - Figure 5.9.

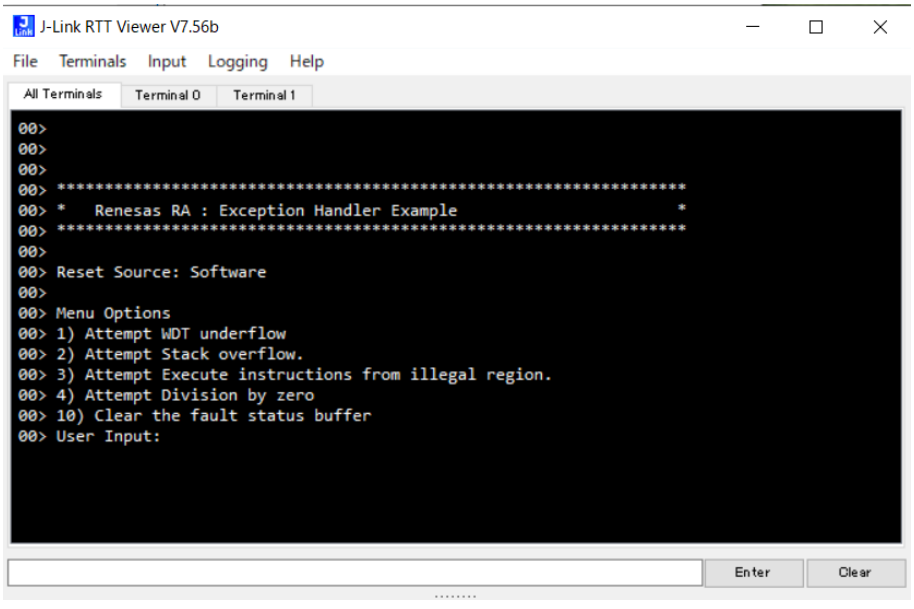



**Figure 5.7 Startup message on J-Link RTT Viewer (EK-RA6M3 Flat project and EK-RA6M5 Flat project)**

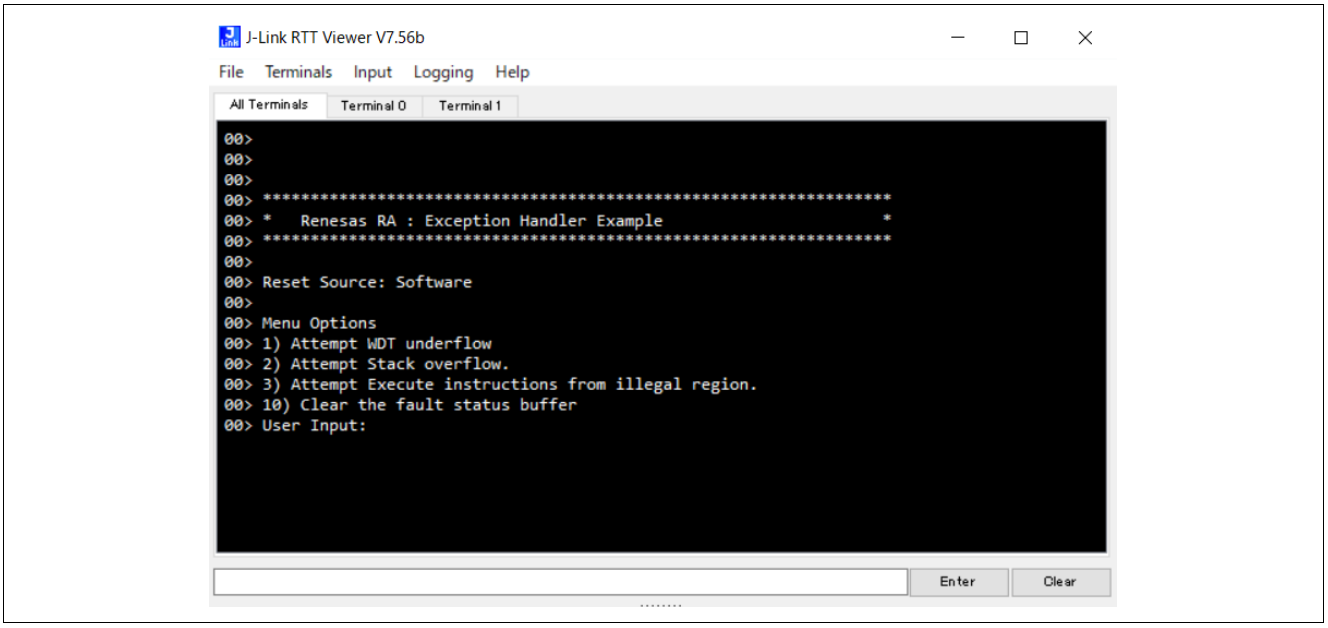



**Figure 5.8 Startup message on J-Link RTT Viewer (EK-RA2E1 Flat project)**

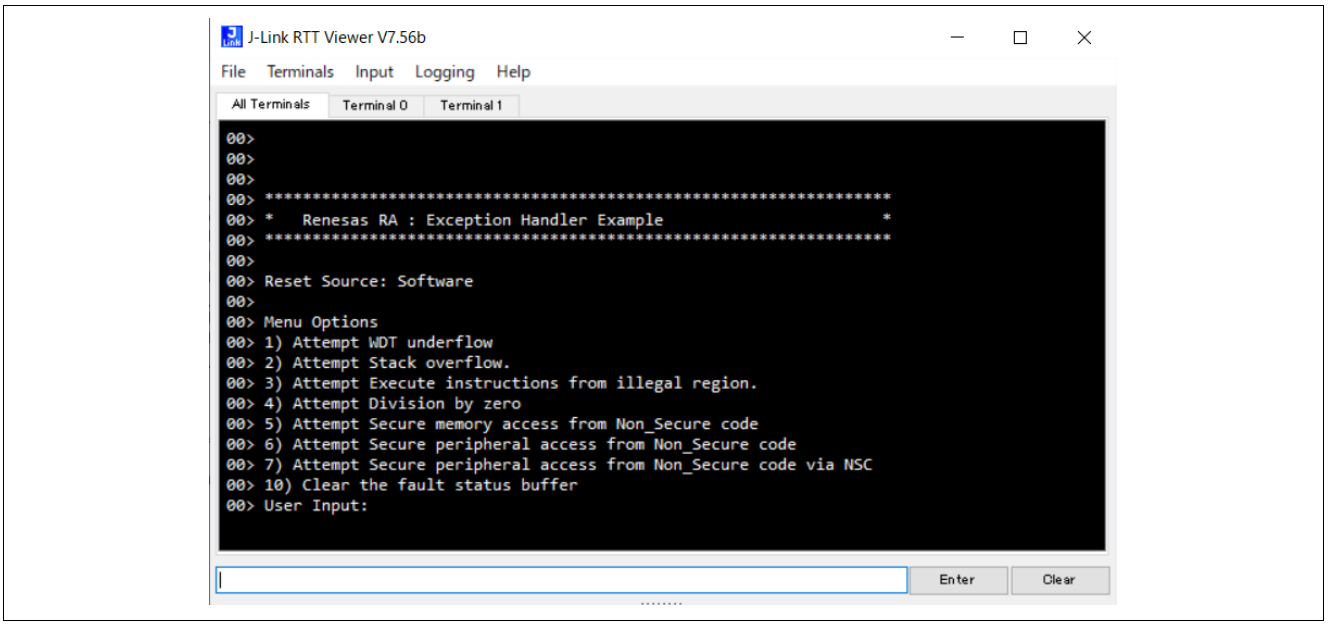



**Figure 5.9 Startup message on J-Link RTT Viewer (EK-RA6M5 Secure/Non-Secure project)**

## 5.7 Expected Results

This section shows the expected results of actions taken by user input. The results shown in this section are examples of running the application project attached to this application note.

For EK-RA6M3 Flat project, please refer to Table 5.5.

For EK-RA2E1 Flat project, please refer to Table 5.6.

For EK-RA6M5 Flat project, please refer to Table 5.7.

For EK-RA6M5 Secure/Non-Secure project, please refer to Table 5.8.

Note: The program address in results will be changed if you change the configurations

Note: The results in RTT Viewer are displayed after the target system restarts, except for successful messages.

**Table 5.5. Expected result on the EK-RA6M3 flat project**

| RTT Viewer Input and Action | Expected Result |
|---|---|
| "1"<br>WDT underflow | • NMI has occurred.<br>• An exception occurred in `bsp_prv_software_delay_loop()` in `bsp_delay.c`<br>• The address that the exception occurs in is not recognized from the buffer data because this sample application acquires the last program counter only when the fault occurs.<br>• The results in RTT Viewer are as follows.<br>`00> NMI WDT Error occurred.` |
| "2"<br>Stack overflow | • NMI has occurred.<br>• An exception occurred at the address 0xCB8 (Line 159 in `common.c`)<br>• The address that the exception occurs in is not recognized from the buffer data because this sample application acquires the last program counter only when the fault occurs.<br>• The results in RTT Viewer are as follows.<br>`00> NMI MPU Stack Pointer error occurred.` |
| "3"<br>Execute instruction from illegal region | • MemManage exception has occurred.<br>• An exception occurred at the address 0xCB4 (Line 147 in `app_common.c`)<br>• The address that the exception occurs in is not recognized from the stack memory that stores the last program counter because this is the program execution error. The above address can be found from the results of the program tracing.<br>• The results in RTT Viewer are as follows.<br>`00> MemManageFault occurred.`<br>`00>  SCB_MMFSR : 0x01`<br>`00>  IACCVIOL: Instruction access violation. The processor attempted an instruction fetch from`<br>`00>  a location that does not permit execution.`<br>`00>`<br>`00>  Last PC address: 0xE0000000` |
| "4"<br>Divide by zero | • UsageFault exception has occurred.<br>• An exception occurred at the address 0xCA0 (Line 133 in `app_common.c`)<br>• The results in RTT Viewer are as follows.<br>`00> UsageFault occurred.`<br>`00>  SCB_UFSR : 0x0200`<br>`00>  DIVBYZERO: The processor has attempted to divide by 0.`<br>`00>`<br>`00>  Last PC address: 0x00000CA0` |
| "10"<br>Clear the fault status buffer | • No exception occurred.<br>• The results in RTT Viewer are as follows.<br>`00> Clear the fault status buffer.`<br>`00> Successful!` |

**Table 5.6. Expected result on the EK-RA2E1 flat project**

| RTT Viewer Input and Action | Expected Result |
|---|---|
| "1"<br>WDT underflow | • NMI has occurred.<br>• An exception occurred in `bsp_prv_software_delay_loop()` in `bsp_delay.c`<br>• The address that the exception occurs in is not recognized from the buffer data because this sample application acquires the last program counter only when the fault occurs.<br>• The results in RTT Viewer are as follows.<br>`00> NMI WDT Error occurred.` |
| "2"<br>Stack overflow | • NMI has occurred.<br>• An exception occurred at the address 0xD54 (Line 159 in `common.c`)<br>• The address that the exception occurs in is not recognized from the buffer data because this sample application acquires the last program counter only when the fault occurs.<br>• The results in RTT Viewer are as follows.<br>`00> NMI MPU Stack Pointer error occurred.` |
| "3"<br>Execute instruction from illegal region | • HardFault exception has occurred.<br>• An exception occurred at the address 0xD48 (Line 147 in `app_common.c`)<br>• The address that the exception occurs in is not recognized from the stack memory that stores the last program counter because this is the program execution error. The above address can be found from the results of the program tracing.<br>• The results in RTT Viewer are as follows.<br>`00> HardFault occurred.`<br>`00>`<br>`00>  Last PC address: 0xE0000000` |
| "10"<br>Clear the fault status buffer | • No exception occurred.<br>• The results in RTT Viewer are as follows.<br>`00> Clear the fault status buffer.`<br>`00> Successful!` |

**Table 5.7. Expected result on the EK-RA6M5 Flat project**

| RTT Viewer Input and Action | Expected Result |
|---|---|
| "1"<br>WDT underflow | • NMI has occurred.<br>• An exception occurred in `bsp_prv_software_delay_loop()` in `bsp_delay.c`<br>• The address that the exception occurs in is not recognized from the buffer data because this sample application acquires the last program counter only when the fault occurs.<br>• The results in RTT Viewer are as follows.<br>`00> NMI WDT Error occurred.` |
| "2"<br>Stack overflow | • UsageFault exception has occurred.<br>• An exception occurred at the address 0x994 (Line 159 in `app_common.c`)<br>• The results in RTT Viewer are as follows.<br>`00> UsageFault occurred.`<br>`00>  SCB_UFSR : 0x0010`<br>`00>  STKOF: Sticky flag indicating whether a stack overflow error has occurred.`<br>`00>`<br>`00>  Last PC address: 0x00000994` |

| RTT Viewer Input and Action | Expected Result |
|---|---|
| “3”<br>Execute instruction from illegal region | • MemManage exception has occurred.<br>• An exception occurred at the address 0x988 (Line 147 in `app_common.c`)<br>• The address that the exception occurs in is not recognized from the stack memory that stores the last program counter because this is the program execution error. The above address can be found from the results of the program tracing.<br>• The results in RTT Viewer are as follows.<br>`00> MemManageFault occurred.`<br>`00>  SCB_MMFSR : 0x01`<br>`00>  IACCVIOL: Instruction access violation. The processor attempted an instruction fetch from`<br>`00>  a location that does not permit execution.`<br>`00>`<br>`00>  Last PC address: 0xE0000000` |
| “4”<br>Divide by zero | • UsageFault exception has occurred.<br>• An exception occurred at the address 0x978 (Line 133 in `app_common.c`)<br>• The results in RTT Viewer are as follows.<br>`00> UsageFault occurred.`<br>`00>  SCB_UFSR : 0x0200`<br>`00>  DIVBYZERO: The processor has attempted to divide by 0.`<br>`00>`<br>`00>  Last PC address: 0x00000978` |
| “10”<br>Clear the fault status buffer | • No exception occurred.<br>• The results in RTT Viewer are as follows.<br>`00> Clear the fault status buffer.`<br>`00> Successful!` |

**Table 5.8. Expected Result on the EK-RA6M5 Secure/Non-Secure project**

| RTT Viewer Input and Action | Expected Result |
|---|---|
| “1”<br>WDT underflow | • Secure world NMI has occurred.<br>• An exception occurred in `bsp_prv_software_delay_loop()` in `bsp_delay.c`<br>• The address that the exception occurs in is not recognized from the buffer data because this sample application acquires the last program counter only when the fault occurs.<br>• The results in RTT Viewer are as follows.<br>`00> S project NMI WDT Error occurred.` |
| “2”<br>Stack overflow | • Non-Secure world UsageFault exception has occurred.<br>• An exception occurred at the address 0x8834 (Line 159 in `app_common.c`)<br>• The results in RTT Viewer are as follows.<br>`00> NS project UsageFault occurred.`<br>`00>  SCB_UFSR : 0x0010`<br>`00>  STKOF: Sticky flag indicating whether a stack overflow error has occurred.`<br>`00>`<br>`00>  Last PC address: 0x00008834` |
| “3”<br>Execute instruction from illegal region | • Non-Secure world MemManage exception has occurred.<br>• An exception occurred at the address 0x882C (Line 147 in `app_common.c`)<br>• The address that the exception occurs in is not recognized from the stack memory that stores the last program counter because this is the program execution error. The above address can be found from the results of the program tracing.<br>• The results in RTT Viewer are as follows.<br>`00> NS project MemManageFault occurred.`<br>`00>  SCB_MMFSR : 0x01`<br>`00>  IACCVIOL: Instruction access violation. The processor attempted an instruction fetch from`<br>`00>  a location that does not permit execution.`<br>`00>`<br>`00>  Last PC address: 0xE0000000` |

| RTT Viewer Input and Action | Expected Result |
|---|---|
| “4”<br>Divide by zero | • Non-Secure world UsageFault exception has occurred.<br>• An exception occurred at the address 0x8818 (Line 133 in app_common.c)<br>• The results in RTT Viewer are as follows.<br>00> NS project UsageFault occurred.<br>00>  SCB_UFSR : 0x0200<br>00>  DIVBYZERO: The processor has attempted to divide by 0.<br>00><br>00>  Last PC address: 0x00008818 |
| “5”<br>Access Secure attribute memory from Non-Secure code | • Secure world SecureFault exception has occurred.<br>• An exception occurred at the address 0x884E (Line 174 in app_common.c)<br>• The results in RTT Viewer are as follows.<br>00> S project SecureFault occurred.<br>00>  SAU_SFSR : 0x00000048<br>00>  AUVIOL: Sticky flag indicating that an attempt was made to access parts of<br>00>  the address spacethat are marked as Secure with NS-Req for the transaction<br>00>  set to Non-secure.<br>00>  SFARVALID: Secure Fault Address Register (SFAR) valid flag.<br>00>  SAU_SFAR : 0x00000010<br>00><br>00>  Last PC address: 0x0000884E |
| “6”<br>Access Secure attribute peripheral register from Non-Secure code | • Secure world NMI and BudFault exception has occurred.<br>• An exception occurred at the address 0x8860 (Line 190 in app_common.c)<br>• The results in RTT Viewer are as follows.<br>00> S project NMI TrustZone error occurred.<br>00> S project BusFault occurred.<br>00>  SCB_BFSR : 0x82<br>00>  PRECISERR: Precise data bus error. A data bus error has occurred, and the PC value stacked<br>00>  for the exception return points to the instruction that caused the fault.<br>00>  BFARVALID: BFAR holds a valid fault address.<br>00>  SCB_BFAR : 0x40169064<br>00><br>00>  Last PC address: 0x00008860 |
| “7”<br>Access Secure attribute peripheral register from Non-Secure code via NSC | • No exception occurred.<br>• The results in RTT Viewer are as follows.<br>00> Attempt to access Secure GPT0 GTPR from Secure code.<br>00> Execution will be successful<br>00> Successful! |
| “10”<br>Clear the fault status buffer | • No exception occurred.<br>• The results in RTT Viewer are as follows.<br>00> Clear the fault status buffer.<br>00> Successful! |

## 5.8 Demonstration

This section demonstrates how to determine the root cause from the related registers and the program tracing results, for the EK-RA6M5 Secure/Non-Secure projects and the following configurations.

| Configurations | Selected value |
|---|---|
| Software reset option in user_exception_handler.h | Not enabled |
| RA6M5 Family → Security → Exceptions → Exception Response | Non-Maskable Interrupt |
| RA6M5 Family → Security → Exceptions →BusFault, HardFault, and NMI Target | Secure State |
| DLM Stage | SSD (Secure Software Development) |

### 5.8.1 Demo 1: Attempt Stack Overflow

Demo 1 shows the demonstration result when attempting a stack overflow.

1. Run the MCU. LED1 blinks.
2. Enter **2** to the input box of the RTT Viewer.
3. System attempts to cause the stack overflow. Then, the system will stop in the NS project `UsageFault_handler()`.
4. Confirm the saved fault status in the buffer to determine the fault factor.


**Figure 5.10. Saved Fault Status**

5. Confirm the stack pointer to determine the location of the root cause
   For RA-CM4 and RA-CM23 project, it can be confirmed from the value “msp” (main stack pointer) or “psp” (process stack pointer) on **Registers** view. For RA-CM33 Secure/Non-Secure projects, the stack pointer separates between Secure and Non-Secure state. Therefore, we should check four stack memories pointed to by msp_s (main stack pointer in secure world), the msp_ns (main stack pointer in Non-Secure world), psp_s (process stack pointer in Secure world) and psp_ns (process stack pointer in Non-Secure world). For an RA-CM33 Flat project, the Non-Secure stack pointer can be ignored since the program is always running in Secure state.
   The stack pointer containing the last program counter can be recognized by the EXC_RETURN value in current link register. Please refer to the section “Exception return” in the processor core’s generic user guide for more details.
   The following figure shows the demonstration that finds the last PC from the stack memory msp_ns points to using **Memory** view.

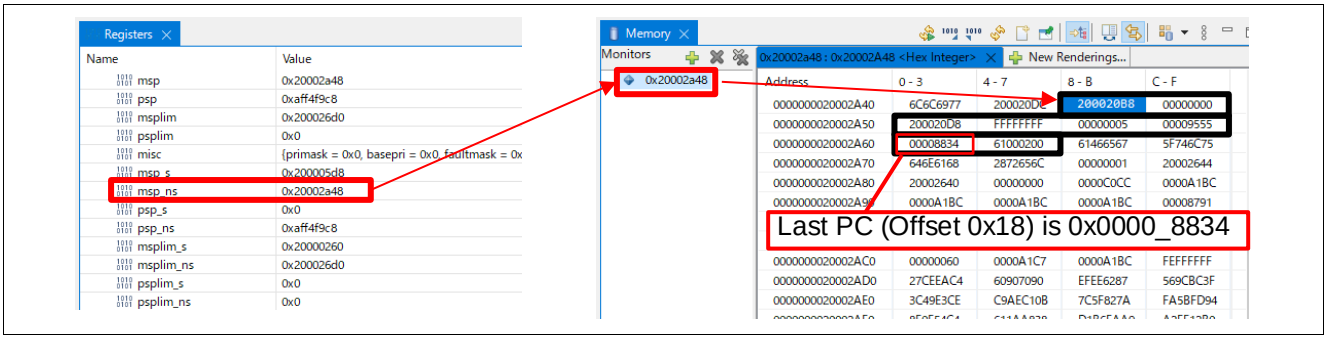



**Figure 5.11. Finding the last PC from msp_ns**

The sample application also implements the last program counter acquisition. So, we can find that result in the buffer as follows.

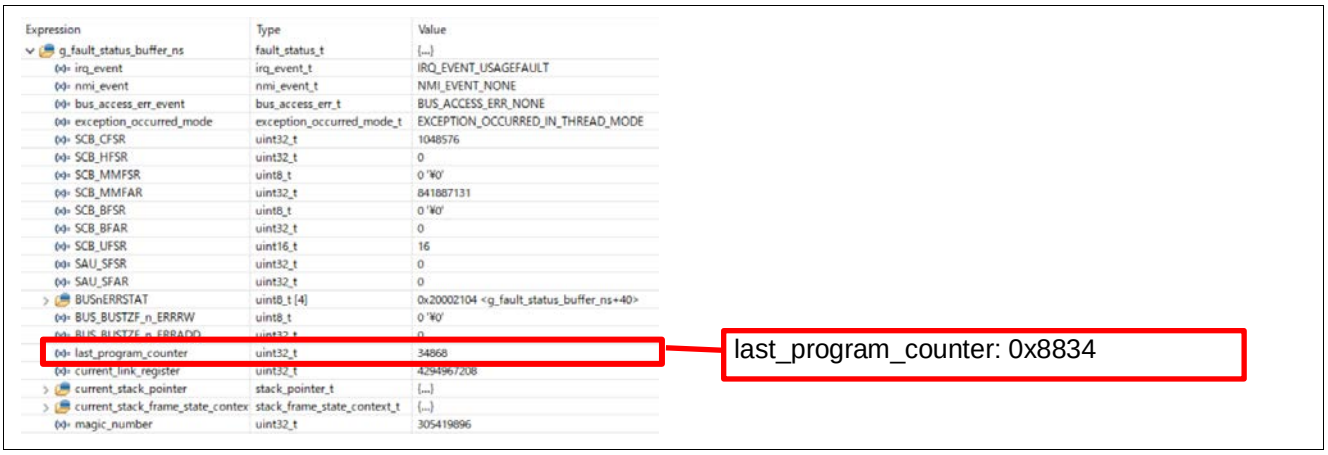



**Figure 5.12. Finding the Last PC from buffer**

From the above results, we found the last executed program address (0x0000_8834).

6. Determine the source code from the last executed program address.
   Open the **Disassembly** view and enter the last program counter address **0x8834** to the input box in top of this view. The view will disassemble the program and highlight the related code as follows.

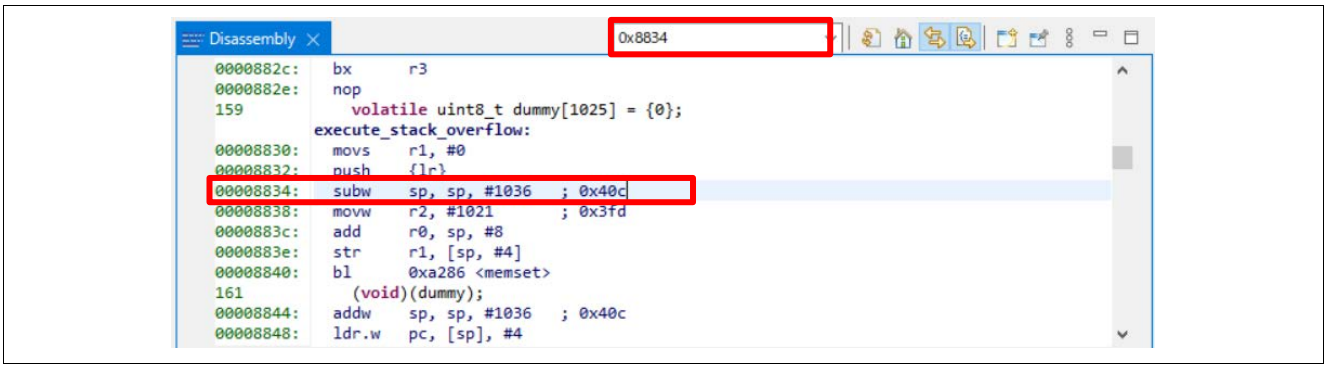



**Figure 5.13. Disassembling code**

You can find the source code and that line number by scrolling up from the highlighted line. Also, when you hover the mouse cursor on the line number of the source code, you can find the file name such as `\Exception_Handling_Example_EK_RA6M5_NS\sec\app_common.c`.

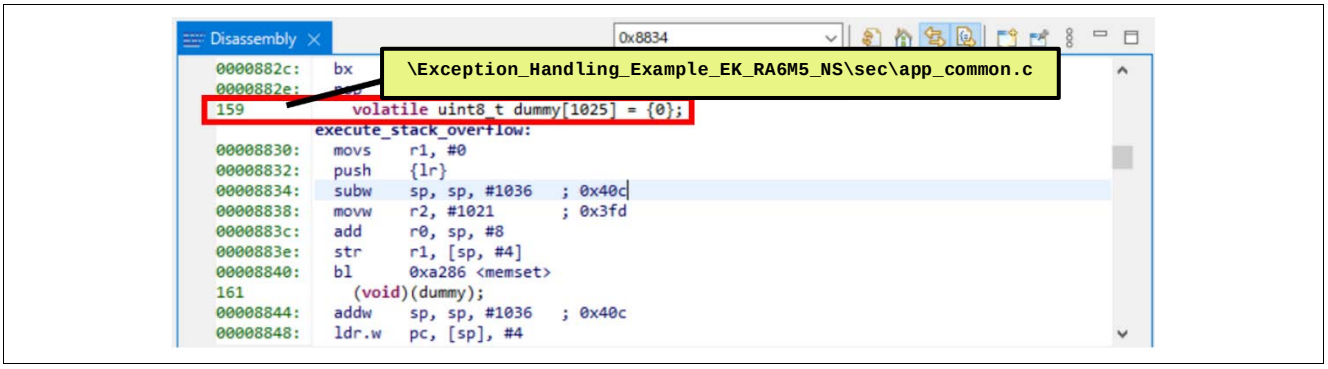



**Figure 5.14. Finding the file name**

Note: If you cannot see the source code, press the **Show Source** button in right-top in this view.

From above, we can find the root cause of the fault that occurred.

- Factor: a stack pointer overflow
- Location: the program address 0x0000_8834 (Line 159 in app_common.c file)

Also, after the system is restarted by pressing the **Reset** button and **Resume** button on e$^2$ studio IDE, the details of the saved fault status are displayed on RTT viewer as follows.

```
00> NS project UsageFault occurred.
00>   SCB_UFSR : 0x0010
00>     STKOF: Sticky flag indicating whether a stack overflow error has occurred.
00>
00>   Last PC address: 0x00008834
```

**Figure 5.15. Saved fault status after restart**

### 5.8.2 Demo 2: Attempt to execute instruction from illegal region

Demo 2 shows the demonstration result when attempting an execution from an illegal region.

1. Run the MCU. LED1 blinks.
2. Enter **3** to the input box of the RTT Viewer.
3. System attempts to execute instruction from an illegal region (0xE0000000). Then the system will stop in the NS project's `MemManage_handler()`.
4. Confirm the saved fault status in the buffer to determine the fault factor.

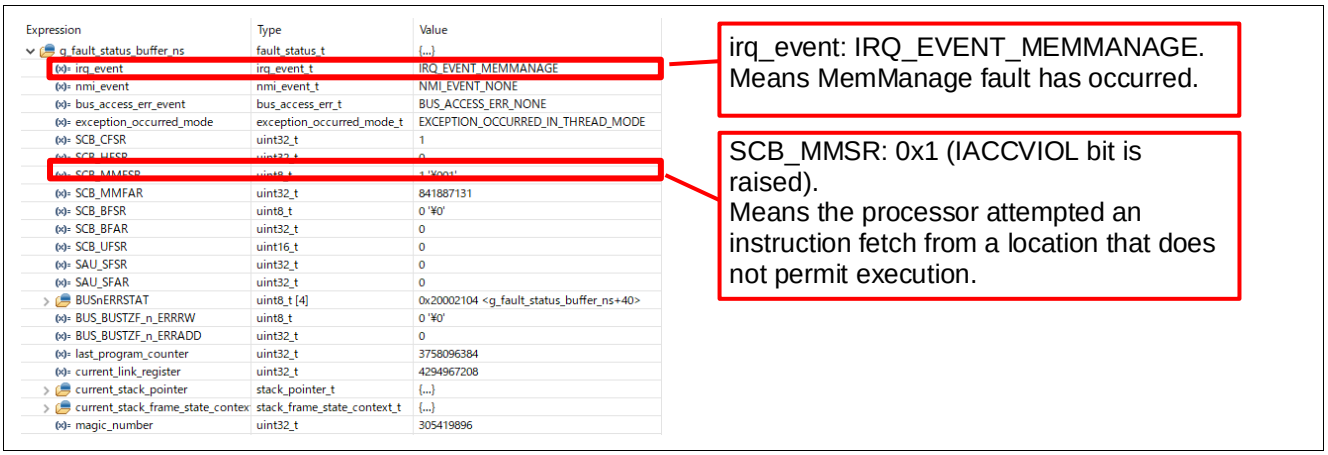



**Figure 5.16. Determine fault factor**

5. Confirm the stack pointer to determine the location of root cause
   From the following results, we found the last executed program address (0xE000_0000) from the buffer. But its address is out of the flash area. Therefore, we cannot get the information from the stack memory.

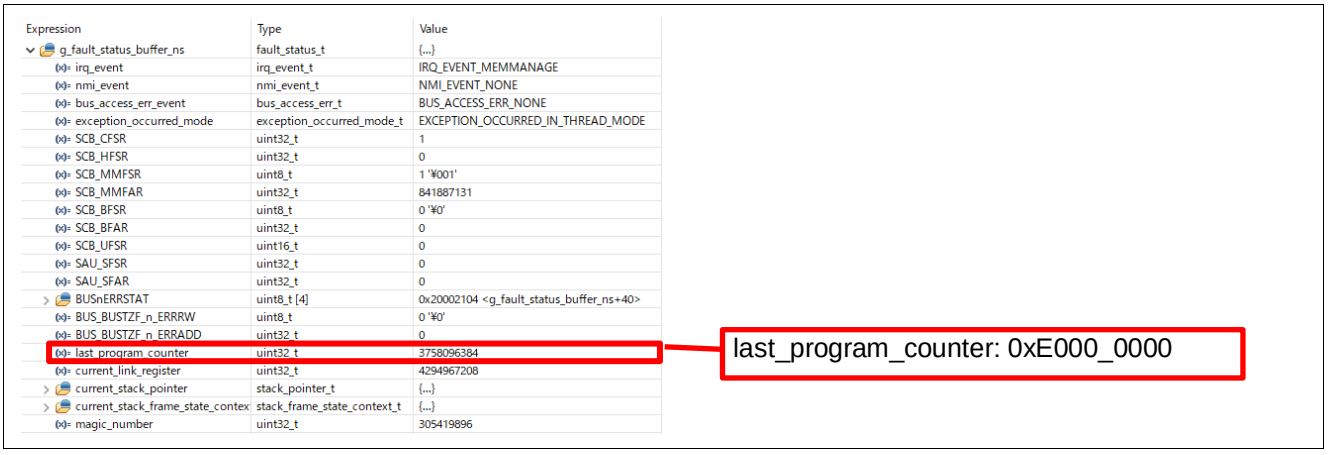



**Figure 5.17. Program counter outside flash area**

6. Check the tracing result.
   When the MCU stops, the **Trace** view will show the tracing result in order of the execution history.
   By default, only the executed program address is displayed. Selecting the **Source** button and **Disassembly** button is recommended to easily understand the related program.
   We can find the exception entry point by scrolling the line. In the below example, the fault has occurred after the record number 89. Also, from the displayed results, we find the related source code, the file name (`app_common.c`), and line number (Line 147).

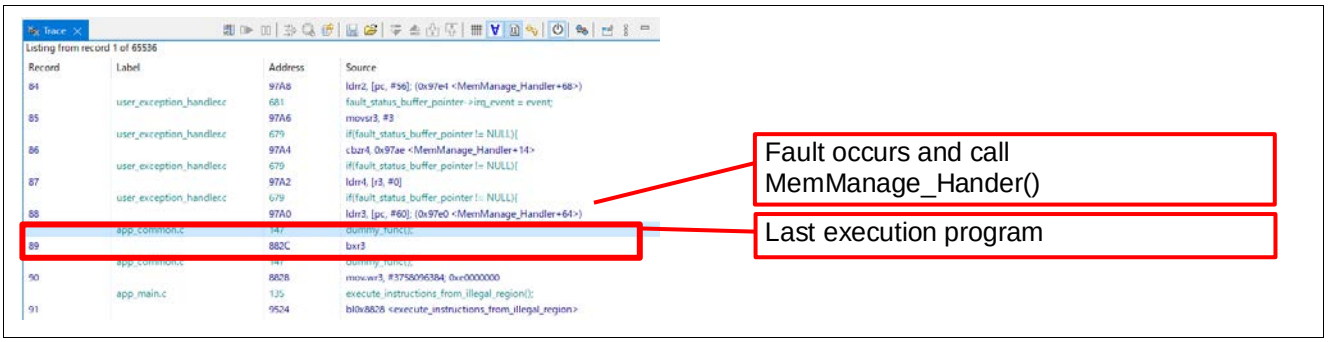



**Figure 5.18. Checking trace results**

From the above, we can find the root cause of the fault that occurred.

- Factor: a processor attempted an execution from an unpermitted location
- Location: the program address 0x0000_882C (Line.147 in app_common.c file)

Also, after pressing the **Reset** button and **Resume** button on e$^2$ studio IDE has restarted the system, the details of the saved fault status are displayed on RTT viewer as follows.

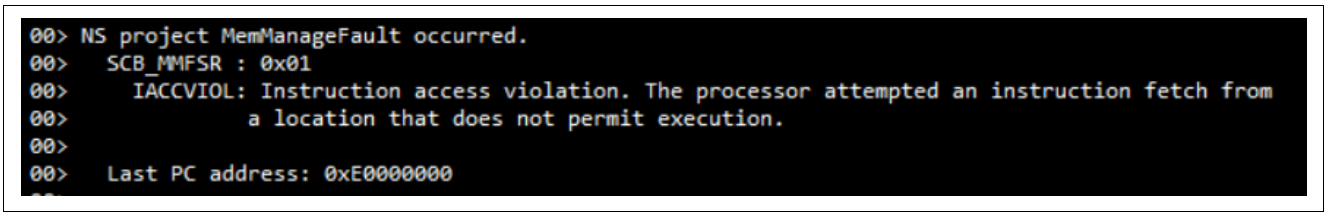



**Figure 5.19. Saved fault status displayed on RTT viewer**

### 5.8.3 Demo 3: Attempt Secure peripheral access from Non-Secure code

The Demo 3 shows the demonstration result when attempting a secure peripheral access from Non-Secure code without NSC call.

1. Run the MCU. LED1 blinks.
2. Enter **6** to the input box of the RTT Viewer.
3. System attempts a Secure peripheral access from Non-Secure code. Then the system will stop in the S project's `BusFault_handler()`.
4. Confirm the status of the fault status buffer.

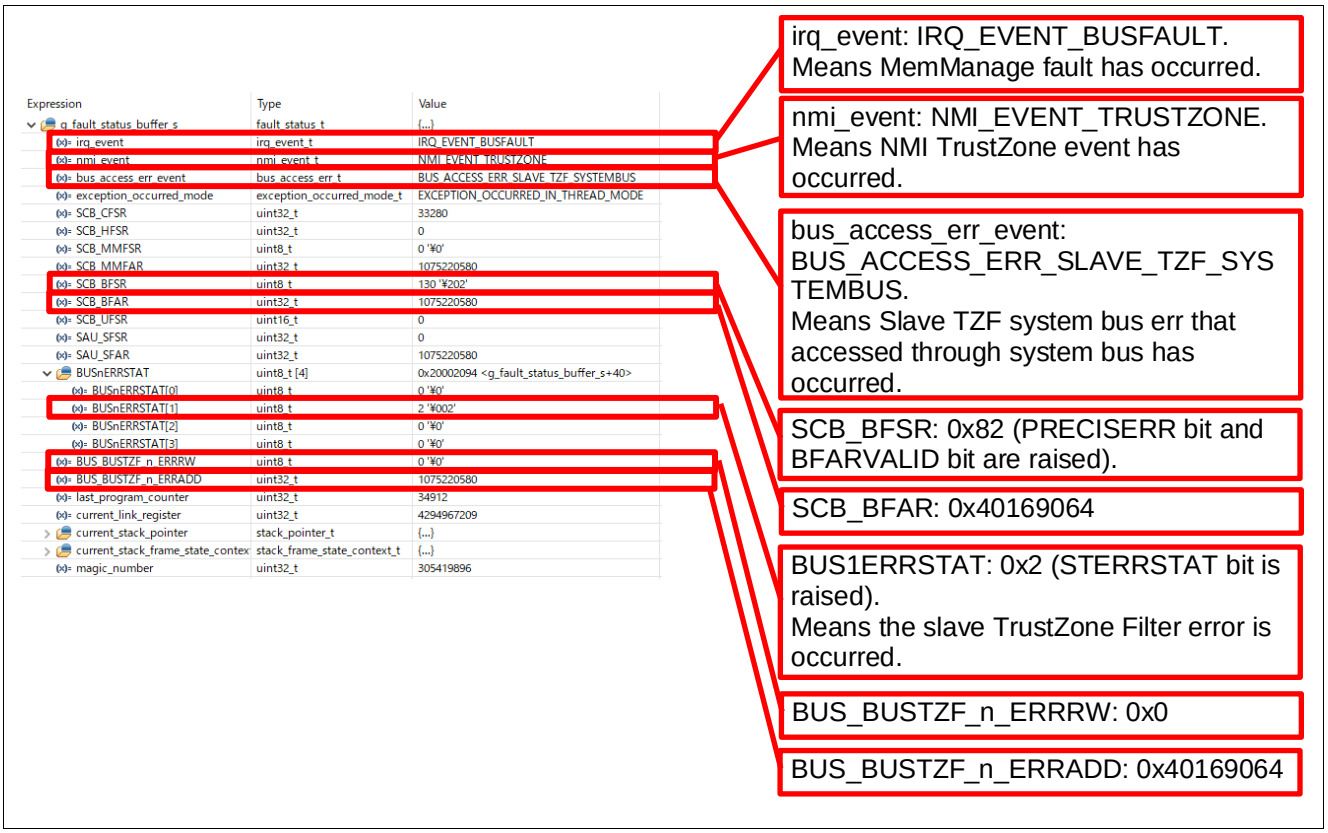



**Figure 5.20. Status of the fault status buffer**

5. Confirm the stack pointer to determine the location of root cause.
   From the following results, we found the last executed program address (0x0000_8860) from the buffer.

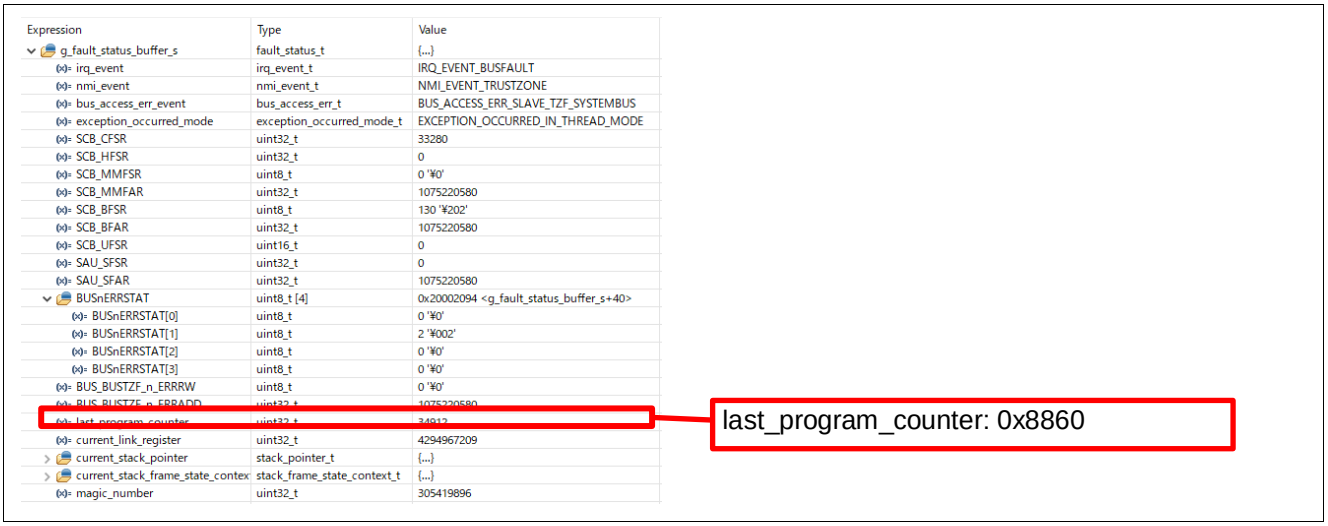



**Figure 5.21. Finding the last PC from buffer**

6. Determine the source code from the last program counter address.
   From the following results, we found the source code (Line 190 in app_common.c).

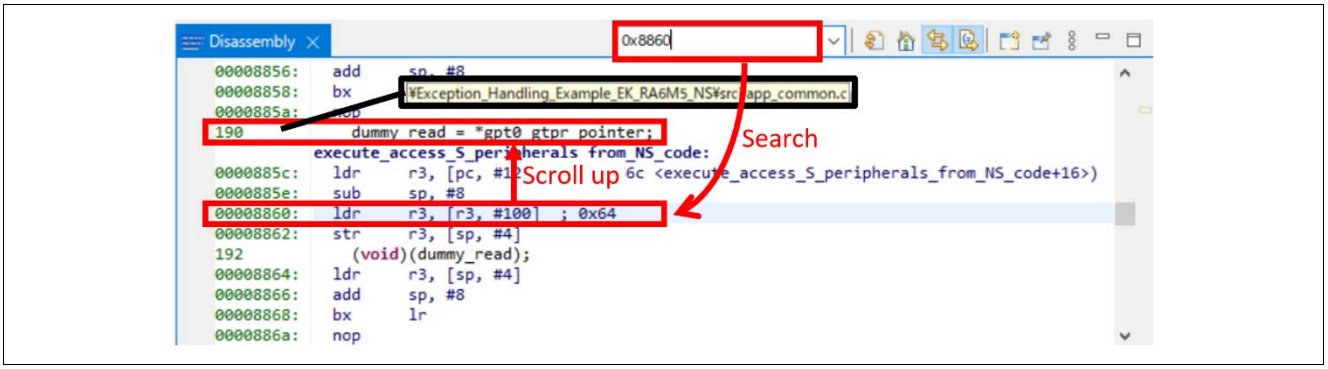



**Figure 5.22. Determine the source file**

From the above, we can find the root cause of the fault that occurred.

- Factor: illegal access from the Non-Secure world to a Secure attributed peripheral register (0x40169064)
- Location: the program address 0x0000_8860 (Line 190 in app_common.c file)

Also, after pressing the **Reset** button and **Resume** button on the e$^2$ studio IDE has restarted the system , the details of the saved fault status are displayed on RTT viewer as follows.

```
00> S project NMI TrustZone error occurred.
00> S project BusFault occurred.
00>   SCB_BFSR : 0x82
00>     PRECISERR: Precise data bus error. A data bus error has occurred, and the PC value stacked
00>               for the exception return points to the instruction that caused the fault.
00>     BFARVALID: BFAR holds a valid fault address.
00>   SCB_BFAR : 0x40169064
00>
00>   Last PC address: 0x00008860
```

**Figure 5.23. Saved fault status displayed on RTT viewer**

## 5.9 Using example exception handler in your projects

This application note provides an example exception handler. You can apply it to your projects in the following manner.

1. Copy the following files to your project.
   — user_exception_handler.c
   — user_exception_hanlder.h
2. Add the following code to your project to enable the example exception handler.

```
#include "user_exception_handler.h"  ← Include directive
fault_status_t   <user-defined buffer name>; ← Definition of user buffer
…
void hal_entry{
f_clear_fault_status_buffer(&<user-defined buffer name>);  ← Initialize user
buffer
f_set_fault_status_buffer(&<user-defined buffer name>);  ← Set user buffer
pointer to program
f_enable_additional_faults(); ← Enable additional faults
…
}
```

## 6. References

- Renesas FSP User's Manual renesas.github.io/fsp
- Renesas RA MCU datasheet Select the relevant MCUs from the www.renesas.com/ra
- Example Projects github.com/renesas/ra-fsp-examples

- Arm® Cortex®-M4 Devices Generic User Guide: https://developer.arm.com/documentation/dui0553
- Arm® Cortex®-M23 Devices Generic User Guide: https://developer.arm.com/documentation/dui1095
- Arm® Cortex®-M33 Devices Generic User Guide: https://developer.arm.com/documentation/100235

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Visit the following URLs to learn about key elements of the RA family, download components and related documentation, and get support.

| | |
|---|---|
| RA Product Information | renesas.com/ra |
| RA Product Support Forum | renesas.com/ra/forum |
| RA Flexible Software Package | renesas.com/FSP |
| Renesas Support | renesas.com/support |

## Revision History

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Mar.23.22 | — | First release document |
| | | | |

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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