Verification Guide

PCB design guideline for DDR4/DDR3L

RZ/G2L PBGA 15.0/21.0sq
RZ/G2LC PBGA 13.0sq
RZ/G2UL PBGA 13.0sq
RZ/V2L PBGA 15.0/21.0sq
RZ/Five PBGA 13.0sq/11.0sq
RZ/A3UL PBGA 13.0sq

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

This guideline provides a PCB design method that considers fulfilling verification items in " [Ref] PCB verification guide for DDR4/DDR3L".

Topologies and net names used in this guideline referred to Evaluation Board Kit for individual RZ MPU and Internal Evaluation Boards manufactured by Renesas Electronics Corporation.

The nine topologies explained in this document are as below:

Topology	DRAM	Product	SoC	System Rank	PCB Layers	SoC to DDR	SoC/DDR	Targeted board
T-1bc T-1vbc (*1)	DDR4	RZ/G2L RZ/V2L	15.0sq	Single	6	1:1	Top/Top	RTK9744L23S01000BE RTK9754L23S01000BE
T-1vc	DDR4	RZ/V2L	15.0sq	Dual	6	1:2	Top/Clamshell	For Renesas Internal Evaluation Only (1)
T-3bc	DDR4	RZ/G2LC	13.0sq	Single	6	1:1	Top/Top	RTK9744C22S01000BE
T-1b	DDR4	RZ/G2L	15.0sq	Single	4	1:1	Top/Top	For Renesas Internal Evaluation Only (2)
T-2c T-2vc (*2)	DDR4	RZ/G2L RZ/V2L	21.0sq	Dual	6	1:2	Top/Clamshell	For Renesas Internal Evaluation Only (3)
T-3cl	DDR3L	RZ/G2LC	13.0sq	Dual	6	1:2	Top/Clamshell	For Renesas Internal Evaluation Only (4)
T-3bcud2	DDR4	RZ/G2UL RZ/Five RZ/A3UL	13.0sq	Single	6	1:1	Top/Top	RTK9743U11S01000BE RTK9743F01S01000BE RTK9763U02S01000BE RTK9763U02S01001BE
T-3bcud	DDR4	RZ/G2UL RZ/Five RZ/A3UL	13.0sq	Single	6	1:1	Top/Top	For Renesas Internal Evaluation Only (5)
T-3bcul	DDR3L	RZ/G2UL RZ/Five RZ/A3UL	13.0sq	Single	6	1:1	Top/Top	For Renesas Internal Evaluation Only (6)
T-11bv	DDR4	RZ/Five	11.0sq	Single	4	1:1	Top/Top	For Renesas Internal Evaluation Only (7)

Note 1. RZ/G2L is pin-compatible with RZ/V2L. The only difference between T-1bc and T-1vbc is the SoC.

Note 2. The only difference between T-2c and T-2vc is the SoC.

Every verification item listed in the REF must be verified through SI and PDN simulations, even if you copied the layout.

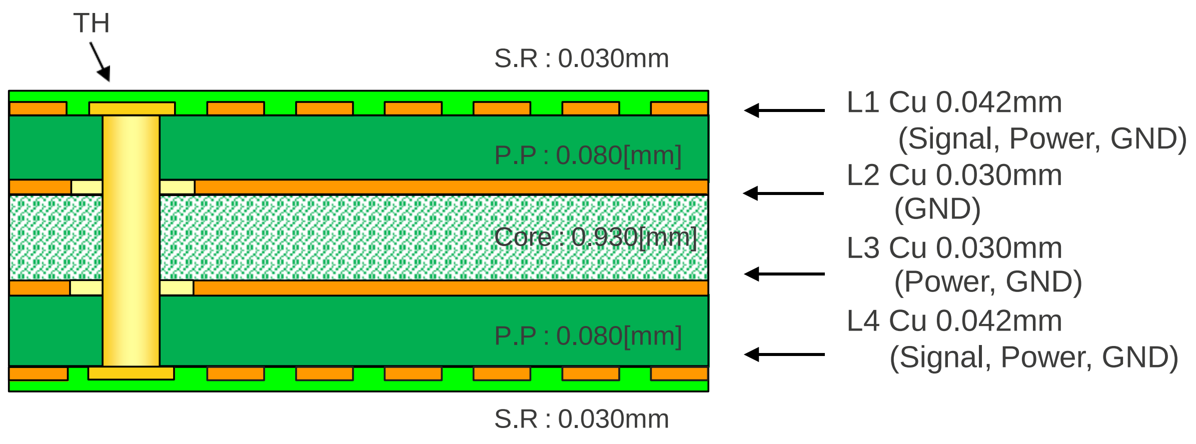
2. Basic information

2.1 PCB Structure

2.1.1 4-Layer

This guideline assumes a 4-layer board and a 6-layer board using through-hole vias.

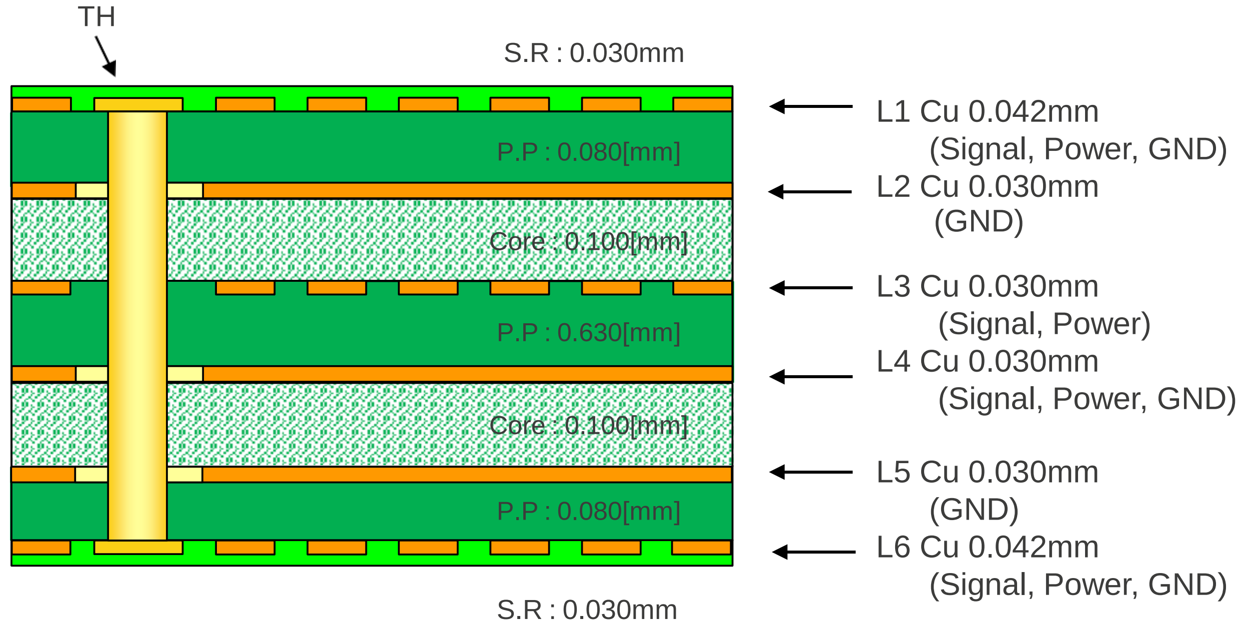
Each layer's assignment signal or power(GND) for a 4-layer board is as follows.



- 4-Layer Through-hole
  Base Material: FR-4
  [Dielectric constant: Relative permittivity / Loss tangent]
  Solder Resist (SR 0.030mm): 3.7/0.017 (for 1GHz)
  Prepreg (PP 0.080mm): 3.6/0.019 (for 1GHz)
  Core (0.930mm): 4.3/0.016 (for 1GHz)

2.1.2 6-Layer

Each layer's assignment signal or power(GND) for a 6-layer board is as follows.

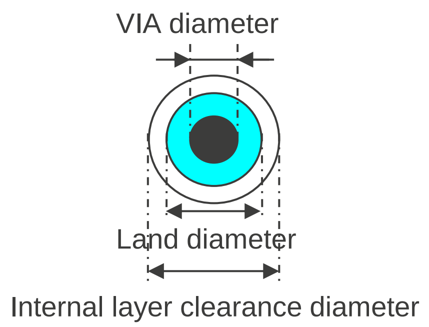


- 6-Layer Through-hole
  Base Material: FR-4
  [Dielectric constant: Relative permittivity / Loss tangent]
  Solder Resist (SR 0.030mm): 3.7/0.017 (for 1GHz)
  Prepreg (PP 0.080mm): 3.6/0.0019 (for 1GHz)
  Prepreg (PP 0.630mm): 4.2/0.017 (for 1GHz)
  Core (0.930mm): 4.3/0.016 (for 1GHz)

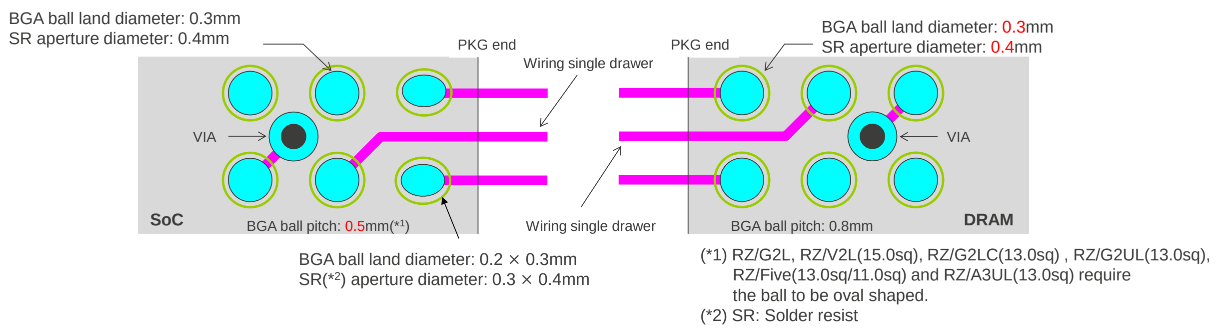
2.2 Design rules

2.2.1 Design rules for DDR4 of RZ/G2L, RZV2L(15.0sq), RZ/G2LC(13.0sq), RZ/G2UL(13.0sq), RZ/Five(13.0sq/11.0sq) and RZ/A3UL(13.0sq)

- Target device
  RZ/G2L, RZ/V2L(15.0sq), RZ/G2LC(13.0sq), RZ/G2UL(13.0sq), RZ/Five(13.0sq/11.0sq) and RZ/A3UL(13.0sq) -DDR4 SDRAM
- VIA specifications
  VIA diameter: 0.2mm
  Physical hole diameter: 0.15mm
  Surface land diameter: 0.45mm
  Internal layer land diameter: 0.45mm
  Internal layer clearance diameter: 0.55mm

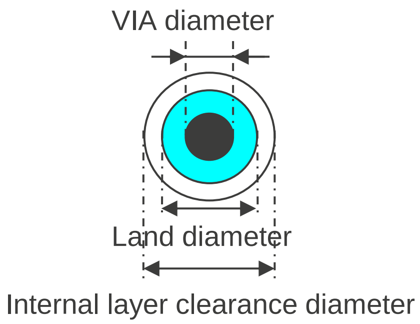


- Minimum trace width
  0.1mm
- Minimum space
  Wiring - Wiring: 0.1mm
  Wiring - VIA: 0.1mm
  Wiring - BGA land: 0.1mm
  VIA - BGA land: 0.1mm
- BGA land diameter (PAD dimension)

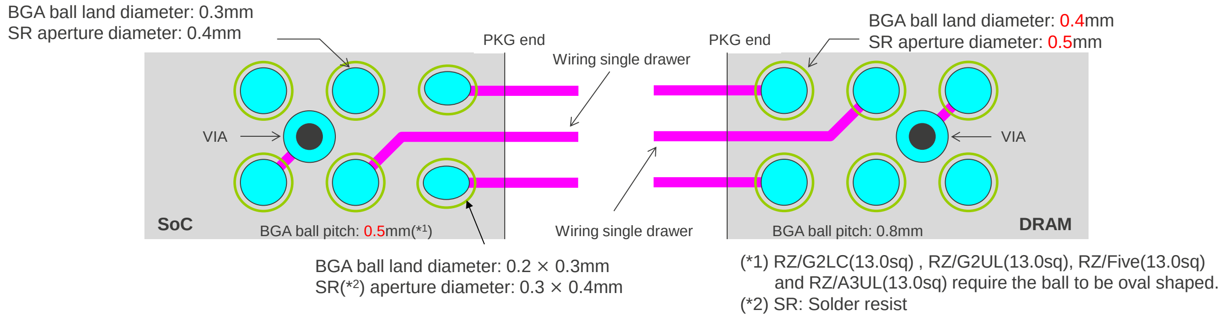


2.2.2 Design rules for DDR3L of RZ/G2LC(13.0sq), RZ/G2UL(13.0sq), RZ/Five(13.0sq) and RZ/A3UL(13.0sq)

- Target device
  RZ/G2LC(13.0sq), RZ/G2UL(13.0sq), RZ/Five(13.0sq) and RZ/A3UL(13.0sq) -DDR3L SDRAM
- VIA specifications
  VIA diameter: 0.2mm
  Physical hole diameter: 0.15mm
  Surface land diameter: 0.45mm
  Internal layer land diameter: 0.45mm
  Internal layer clearance diameter: 0.55mm



- Minimum trace width
  0.1mm
- Minimum space
  Wiring - Wiring: 0.1mm
  Wiring - VIA: 0.1mm
  Wiring - BGA land: 0.1mm
  VIA - BGA land: 0.1mm
- BGA land diameter (PAD dimension)



3. Net swap guidelines

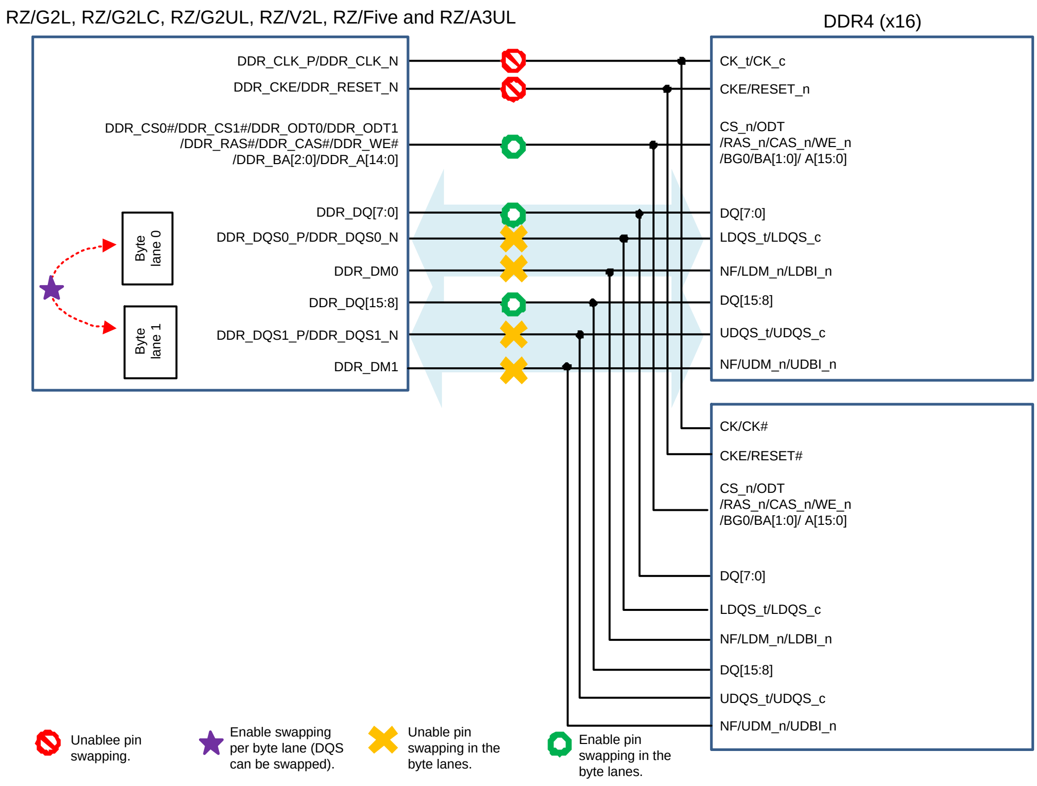
3.1 Net swap restriction for DDR4

- Address, command and control signals are swappable.
  - Address signals: DDR_A[15:0]
  - Command signals: DDR_BA[2:0], DDR_WE#, DDR_RAS#, DDR_CAS#
  - Control signals: DDR_ODT[1:0], DDR_CS[1:0]#, DDR_CKE

- During write leveling, the SoC monitors changes for all DQ signals. The designers can swap DQ signals in the same byte as needed.

- DQS/DQS#[1:0] differential pairs are swappable if the designer keeps the polarity.

- DM signals are not swappable with DQ signals.



Remarks: 1. The bus width of the RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five and RZ/A3UL is 16 bits.
2. DQ signals can only be swapped in the same byte lane. They cannot be swapped between different byte lanes.
Example: The DQ3 signal cannot be swapped with the DQ15 signal.

3.2 Net swap rules DQ for DDR4

Ball Name	RZ/G2LC 13mm PKG	RZ/G2L RZ/V2L 15mm PKG	RZ/G2L RZ/V2L 21mm PKG	RZ/G2UL 13mm PKG	RZ/Five 13mm PKG	RZ/A3UL 13mm PKG	RZ/Five 11mm PKG	DDR4	Remark
DDR_DQS0_P	√	√	√	√	√	√	√	LDQS_t	No Remap
DDR_DQS0_N	√	√	√	√	√	√	√	LDQS_c	No Remap
DDR_DQ0	√	√	√	√	√	√	√	DQ0	PHY doesn't care bit connection in Bytes group. Any connection is OK. No register setting is necessary.
DDR_DQ1	√	√	√	√	√	√	√	DQ1	
DDR_DQ2	√	√	√	√	√	√	√	DQ2	
DDR_DQ3	√	√	√	√	√	√	√	DQ3	
DDR_DQ4	√	√	√	√	√	√	√	DQ4	
DDR_DQ5	√	√	√	√	√	√	√	DQ5	
DDR_DQ6	√	√	√	√	√	√	√	DQ6	
DDR_DQ7	√	√	√	√	√	√	√	DQ7	
DDR_DM0	√	√	√	√	√	√	√	NF/LDM_n/LDBI_n	No Remap
DDR_DQS1_P	√	√	√	√	√	√	√	UDQS_t	No Remap
DDR_DQS1_N	√	√	√	√	√	√	√	UDQS_c	No Remap
DDR_DQ8	√	√	√	√	√	√	√	DQ8	PHY doesn't care bit connection in Bytes group. Any connection is OK. No register setting is necessary.
DDR_DQ9	√	√	√	√	√	√	√	DQ9	
DDR_DQ10	√	√	√	√	√	√	√	DQ10	
DDR_DQ11	√	√	√	√	√	√	√	DQ11	
DDR_DQ12	√	√	√	√	√	√	√	DQ12	
DDR_DQ13	√	√	√	√	√	√	√	DQ13	
DDR_DQ14	√	√	√	√	√	√	√	DQ14	
DDR_DQ15	√	√	√	√	√	√	√	DQ15	
DDR_DM1	√	√	√	√	√	√	√	NF/UDM_n/UDBI_n	No Remap

Note: Bytes group are swappable.

3.3 Net swap rules CA for DDR4

Ball Name	RZ/G2LC 13mm PKG	RZ/G2L RZ/V2L 15mm PKG	RZ/G2L RZ/V2L 21mm PKG	RZ/G2UL 13mm PKG	RZ/Five 13mm PKG	RZ/A3UL 13mm PKG	RZ/Five 11mm PKG	DDR4	Remark
DDR_CLK_P	√	√	√	√	√	√	√	CK_t	No Remap
DDR_CLK_N	√	√	√	√	√	√	√	CK_c	No Remap
DDR_CKE	√	√	√	√	√	√	√	CKE	No Remap
DDR_RESET#	√	√	√	√	√	√	√	RESET_n	No Remap
DDR_ADDR0	√	√	√	√	√	√	√	A0	Any bit assignment is OK by register setting.
DDR_ADDR1	√	√	√	√	√	√	√	A1	
DDR_ADDR2	√	√	√	√	√	√	√	A2	
DDR_ADDR3	√	√	√	√	√	√	√	A3	
DDR_ADDR4	√	√	√	√	√	√	√	A4	
DDR_ADDR5	√	√	√	√	√	√	√	A5	
DDR_ADDR6	√	√	√	√	√	√	√	A6	
DDR_ADDR7	√	√	√	√	√	√	√	A7	
DDR_ADDR8	√	√	√	√	√	√	√	A8	
DDR_ADDR9	√	√	√	√	√	√	√	A9	
DDR_ADDR10	√	√	√	√	√	√	√	A10/AP	
DDR_ADDR11	√	√	√	√	√	√	√	A11	
DDR_ADDR12	√	√	√	√	√	√	√	A12/BC_n	
DDR_ADDR13	√	√	√	√	√	√	√	A13	
DDR_ADDR14	√	√	√	√	√	√	√	ACT_n	
DDR_ADDR15	√	√	√	√	√	√	√	BG1*1	
DDR_BA0	√	√	√	√	√	√	√	BA0	
DDR_BA1	√	√	√	√	√	√	√	BA1	
DDR_BA2	√	√	√	√	√	√	√	BG0	
DDR_WE#	√	√	√	√	√	√	√	WE_n/A14	
DDR_RAS#	√	√	√	√	√	√	√	RAS_n/A16	
DDR_CAS#	√	√	√	√	√	√	√	CAS_n/A15	
DDR_CS0#	√	√	√	√	√	√	√	CS_n (each ranks)	
DDR_CS1#	√	√	√	√	√	√	√		
DDR_ODT0	√	√	√	√	√	√	√	ODT (each ranks)	
DDR_ODT1	√	√	√	√	√	√	√		
DDR_CALIBRATION	√	√	√	√	√	√	√	—	Pull-down to GND via 240Ω

Note 1. BG1 is not used for ×16

3.4 Net swap restriction for DDR3L

- Address, command and control signals are swappable.
  - Address signals: DDR_A[15:0]
  - Command signals: DDR_BA[2:0], DDR_WE#, DDR_RAS#, DDR_CAS#
  - Control signals: DDR_ODT[1:0], DDR_CS[1:0]#, DDR_CKE

- During write leveling, the SoC monitors changes for all DQ signals. The designers can swap DQ signals in the same byte as needed.

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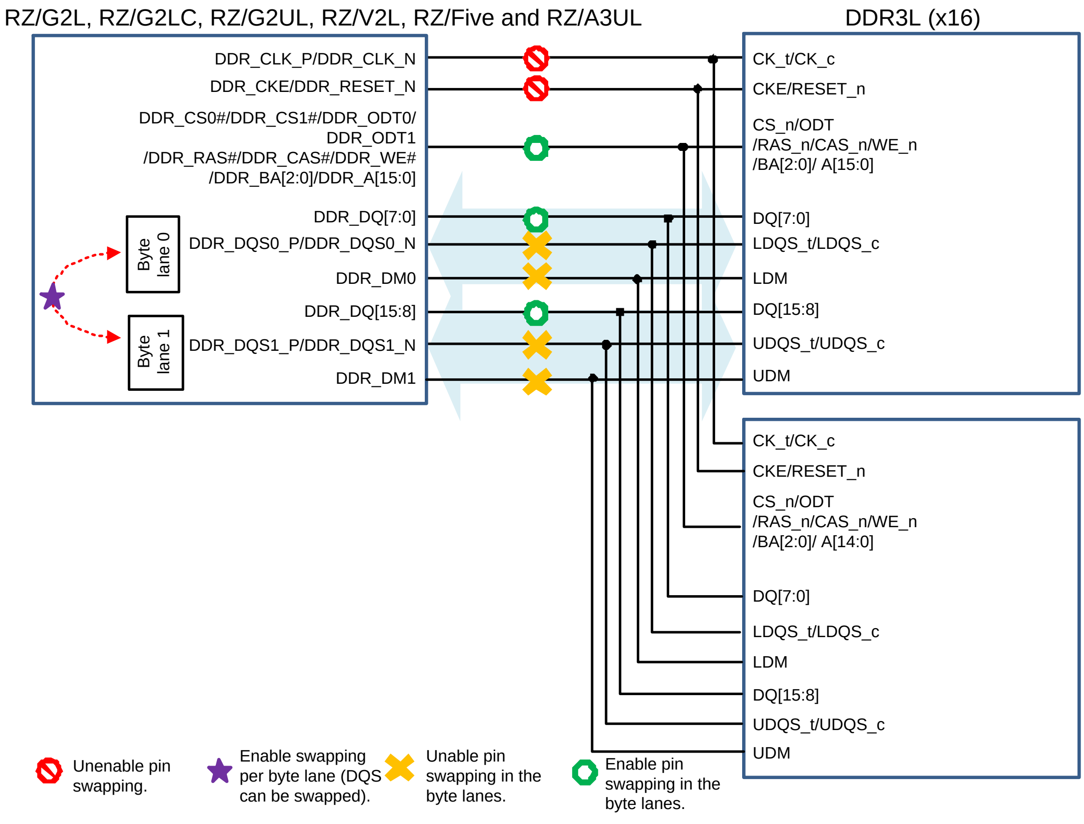


Remarks: 1. The bus width of the RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five and RZ/A3UL is 16 bits.
2. DQ signals can only be swapped in the same byte lane. They cannot be swapped between different byte lanes.
Example: The DQ3 signal cannot be swapped with the DQ15 signal.

3.5 Net swap rules DQ for DDR3L

Ball Name	RZ/G2LC 13mm PKG	RZ/G2UL 13mm PKG	RZ/Five 13mm PKG	RZ/A3UL 13mm PKG	DDR3L	Remark
DDR_DQS0_P	√	√	√	√	LDQS	No Remap
DDR_DQS0_N	√	√	√	√	LDQS#	No Remap
DDR_DQ0	√	√	√	√	DQ0	PHY doesn't care bit connection in Bytes group. Any connection is OK. No register setting is necessary.
DDR_DQ1	√	√	√	√	DQ1	
DDR_DQ2	√	√	√	√	DQ2	
DDR_DQ3	√	√	√	√	DQ3	
DDR_DQ4	√	√	√	√	DQ4	
DDR_DQ5	√	√	√	√	DQ5	
DDR_DQ6	√	√	√	√	DQ6	
DDR_DQ7	√	√	√	√	DQ7	
DDR_DM0	√	√	√	√	LDM	No Remap
DDR_DQS1_P	√	√	√	√	UDQS	No Remap
DDR_DQS1_N	√	√	√	√	UDQS#	No Remap
DDR_DQ8	√	√	√	√	DQ8	PHY doesn't care bit connection in Bytes group. Any connection is OK. No register setting is necessary.
DDR_DQ9	√	√	√	√	DQ9	
DDR_DQ10	√	√	√	√	DQ10	
DDR_DQ11	√	√	√	√	DQ11	
DDR_DQ12	√	√	√	√	DQ12	
DDR_DQ13	√	√	√	√	DQ13	
DDR_DQ14	√	√	√	√	DQ14	
DDR_DQ15	√	√	√	√	DQ15	
DDR_DM1	√	√	√	√	UDM	No Remap

Note: Bytes group are swappable.

3.6 Net swap rules CA for DDR3L

Ball Name	RZ/G2LC 13mm PKG	RZ/G2UL 13mm PKG	RZ/Five 13mm PKG	RZ/A3UL 13mm PKG	DDR3L	Remark
DDR_CLK_P	√	√	√	√	CK	No Remap
DDR_CLK_N	√	√	√	√	CK#	No Remap
DDR_CKE	√	√	√	√	CKE	No Remap
DDR_RESET#	√	√	√	√	RESET#	No Remap
DDR_ADDR0	√	√	√	√	A0	Any bit assignment is OK by register setting.
DDR_ADDR1	√	√	√	√	A1	
DDR_ADDR2	√	√	√	√	A2	
DDR_ADDR3	√	√	√	√	A3	
DDR_ADDR4	√	√	√	√	A4	
DDR_ADDR5	√	√	√	√	A5	
DDR_ADDR6	√	√	√	√	A6	
DDR_ADDR7	√	√	√	√	A7	
DDR_ADDR8	√	√	√	√	A8	
DDR_ADDR9	√	√	√	√	A9	
DDR_ADDR10	√	√	√	√	A10/AP	
DDR_ADDR11	√	√	√	√	A11	
DDR_ADDR12	√	√	√	√	A12/BC#	
DDR_ADDR13	√	√	√	√	A13	
DDR_ADDR14	√	√	√	√	A14	
DDR_ADDR15	√	√	√	√	A15	
DDR_BA0	√	√	√	√	BA0	
DDR_BA1	√	√	√	√	BA1	
DDR_BA2	√	√	√	√	BA2	
DDR_WE#	√	√	√	√	WE#	
DDR_RAS#	√	√	√	√	RAS#	
DDR_CAS#	√	√	√	√	CAS#	
DDR_CS0#	√	√	√	√	CS# (each ranks)	
DDR_CS1#	√	√	√	√		
DDR_ODT0	√	√	√	√	ODT (each ranks)	
DDR_ODT1	√	√	√	√		
DDR_ CALIBRATION	√	√	√	√	—	Pull-down to GND via 240Ω

3.7 Net swap setting

Please refer to **Section 1, Overview** or **Section 5, Topology of signal trace** onwards regarding the detail of each topology.

Ball Name	T-1bc	T-1c	T-3bc	T-1b	T-2c	T-3cl	T-3bcud2	T-3bcud	T-3bcul	T-11bv
DDR_CLK_P	DDR_CLK_P	DDR_CLK_P	DDR_CLK_P	DDR_CLK_P	DDR_CLK_P	DDR_CLK_P	DDR_CLK_P	DDR_CLK_P	DDR_CLK_P	DDR_CLK_P
DDR_CLK_N	DDR_CLK_N	DDR_CLK_N	DDR_CLK_N	DDR_CLK_N	DDR_CLK_N	DDR_CLK_N	DDR_CLK_N	DDR_CLK_N	DDR_CLK_N	DDR_CLK_N
DDR_CKE	DDR_CKE	DDR_CKE	DDR_CKE	DDR_CKE	DDR_CKE	DDR_CKE	DDR_CKE	DDR_CKE	DDR_CKE	DDR_CKE
DDR_RESET#	DDR_RESET#	DDR_RESET#	DDR_RESET#	DDR_RESET#	DDR_RESET#	DDR_RESET#	DDR_RESET#	DDR_RESET#	DDR_RESET#	DDR_RESET#
DDR_WE#	—	DDR_ADDR5	DDR_ADDR10	—	DDR_ADDR5	DDR_ADDR11	DDR_ADDR12	DDR_ADDR6	DDR_ADDR3	DDR_ACT_N
DDR_CAS#	DDR_ADDR1	DDR_BA0	DDR_ADDR7	DDR_ADDR1	DDR_ADDR12	DDR_ADDR1	DDR_ADDR7	DDR_ADDR5	DDR_ADDR8	DDR_ODT0
DDR_RAS#	DDR_ADDR10	DDR_ADDR15	DDR_ADDR12	DDR_ADDR10	DDR_ADDR0	DDR_ADDR3	—	DDR_ADDR11	DDR_ADDR15	DDR_BG1
DDR_CS0#	—	DDR_CS1_N	DDR_CS0_N	—	DDR_CS1_N	DDR_CS0_N	DDR_CS0_N	DDR_CS0_N	DDR_CS0#	DDR_ADDR12
DDR_CS1#	DDR_CAS_N	DDR_ADDR3	—	DDR_CAS_N	DDR_RAS_N	DDR_RAS_N	—	DDR_CS1_N	DDR_CS1#	DDR_ADDR7
DDR_BA0	DDR_ADDR3	DDR_CAS_N	DDR_ADDR6	DDR_ADDR3	DDR_WE_N	DDR_ADDR5	DDR_ADDR4	DDR_ACT_N	DDR_ADDR2	DDR_ADDR10
DDR_BA1	DDR_ADDR13	DDR_ADDR1	DDR_RAS_N	DDR_ADDR13	DDR_BA1	DDR_ADDR0	DDR_RAS_N	DDR_RAS_N	DDR_BA1	DDR_BA1
DDR_BA2	DDR_ADDR0	DDR_ADDR7	DDR_ADDR0	DDR_ADDR0	DDR_ADDR6	DDR_BA2	DDR_ADDR11	DDR_BA0	DDR_ADDR14	DDR_ADDR3
DDR_ADDR0	DDR_ADDR2	DDR_ADDR6	DDR_ADDR11	DDR_ADDR2	DDR_ADDR10	DDR_ADDR14	DDR_BA0	DDR_BG0	DDR_ADDR7	DDR_BA0
DDR_ADDR1	DDR_ADDR7	DDR_ADDR14	DDR_CAS_N	DDR_ADDR7	DDR_ADDR4	DDR_BA1	DDR_CAS_N	DDR_CAS_N	DDR_ADDR12	DDR_ADDR13
DDR_ADDR2	DDR_ADDR11	DDR_ADDR13	DDR_BG0	DDR_ADDR11	DDR_ADDR2	DDR_ADDR6	DDR_ADDR2	DDR_ADDR13	DDR_ADDR13	DDR_ADDR11
DDR_ADDR3	DDR_ADDR8	DDR_ADDR2	DDR_ADDR14	DDR_ADDR8	DDR_ADDR7	DDR_ADDR9	DDR_ADDR8	DDR_WE_N	DDR_WE#	DDR_ADDR0
DDR_ADDR4	DDR_ADDR9	DDR_BA1	DDR_ADDR9	DDR_ADDR9	DDR_ADDR1	DDR_CAS_N	DDR_WE_N	DDR_BA1	DDR_ADDR0	DDR_ADDR5
DDR_ADDR5	DDR_ADDR14	DDR_ADDR10	DDR_WE_N	DDR_ADDR14	DDR_ADDR13	DDR_ADDR13	DDR_ADDR6	DDR_ADDR2	DDR_CAS#	DDR_ADDR8
DDR_ADDR6	DDR_ADDR5	DDR_ADDR4	DDR_ADDR13	DDR_ADDR5	DDR_BA0	DDR_BA0	DDR_ADDR9	DDR_ADDR12	DDR_ADDR6	DDR_ADDR9
DDR_ADDR7	DDR_WE_N	DDR_ADDR8	DDR_ADDR2	DDR_WE_N	DDR_ADDR8	DDR_ADDR7	DDR_ADDR13	DDR_ADDR9	DDR_ADDR5	DDR_WE#
DDR_ADDR8	DDR_ADDR4	DDR_ADDR9	DDR_ADDR4	DDR_ADDR4	DDR_ADDR9	DDR_ADDR2	DDR_ADDR10	DDR_ADDR0	DDR_ADDR9	DDR_ADDR4
DDR_ADDR9	DDR_BG0	DDR_BG0	DDR_ADDR8	DDR_BG0	DDR_BG0	DDR_ADDR8	DDR_BG0	DDR_ADDR8	DDR_RAS#	DDR_BG0
DDR_ADDR10	DDR_RAS_N	DDR_CS0_N	DDR_ADDR3	DDR_RAS_N	DDR_ADDR3	DDR_CS1_N	DDR_ADDR3	DDR_ADDR7	DDR_ADDR10	DDR_RAS#
DDR_ADDR11	DDR_ADDR12	DDR_ADDR12	DDR_ADDR5	DDR_ADDR12	DDR_ADDR14	DDR_ADDR4	DDR_ADDR1	DDR_ADDR4	DDR_ADDR1	DDR_ADDR1

Ball Name	T-1bc	T-1c	T-3bc	T-1b	T-2c	T-3cl	T-3bcud2	T-3bcud	T-3bcul	T-11bv
DDR_ADDR12	DDR_ODT0	DDR_ODT0	DDR_BA1	DDR_ODT0	DDR_ODT0	DDR_ODT1	DDR_BA1	DDR_ADDR3	DDR_BA2	DDR_CS1#
DDR_ADDR13	DDR_ADDR6	DDR_ADDR11	DDR_BA0	DDR_ADDR6	DDR_ADDR11	DDR_ADDR10	DDR_ACT_N	DDR_ADDR1	DDR_ADDR11	DDR_ADDR6
DDR_ADDR14	DDR_BA0	DDR_ADDR0	DDR_ADDR1	DDR_BA0	DDR_CAS_N	DDR_WE_N	DDR_ADDR5	DDR_ADDR10	DDR_ADDR4	DDR_ODT1
DDR_ADDR15	DDR_BA1	DDR_WE_N	—	DDR_BA1	—	DDR_ADDR15	DDR_ADDR0	DDR_BG1	DDR_BA0	DDR_ADDR2
DDR_DM0	DDR_DM0	DDR_DM0	DDR_DM0	DDR_DM0	DDR_DM0	DDR_DM0	DDR_DM0	DDR_DM0	DDR_DM0	DDR_DM0
DDR_DM1	DDR_DM1	DDR_DM1	DDR_DM1	DDR_DM1	DDR_DM1	DDR_DM1	DDR_DM1	DDR_DM1	DDR_DM1	DDR_DM1
DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P
DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N
DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P
DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N
DDR_DQ0	DDR_DQ5	DDR_DQ4	DDR_DQ4	DDR_DQ5	DDR_DQ4	DDR_DQ4	DDR_DQ5	DDR_DQ5	DDR_DQ7	DDR_DQ3
DDR_DQ1	DDR_DQ0	DDR_DQ1	DDR_DQ0	DDR_DQ0	DDR_DQ5	DDR_DQ7	DDR_DQ0	DDR_DQ2	DDR_DQ0	DDR_DQ0
DDR_DQ2	DDR_DQ7	DDR_DQ0	DDR_DQ3	DDR_DQ7	DDR_DQ2	DDR_DQ2	DDR_DQ3	DDR_DQ3	DDR_DQ6	DDR_DQ6
DDR_DQ3	DDR_DQ4	DDR_DQ3	DDR_DQ1	DDR_DQ4	DDR_DQ7	DDR_DQ3	DDR_DQ1	DDR_DQ1	DDR_DQ1	DDR_DQ2
DDR_DQ4	DDR_DQ2	DDR_DQ7	DDR_DQ5	DDR_DQ2	DDR_DQ0	DDR_DQ0	DDR_DQ6	DDR_DQ6	DDR_DQ2	DDR_DQ5
DDR_DQ5	DDR_DQ1	DDR_DQ5	DDR_DQ2	DDR_DQ1	DDR_DQ1	DDR_DQ5	DDR_DQ4	DDR_DQ4	DDR_DQ3	DDR_DQ0
DDR_DQ6	DDR_DQ3	DDR_DQ6	DDR_DQ7	DDR_DQ3	DDR_DQ6	DDR_DQ6	DDR_DQ7	DDR_DQ7	DDR_DQ5	DDR_DQ7
DDR_DQ7	DDR_DQ6	DDR_DQ2	DDR_DQ6	DDR_DQ6	DDR_DQ3	DDR_DQ1	DDR_DQ2	DDR_DQ0	DDR_DQ4	DDR_DQ4
DDR_DQ8	DDR_DQ9	DDR_DQ11	DDR_DQ12	DDR_DQ9	DDR_DQ14	DDR_DQ14	DDR_DQ14	DDR_DQ14	DDR_DQ15	DDR_DQ10
DDR_DQ9	DDR_DQ14	DDR_DQ12	DDR_DQ13	DDR_DQ14	DDR_DQ8	DDR_DQ15	DDR_DQ13	DDR_DQ13	DDR_DQ14	DDR_DQ14
DDR_DQ10	DDR_DQ15	DDR_DQ8	DDR_DQ15	DDR_DQ15	DDR_DQ12	DDR_DQ9	DDR_DQ15	DDR_DQ9	DDR_DQ10	DDR_DQ9
DDR_DQ11	DDR_DQ12	DDR_DQ10	DDR_DQ11	DDR_DQ12	DDR_DQ15	DDR_DQ12	DDR_DQ9	DDR_DQ15	DDR_DQ9	DDR_DQ13
DDR_DQ12	DDR_DQ8	DDR_DQ15	DDR_DQ8	DDR_DQ8	DDR_DQ9	DDR_DQ8	DDR_DQ8	DDR_DQ12	DDR_DQ11	DDR_DQ12
DDR_DQ13	DDR_DQ13	DDR_DQ14	DDR_DQ9	DDR_DQ13	DDR_DQ10	DDR_DQ11	DDR_DQ11	DDR_DQ10	DDR_DQ12	DDR_DQ15
DDR_DQ14	DDR_DQ11	DDR_DQ9	DDR_DQ14	DDR_DQ11	DDR_DQ11	DDR_DQ13	DDR_DQ12	DDR_DQ11	DDR_DQ8	DDR_DQ11
DDR_DQ15	DDR_DQ10	DDR_DQ13	DDR_DQ10	DDR_DQ10	DDR_DQ13	DDR_DQ10	DDR_DQ10	DDR_DQ8	DDR_DQ13	DDR_DQ8
DDR_ODT0	—	DDR_ODT1	DDR_ODT0	—	DDR_ODT1	DDR_ODT0	DDR_ODT0	DDR_ODT0	DDR_ODT0	DDR_CS0#

Ball Name	T-1bc	T-1c	T-3bc	T-1b	T-2c	T-3cl	T-3bcud2	T-3bcud	T-3bcul	T-11bv
DDR_ODT1	DDR_CS0_N	DDR_RAS_N	—	DDR_CS0_N	DDR_CS0_N	DDR_ADDR12	—	DDR_ODT1	DDR_ODT1	DDR_CAS#

4. Common guidelines

4.1 Component placement

Component placement assumptions: U1 indicates SoC, M1 and M2 indicates DRAM.

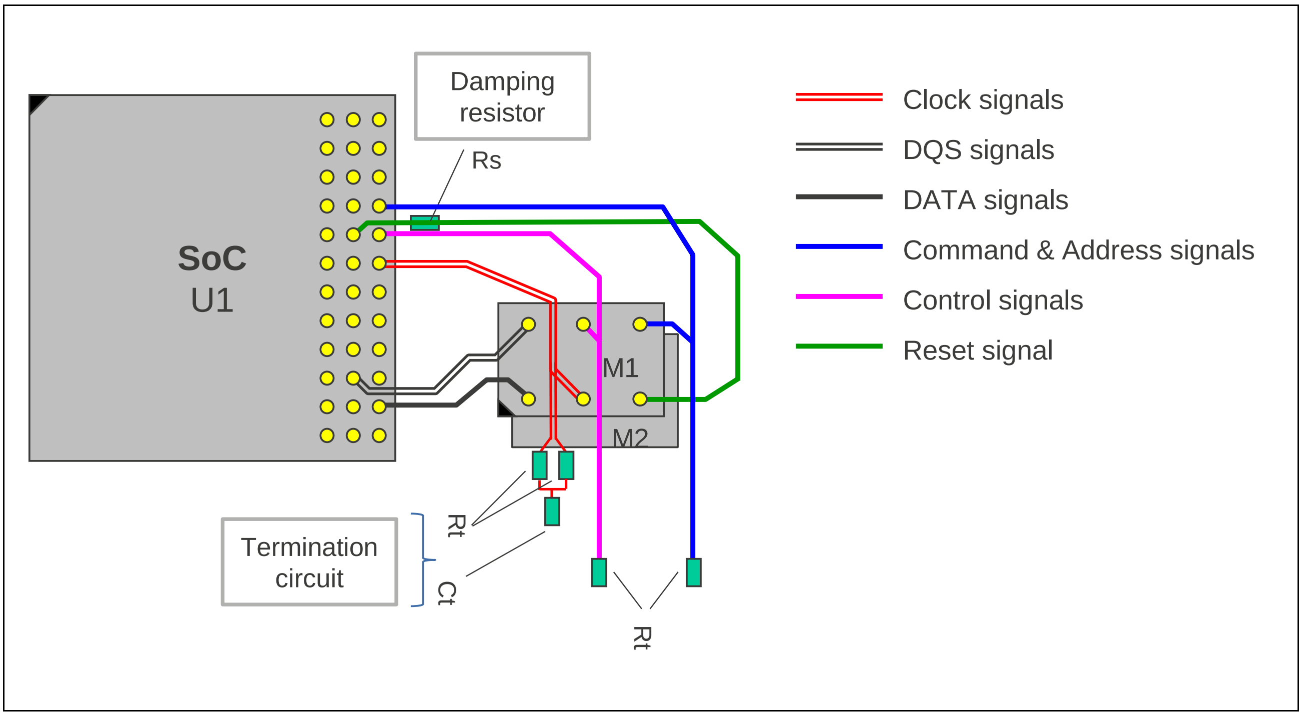
- 1RANK case: Place U1 and M1 on L1.
- 2RANKs case:Place U1 and M1 on L1. M2 should be placed at L6 so that it is a clamshell with M1.

(1) Place the clock termination resistor (Rt) and termination capacitance (Ct) on L6 near UM1.

(2) Place the termination resistor (Rt) of control signals on L1 near UM1.

(3) Place the termination resistor (Rt) for command address signals on L1 or L6 near UM1.

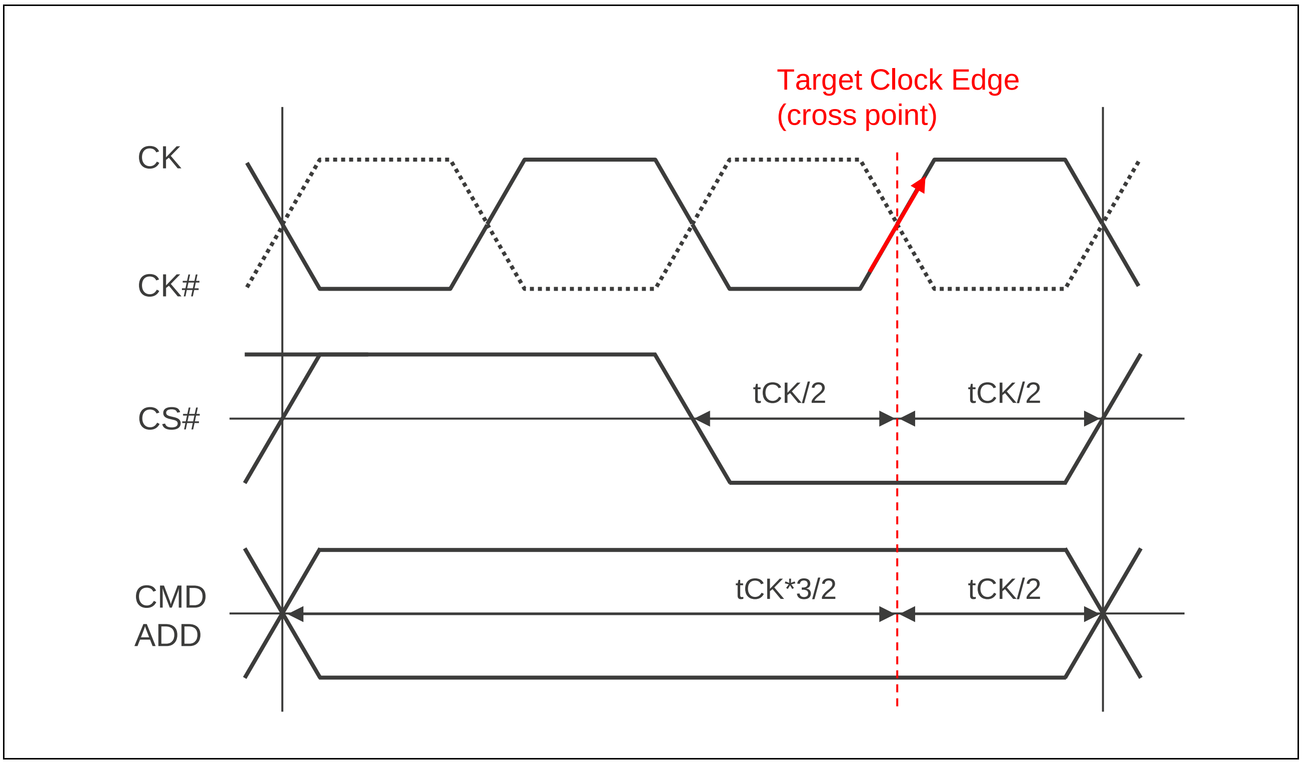
(4) Place the reset damping resistor (Rs) near UM1 on the same side as UM1.



4.2 ADD/CMD Layout Guideline

The figure below shows timing relation between the "Command & Address" and the "Clock".
Set the signal to be output according to the timing relationship below.

Command & Address signals are DDR_A[15:0], DDR_BA[2:0], DDR_BG0, DDR_ACT_N, DDR_CAS_N, DDR_RAS_N, DDR_WE_N
Control signals (DDR_CKE0, DDR_CS[1:0]_N, DDR_ODT[1:0]) and reset signal (DDR_RESET_N) are not applicable.

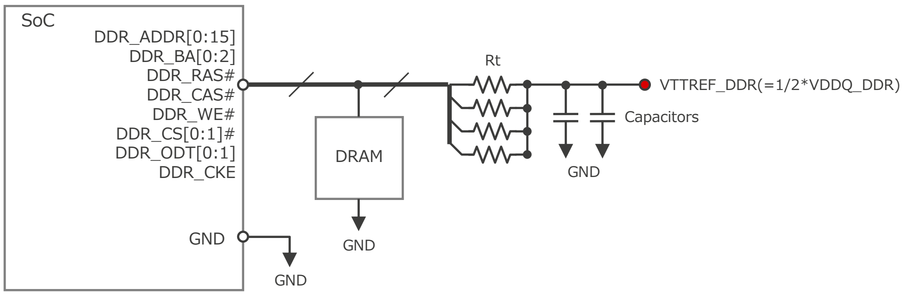


4.3 VTT termination resistor Layout Guideline

We recommend the use of VTT termination resistors to absorb through-hole VIAs and DRAM package reflection.

VTT power supply voltage is 1/2*VDDQ_DDR. Place two 0.1uF capacitors per four VTT termination resistors.

The distance between the termination resistors and the capacitor should be within 3mm.



Capacitors selections

T-1bc, T-3bc, T-1b, T-3bcud2, T-3bcud, T-3bcul	Value	Pics.
VTTREF_DDR - GND	0.1uF	13
	10uF	1

T-1c	Value	Pics.
VTTREF_DDR - GND	0.1uF	10
	10uF	1

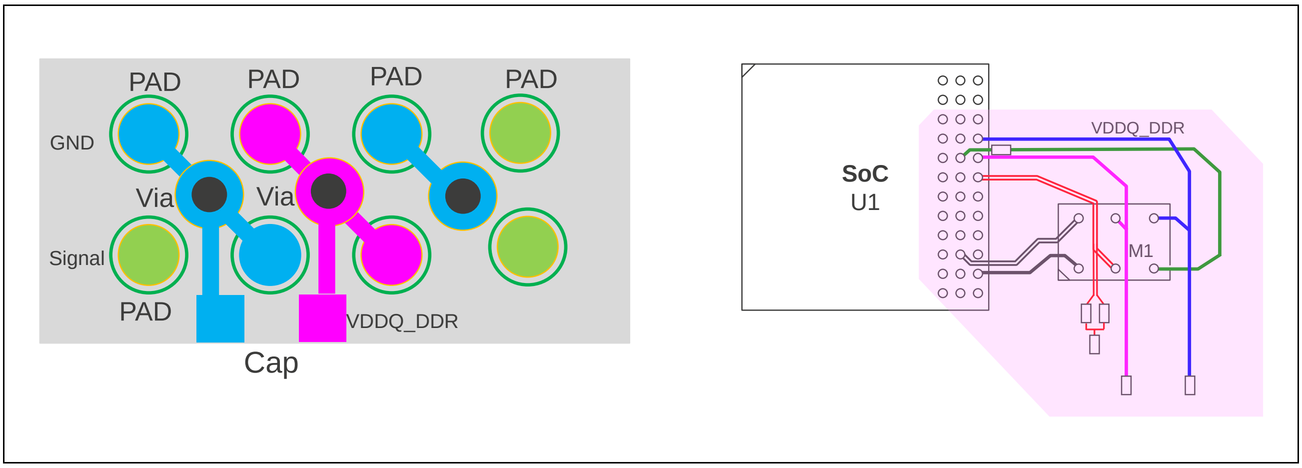
T-2c	Value	Pics.
VTTREF_DDR - GND	0.1uF	13
	10uF	2

T-3cl	Value	Pics.
VTTREF_DDR - GND	0.1uF	14
	10uF	2

T-11bv	Value	Pics.
VTTREF_DDR - GND	0.1uF	13
	10uF	3

4.4 IO Power Supply Layout Guideline

The IO power supply (VDDQ_DDR) should be formed on L4 as a plane and should be large enough to cover all signals traces and DRAM. Place one VIA for every two PADs of the IO power supply near the SoC and place a capacitor per number of VIAs. Use GND PADs near the VDDQ_DDR to place VIAs for GND using to the same rule. To shorten the current return path for the IO power supply, consider placing capacitors with the shortest trace possible to the IO power supply and GND. Verify the layout using PDN analysis and check if the results satisfy the specification described in [REF].



5. Topology of signal trace

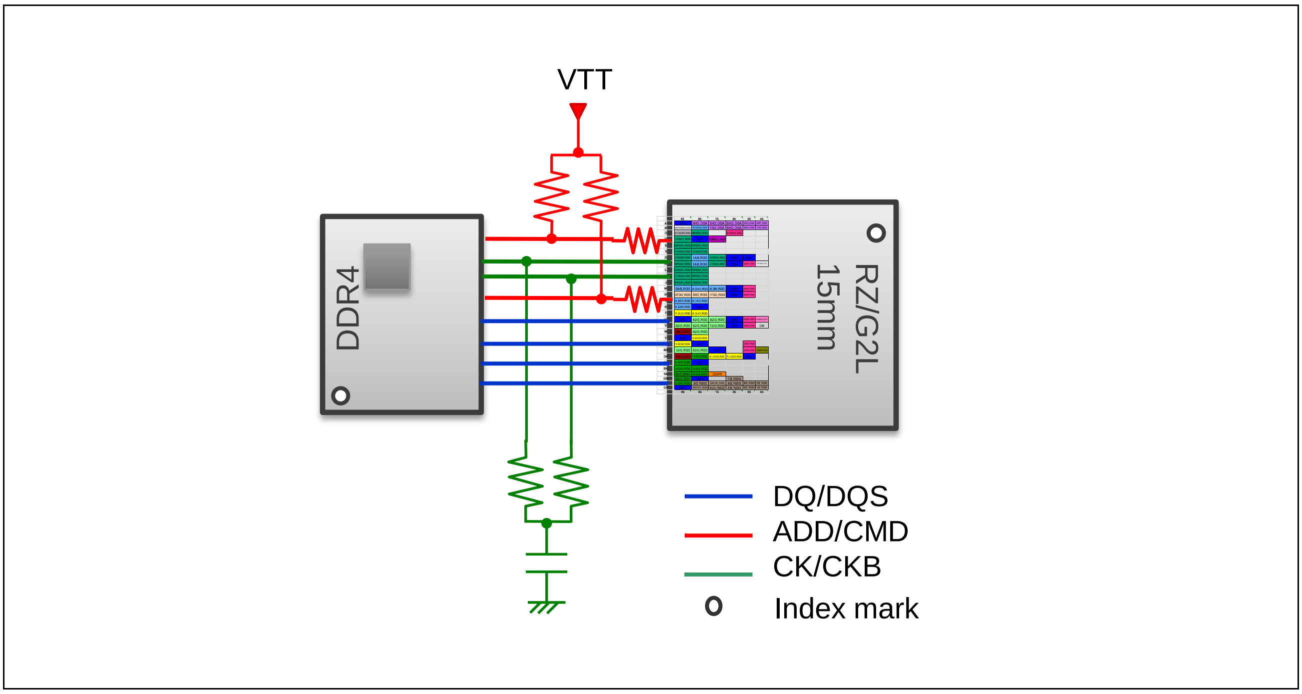
5.1 Topology T-1bc

System RANK: Single

16Gb: ×16 Single-Rank DDR4 SDRAM

Target Device: MT40A1G16KD-062E

PCB: 6layers / One to One / Top mounting



Signal	IO drive strength	VTT termination resistance	Termination resistance / Capacitance	Damping resistor	ODT termination resistance		
					SoC	DRAM Access side	DRAM Non-Access side
CLK	60Ω	—	56Ω × 2 / 0.1uF	—	—	—	—
CA (CMD, ADD)	60Ω	82Ω*1	—	22Ω	—	—	—
CTRL (CS, ODT, CKE)	60Ω	82Ω*1	—	—	—	—	—
RESET	60Ω	—	—	22Ω	—	—	—
DQ, DQS (Write)	40Ω	—	—	—	OFF	60Ω	60Ω
DQ, DQS (Read)	34Ω	—	—	—	40Ω	OFF	OFF

Note 1. Design a VTT termination resistance with 100Ω or more in the customer's system.
The PVB verification guide is based on the JEDEC standard (Vddq: 1.14(Vmin), ±5% accuracy), so it is recommend a VTT termination resistance of 100Ω or more for DDR design in customer's system. Our board is designed for DDR within the guaranteed range of the PMIC (Vddq: 1.188V(Vmin), ±1% accuracy), so a VTT termination resistance of 82Ω is acceptable.

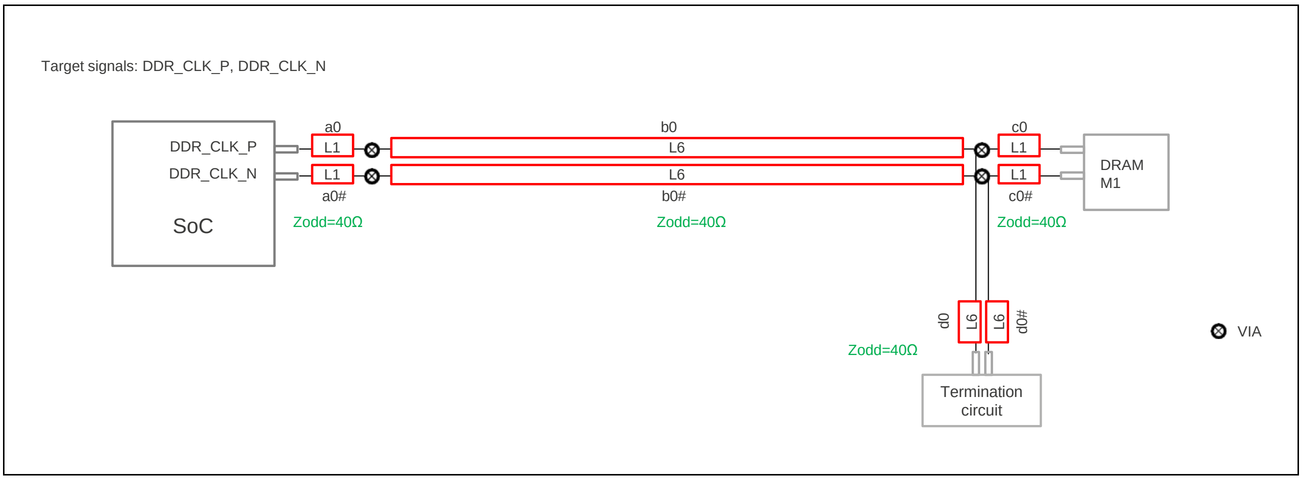
5.1.1 CLK topology

L1 and L6 in the figure below indicate the trace layers. a0 to d0# indicate the trace length. “ ⊗ ” are VIAs.

The odd mode impedance (Zodd) is equal to Zdiff/2. The clock traces Zodd should be 40Ω±10%.

Design the clock following the topology described in this figure.

1. CLK pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#
2. Keep 0.1mm or more between each signal traces.
3. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



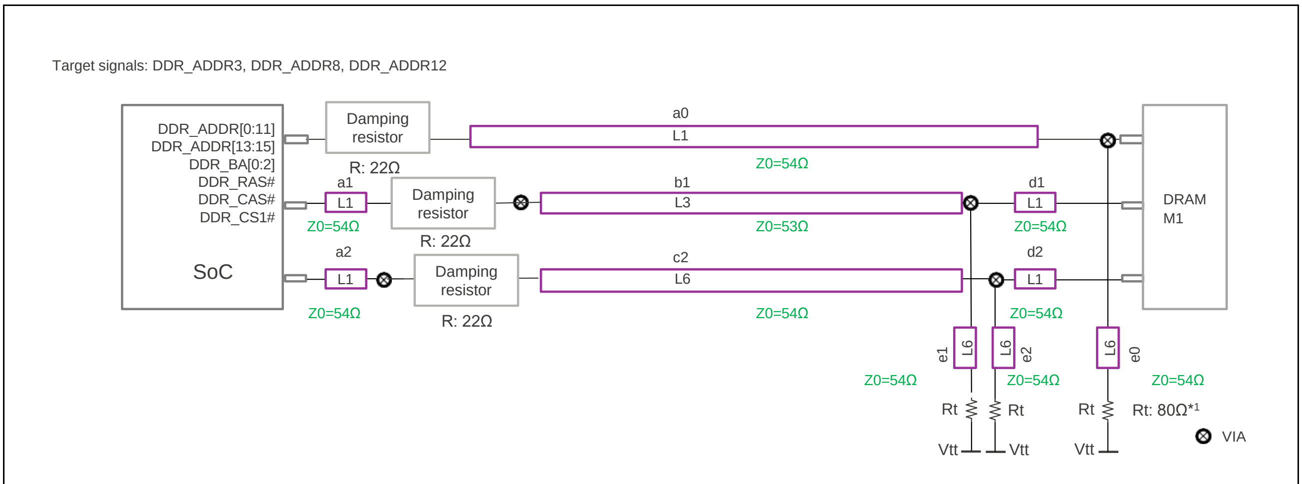
5.1.2 ADD/CMD topology

L1, L3 and L6 in the figure below indicate the trace layers. a0 to e2 indicate the wiring length. “ ⊗ ” are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 55Ω±10%.

Design address and command signals following the topology described in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



Note 1. Design a VTT termination resistance with 100Ω or more in the customer's system.

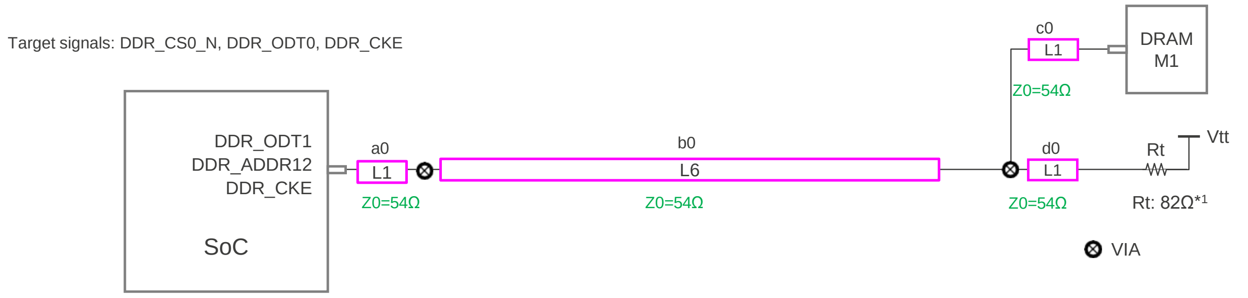
5.1.3 CTRL CS/ODT/CKE topology

L1 and L6 in the figure below indicate the trace layers. a0 to d0 indicate the trace length. “ ⊗ ” are VIAs.

Control signals are singled-ended, and their impedance (Z0) should be 55Ω±10%.

Design control signals following the topology described in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



Note 1. Design a VTT termination resistance with 100Ω or more in the customer's system.

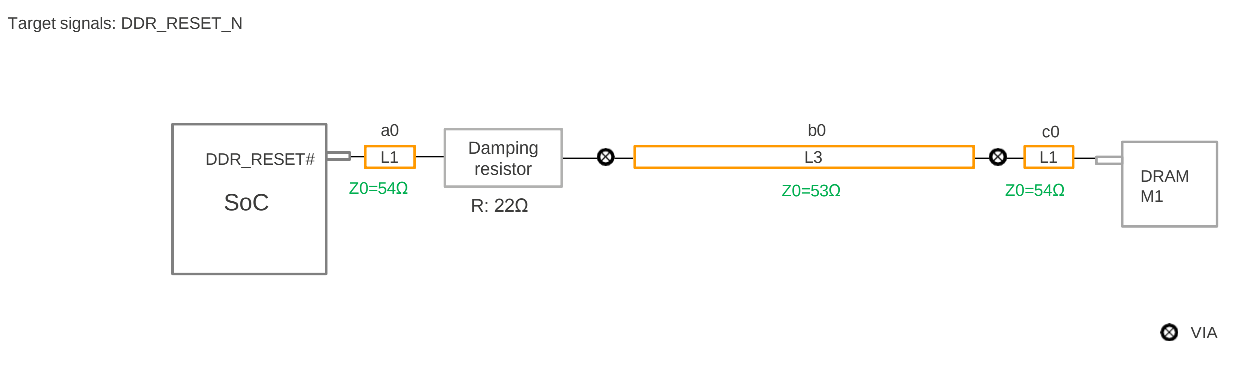
5.1.4 RESET topology

L1 and L3 in the figure below indicate trace layers. a0 to c0 indicate the trace length. “ ⊗ ” are VIAs.

The reset signal is single-ended, and his impedances (Z0) should be 55Ω±10%.

Design the wiring so that the wiring topology is as shown in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from waveform restrictions specifications. (Mandatory)



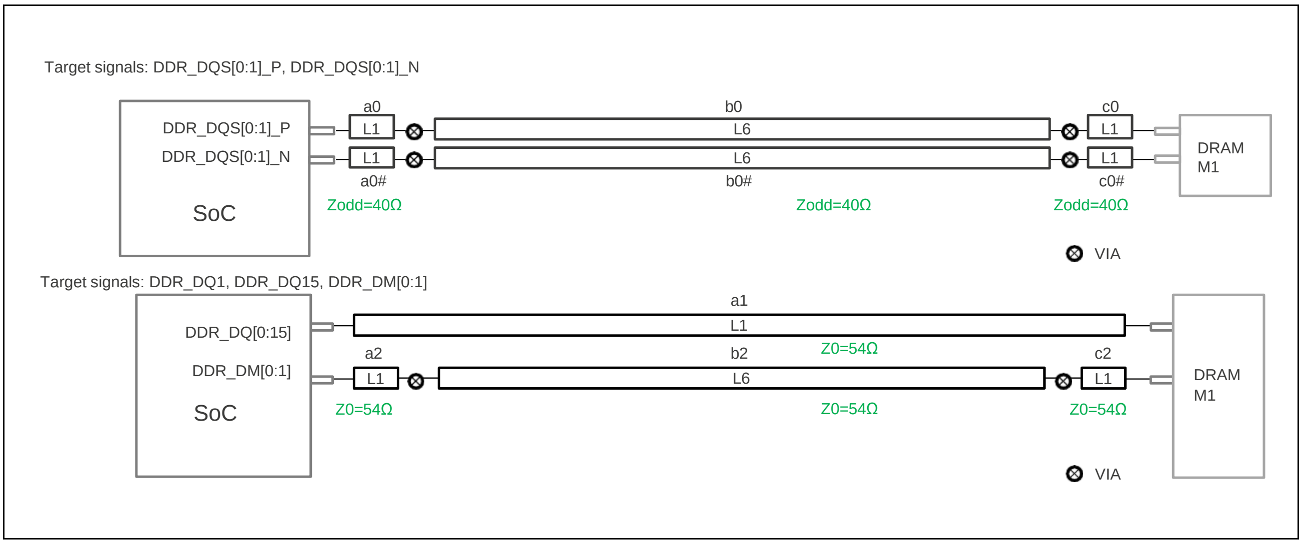
5.1.5 DQS/DQ topology

L1 and L6 int the figure below indicate the trace layers. a0 to c2 indicate the trace length. " ⊗ " are VIAs.

Zodd for DQS and DQS# traces should be 40Ω±10%. Z0 for DQ and DM should be 55Ω±10%.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#
2. Keep 0.1mm or more between each signal traces.
3. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



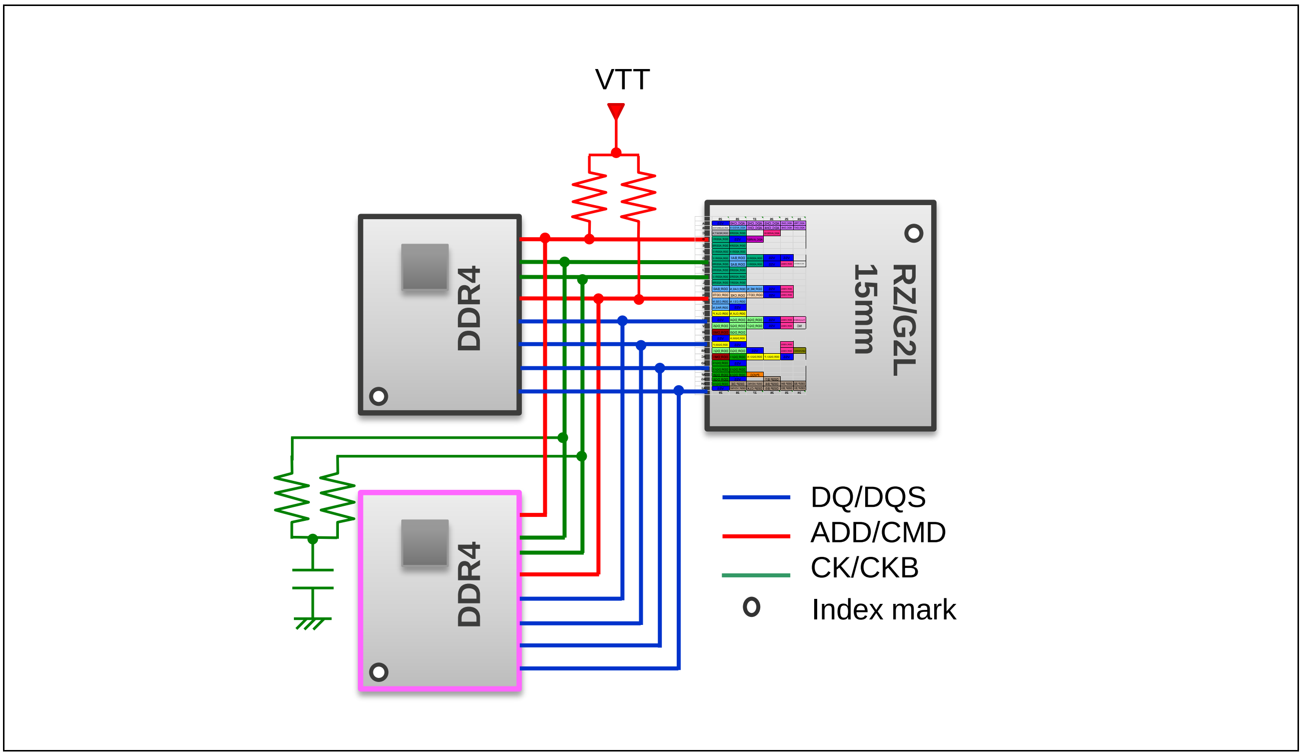
5.2 Topology T-1c

System RANK: Dual

32Gb: 16Gb(×16 Single Die Single-Rank DDR4 SDRAM) × 2

Target Device: MT40A1G16RC-062E

PCB: 6layers / One to Two / Clamshell mounting



Signal	IO drive strength	VTT termination resistance	Termination resistance / Capacitance	Damping resistor	ODT termination resistance		
					SoC	DRAM Access side	DRAM Non-Access side
CLK	60Ω	—	56Ω × 2 / 0.1uF	—	—	—	—
CA (CMD, ADD)	60Ω	47Ω	—	—	—	—	—
CTRL (CS, ODT)	60Ω	47Ω	—	—	—	—	—
CKE	60Ω	47Ω	—	—	—	—	—
RESET	60Ω	—	—	47Ω	—	—	—
DQ, DQS (Write)	34Ω	—	—	—	OFF	120Ω	34Ω
DQ, DQS (Read)	34Ω	—	—	—	60Ω	OFF	34Ω

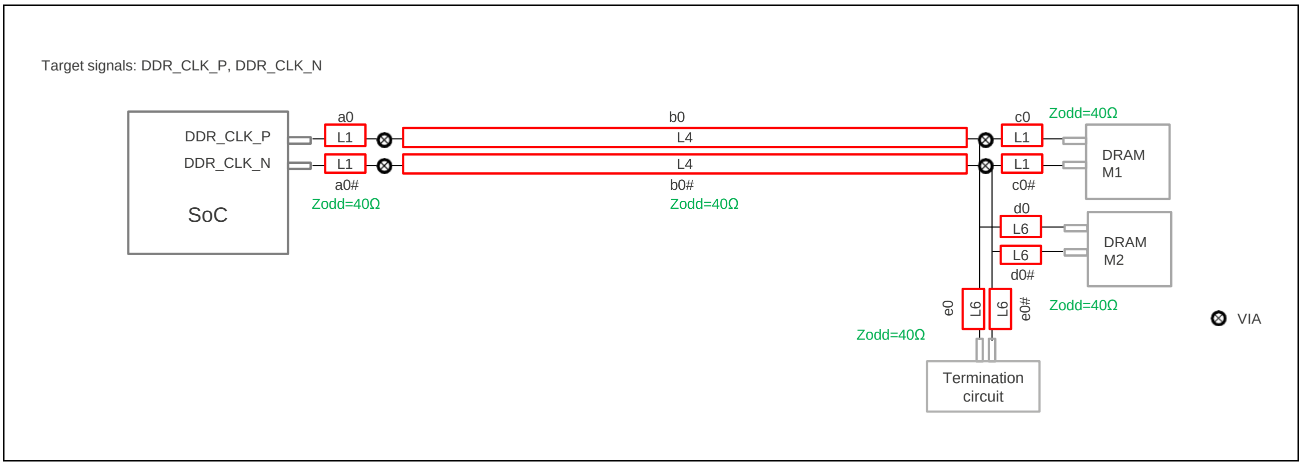
5.2.1 CLK topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to e0# indicate the trace length. " ⊗ " are VIAs.

The odd mode impedance (Zodd) is equal to Zdiff/2. The clock traces Zodd should be 40Ω±10%.

Design the clock following the topology described in this figure.

1. CLK pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#, e0=e0#
2. Keep 0.1mm or more between each signal traces.
3. Top and bottom branches to memory should be of equal length.
4. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



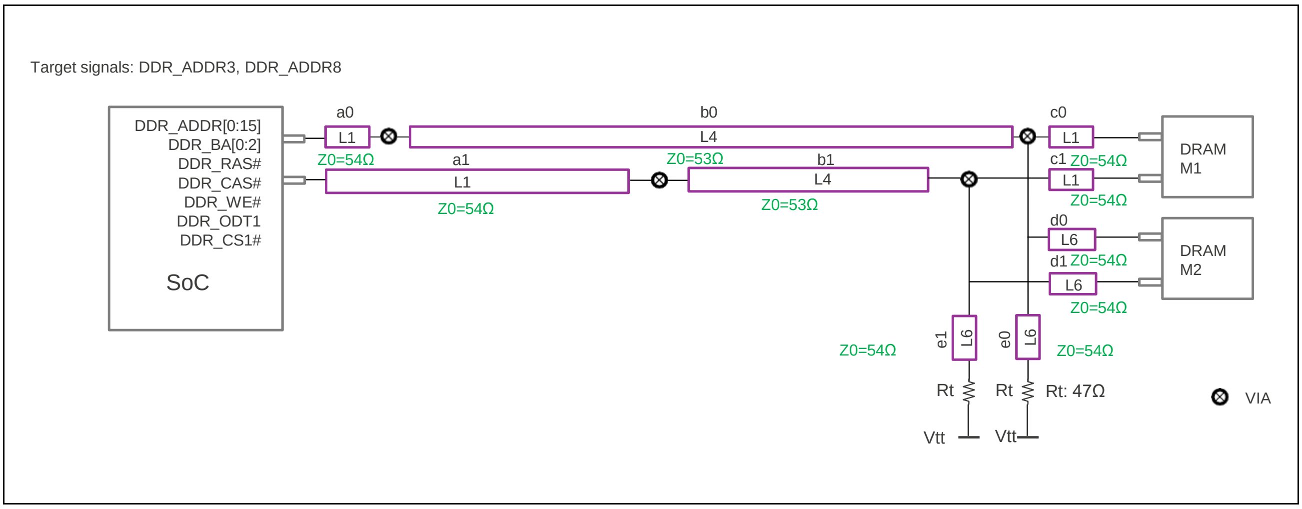
5.2.2 ADD/CMD topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to e1 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 55Ω±10%.

Design address and command signals following the topology described in this figure.

1. Top and bottom branches to memory should be of equal length.
2. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



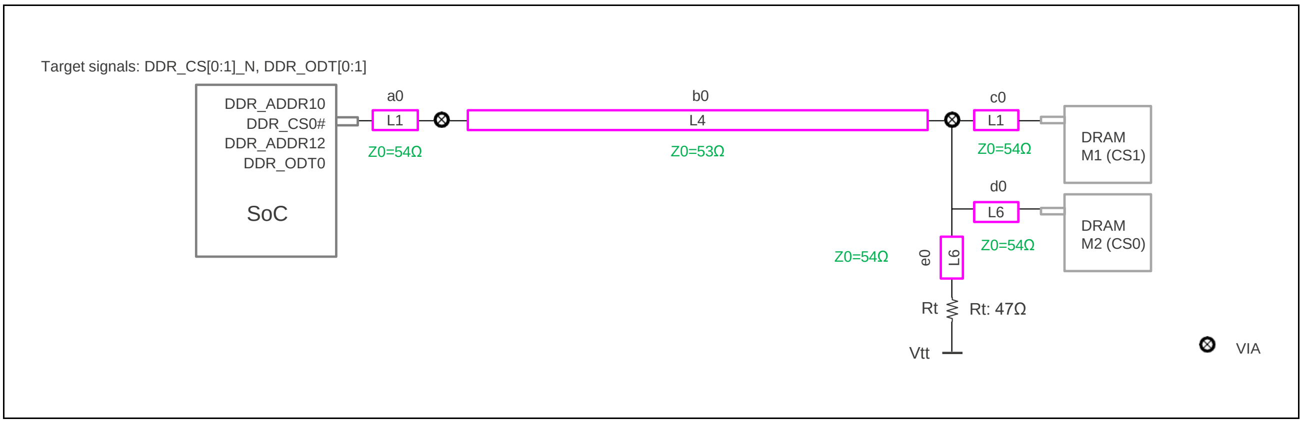
5.2.3 CTRL CS/ODT topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to e0 indicate the trace length. " ⊗ " are VIAs.

Control signals are singled-ended, and their impedance (Z0) should be 55Ω±10%.

Design control signals following the topology described in this figure.

1. Top and bottom branches to memory should be of equal length.
2. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



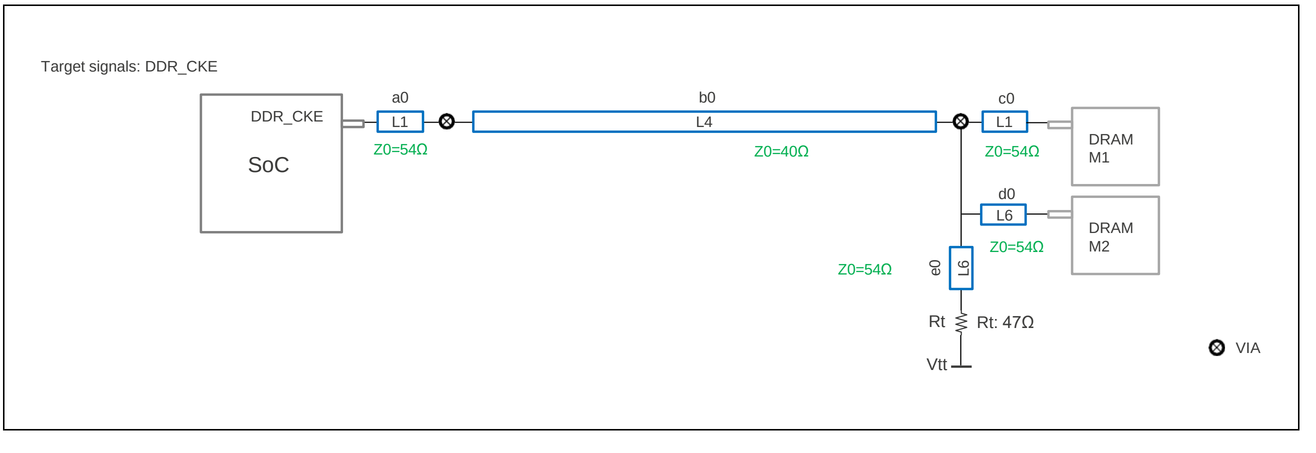
5.2.4 CTRL CKE topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to e0 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 55Ω±10%.

Design address and command signals following the topology described in this figure.

1. Top and bottom branches to memory should be of equal length.
2. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



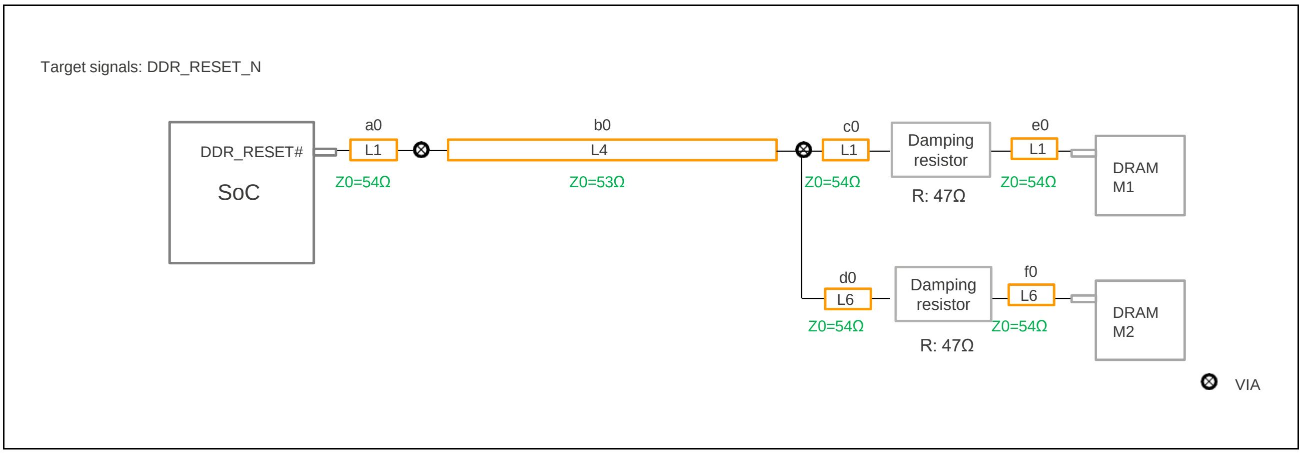
5.2.5 RESET topology

L1, L4 and L6 in the figure below indicate trace layers. a0 to f0 indicate the trace length. " ⊗ " are VIAs.

The reset signal is single-ended, and his impedances (Z0) should be 55Ω±10%.

Design the wiring so that the wiring topology is as shown in this figure.

1. Top and bottom branches to memory should be of equal length.
2. Verify the layout using SI simulation. Check simulation results using [REF] from waveform restrictions specifications. (Mandatory)



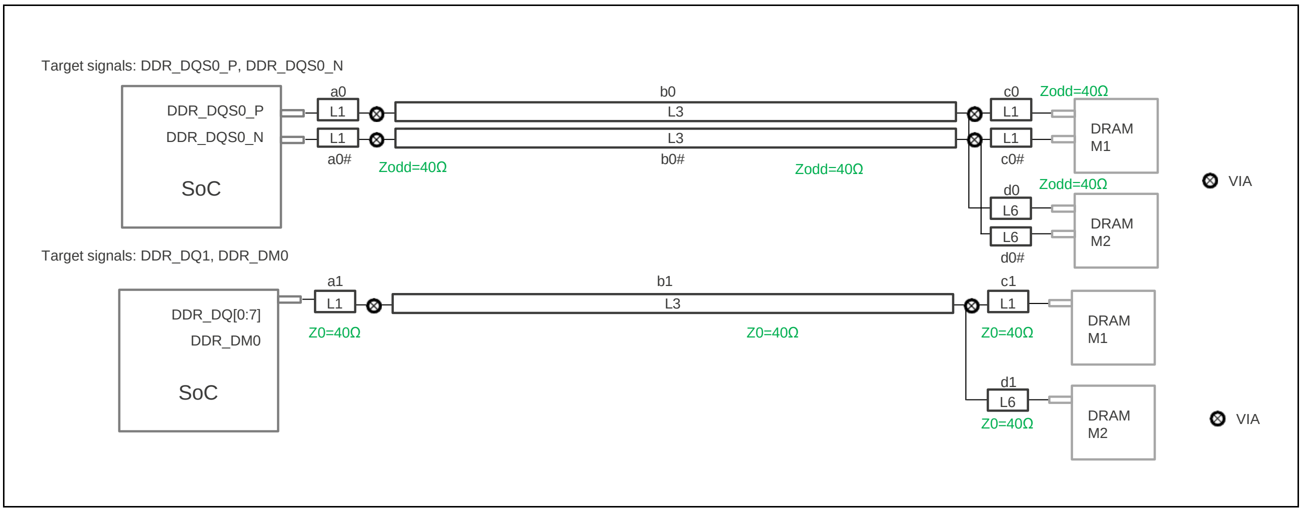
5.2.6 DQS0/DQ_L topology

L1, L3 and L6 in the figure below indicate the trace layers. a0 to d1 indicate the trace length. " ⊗ " are VIAs.

Zodd for DQS and DQS# traces should be 40Ω±10%. Z0 for DQ and DM should be 55Ω±10%.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#
2. Keep 0.1mm or more between each signal traces.
3. Top and bottom branches to memory should be of equal length.
4. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



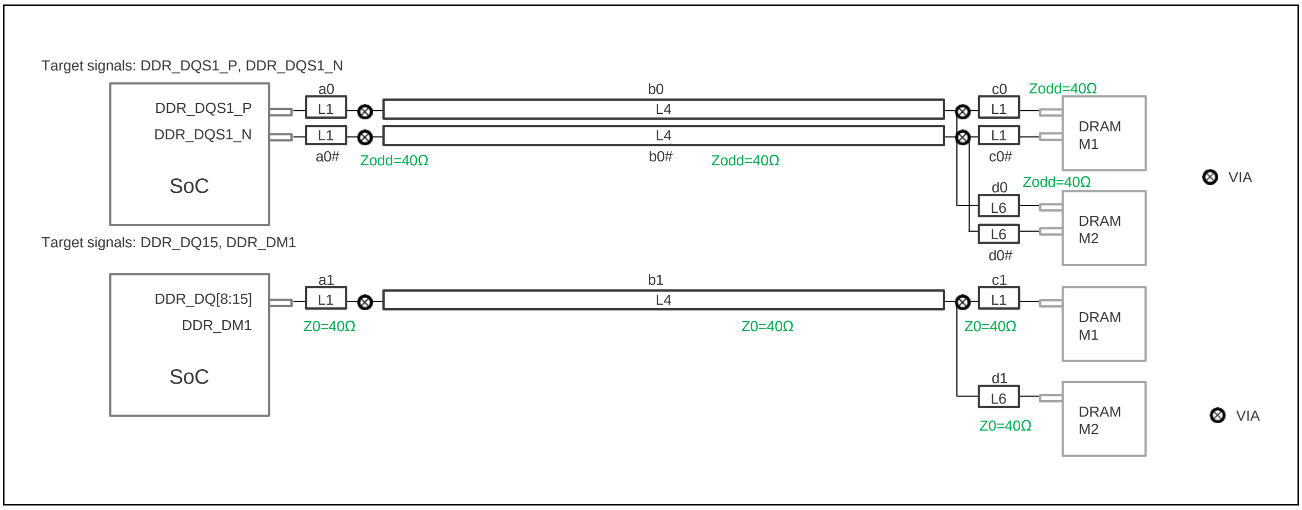
5.2.7 DQS1/DQ_H topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to d1 indicate the trace length. " ⊗ " are VIAs.

Zodd for DQS and DQS# traces should be 40Ω±10%. Z0 for DQ and DM should be 40Ω±10%.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#
2. Keep 0.1mm or more between each signal traces.
3. Top and bottom branches to memory should be of equal length.
4. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



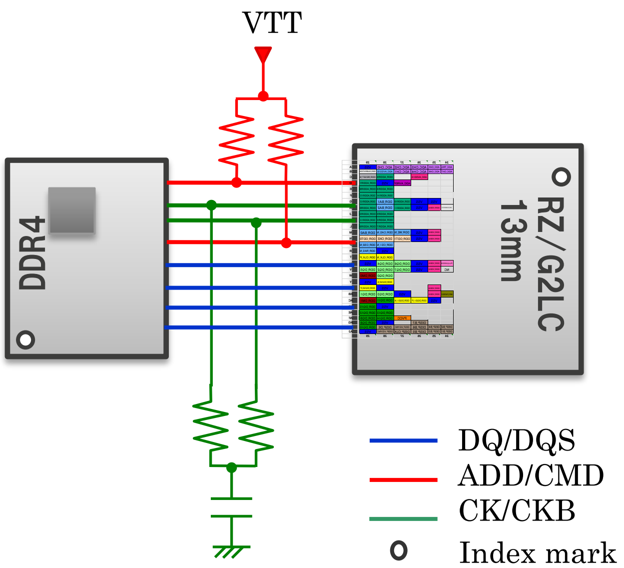
5.3 Topology T-3bc

System RANK: Single

16Gb: ×16 Single-Rank DDR4 SDRAM

Target Device: MT40A1G16KD-062E

PCB: 6layers / One to One / Top mounting



Signal	IO drive strength	VTT termination resistance	Termination resistance / Capacitance	Damping resistor	ODT termination resistance		
					SoC	DRAM Access side	DRAM Non-Access side
CLK	60Ω	—	56Ω × 2 / 0.1uF	—	—	—	—
CA (CMD, ADD)	60Ω	82Ω	—	—	—	—	—
CTRL (CS, ODT, CKE)	60Ω	82Ω	—	—	—	—	—
RESET	60Ω	—	—	33Ω	—	—	—
DQ, DQS (Write)	40Ω	—	—	—	OFF	60Ω	60Ω
DQ, DQS (Read)	34Ω	—	—	—	40Ω	OFF	OFF

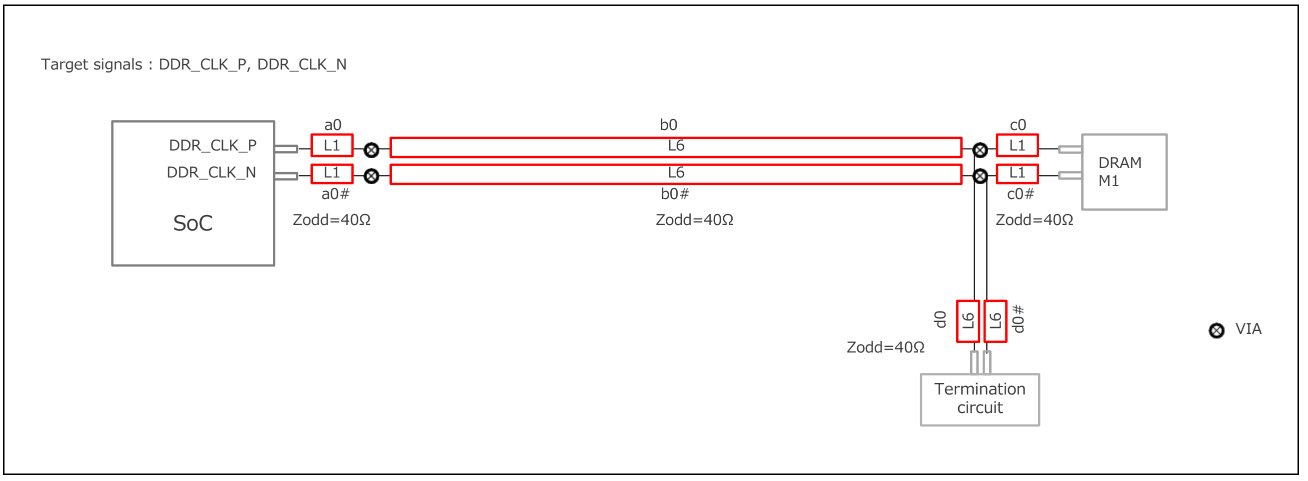
5.3.1 CLK topology

L1 and L6 in the figure below indicate the trace layers. a0 to d0# indicate the trace length. " ⊗ " are VIAs.

The odd mode impedance (Zodd) is equal to Zdiff/2. The clock traces should be 80Ω.

Design the clock following the topology described in this figure.

1. CLK pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#
2. Keep 0.1mm or more between each signal traces.
3. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



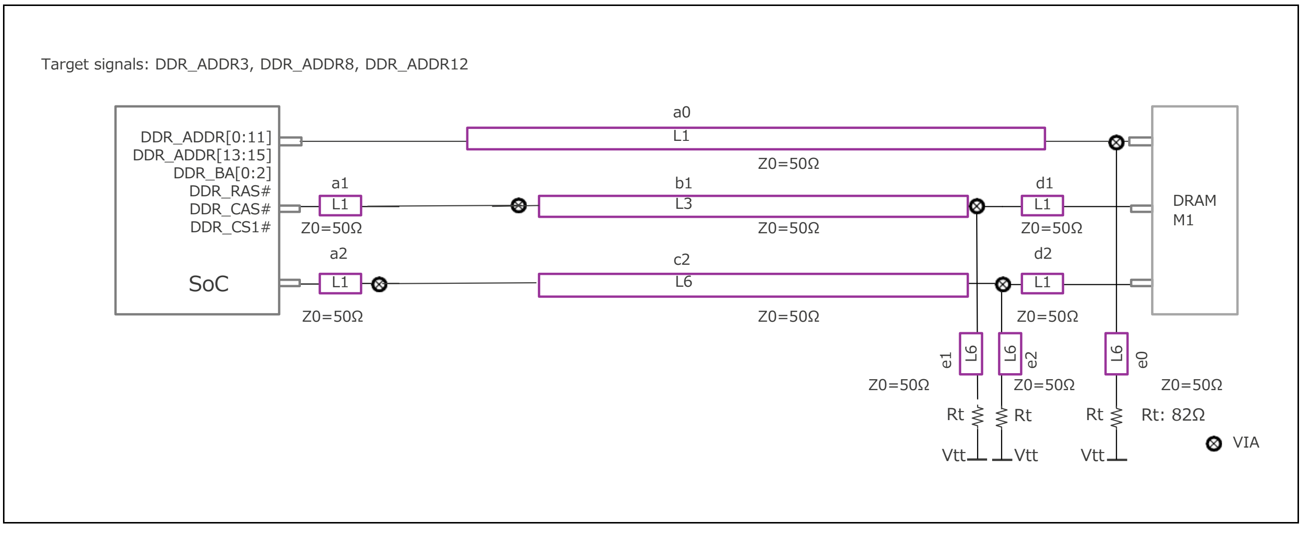
5.3.2 ADD/CMD topology

L1, L3 and L6 in the figure below indicate the trace layers. a0 to e2 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be undetermined.

Design address and command signals following the topology described in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



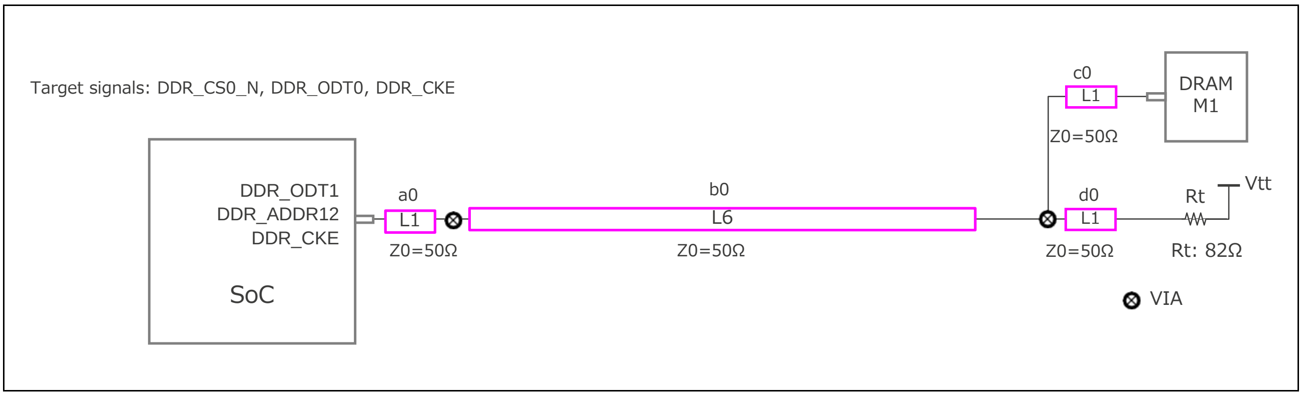
5.3.3 CTRL CS/ODT/CKE topology

L1 and L6 in the figure below indicate the trace layers. a0 to d0 indicate the trace length. “ ⊗ ” are VIAs.

Control signals are singled-ended, and their impedance (Z0) is undetermined.

Design control signals following the topology described in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



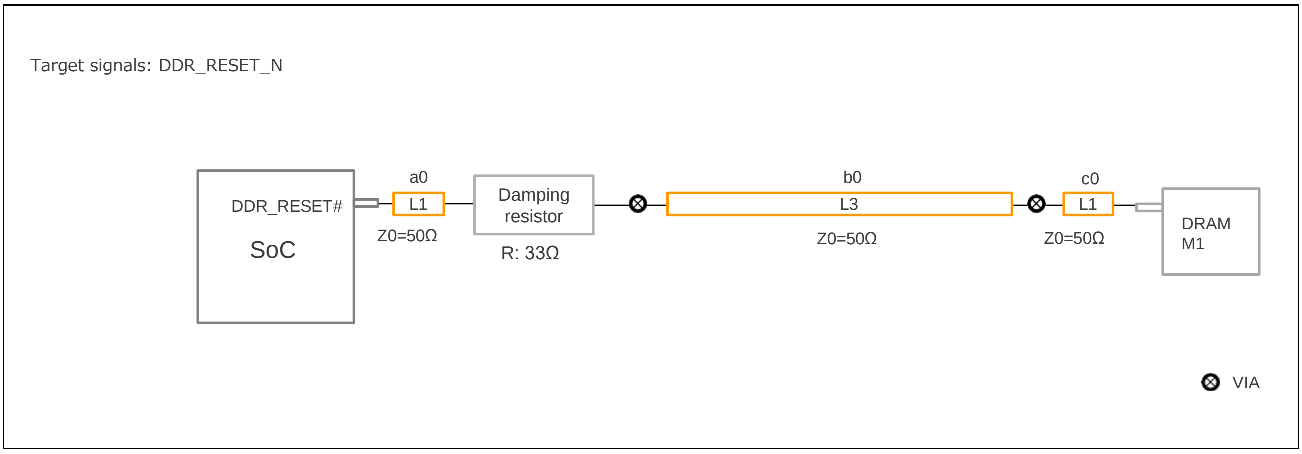
5.3.4 RESET topology

L1 and L3 in the figure below indicate trace layers. a0 to c0 indicate the trace length. “ ⊗ ” are VIAs.

The reset signal is single-ended, and his impedances (Z0) is undetermined.

Design the wiring so that the wiring topology is as shown in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from waveform restrictions specifications. (Mandatory)



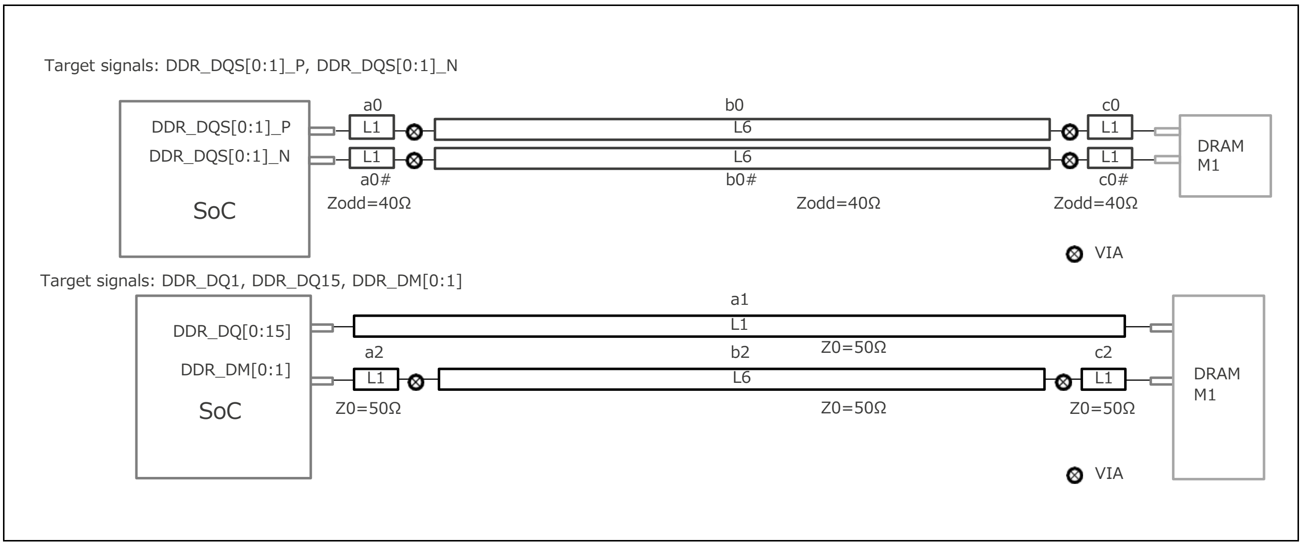
5.3.5 DQS/DQ topology

L1 and L6 int the figure below indicate the trace layers. a0 to c2 indicate the trace length. “ ⊗ ” are VIAs.

Zodd for DQS and DQS# traces should be 40Ω±10%. Z0 for DQ and DM should be 50Ω±10%.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#
2. Keep 0.1mm or more between each signal traces.
3. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



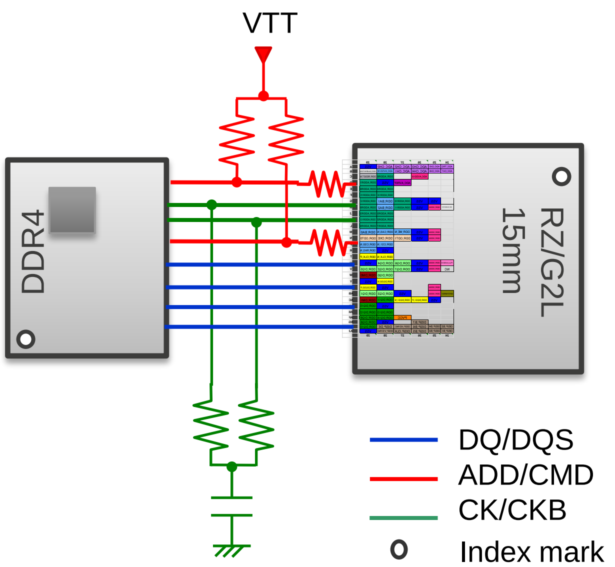
5.4 Topology T-1b

System RANK: Single

16Gb: ×16 Single-Rank DDR4 SDRAM

Target Device: MT40A1G16KD-062E

PCB: 4layers / One to One / Top mounting



Signal	IO drive strength	VTT termination resistance	Termination resistance / Capacitance	Damping resistor	ODT termination resistance		
					SoC	DRAM Access side	DRAM Non-Access side
CLK	60Ω	—	56Ω × 2 / 0.1uF	—	—	—	—
CA (A14, BA1, RAS, WE)	60Ω	100Ω	—	—	—	—	—
CA (Other than above)	60Ω	100Ω	—	22Ω	—	—	—
CTRL	60Ω	100Ω	—	—	—	—	—
RESET	60Ω	—	—	47Ω	—	—	—
DQ, DQS (Write)	40Ω	—	—	—	OFF	60Ω	60Ω
DQ, DQS (Read)	34Ω	—	—	—	40Ω	OFF	OFF

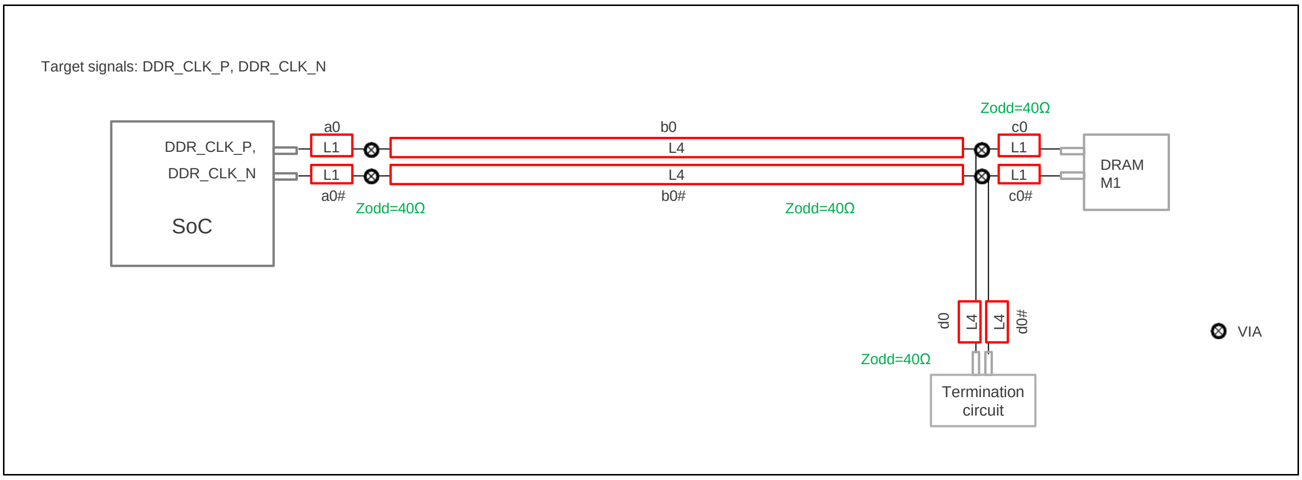
5.4.1 CLK topology

L1 and L4 in the figure below indicate the trace layers. a0 to d0# indicate the trace length. " ⊗ " are VIAs.

The odd mode impedance (Zodd) is equal to Zdiff/2. The clock traces Zodd should be 40Ω±10%.

Design the clock following the topology described in this figure.

1. CLK pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#
2. Keep 0.1mm or more between each signal traces.
3. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



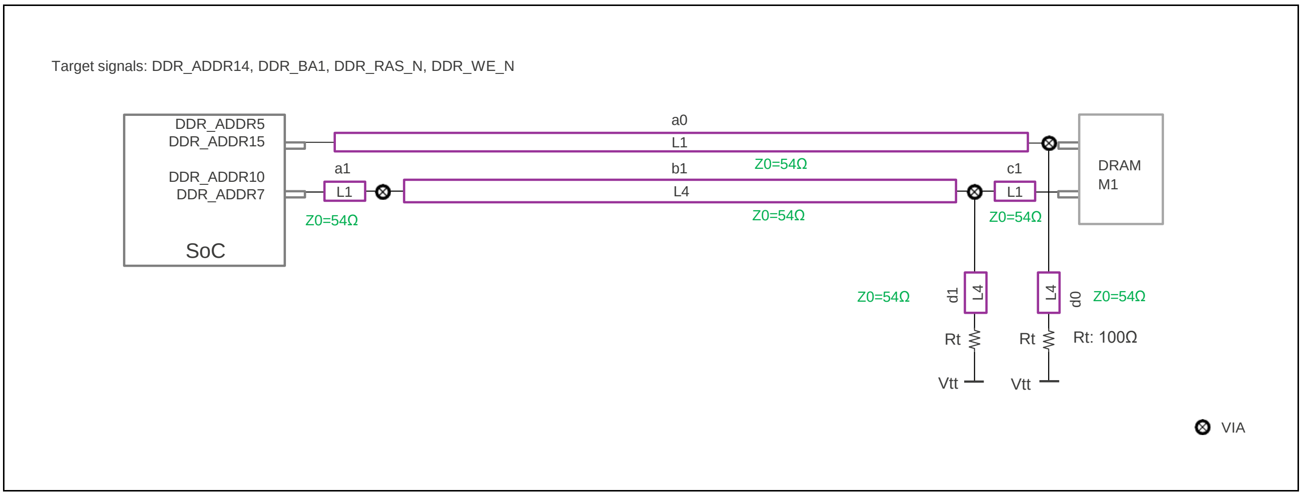
5.4.2 ADD/CMD1 topology

L1 and L4 in the figure below indicate the trace layers. a0 to d1 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 55Ω±10%.

Design address and command signals following the topology described in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



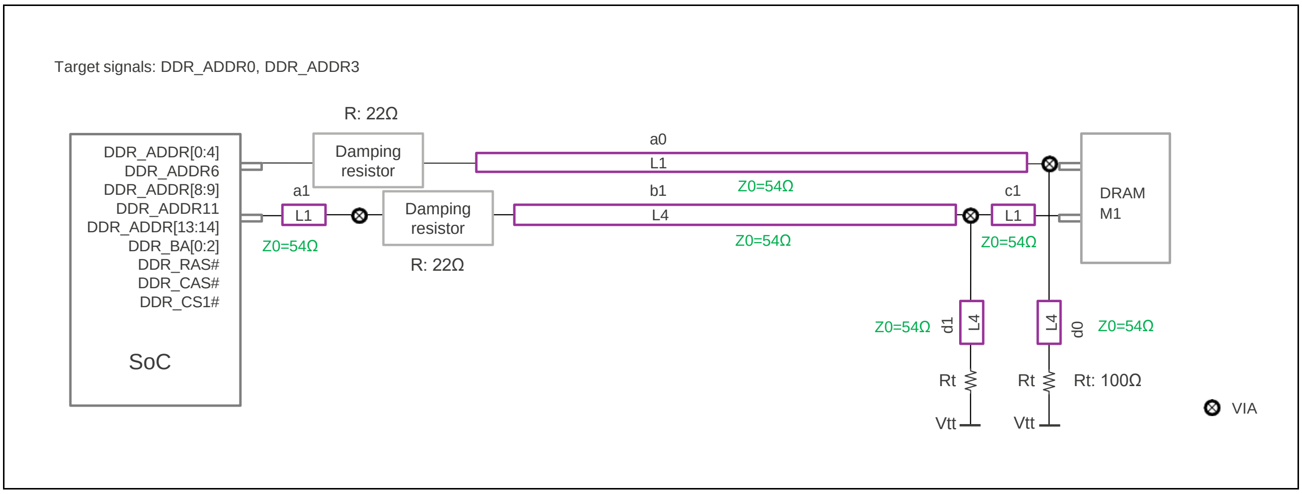
5.4.3 ADD/CMD2 topology

L1 and L4 in the figure below indicate the trace layers. a0 to d1 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 55Ω±10%.

Design address and command signals following the topology described in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



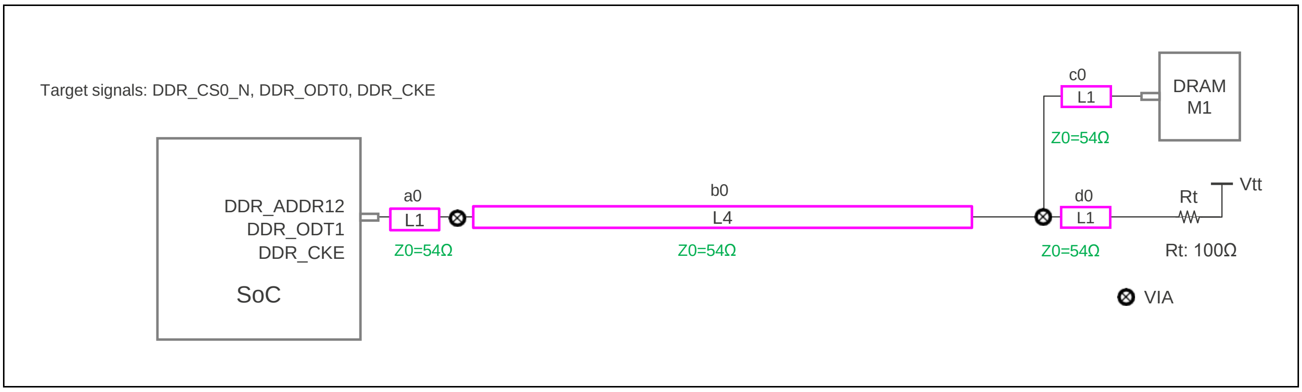
5.4.4 CTRL CS/ODT/CKE topology

L1 and L4 in the figure below indicate the trace layers. a0 to d0 indicate the trace length. " ⊗ " are VIAs.

Control signals are singled-ended, and their impedance (Z0) should be 55Ω±10%.

Design control signals following the topology described in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



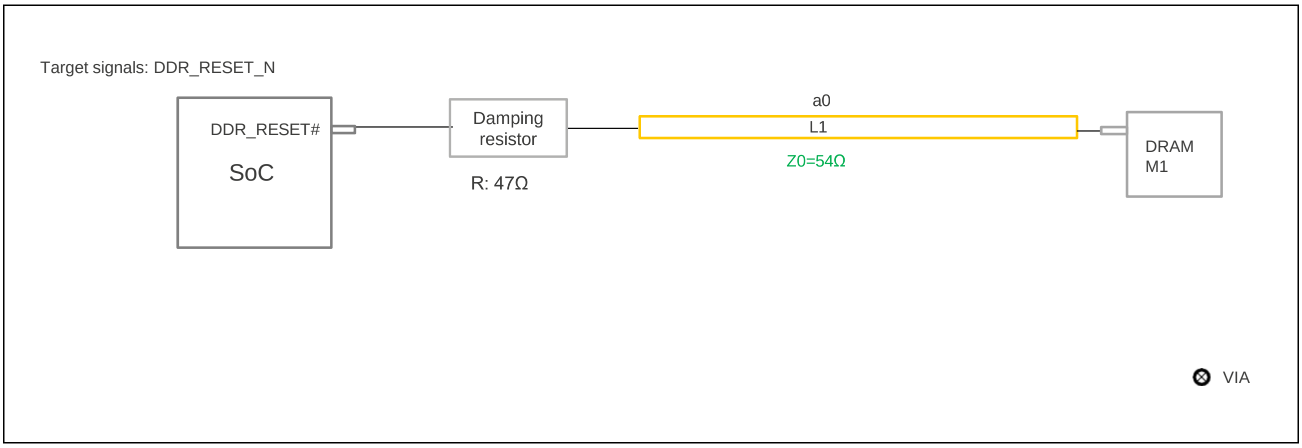
5.4.5 RESET topology

L1 in the figure below indicates trace layers. a0 indicates the trace length. “ ⊗ ” are VIAs.

The reset signal is single-ended, and his impedances (Z0) should be 55Ω±10%.

Design the wiring so that the wiring topology is as shown in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from waveform restrictions specifications. (Mandatory)



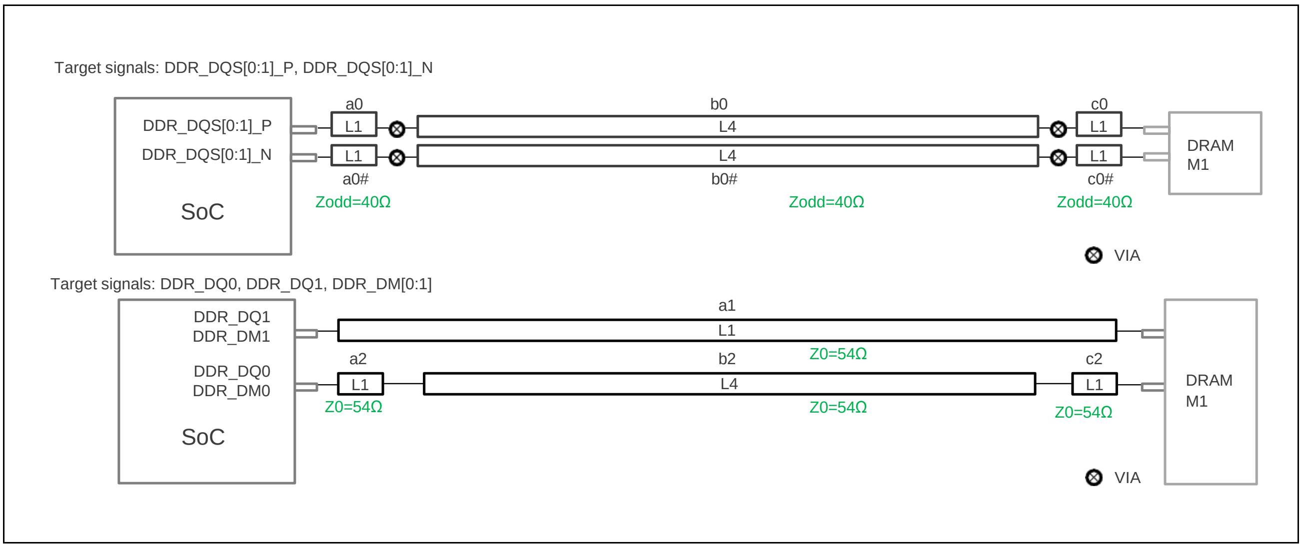
5.4.6 DQS/DQ topology

L1 and L4 int the figure below indicate the trace layers. a0 to c2 indicate the trace length. “ ⊗ ” are VIAs.

Zodd for DQS and DQS# traces should be 40Ω±10%. Z0 for DQ and DM should be 55Ω±10%.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#
2. Keep 0.1mm or more between each signal traces.
3. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



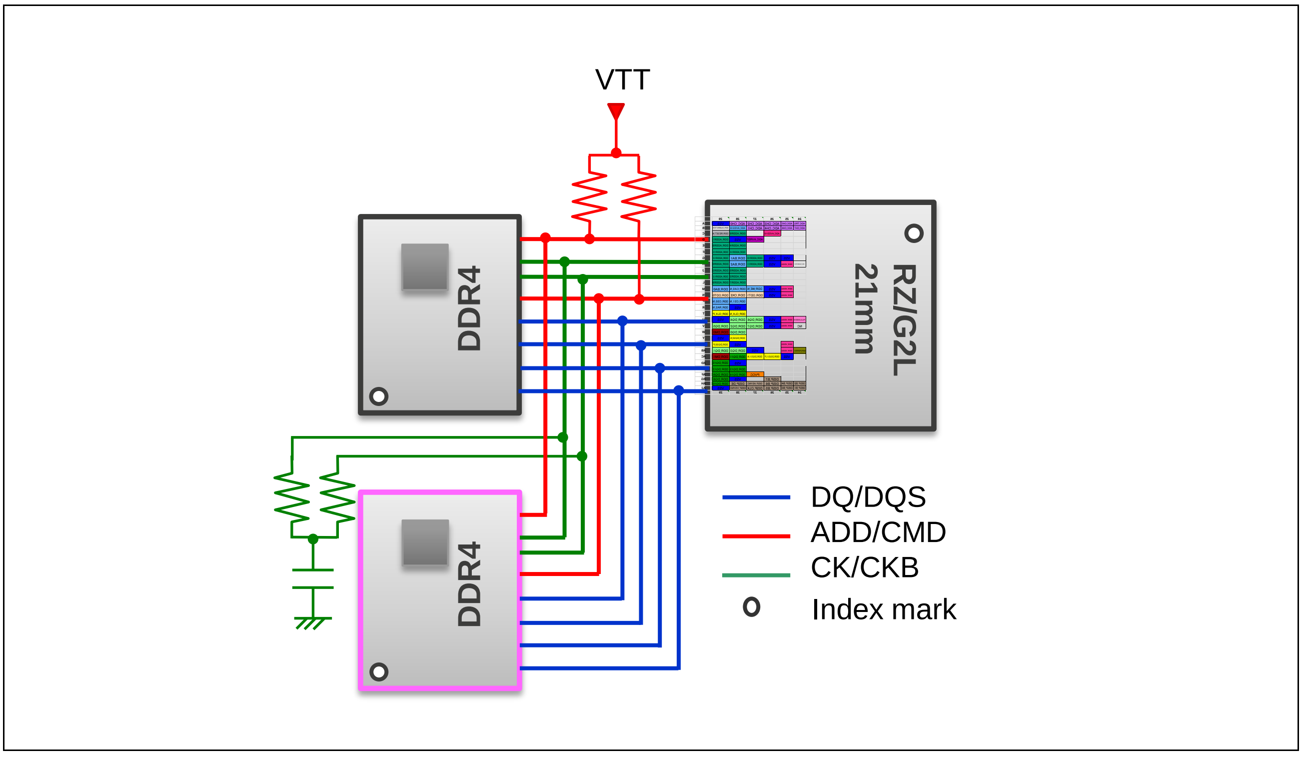
5.5 Topology T-2c

System RANK: Dual

32Gb: 16Gb(×16 Single Die Single-Rank DDR4 SDRAM) × 2

Target Device: MT40A1G16RC-062E

PCB: 6layers / One to Two / Clamshell mounting



Signal	IO drive strength	VTT termination resistance	Termination resistance / Capacitance	Damping resistor	ODT termination resistance		
					SoC	DRAM Access side	DRAM Non-Access side
CLK	60Ω	—	56Ω × 2 / 0.1uF	—	—	—	—
CA (CMD, ADD)	60Ω	47Ω	—	—	—	—	—
CTRL (CS, ODT)	60Ω	47Ω	—	—	—	—	—
CKE	60Ω	47Ω	—	—	—	—	—
RESET	60Ω	—	—	47Ω	—	—	—
DQ, DQS (Write)	34Ω	—	—	—	OFF	120Ω	34Ω
DQ, DQS (Read)	34Ω	—	—	—	60Ω	OFF	34Ω

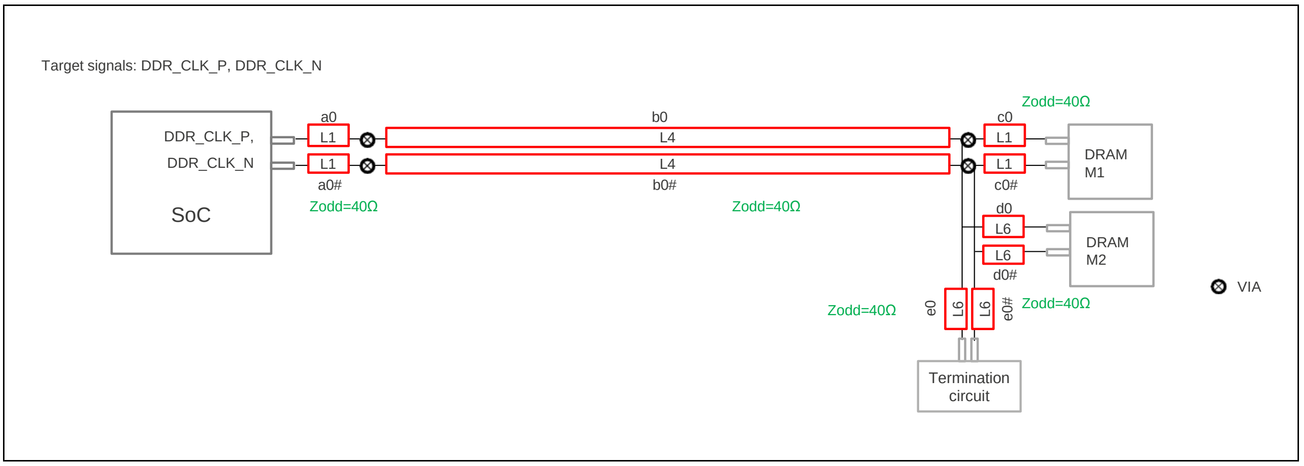
5.5.1 CLK topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to e0# indicate the trace length. " ⊗ " are VIAs.

The odd mode impedance (Zodd) is equal to Zdiff/2. The clock traces Zodd should be 40Ω±10%.

Design the clock following the topology described in this figure.

1. CLK pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#, e0=e0#
2. Keep 0.1mm or more between each signal traces.
3. Top and bottom branches to memory should be of equal length.
4. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



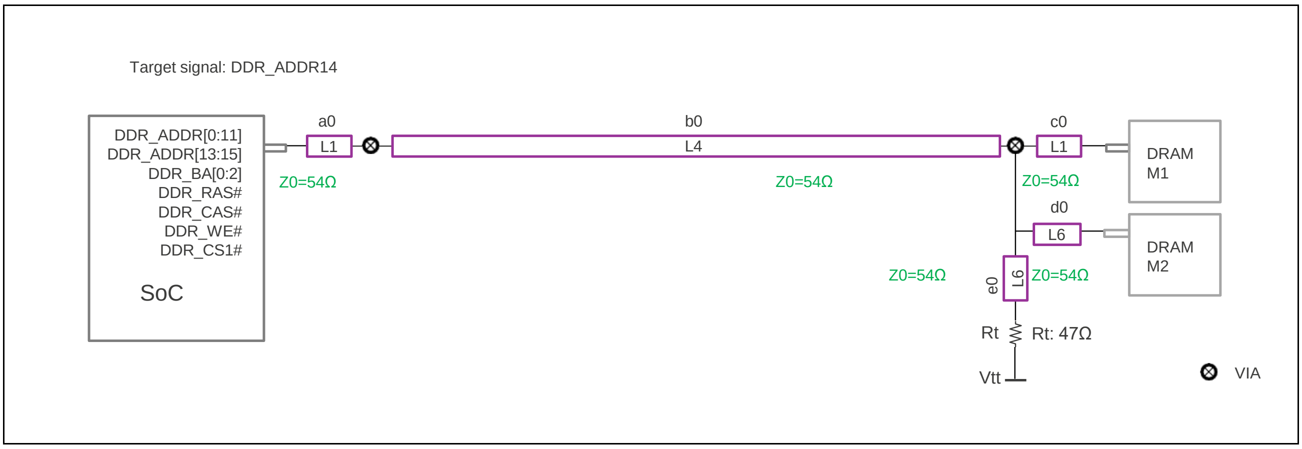
5.5.2 ADD/CMD topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to e0 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 55Ω±10%.

Design address and command signals following the topology described in this figure.

1. Top and bottom branches to memory should be of equal length.
2. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



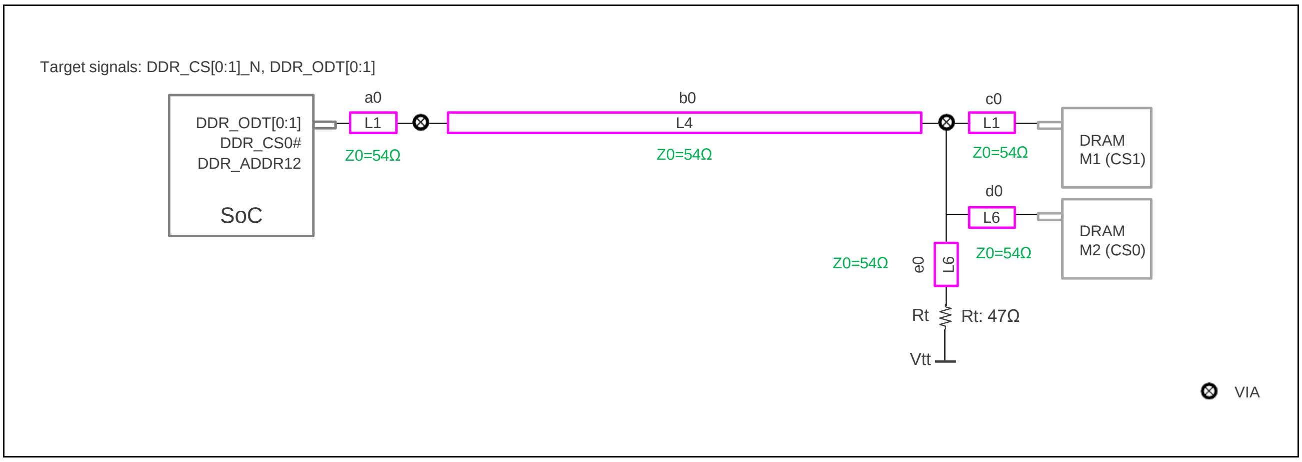
5.5.3 CTRL CS/ODT topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to e0 indicate the trace length. " ⊗ " are VIAs.

Control signals are singled-ended, and their impedance (Z0) should be 55Ω±10%.

Design control signals following the topology described in this figure.

1. Top and bottom branches to memory should be of equal length.
2. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



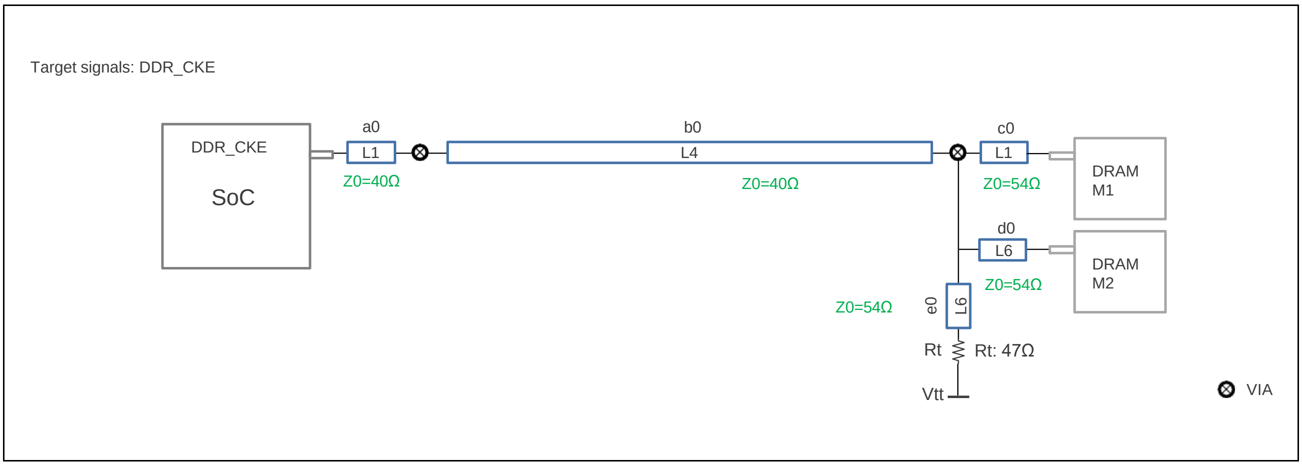
5.5.4 CTRL CKE topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to e0 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 55Ω±10%.

Design address and command signals following the topology described in this figure.

1. Top and bottom branches to memory should be of equal length.
2. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



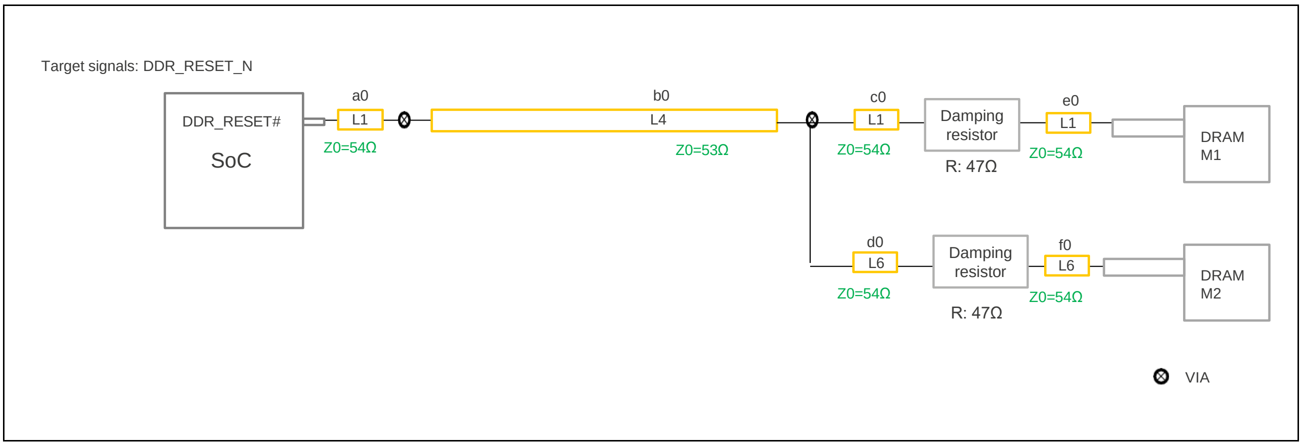
5.5.5 RESET topology

L1, L4 and L6 in the figure below indicate trace layers. a0 to f0 indicate the trace length. “ ⊗ ” are VIAs.

The reset signal is single-ended, and his impedances (Z0) should be 55Ω±10%.

Design the wiring so that the wiring topology is as shown in this figure.

1. Top and bottom branches to memory should be of equal length.
2. Verify the layout using SI simulation. Check simulation results using [REF] from waveform restrictions specifications. (Mandatory)



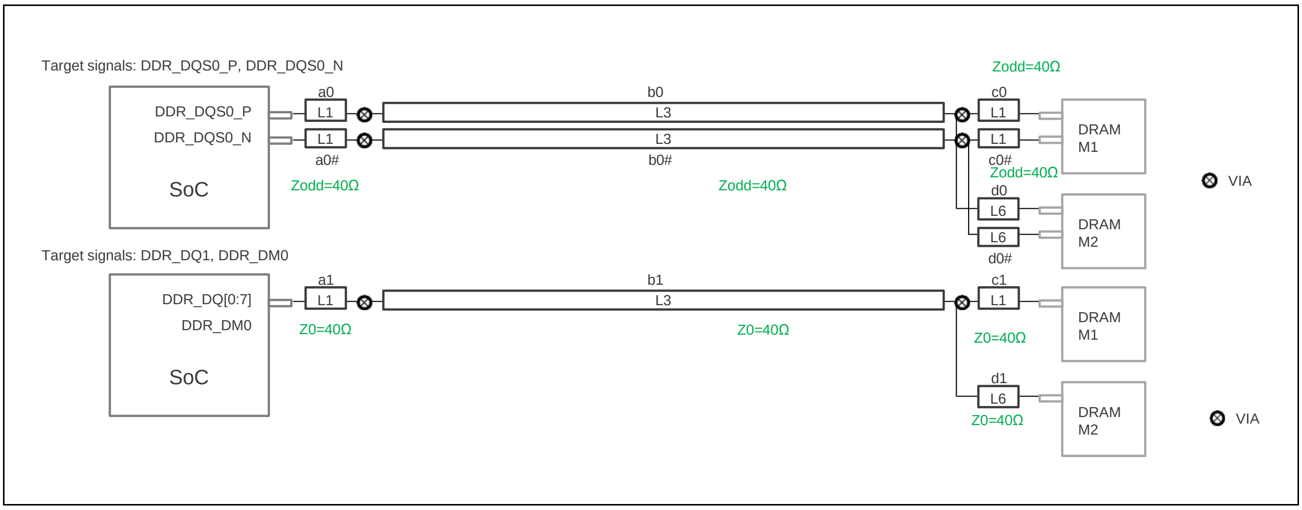
5.5.6 DQS0/DQ_L topology

L1, L3 and L6 in the figure below indicate the trace layers. a0 to d1 indicate the trace length. " ⊗ " are VIAs.

Zodd for DQS and DQS# traces should be 40Ω±10%. Z0 for DQ and DM should be 40Ω±10%.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#
2. Keep 0.1mm or more between each signal traces.
3. Top and bottom branches to memory should be of equal length.
4. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



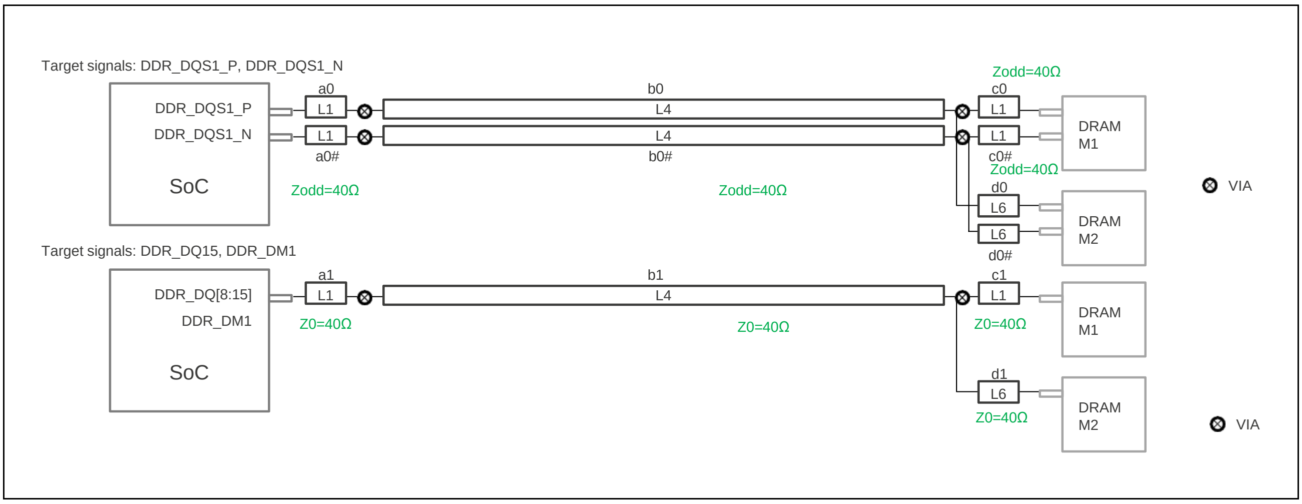
5.5.7 DQS1/DQ_H topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to d1 indicate the trace length. “ ⊗ ” are VIAs.

Zodd for DQS and DQS# traces should be 40Ω±10%. Z0 for DQ and DM should be 55Ω±10%.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#
2. Keep 0.1mm or more between each signal traces.
3. Top and bottom branches to memory should be of equal length.
4. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



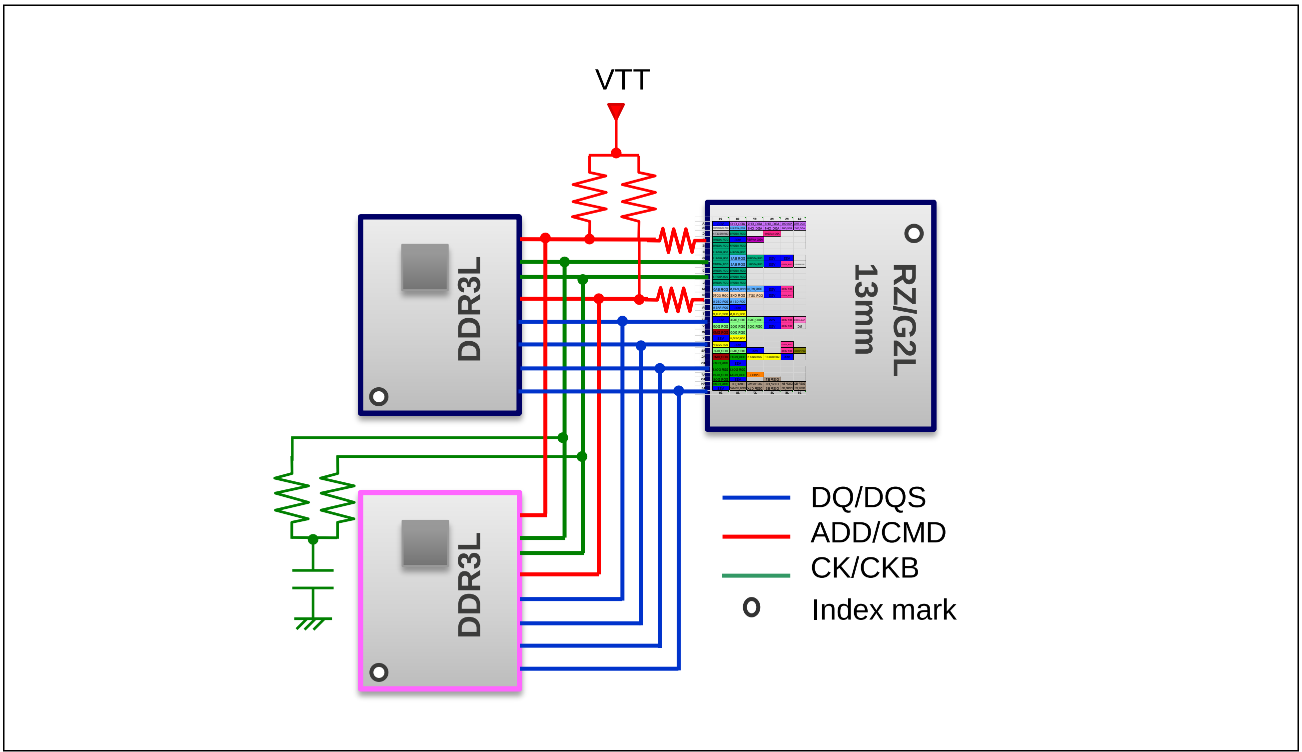
5.6 Topology T-3cl

System RANK: Dual

8Gb: 4Gb(×16 Single Die Single-Rank DDR3L SDRAM) × 2

Target Device: MT41K256M16TW-107 IT:P

PCB: 6layers / One to Two / Clamshell mounting



Signal	IO drive strength	VTT termination resistance	Termination resistance / Capacitance	Damping resistor	ODT termination resistance		
					SoC	DRAM Access side	DRAM Non-Access side
CLK	60Ω	—	56Ω × 2 / 0.1uF	—	—	—	—
CA (A10, BA2, CAS, RAS, WE)	60Ω	82Ω	—	22Ω	—	—	—
CA (Other than above)	60Ω	56Ω	—	—	—	—	—
CTRL (CS, ODT)	60Ω	82Ω	—	22Ω	—	—	—
CKE	60Ω	160Ω × 2	—	0Ω	—	—	—
RESET	60Ω	—	—	47Ω	—	—	—
DQ, DQS (Write)	34Ω	—	—	—	OFF	60Ω	30Ω
DQ, DQS (Read)	34Ω	—	—	—	120Ω	OFF	30Ω

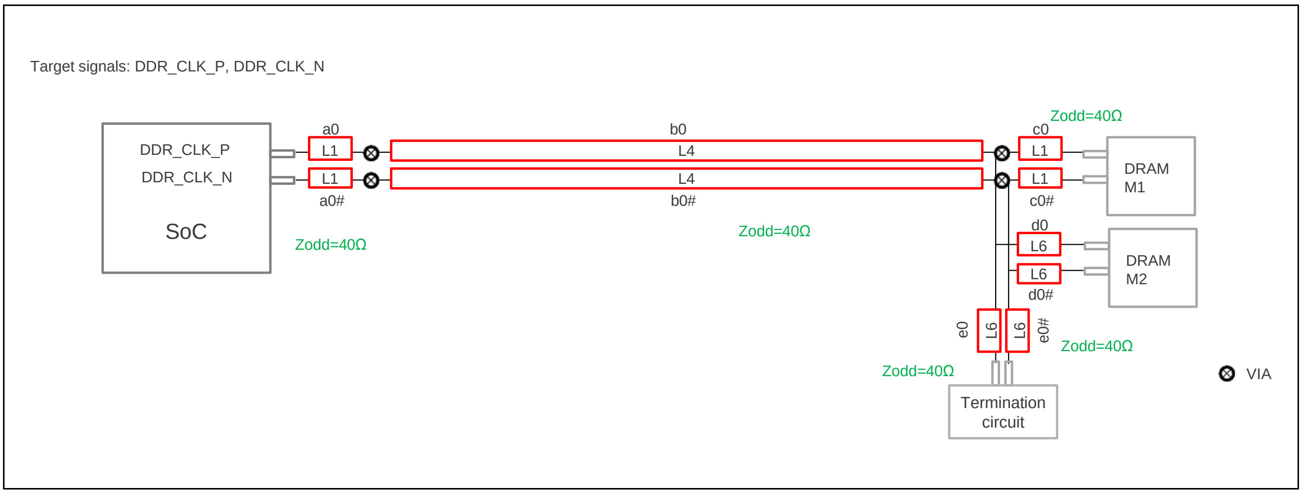
5.6.1 CLK topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to e0# indicate the trace length. “ ⊗ ” are VIAs.

The odd mode impedance (Zodd) is equal to Zdiff/2. The clock traces Zodd should be 40Ω±10%.

Design the clock following the topology described in this figure.

1. CLK pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#, e0=e0#
2. Keep 0.1mm or more between each signal traces.
3. Top and bottom branches to memory should be of equal length.
4. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



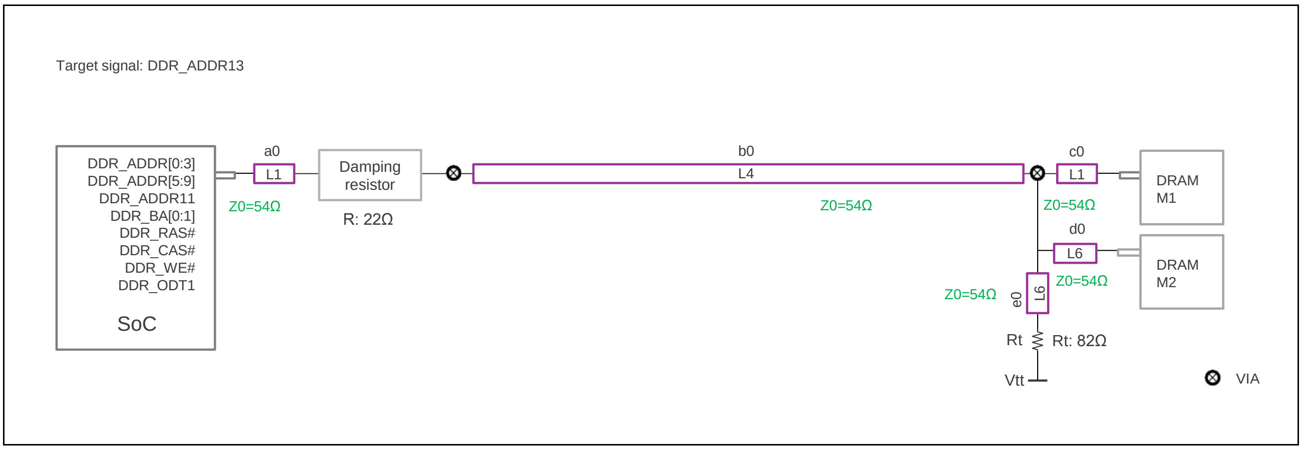
5.6.2 ADD/CMD1 topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to e0 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 55Ω±10%.

Design address and command signals following the topology described in this figure.

1. Top and bottom branches to memory should be of equal length.
2. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



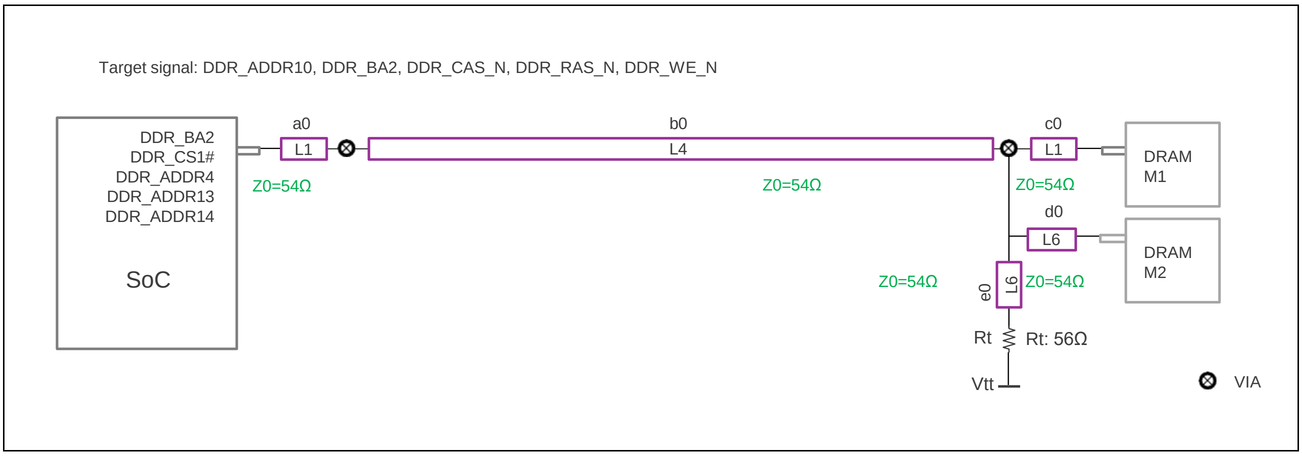
5.6.3 ADD/CMD2 topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to e0 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 55Ω±10%.

Design address and command signals following the topology described in this figure.

1. Top and bottom branches to memory should be of equal length.
2. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



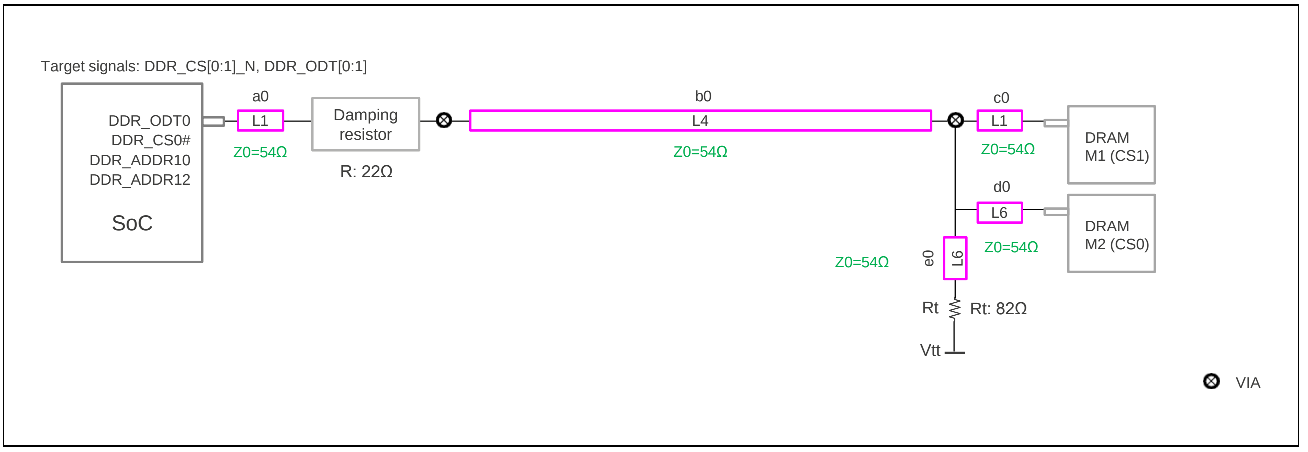
5.6.4 CTRL CS/ODT topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to e0 indicate the trace length. " ⊗ " are VIAs.

Control signals are singled-ended, and their impedance (Z0) should be 55Ω±10%.

Design control signals following the topology described in this figure.

1. Top and bottom branches to memory should be of equal length.
2. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



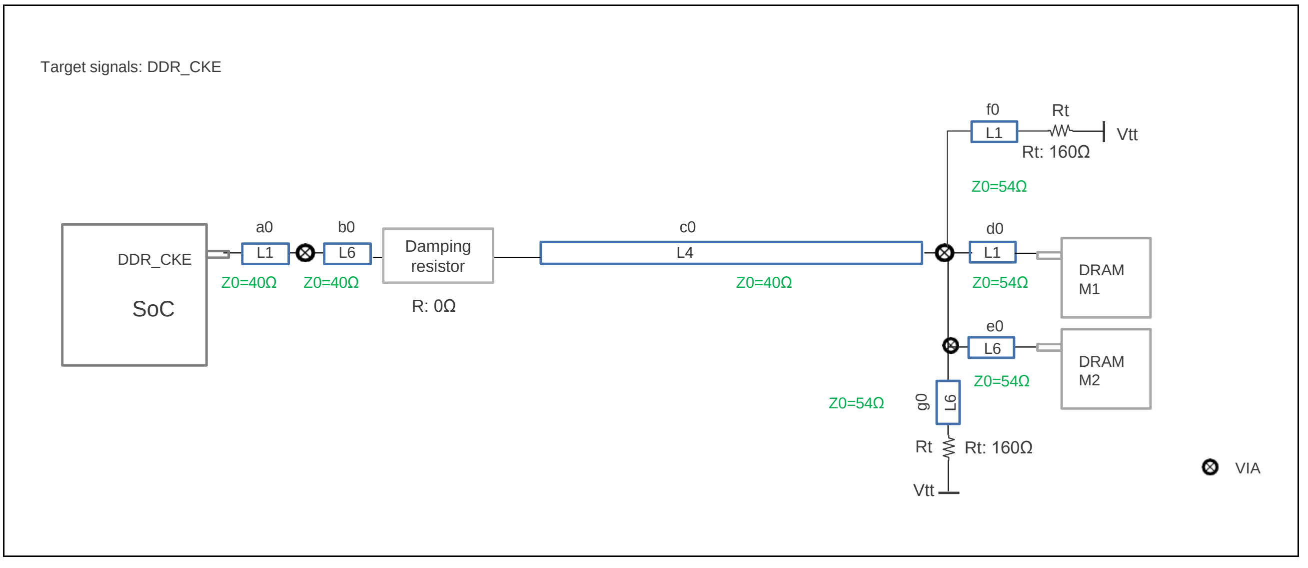
5.6.5 CTRL CKE topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to g0 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 55Ω±10%.

Design address and command signals following the topology described in this figure.

1. Top and bottom branches to memory should be of equal length.
2. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



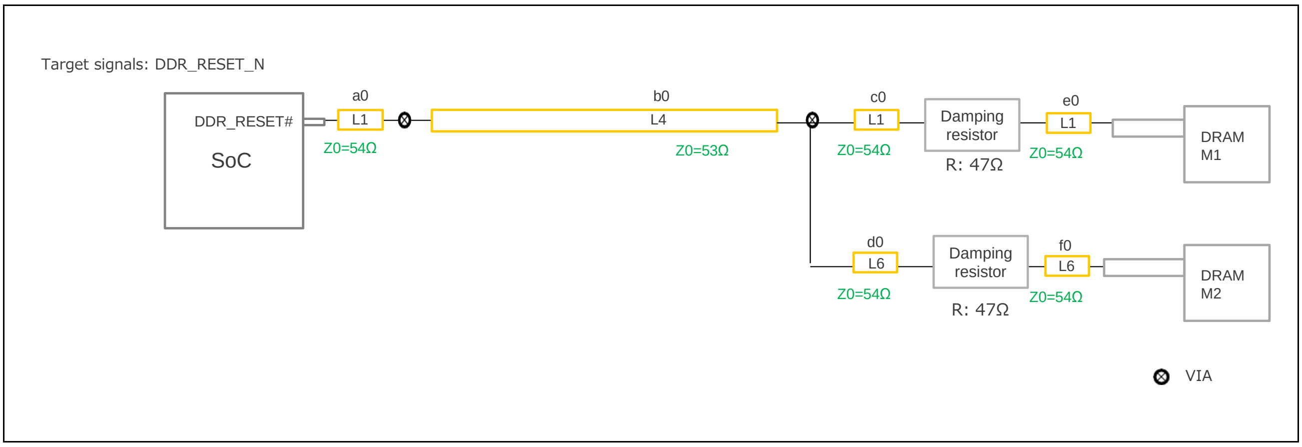
5.6.6 RESET topology

L1, L4 and L6 in the figure below indicate trace layers. a0 to f0 indicate the trace length. “ ⊗ ” are VIAs.

The reset signal is single-ended, and his impedances (Z0) should be 55Ω±10%.

Design the wiring so that the wiring topology is as shown in this figure.

1. Top and bottom branches to memory should be of equal length.
2. Verify the layout using SI simulation. Check simulation results using [REF] from waveform restrictions specifications. (Mandatory)



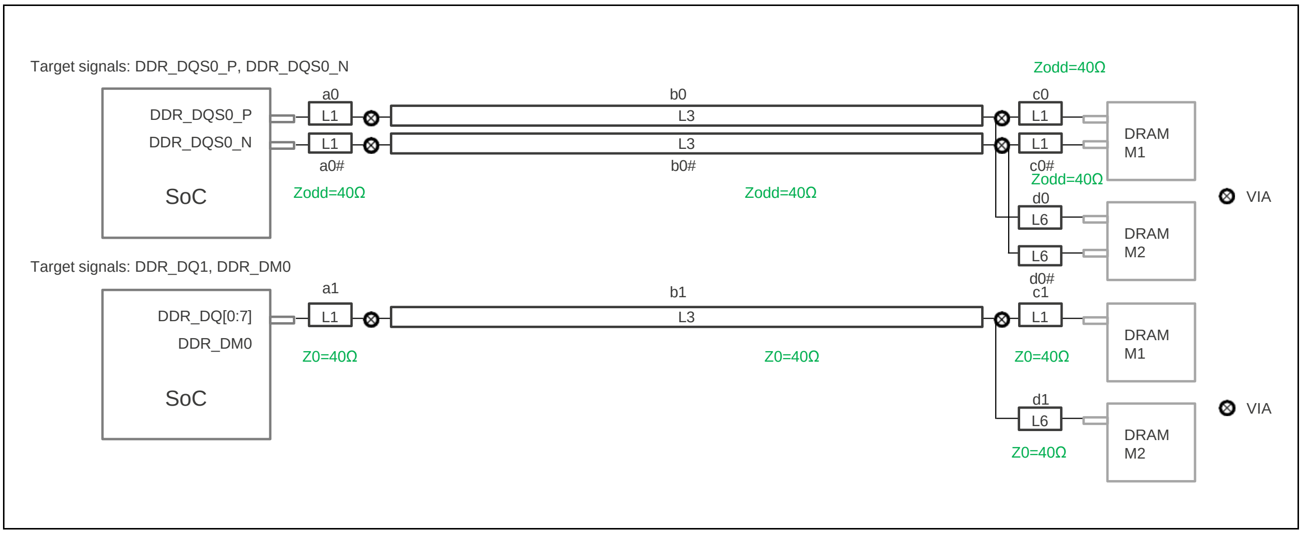
5.6.7 DQS0/DQ_L topology

L1, L3 and L6 in the figure below indicate the trace layers. a0 to d1 indicate the trace length. “ ⊗ ” are VIAs.

Zodd for DQS and DQS# traces should be 40Ω±10%. Z0 for DQ and DM should be 55Ω±10%.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#
2. Keep 0.1mm or more between each signal traces.
3. Top and bottom branches to memory should be of equal length.
4. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



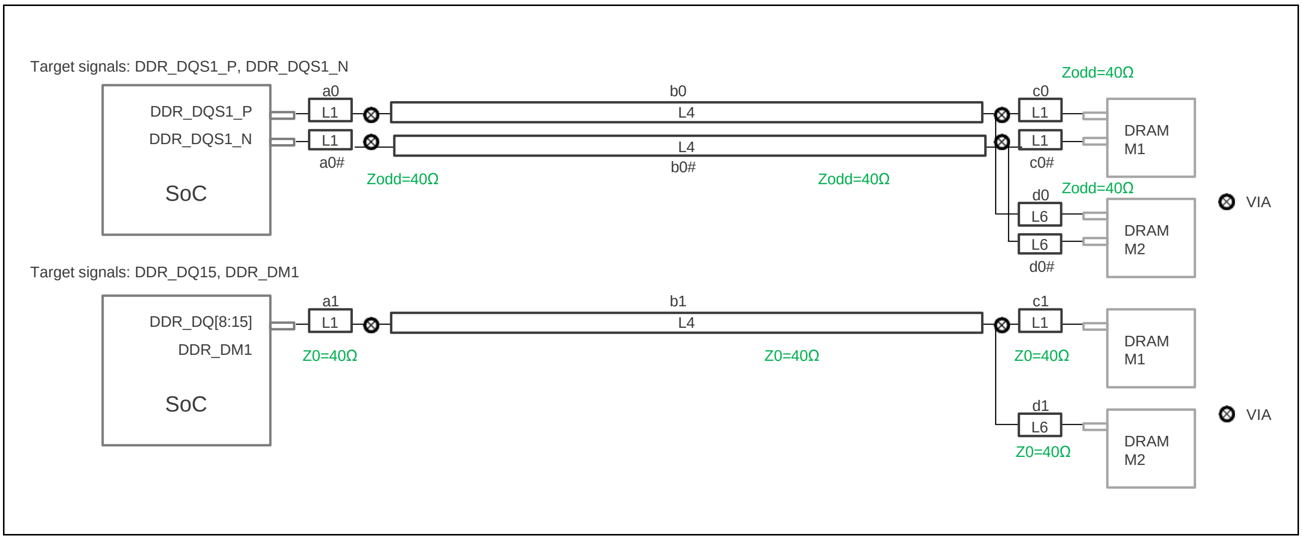
5.6.8 DQS1/DQ_H topology

L1, L4 and L6 in the figure below indicate the trace layers. a0 to d1 indicate the trace length. “ ⊗ ” are VIAs.

Zodd for DQS and DQS# traces should be 40Ω±10%. Z0 for DQ and DM should be 55Ω±10%.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#
2. Keep 0.1mm or more between each signal traces.
3. Top and bottom branches to memory should be of equal length.
4. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



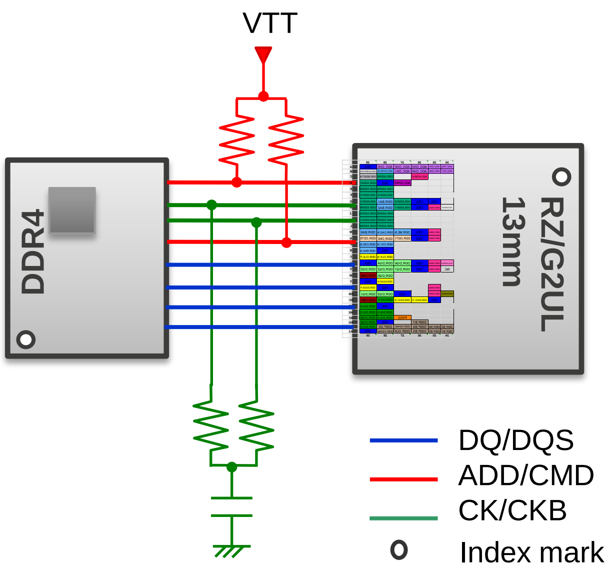
5.7 Topology T-3bcud2

System RANK: Single

8Gb: ×16 Single-Rank DDR4 SDRAM

Target Device: MT40A512M16TB-062E

PCB: 6layers / One to One / Top mounting



Signal	IO drive strength	VTT termination resistance	Termination resistance / Capacitance	Damping resistor	ODT termination resistance		
					SoC	DRAM Access side	DRAM Non-Access side
CLK	60Ω	—	56Ω × 2 / 0.1uF	—	—	—	—
CA (CMD, ADD)	60Ω	82Ω	—	—	—	—	—
CTRL (CS, ODT, CKE)	60Ω	82Ω	—	—	—	—	—
RESET	60Ω	—	—	22Ω	—	—	—
DQ, DQS (Write)	40Ω	—	—	—	OFF	60Ω	60Ω
DQ, DQS (Read)	34Ω	—	—	—	40Ω	OFF	OFF

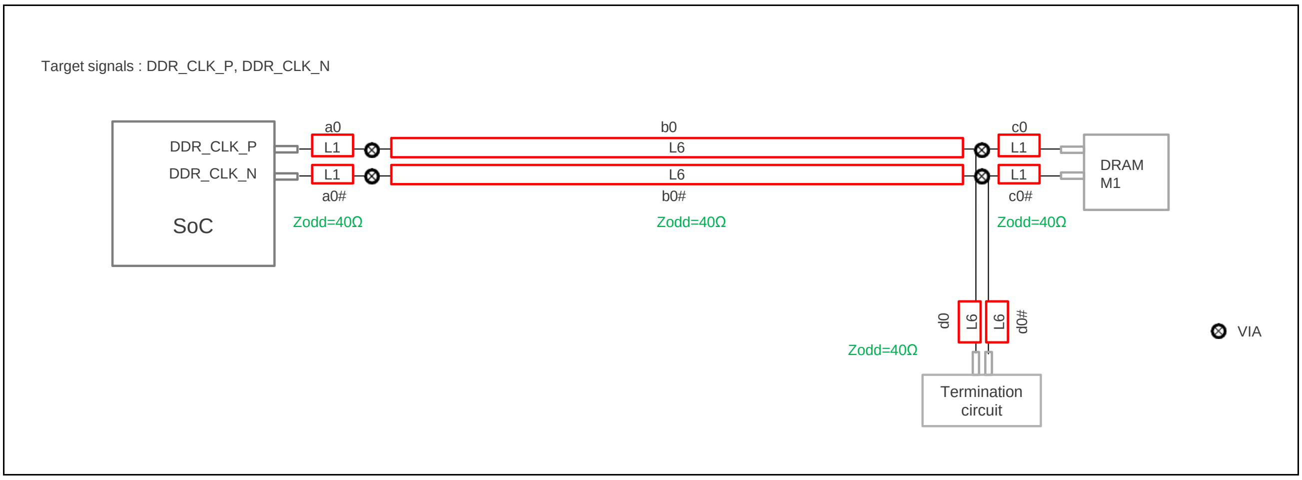
5.7.1 CLK topology

L1 and L6 in the figure below indicate the trace layers. a0 to d0# indicate the trace length. " ⊗ " are VIAs.

The odd mode impedance (Zodd) is equal to Zdiff/2. The clock traces Zodd should be 40Ω±10%.

Design the clock following the topology described in this figure.

1. CLK pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#
2. Keep 0.1mm or more between each signal traces.
3. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



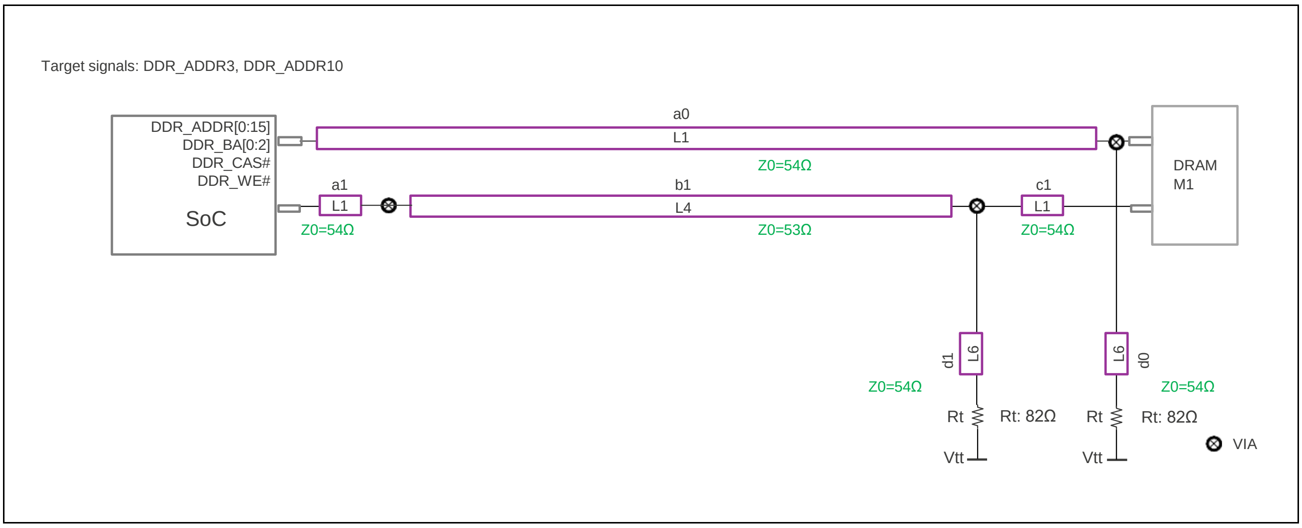
5.7.2 ADD/CMD topology

L1, L3 and L6 in the figure below indicate the trace layers. a0 to d1 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 55Ω±10%.

Design address and command signals following the topology described in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



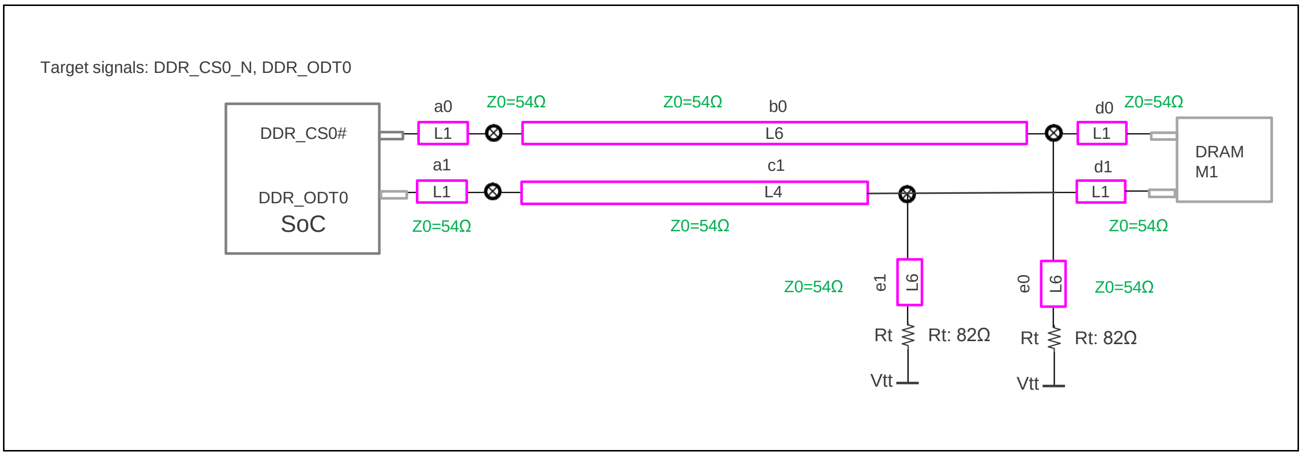
5.7.3 CTRL CS/ODT topology

L1 and L6 in the figure below indicate the trace layers. a0 to e1 indicate the trace length. “ ⊗ ” are VIAs.

Control signals are singled-ended, and their impedance (Z0) should be 55Ω±10%.

Design control signals following the topology described in this figure

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



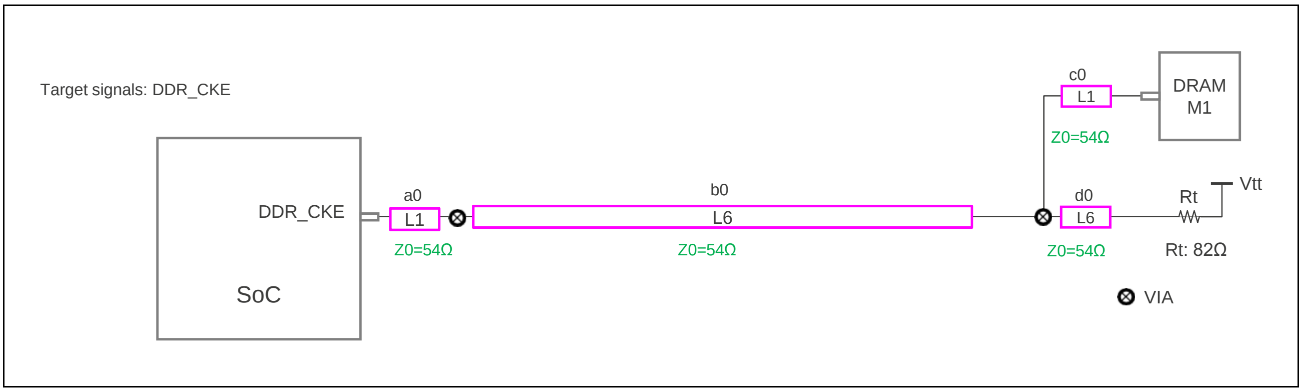
5.7.4 CTRL CKE topology

L1 and L6 in the figure below indicate the trace layers. a0 to d0 indicate the trace length. “ ⊗ ” are VIAs.

Control signals are singled-ended, and their impedance (Z0) should be 55Ω±10%.

Design control signals following the topology described in this figure

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



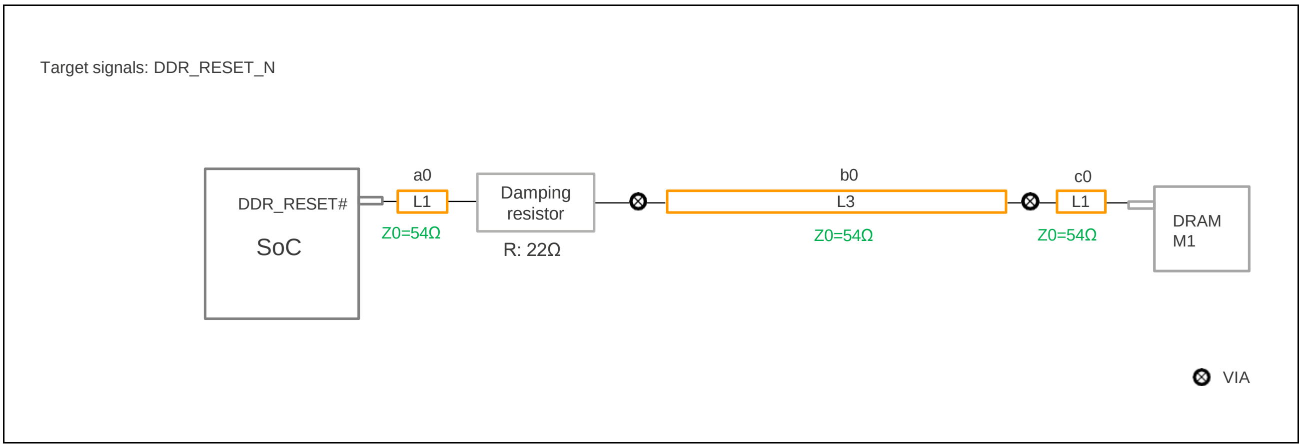
5.7.5 RESET topology

L1 and L3 in the figure below indicate trace layers. a0 to c0 indicate the trace length. " ⊗ " are VIAs.

The reset signal is single-ended, and his impedances (Z0) should be 55Ω±10%.

Design the wiring so that the wiring topology is as shown in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from waveform restrictions specifications. (Mandatory)



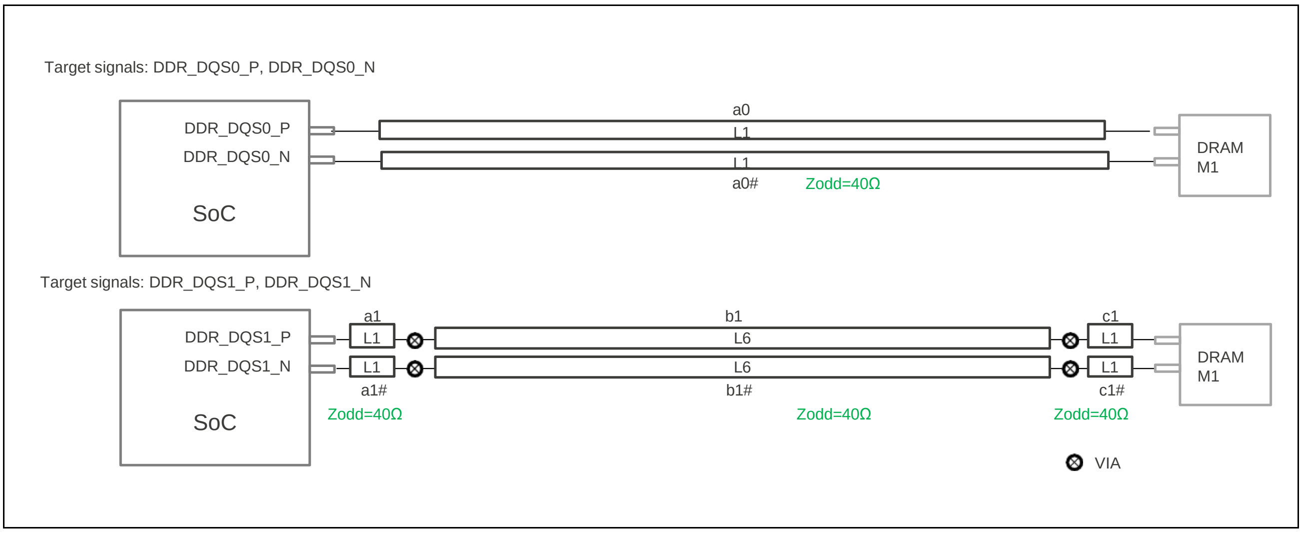
5.7.6 DQS0/1 topology

L1 and L6 int the figure below indicate the trace layers. a0 to c1# indicate the trace length. " ⊗ " are VIAs.

Zodd for DQS and DQS# traces should be 40Ω±10%.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#
2. Keep 0.1mm or more between each signal traces.
3. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



5.7.7 DQ_H/L topology

L1 and L6 int the figure below indicate the trace layers. a0 to c1 indicate the trace length. “ ⊗ ” are VIAs.

Z0 for DQ and DM should be 55Ω±10%.

Design the DQ following the topology described in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)

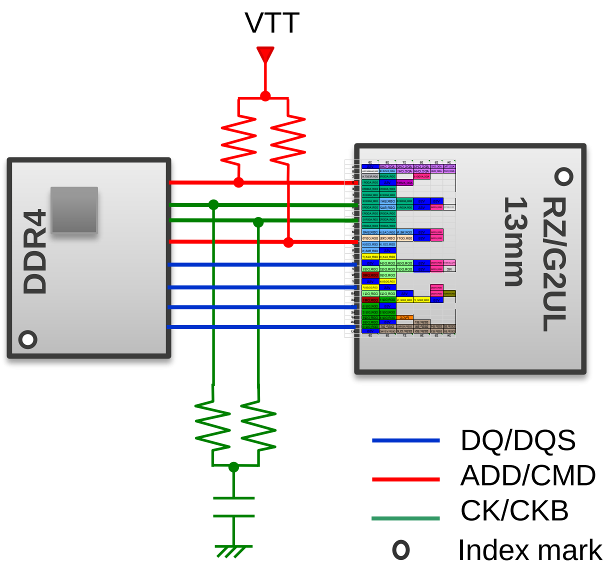
5.8 Topology T-3bcud

System RANK: Single

8Gb: ×16 Single-Rank DDR4 SDRAM

Target Device: MT40A512M16TB-062E

PCB: 6layers / One to One / Top mounting



Signal	IO drive strength	VTT termination resistance	Termination resistance / Capacitance	Damping resistor	ODT termination resistance		
					SoC	DRAM Access side	DRAM Non-Access side
CLK	60Ω	—	56Ω × 2 / 0.1uF	—	—	—	—
CA (CMD, ADD)	60Ω	82Ω	—	—	—	—	—
CTRL (CS, ODT, CKE)	60Ω	82Ω	—	—	—	—	—
RESET	60Ω	—	—	47Ω	—	—	—
DQ, DQS (Write)	40Ω	—	—	—	OFF	60Ω	60Ω
DQ, DQS (Read)	34Ω	—	—	—	40Ω	OFF	OFF

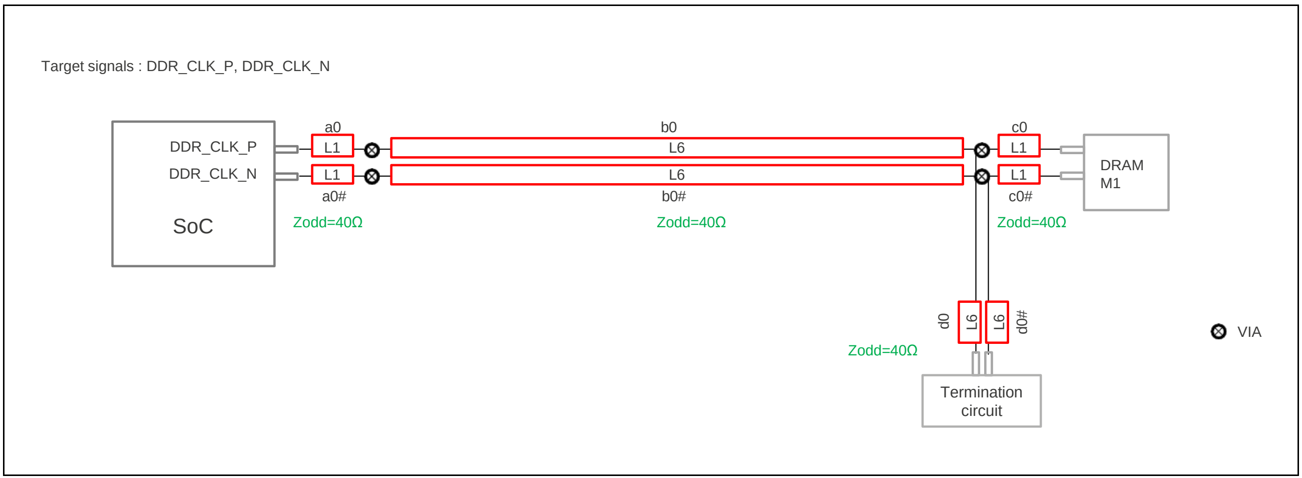
5.8.1 CLK topology

L1 and L6 in the figure below indicate the trace layers. a0 to d0# indicate the trace length. " ⊗ " are VIAs.

The odd mode impedance (Zodd) is equal to Zdiff/2. The clock traces Zodd should be 40Ω±10%.

Design the clock following the topology described in this figure.

1. CLK pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#
2. Keep 0.1mm or more between each signal traces.
3. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



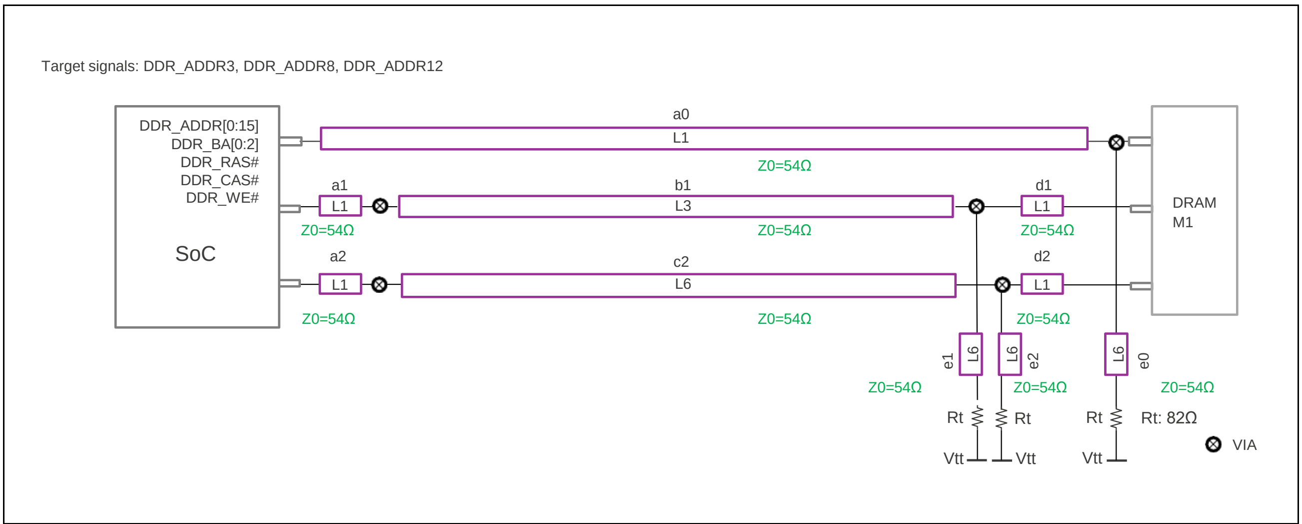
5.8.2 ADD/CMD topology

L1, L3 and L6 in the figure below indicate the trace layers. a0 to e2 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 55Ω±10%.

Design address and command signals following the topology described in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



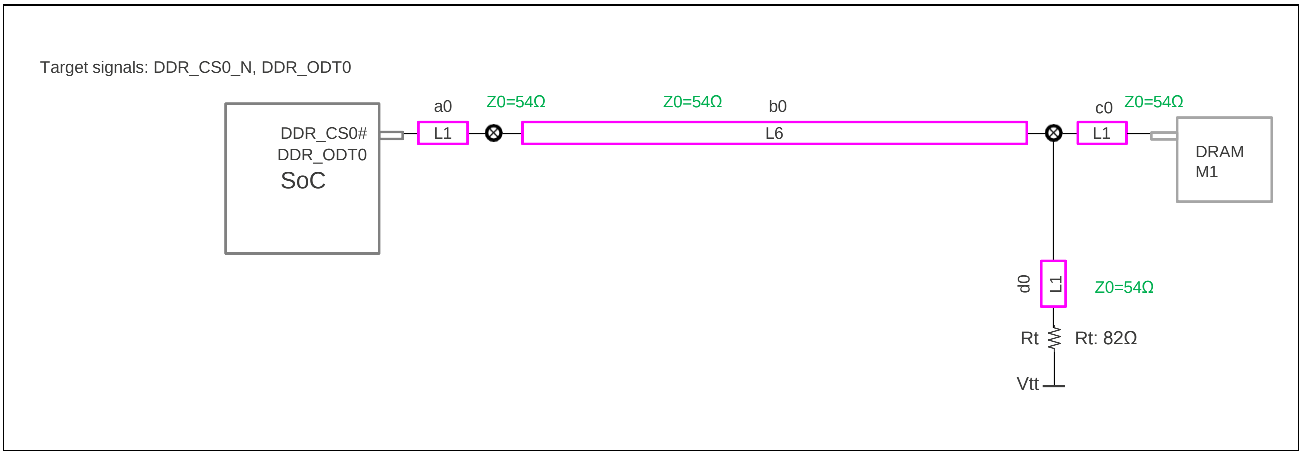
5.8.3 CTRL CS/ODT topology

L1 and L6 in the figure below indicate the trace layers. a0 to d0 indicate the trace length. " ⊗ " are VIAs.

Control signals are singled-ended, and their impedance (Z0) should be 55Ω±10%.

Design control signals following the topology described in this figure

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



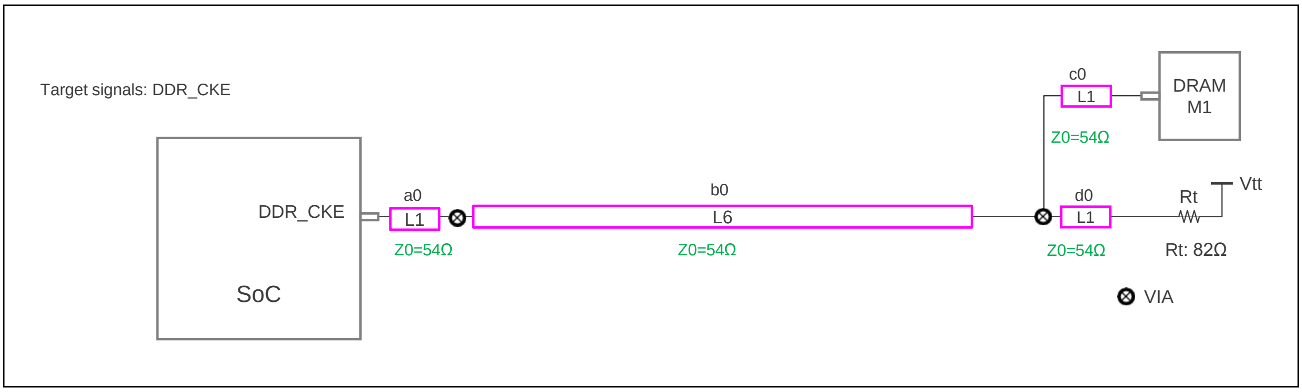
5.8.4 CTRL CKE topology

L1 and L6 in the figure below indicate the trace layers. a0 to d0 indicate the trace length. " ⊗ " are VIAs.

Control signals are singled-ended, and their impedance (Z0) should be 55Ω±10%.

Design control signals following the topology described in this figure

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



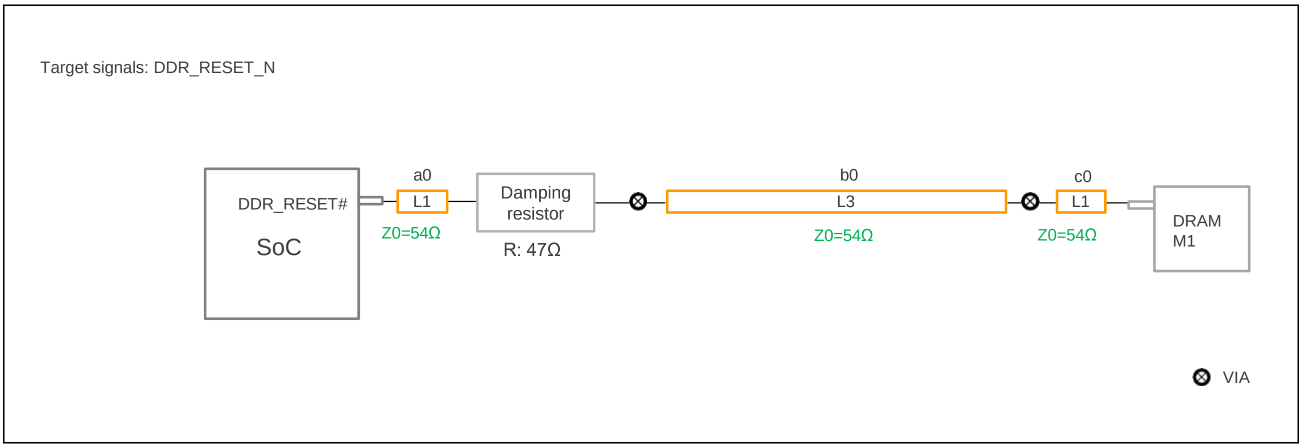
5.8.5 RESET topology

L1 and L3 in the figure below indicate trace layers. a0 to c0 indicate the trace length. " ⊗ " are VIAs.

The reset signal is single-ended, and his impedances (Z0) should be 55Ω±10%.

Design the wiring so that the wiring topology is as shown in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from waveform restrictions specifications. (Mandatory)



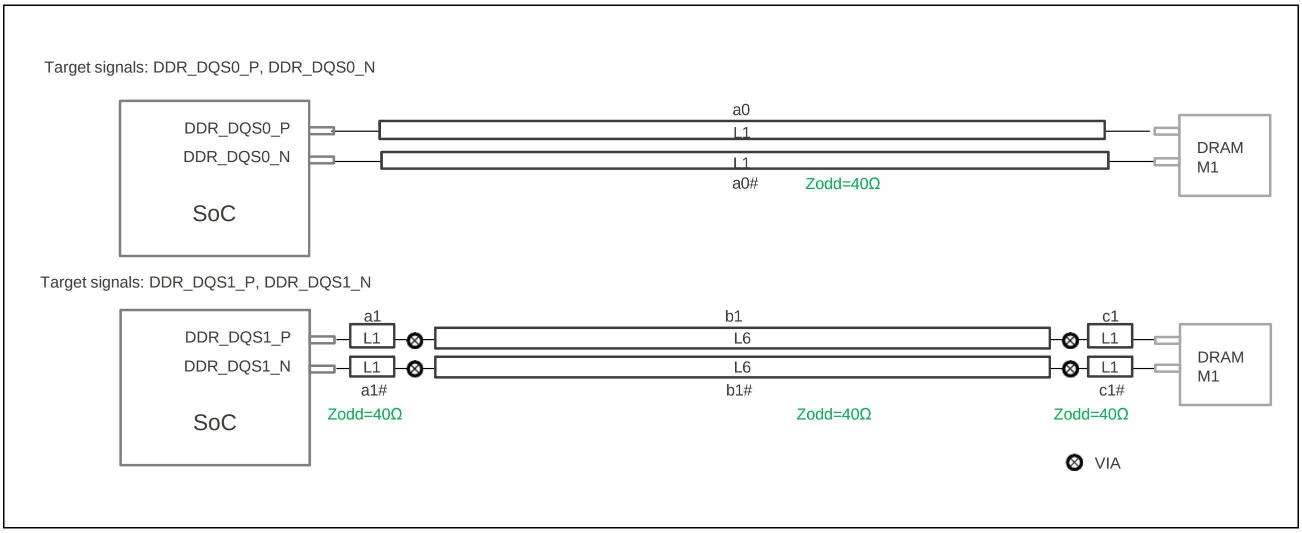
5.8.6 DQS0/1 topology

L1 and L6 int the figure below indicate the trace layers. a0 to c1# indicate the trace length. " ⊗ " are VIAs.

Zodd for DQS and DQS# traces should be 40Ω±10%.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#
2. Keep 0.1mm or more between each signal traces.
3. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



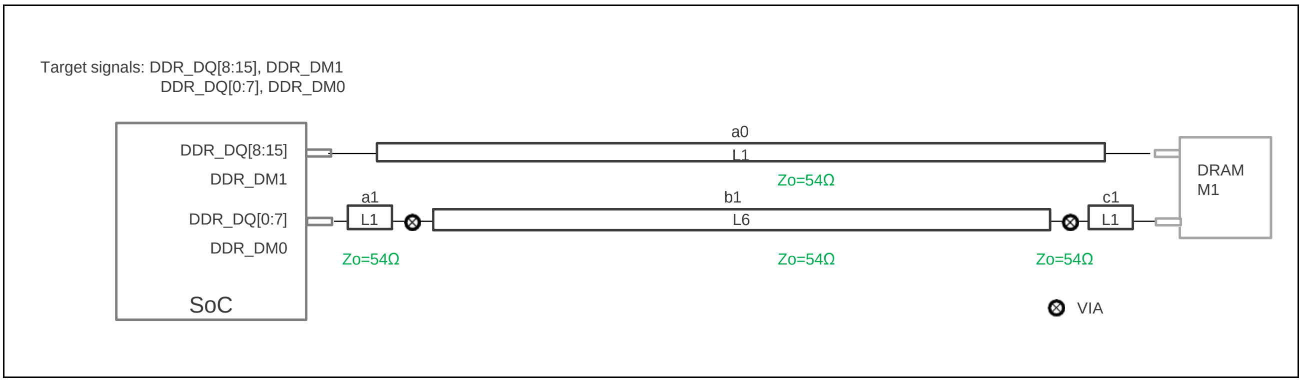
5.8.7 DQ_H/L topology

L1 and L6 int the figure below indicate the trace layers. a0 to c1 indicate the trace length. " ⊗ " are VIAs.

Z0 for DQ and DM should be 55Ω±10%.

Design the DQ following the topology described in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



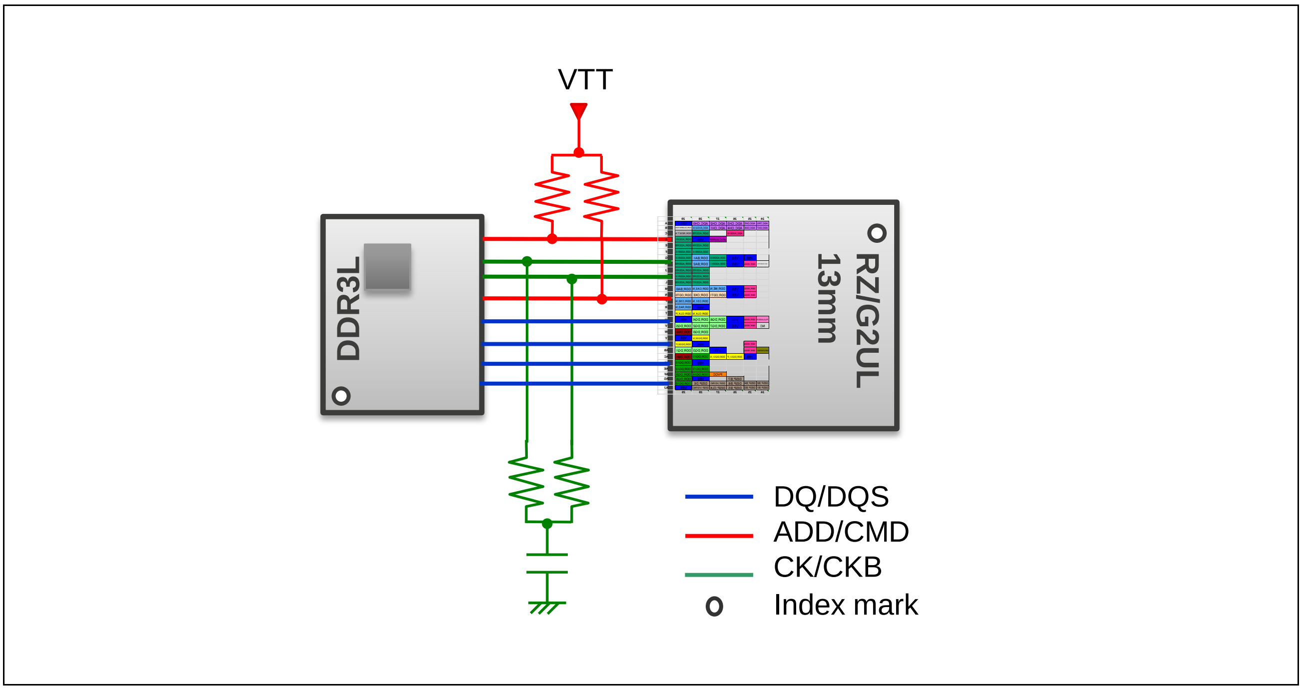
5.9 Topology T-3bcul

System RANK: Single

4Gb: ×16 Single Die Single-Rank DDR3L SDRAM

Target Device: MT41K256M16TW-107 IT:P

PCB: 6layers / One to One / Top mounting



Signal	IO drive strength	VTT termination resistance	Termination resistance / Capacitance	Damping resistor	ODT termination resistance		
					SoC	DRAM Access side	DRAM Non-Access side
CLK	60Ω	—	56Ω × 2 / 0.1uF	—	—	—	—
CA (CMD, ADD)	60Ω	82Ω	—	—	—	—	—
CTRL (CS, ODT, CKE)	60Ω	82Ω	—	—	—	—	—
RESET	60Ω	—	—	47Ω	—	—	—
DQ, DQS (Write)	34Ω	—	—	—	OFF	60Ω	60Ω
DQ, DQS (Read)	34Ω	—	—	—	120Ω	OFF	OFF

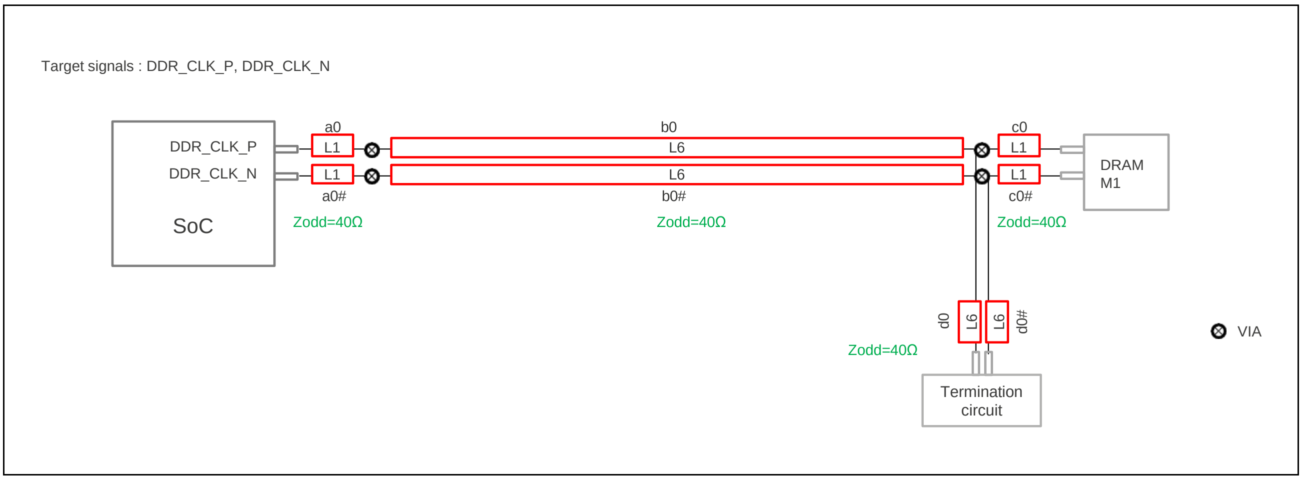
5.9.1 CLK topology

L1 and L6 in the figure below indicate the trace layers. a0 to d0# indicate the trace length. " ⊗ " are VIAs.

The odd mode impedance (Zodd) is equal to Zdiff/2. The clock traces Zodd should be 40Ω±10%.

Design the clock following the topology described in this figure.

1. CLK pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#
2. Keep 0.1mm or more between each signal traces.
3. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



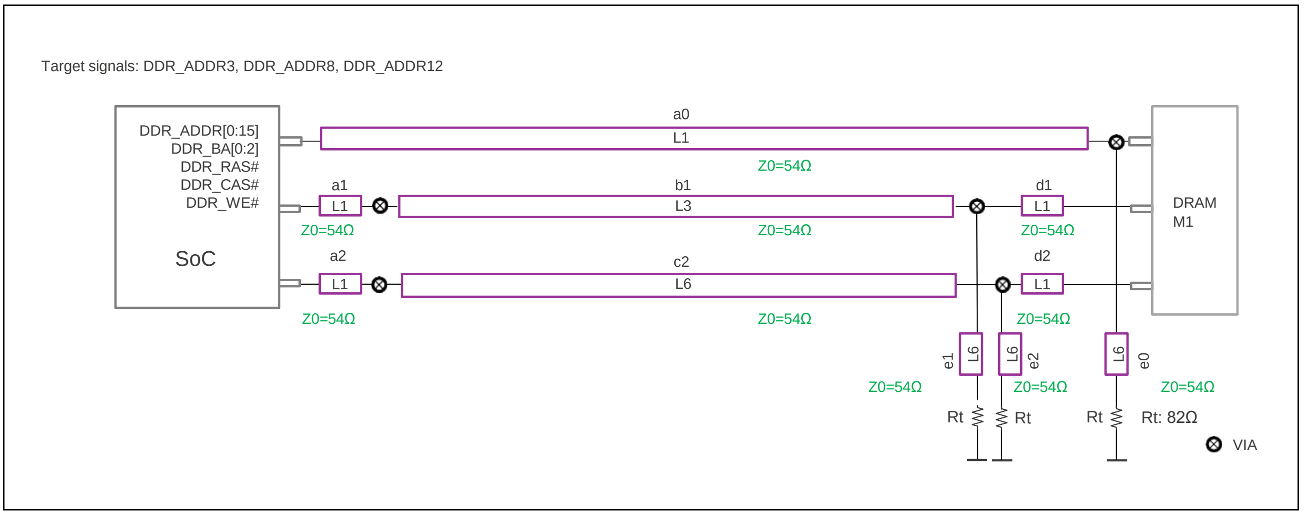
5.9.2 ADD/CMD topology

L1, L3 and L6 in the figure below indicate the trace layers. a0 to e2 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended, and their impedance (Z0) should be 55Ω±10%.

Design address and command signals following the topology described in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



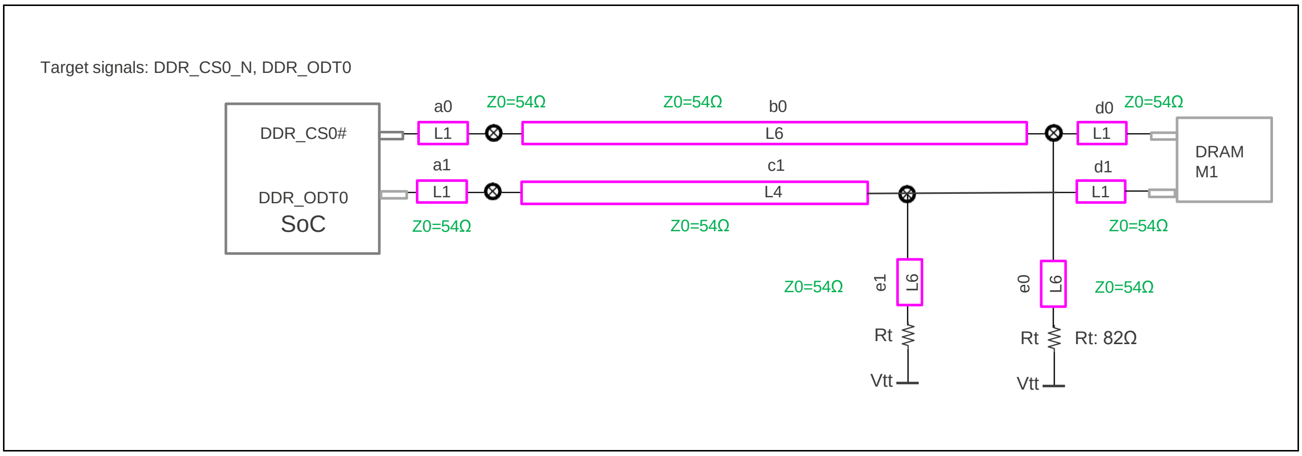
5.9.3 CTRL CS/ODT topology

L1 and L6 in the figure below indicate the trace layers. a0 to e0# indicate the trace length. “ ⊗ ” are VIAs.

Control signals are singled-ended, and their impedance (Z0) should be 55Ω±10%.

Design control signals following the topology described in this figure

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



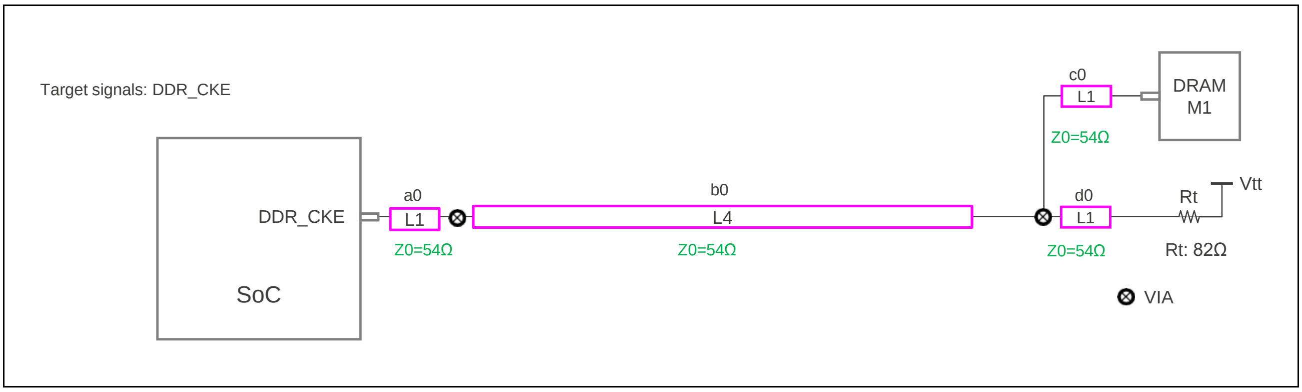
5.9.4 CTRL CKE topology

L1 and L6 in the figure below indicate the trace layers. a0 to d0 indicate the trace length. “ ⊗ ” are VIAs.

Control signals are singled-ended, and their impedance (Z0) should be 55Ω±10%.

Design control signals following the topology described in this figure

1. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



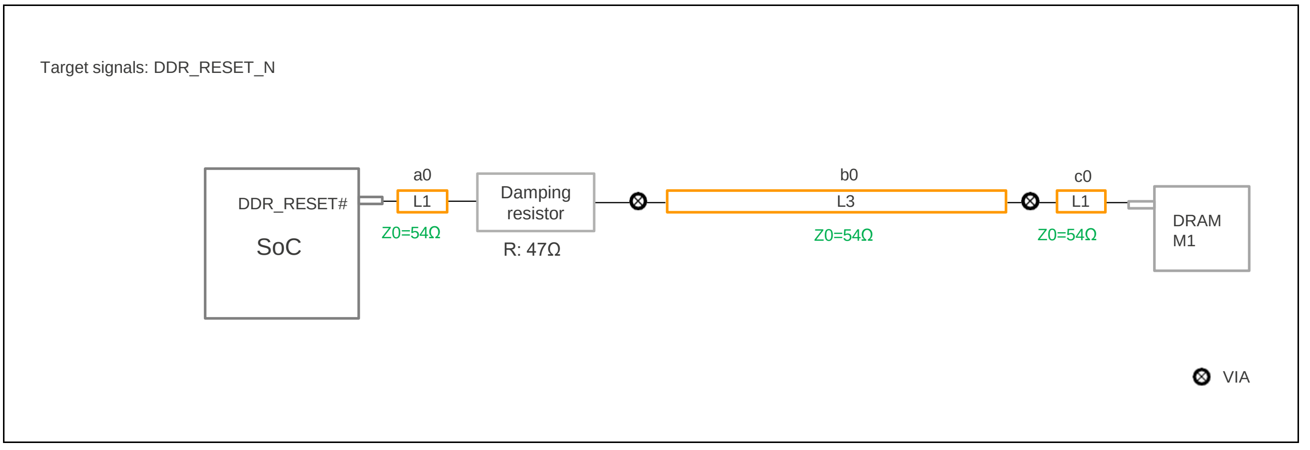
5.9.5 RESET topology

L1 and L3 in the figure below indicate trace layers. a0 to c0 indicate the trace length. “ ⊗ ” are VIAs.

The reset signal is single-ended, and his impedances (Z0) should be 55Ω±10%.

Design the wiring so that the wiring topology is as shown in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] from waveform restrictions specifications. (Mandatory)



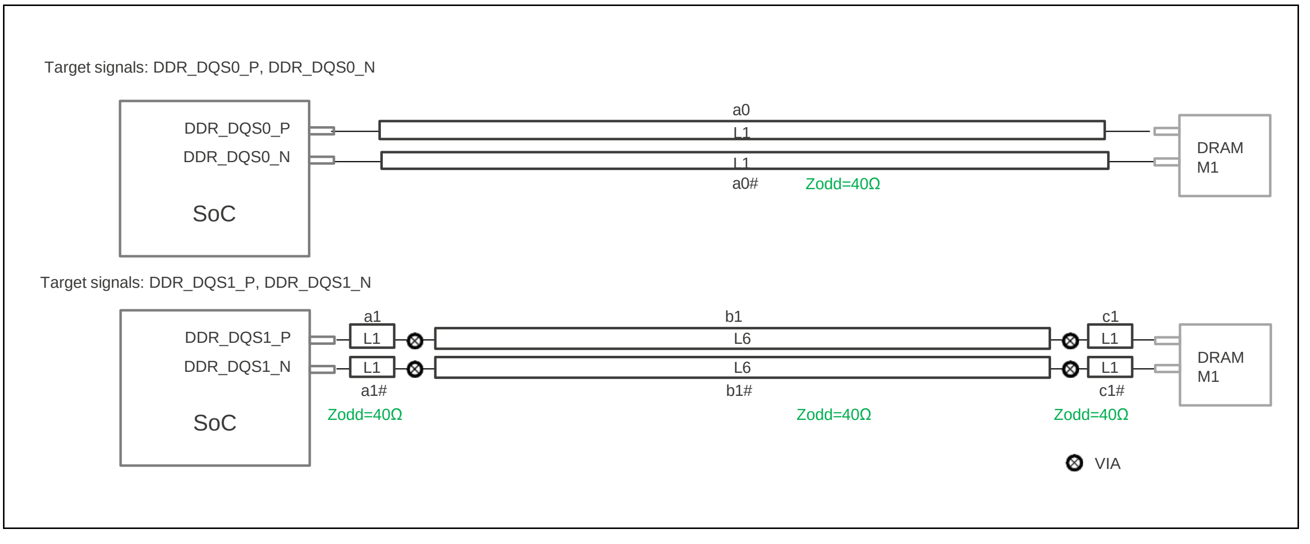
5.9.6 DQS0/1 topology

L1 and L6 int the figure below indicate the trace layers. a0 to c1# indicate the trace length. “ ⊗ ” are VIAs.

Zodd for DQS and DQS# traces should be 40Ω±10%.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#
2. Keep 0.1mm or more between each signal traces.
3. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



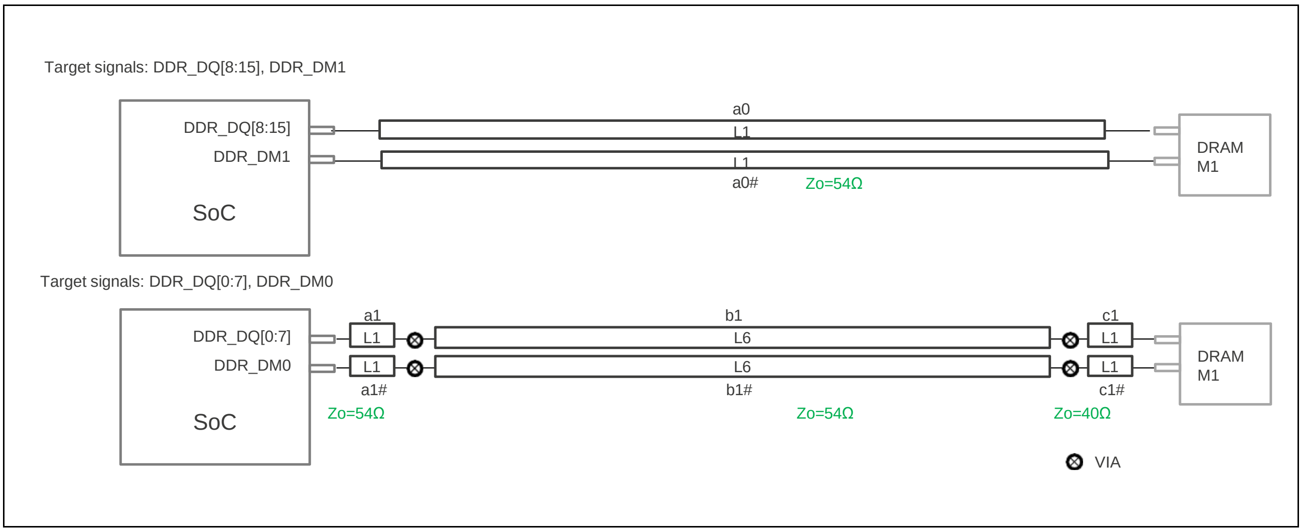
5.9.7 DQ_H/L topology

L1 and L6 int the figure below indicate the trace layers. a0 to c1# indicate the trace length. " ⊗ " are VIAs.

Z0 for DQ and DM should be 55Ω±10%.

Design the DQ following the topology described in this figure.

1. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



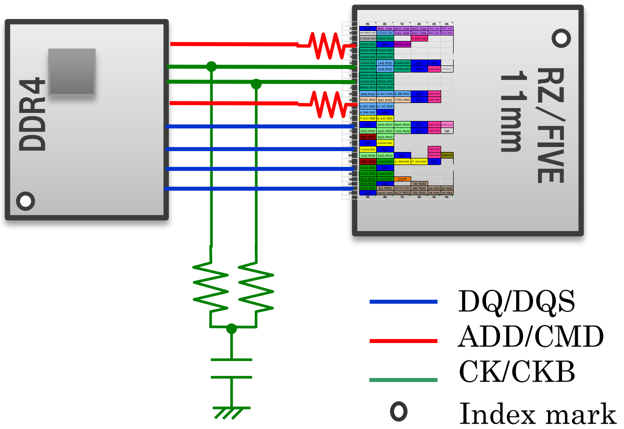
5.10 Topology T-11bv

System RANK: Single

8Gb: ×16 Single-Rank DDR4 SDRAM

Target Device: MT40A512M16TB-062E

PCB: 4layers / One to One / Top mounting



Signal	IO drive strength	VTT termination resistance	Termination resistance / Capacitance	Damping resistor	ODT termination resistance		
					SoC	DRAM Access side	DRAM Non-Access side
CLK	60Ω	—	47Ω × 2 / 0.1uF	—	—	—	—
CA (CMD, ADD)	60Ω	—	—	56Ω	—	—	—
CTRL (CS, ODT, CKE)	60Ω	—	—	10Ω	—	—	—
RESET	60Ω	—	—	120Ω	—	—	—
DQ, DQS (Write)	40Ω	—	—	—	OFF	60Ω	60Ω
DQ, DQS (Read)	34Ω	—	—	—	40Ω	OFF	OFF

5.10.1 CLK topology

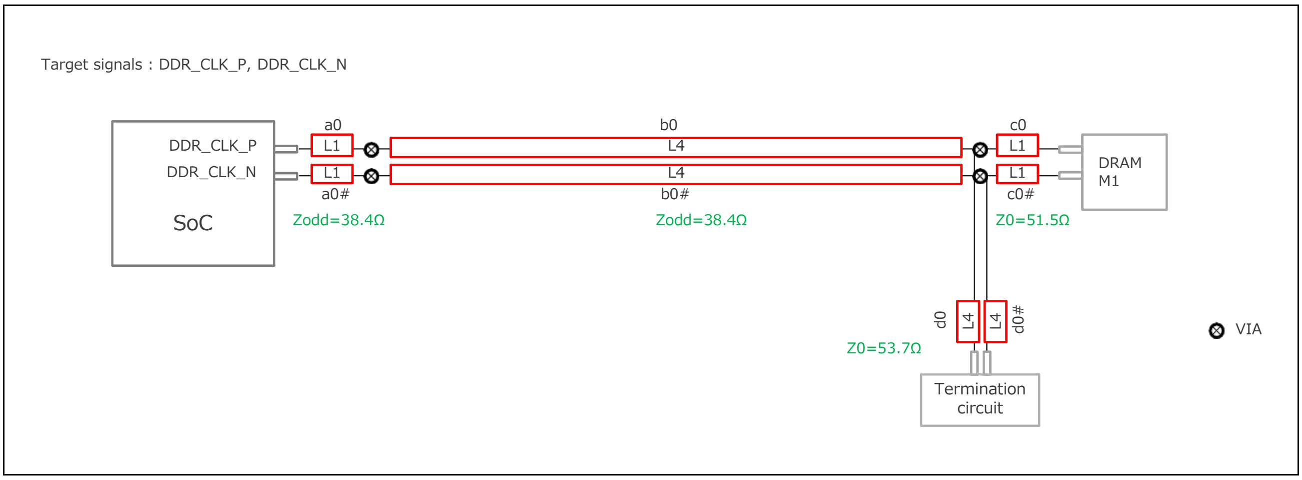
L1 and L4 in the figure below indicate the trace layers. a0 to d0# indicate the trace length. “ ⊗ ” are VIAs.

The odd mode impedance (Zodd) is equal to Zdiff/2. Keep 0.11mm signal trace width and 0.10mm or more between each signal traces.

Shield the differential pair trace of the L1 and L4 with GND planes running parallel on the left and right sides. The distance rom the GND shield should be 0.14mm. Be sure to connect the GND shield wires to the GND pins of the SoC and DRAM.

Design the clock following the topology described in this figure.

1. CLK pairs should be of equal length. → a0=a0#, b0=b0#, c0=c0#, d0=d0#
2. Keep 1.0mm or less for c0# connecting from the back surface to DRAM.
3. Keep 1.0mm or less for d0 and d0# at the termination.
4. Verify the layout using SI simulation. Check simulation results using [REF] timing and waveform restrictions specifications. (Mandatory)



5.10.2 ADD/CMD topology

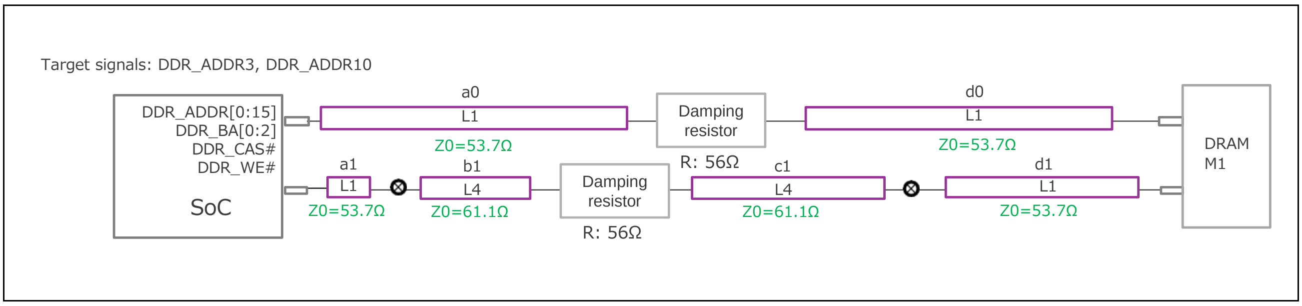
L1 and L4 in the figure below indicate the trace layers. a0 to d1 indicate the wiring length. " ⊗ " are VIAs.

Address and command signals are single-ended. Keep 0.10mm signal trace width.

Shield a signal trace with GND planes running parallel on the left and right sides. The distance rom the GND shield should be 0.10mm. Be sure to connect the GND shield wires to the GND pins of the SoC and DRAM.

Design address and command signals following the topology described in this figure.

1. Keep 6.5mm or less for d1 connecting from the back surface to DRAM.
2. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



5.10.3 CTRL CS/ODT/CKE topology

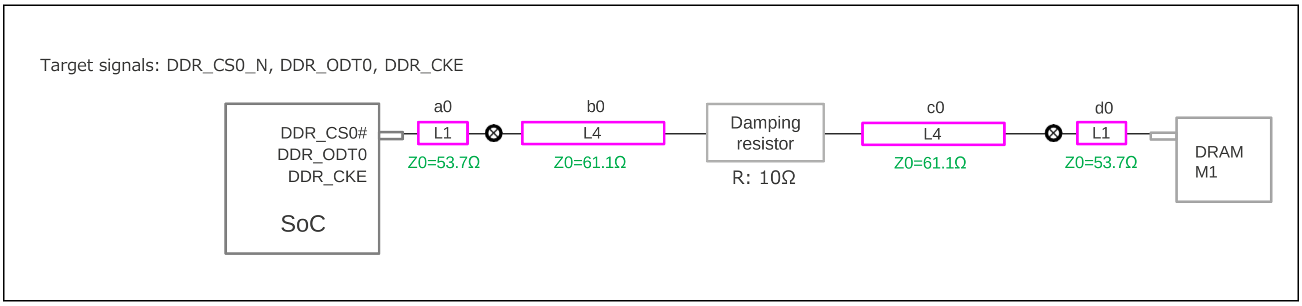
L1 and L4 in the figure below indicate the trace layers. a0 to d0 indicate the trace length. " ⊗ " are VIAs.

Control signals are singled-ended. Keep 0.10mm signal trace width.

Shield a signal trace of the L4 with GND planes running parallel on the left and right sides. The distance rom the GND shield should be 0.10mm. Be sure to connect the GND shield wires to the GND pins of the SoC and DRAM.

Design control signals following the topology described in this figure

1. Keep 1.8mm or less for d0 connecting from the back surface to DRAM.
2. Verify the layout using SI simulation. Check simulation results using [REF] from timing and waveform restrictions specifications. (Mandatory)



5.10.4 RESET topology

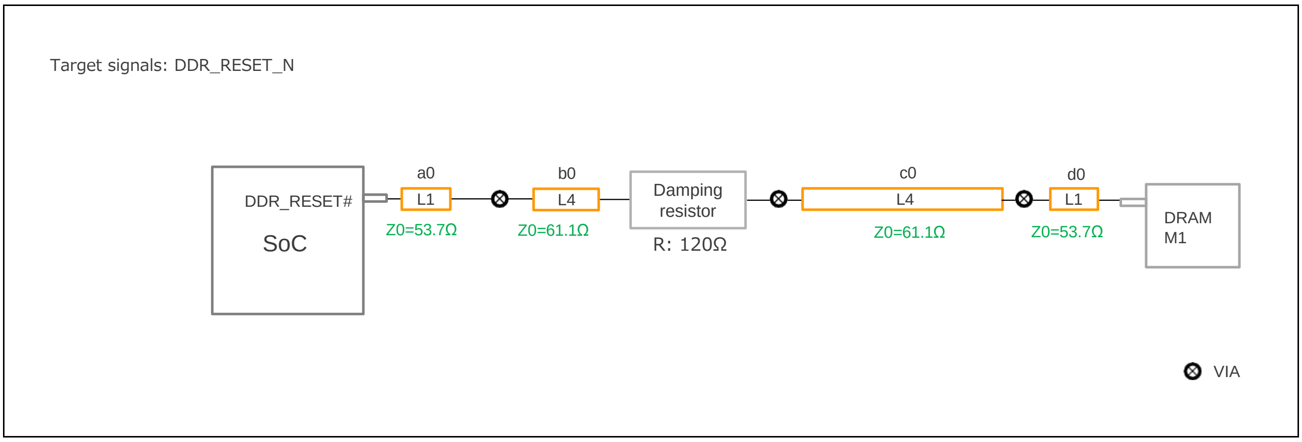
L1 and L4 in the figure below indicate trace layers. a0 to d0 indicate the trace length. " ⊗ " are VIAs.

The reset signal is single-ended. Keep 0.10mm signal trace width.

Shield a signal trace of the L4 with GND planes running parallel on the left and right sides. The distance rom the GND shield should be 0.10mm. Be sure to connect the GND shield wires to the GND pins of the SoC and DRAM.

Design the wiring so that the wiring topology is as shown in this figure.

1. The trace length to the DRAM should be less than 44.0mm.
   → a0+b0+c0+d0≤44
2. Keep a distance of 0.40mm or more from adjacent signal traces on the same layer. *Exclude the area around the drawer from the terminal.
3. Verify the layout using SI simulation. Check simulation results using [REF] from waveform restrictions specifications. (Mandatory)



5.10.5 DQS0/1 topology

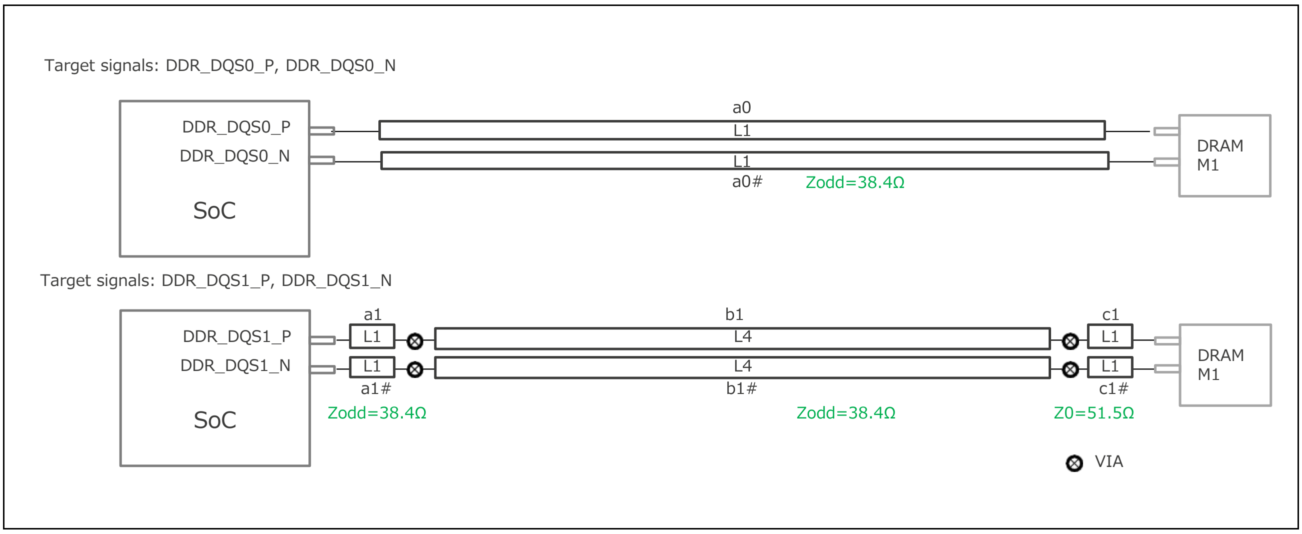
L1 and L4 int the figure below indicate the trace layers. a0 to c1# indicate the trace length. “ ⊗ ” are VIAs.

The odd mode impedance (Zodd) is equal to Zdiff/2. Keep 0.11mm signal trace width and 0.10mm or more between each signal traces.

Shield the differential pair trace of the L1 and L4 with GND planes running parallel on the left and right sides. The distance rom the GND shield should be 0.14mm. Be sure to connect the GND shield wires to the GND pins of the SoC and DRAM.

Design the DQS following the topology described in this figure.

1. DQS pairs should be of equal length. → a0=a0#, a1=a1#, b1=b1#, c1=c1#
2. Verify the layout using SI simulation. Check simulation results using [REF] skew, timing and waveform restrictions specifications. (Mandatory)



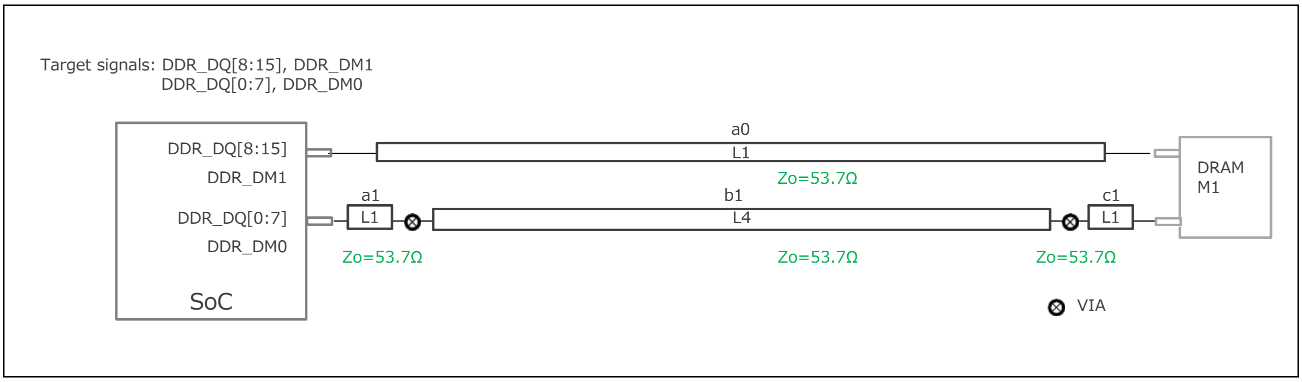
5.10.6 DQ_H/L topology

L1 and L4 int the figure below indicate the trace layers. a0 to c1 indicate the trace length. " ⊗ " are VIAs.

The DQ and DM signals are singled-ended. Keep 0.10mm signal trace width.

Design the DQ following the topology described in this figure.

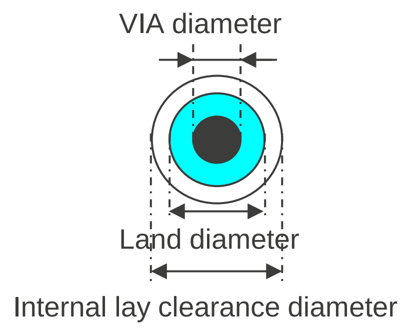
1. Verify the layout using SI simulation. Check simulation results using [REF] skew, timing and waveform restrictions specifications. (Mandatory)



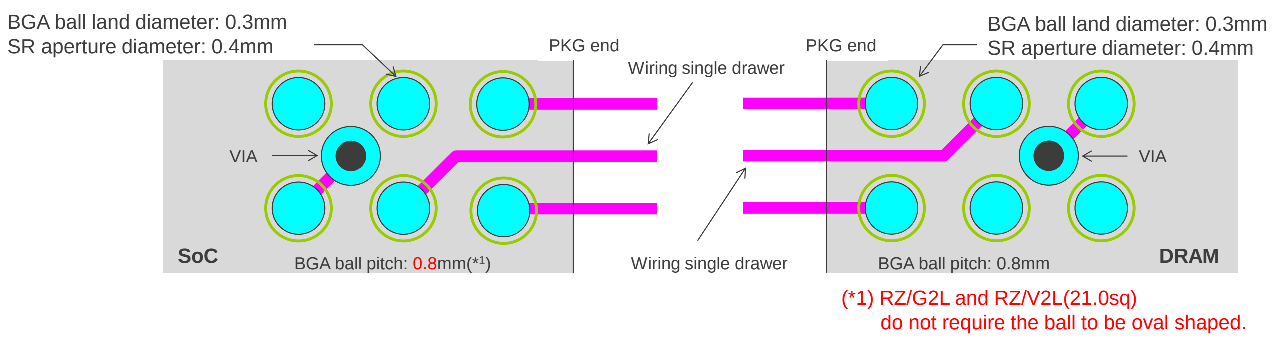
Appendix A Design rules for DDR4 of RZ/G2L and RZ/V2L(21.0sq)

Design rules for DDR4 of RZ/G2L and RZ/V2L(21.0sq)

- Target device
  RZ/G2L, RZ/V2L(21.0sq) – DDR4 SDRAM
- VIA specification
  VIA diameter: 0.2mm
  Physical hole diameter: 0.15mm
  Surface land diameter: 0.45mm
  Internal layer land diameter: 0.45mm
  Internal layer clearance diameter: 0.55mm



- Minimum wiring width
  0.1mm
- Minimum space
  Wiring - Wiring: 0.1mm
  Wiring - VIA: 0.1mm
  Wiring - BGA land: 0.1mm
  VIA - BGA land: 0.1mm
- BGA land diameter (PAD dimension)



REVISION HISTORY	RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five, RZ/A3UL PCB design guideline for DDR4/DDR3L

Rev.	Date	Description	
		Page	Summary
1.00	Oct 29, 2021	—	First edition released
1.01	Jan 07, 2022	All	RZ/G2UL product is added. Topology names are changed. <Chapter 1> Three topologies are added. A column "Product" is added. A column "Topology" is renamed. A column "SoC" is renamed to a column "PKG". A column "SoC/DDR Placement" is renamed to "SoC/DDR/Socket Placement" and added a socket to each topology. <Section 3.1><Section3.4> Figure is modified. <Section 3.2><Section 3.3><Section 3.5><Section 3.6> RZ/G2UL product is added. <Section 3.7> Three topologies are added. <Section 4.3> Terminal names are updated. <Chapter 5> Three topologies are added. <Section 5.1.2><Section 5.2.2><Section 5.3.2><Section 5.4.2><Section 5.4.3> <Section 5.5.2><Section 5.6.2><Section 5.6.3> Terminal names of ADD/CMD topology are updated. <Section 5.4.4> Terminal names of CTRL topology are updated.
1.02	Mar 25, 2022	All	RZ/Five product is added. <Chapter 1> One topology is added. A column "SoC/DDR/Socket Placement" is renamed to "SoC/DDR" and removed a socket to each topology. For a column "Targeted board", the description is changed from "Reference board" to "For Renesas Internal Evaluation Only". For the "Targeted board" of a topology "T-1vc", the description is changed from "RTK9754L23S00000BE" to "For Renesas Internal Evaluation Only (1)". <Section 3.2><Section 3.3><Section 3.5><Section 3.6> RZ/Five product is added. <Section 3.7> One topology is added. <Chapter 5> One topology is added. <Section 5.3> An impedance value of each topology is updated.
1.03	Apr 20, 2022	All	The topologies corresponds to "Dual" for a system rank and "1:2" for SoC to DDR connection is supported.
		12, 15	<Section 3.1, Section 3.4> The SoC to DDR connection is changed from “1:1” to “1:2”.
1.04	Jun 30, 2022	25	<Section 5.1> For the signal "CTRL" of a topology "T-1bc", the VTT termination resistance is changed from "47Ω" to "100Ω".

Rev.	Date	Description	
		Page	Summary
1.04	Jun 30, 2022	27	<Section 5.1.3> The VTT termination resistance of CTRL topology is changed from "47Ω" to "100Ω".
1.05	Jul 01, 2022	All	RZ/A3UL product is added.
1.06	Aug 03, 2022	25	<Section 5.1> For the signal "ADD/CMD" and “CTRL” of a topology "T-1bc", the VTT termination resistance is changed from "100Ω" to "82Ω" and a note is added. For the signal “RESET” of a topology "T-1bc", the damping resistance is changed from "47Ω" to "22Ω".
		26	<Section 5.1.2> The VTT termination resistance of ADD/CMD topology is changed from "100Ω" to "82Ω".
		27	<Section 5.1.3, Section 5.1.4> The VTT termination resistance of CTRL topology is changed from "100Ω" to "82Ω". The damping resistance of RESET topology is changed from "47Ω" to "22Ω".
		34	<Section 5.3> For the signal “RESET” of a topology "T-3bc", the damping resistance is changed from "47Ω" to "33Ω".
		36	<Section 5.3.4> The damping resistance of RESET topology is changed from "47Ω" to "33Ω".

RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five, RZ/A3UL
PCB design guideline for DDR4/DDR3L

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RZ/Five, RZ/A3UL

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