RZ/T2M, RZ/N2L Group Hardware Design Guide

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Introduction

This application note is a summary of the items serving as design points as reference materials for use when designing hardware which incorporates RZ/T2M and RZ/N2L Series LSIs.

Target Device

- RZ/T2M Group
- RZ/N2L Group

Trademark

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1. Power Supply

1.1 Power Supply

LSI of this series have the power supplies shown in **Table 1.1**.

- When designing a board, separate the digital power supply and the analog power supply as far away as possible to prevent switching noise from the digital power supply.
- Connect all power supply and ground pins. LSI operation is not guaranteed if there are open pins.

Table 1.1 Power Supply

Parameter	Symbol	Value	Min.	Typ.	Max.	Unit
Power supply voltages	VCC33		3.135	—	3.465	V
	VDD		1.05	1.1	1.15	V
	VSS		—	0	—	V
Power supply voltages supporting multi voltage mode	VCC1833_0, VCC1833_1, VCC1833_2, VCC1833_3, VCC1833_4	3.3V mode	3.135	3.3	3.465	V
		1.8V mode (VCC18)	1.70	1.8	1.95	V
Analog power supply voltages	VCC18_PLL0		—	VCC18	—	V
	VCC18_PLL1		—	VCC18	—	V
	VCC33_USB		—	VCC33	—	V
	VCC18_USB		—	VCC18	—	V
	AVCC18_USB		—	VCC18	—	V
	VCC18_ADC0		—	VCC18	—	V
	VCC18_ADC1		—	VCC18	—	V
	AVCC18_TSU		—	VCC18	—	V
	VSS_USB		—	0	—	V

Note: The 176LQFP and 128LQFP packages of the RZ/T2M products do not have pins VCC1833_n, VCC18_ADC1, and VREFH1. Also, the 121FBGA package of the RZ/N2L product does not have pins VCC33_USB, VCC18_USB, AVCC18_USB, VCC18_ADC0, VCC18_ADC1, VSS_USB.

1.2 Power On/Off Sequence

Power on/off sequence and timing are shown in the figure and table below.

For power-up, 1.1-V and 1.8-V power (i.e. VDD, VCC18, and AVCC) must be supplied first, then 3.3-V power (i.e.VCC33) must be supplied. The power-up sequence must be completed within 100 ms. Reset signal (i.e. RES#) must be held to Low level during the power-up.

For Power-down, 3.3-V power (i.e. VCC33) must go down first and then 1.1-V and 1.8-V power (i.e. VDD, VCC18, and AVCC). The power-down sequence must be completed within 100 ms.

Rise and fall time of each power supply for the power-up and the power-down must be larger than 10 μs.

Power supply voltages and reset signal must be applied with monotonic increase.

Do not apply a negative voltage to power supply voltages.

Stable clock must be supplied to EXTAL/XTAL or EXTCLKIN pin when reset signal (i.e. RES#) is driven high.

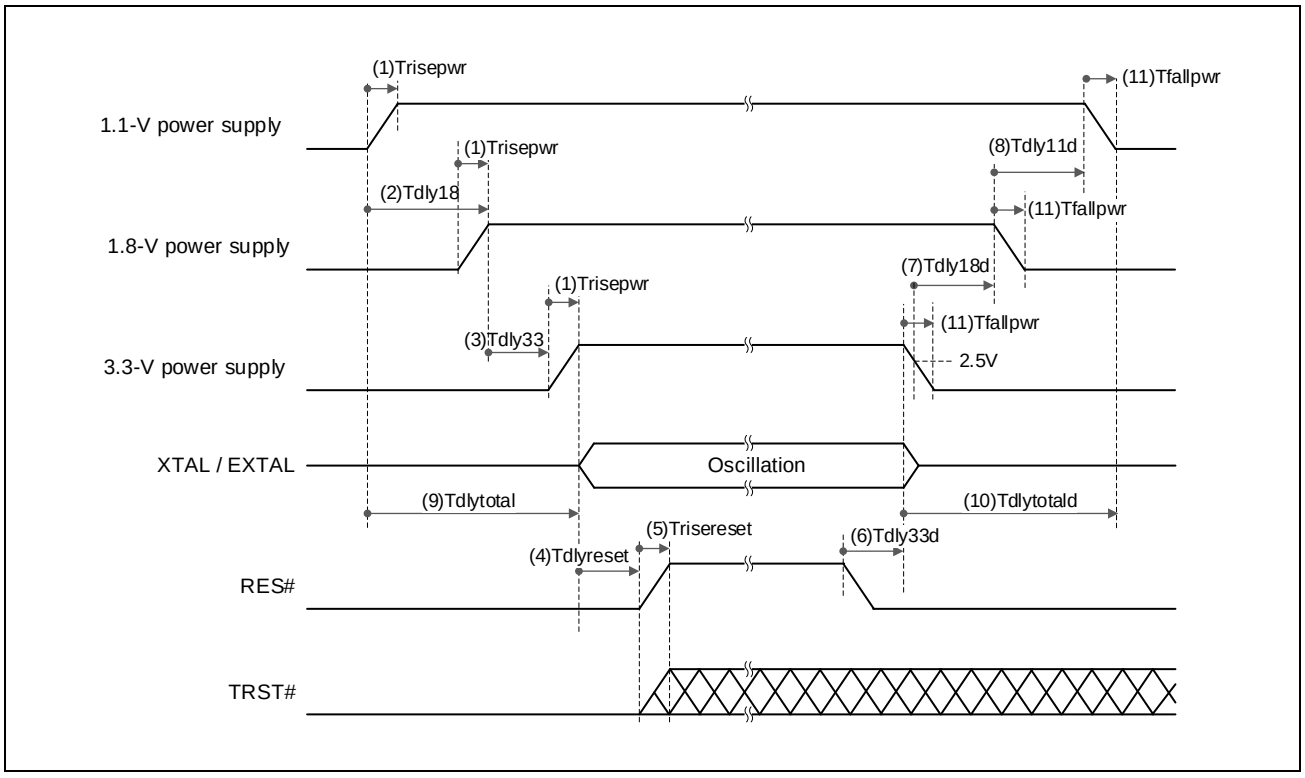

Figure 1.1 Power on/off sequence

Table 1.2 Power on/off sequence timing

No	Symbol	Description	Value		
			Min.	Typ.	Max.
(1)	Trisepwr	Rising time of the power supply voltage	10 µs	—	30 ms
(2)	Tdly18	Delay time from start of rising of the 1.1-V power supply voltage to completion of rising of the 1.8-V power supply voltage	0	—	100 ms
(3)	Tdly33	Delay time from completion of rising of the 1.8-V power supply voltage to start of rising of the 3.3-V power supply voltage	0	—	100 ms
(4)	Tdlyreset	Delay time from completion of rising of the 3.3V power supply voltage to start of rising of RES#	10 ms	—	—
		Delay time from completion of rising of the 3.3-V power supply voltage to start of rising of RES# when EXTCLKIN is used.	1 ms		
(5)	Trisereset	Rising time of RES#	—	—	150 µs
(6)	Tdly33d	Delay time from start of falling of RES# to start of falling of the 3.3-V power supply voltage	10 µs	—	
(7)	Tdly18d	Delay time from start of falling of the 3.3-V power supply voltage to start of falling of the 1.8-V power supply voltage	0	—	100 ms
(8)	Tdly11d	Delay time from start of falling of the 1.8-V power supply voltage to start of falling of the 1.1-V power supply voltage	0	—	100 ms
(9)	Tdlytotal	Startup time of all power supply voltage	—	—	100 ms
(10)	Tdlytotald	Shut down time of all power supply voltage	—	—	100 ms
(11)	Tfallpwr	Falling time of the power supply voltage	10 µs		30 ms

2. Operating Mode

2.1 Overview

The LSI is intended for booting up from an external flash memory. Boot modes are available for the types of flash memory that supports multiple operating modes. In each of the boot modes, the user program stored in the corresponding external flash memory is booted up and runs. Secure boot mode (in which a user program is protected by encryption) can also be selected for the products that support security functions.

2.2 Boot mode setting (MDn)

One types of operating modes can be selected, depending on the method of connecting to an external flash memory and device. An operating mode is selected based on the input levels of the mode setting pins (MD2, MD1, and MD0) when pin reset (except software reset) is released.

Table 2.1 describes the relationship between the input levels of the mode setting pins (MD2, MD1, and MD0) at the time reset is released and the selected operating mode. Value of the pins (MD2 to MD0) are latched to the registers when reset is released.

Table 2.1 MDn setting pin setting for RZ/T2M

Mode setting pins			
MD2	MD1	MD0	Operating mode
Low	Low	Low	xSPI0 boot mode (x1 boot serial flash) Boots a program from x1 boot serial flash memory connected to the xSPI0 CS0 space. Supporting voltage (3.3 V or 1.8 V*1)
Low	Low	High	xSPI0 boot mode (x8 boot serial flash) *2 Boots a program from x8 boot serial flash memory such as HyperFlash™ memory connected to the xSPI0 CS0 space. Supporting voltage (3.3 V or 1.8 V*1)
Low	High	Low	16-bit bus boot mode (NOR flash) Boots a program from a NOR flash memory (bus width: 16 bits) connected to the CS0 space.
Low	High	High	32-bit bus boot mode (NOR flash) *3 Boots a program from a NOR flash memory (bus width: 32 bits) connected to the CS0 space.
High	Low	Low	xSPI1 boot mode (x1 boot serial flash) *4 Boots a program from x1 boot serial flash memory connected to the xSPI1 CS0 space. Supporting voltage (3.3 V or 1.8 V*5)
High	Low	High	SCI (UART) boot mode Boots a program from host PC through UART communication connected to the SCI0. For flash writer use.
High	High	Low	USB boot mode Boots a program from host PC through USB. For flash writer use.
High	High	High	Reserved (setting prohibited)

Note 1. 1.8 V is supported on 320 FBGA and 225 FBGA.

Note 2. This boot mode is not supported on 176 and 128 LQFP.

Note 3. This boot mode is not supported on 128 LQFP.

Note 4. This boot mode is not supported on 225 FBGA.

Note 5. 1.8 V is supported on 320 FBGA only.

Table 2.2 MDn setting pin setting for RZ/N2L

Mode setting pins			
MD2	MD1	MD0	Operating mode
Low	Low	Low	xSPI0 boot mode (x1 boot serial flash) Boots a program from x1 boot serial flash memory connected to the xSPI0 CS0 space. Supporting voltage (3.3 V or 1.8 V*1)
Low	Low	High	xSPI0 boot mode (x8 boot serial flash) *2 Boots a program from x8 boot serial flash memory such as HyperFlash memory connected to the xSPI0 CS0 space. Supporting voltage (3.3 V or 1.8 V)
Low	High	Low	16-bit bus boot mode (NOR flash) *2 Boots a program from a NOR flash memory (bus width: 16 bits) connected to the CS0 space.
Low	High	High	Serial host interface boot mode Boots a program downloaded from an external host CPU connected to SHOSTIF. Supporting voltage (3.3 V or 1.8 V*1)
High	Low	Low	Parallel host interface boot mode*2 Boots a program downloaded from an external host CPU connected to PHOSTIF.
High	Low	High	SCI (UART) boot mode Boots a program from host PC through UART communication connected to the SCI0. For flash writer use.
High	High	Low	USB boot mode*2 Boots a program from host PC through USB. For flash writer use.
High	High	High	xSPI1 boot mode (x1 boot serial flash) *2 Boots a program from x1 boot serial flash memory connected to the xSPI1 CS0 space. Supporting voltage (3.3 V or 1.8 V)

Note 1. 1.8 V is supported on 225 FBGA.

Note 2. This boot mode is not supported on 121 FBGA.

2.3 Operating voltage of I/O domain (MDVn)

As shown in **Table 1.1** in Chapter 1, this LSI has five power supply domains (VCC1833_0 to VCC1833_4), and 3.3V or 1.8V can be selected according to the intended use.

Table 2.3 and **Table 2.4** shows the list of MDVn pins. Set the input level of the voltage setting pins (MDV4 to MDV0) according to the voltage setting of each power supply domain (I/O domain 0 to 4). Otherwise, it may cause malfunctions or permanent damage to the device.

Table 2.3 List of MDVn pins for RZ/T2M

I/O Voltage Setting pins	Power Voltage	Operating voltage of I/O domain *1		Pin number		Pin name
		320FBGA	225FBGA	320FBGA	225FBGA	
MDV0	VCC1833_0	1.8V or 3.3V	1.8V or 3.3V	C11	B9	P20_1 / ETHSW_TDMAOUT0 / ESC_LINKACT0
MDV1	VCC1833_1	1.8V or 3.3V	1.8V or 3.3V	A10	D8	P20_2 / ETHSW_TDMAOUT1 / ESC_LEDRUN / ESC_LEDSTER / DE3
MDV2	VCC1833_2	1.8V or 3.3V	1.8V or 3.3V	C9	D9	P20_3 / ETHSW_TDMAOUT2 / ESC_LEDERR
MDV3	VCC1833_3	1.8V or 3.3V	1.8V or 3.3V	B10	A9	P20_4 / ETHSW_TDMAOUT3 / ESC_LINKACT1
MDV4	VCC1833_4	1.8V or 3.3V	3.3V*2	D20	B15	P19_0 / USB_VBUSEN

Note 1. The 176LQFP and 128LQFP products do not have I/O domains and operating IO voltage is fixed to 3.3 V.

Note 2. The 225FBGA products have MDV4 pin, but the operating I/O voltage is fixed to 3.3 V regardless of the MDV4 value.

Table 2.4 List of MDVn pins for RZ/N2L

I/O Voltage Setting pins	Power Voltage	Operating voltage of I/O domain*1		Pin number		Pin name
		225FBGA	121FBGA	225FBGA	121FBGA	
MDV0	VCC1833_0	1.8V or 3.3V	3.3V*1	B9	B9	P20_1 / ETHSW_TDMAOUT0 / ETHSW_PTPOUT3 / ESC_LINKACT0
MDV1	VCC1833_1	1.8V or 3.3V	1.8V or 3.3V	D8	B8	P20_2 / ETHSW_TDMAOUT1 / ETHSW_PTPOUT2 / ESC_LEDRUN / ESC_LEDSTER / DE3
MDV2	VCC1833_2	1.8V or 3.3V	1.8V or 3.3V	D9	C8	P20_3 / ETHSW_TDMAOUT2 / ETHSW_PTPOUT1 / ESC_LEDERR
MDV3	VCC1833_3	1.8V or 3.3V	3.3V*1	A9	A10	P20_4 / ETHSW_TDMAOUT3 / ETHSW_PTPOUT0 / ESC_LINKACT1
MDV4	VCC1833_4	1.8V or 3.3V	3.3V*2	B15	—	P19_0 / USB_VBUSEN

Note 1. The 121FBGA products have MDV0 and MDV3 pin, but the operating I/O voltage is fixed to 3.3 V regardless of the MDV0 and MDV3 value.

Note 2. The 121FBGA products do not have MDV4 pin and operating IO voltage is fixed to 3.3 V.

Table 2.5 shows the selection of operating voltage of I/O domain 0 to 4. Value of the pins (MDV4 to MDV0) are latched to the registers when reset is released. Depending on the selected I/O domain voltage, add a pull-up or pull-down resistor to the MDVn pin. Do not change the signal level of this pin during the transition of the operation mode after reset release.

Table 2.5 Selection of operating voltage of I/O domain 0 to 4 (MDV4 to MDV0)

Operation voltage of I/O domain n VCC1833_n (n = 0 to 4)	MDVn (n= 0 to 4)
1.8V	Low (Place a pull-down resistor between MDVn and VSS)
3.3V	High (Place a pull-up resistor between MDVn and VCC33)

Appropriate voltage level (VIHH33, VLI33) that satisfies **Table 2.6** must be input to the MDVn pin, and it must satisfy the mode hold time shown in **Table 2.7**, until the operation mode transition is completed after the reset is released.

Table 2.6 Input level voltage

Item	Symbol	Condition	Min	Typ	Max	Unit
Input High-level voltage	V_{IH33}		2.0	—	VCC+0.3	ns
Input Low-level voltage	V_{IL33}		-0.3	—	0.8	

Table 2.7 Mode hold time

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Mode hold time (From RES#)	t_{MDH}		250	—	—	ns

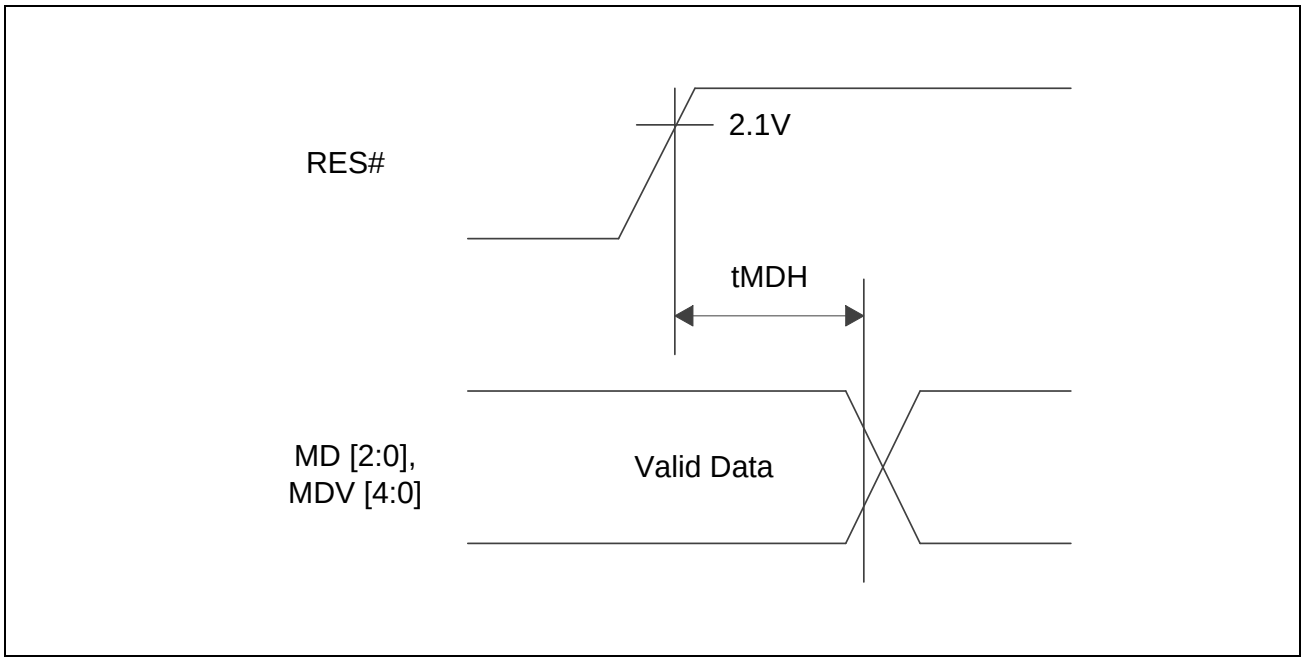

Figure 2.1 Mode input timing

2.3.1 Supporting EtherCAT

As shown in **Table 2.3** and **Table 2.4**, the MDV0 to MDV3 pins are also used as LED pins for EtherCAT.

Therefore, when designing a circuit configuration that uses EtherCAT, the LED control circuit must be considered the MDVn mode transition time and MDVn input voltage when reset is released. Even if EtherCAT is not used, be careful of the MDVn input level when reset is released when using the MDVn pin in a mode other than the operation mode setting.

(1) Example of MDVn circuit for Low setting

Figure 2.2 shows an example of MDVn.circuit for Low setting. The mode setting voltage of the MDVn pin is input between the pull-down resistor R2. When the mode transition is completed and the main program starts, LED1 is controlled.

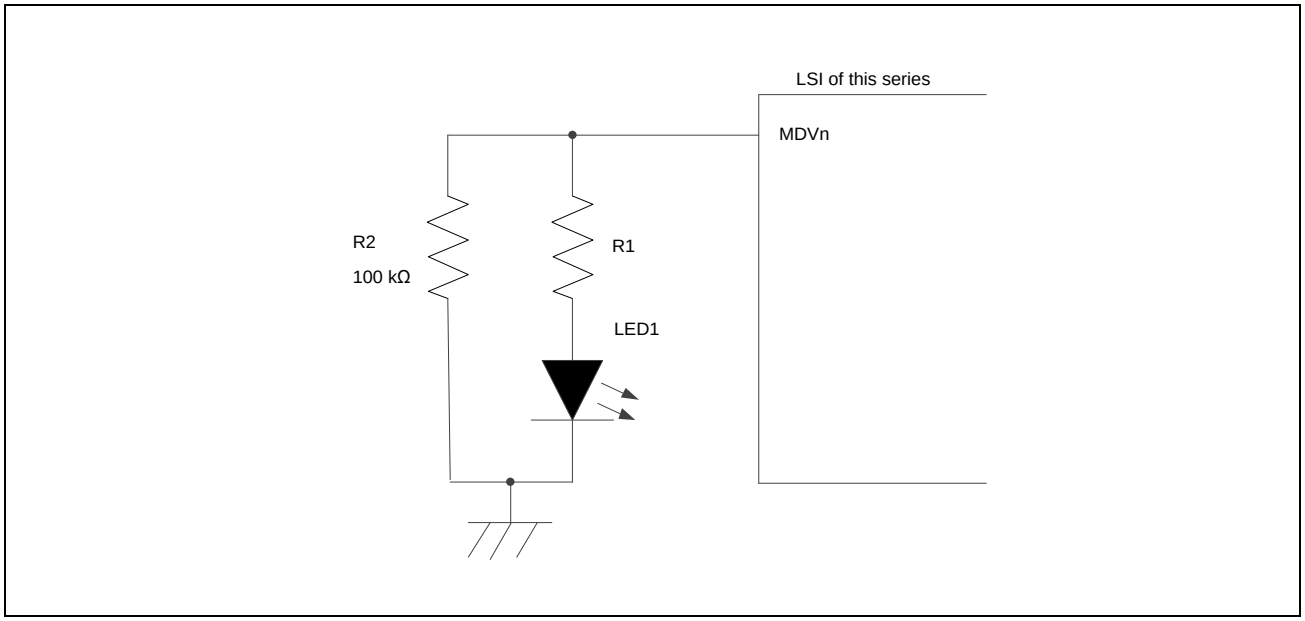

Figure 2.2 Example of the circuit for MDVn = Low (1.8 V) setting

(2) Example of MDVn circuit for High setting

Figure 2.3 shows an example MDVn circuit for High setting, and **Figure 2.4** shows an example timing chart for this circuit example. In this circuit example, during reset (RESET# = Low), SPDT (Single Pole Double Throw) switch S1 is on, S2 is off, and MDVn is pulled high by pull-up resistor R3.

When the reset is released, after a hold time tMDH of 250 ns (minimum) or more is secured by the tMDH time constant of R6 and Cd, S1 turns off, S2 turns on, and the MDVn terminal switches to the LED circuit side.

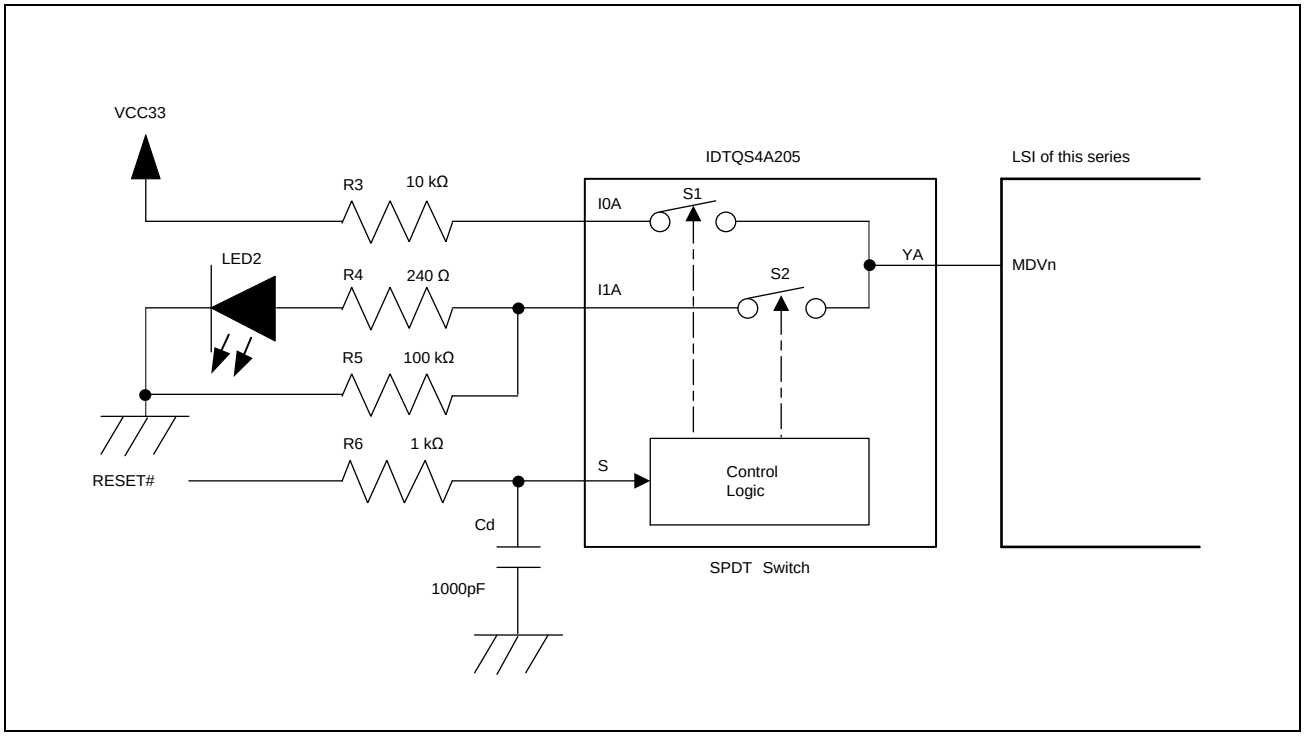

Figure 2.3 Example of the circuit for MDVn = High (3.3 V) setting

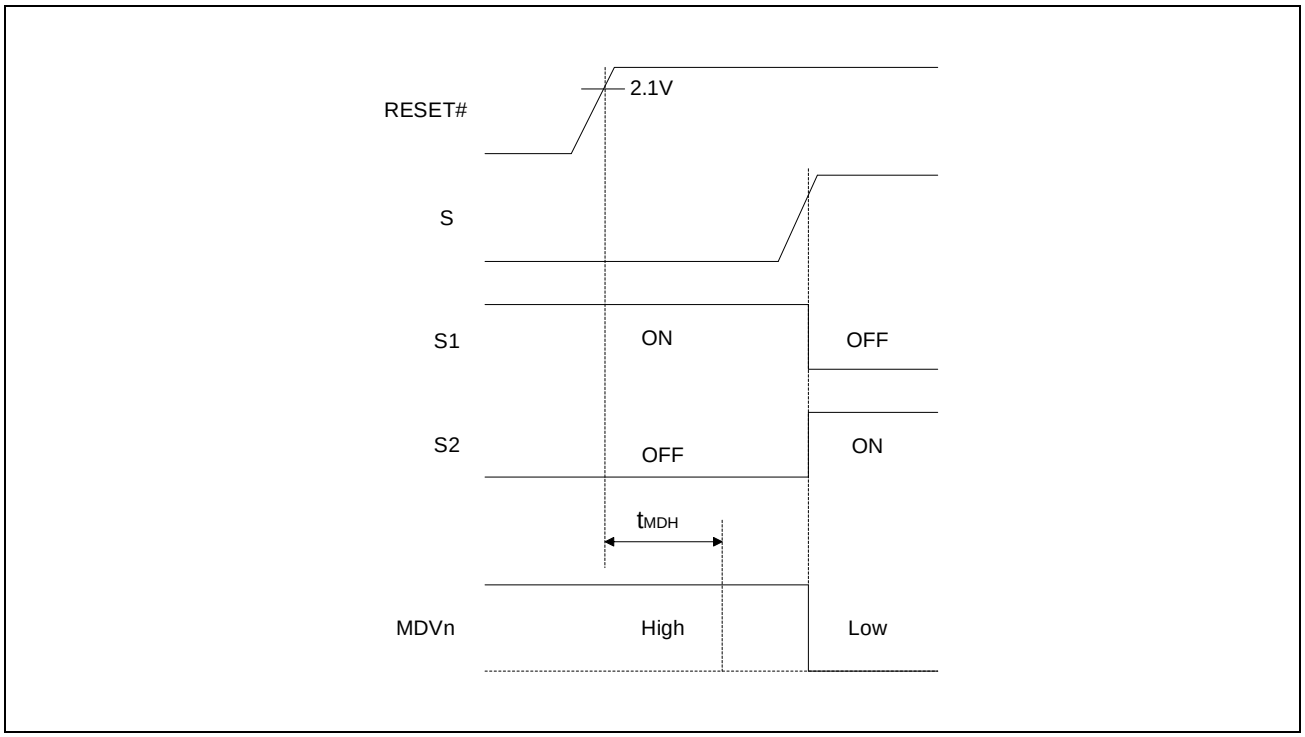

Figure 2.4 MDVn circuit timing chart for MDVn = High setting

3. Oscillator Circuit

3.1 Clock Pins

RZ/T2M and RZ/N2L have some method of inputting an external clock and a method of connecting a crystal oscillator as a main clock oscillator.

Table 3.1 shows pins to which a crystal resonator can be connected to, or a clock as input, and their frequencies.

Table 3.1 Clock Pins

Xin Pin	Xout Pin	Description	Conditions	Frequency
EXTAL	XTAL	EXTAL clock input frequency	—	25.00 MHz ± 50ppm
			EtherCAT in use	25.00 MHz ± 25ppm

3.2 Example of External Clock Connection

Figure 3.1 shows an example of connection of external clock input. Connect EXTAL to VSS via a resistor and leave XTAL open. If a crystal oscillator is used, it should be placed as close as possible to the EXTCLKIN pin. The GND traces used for shielding should be at least 0.3 mm wide and there should be a space of 0.3 mm to 2.0 mm between them and adjacent traces.

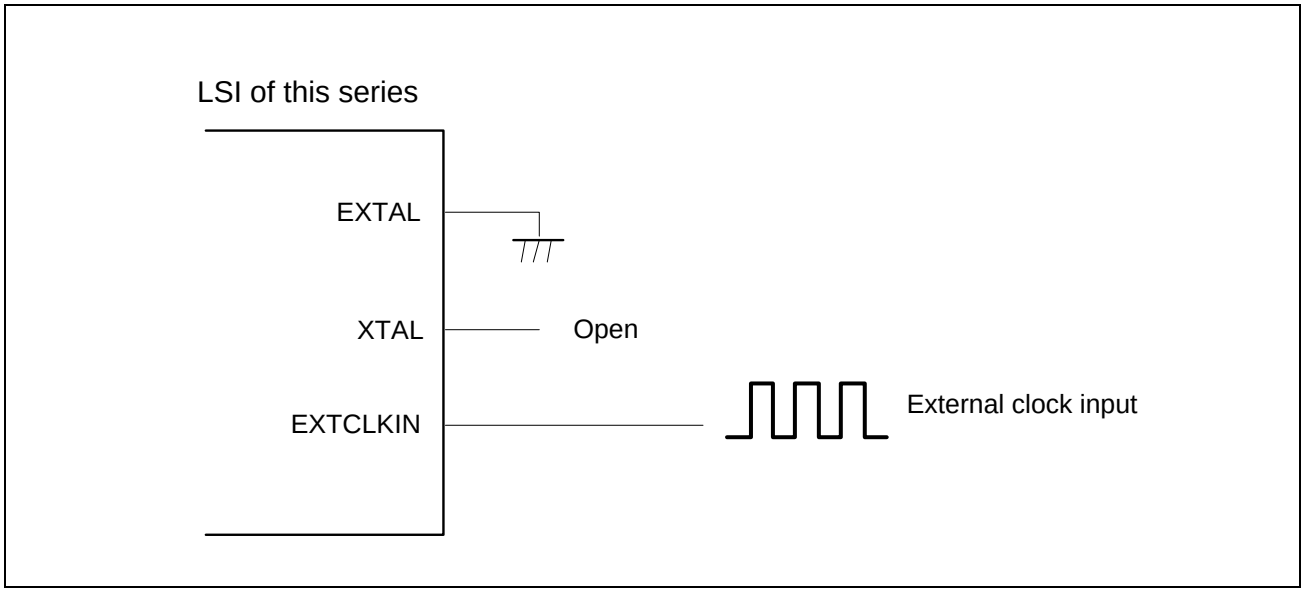

Figure 3.1 Example of external clock connection

3.3 Example of Crystal Resonator Connection

Figure 3.2 shows an example of a crystal resonator connection.

It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors Rf and Rd in case they are required for proper oscillator operation when combined with crystal circuit components.

The RZ/T2M series LSI's have a built-in feedback resistor Rif, so basically there is no need to mount an external feedback resistor Rf. Also, 0 Ω is recommended for the limiting resistance Rd, so it is not necessary to implement it on the PCB.

However, depending on crystal characteristics, an optional external resistor (Rd or Rf) may be required.

Also, the CL1 and CL2 constants shown in **Figure 3.2** are reference values, and the optimum values differ depending on the oscillator characteristics.

Therefore, if you need the optimum oscillator circuit constants for your system, please contact your crystal oscillator manufacturer.

Finally, these resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

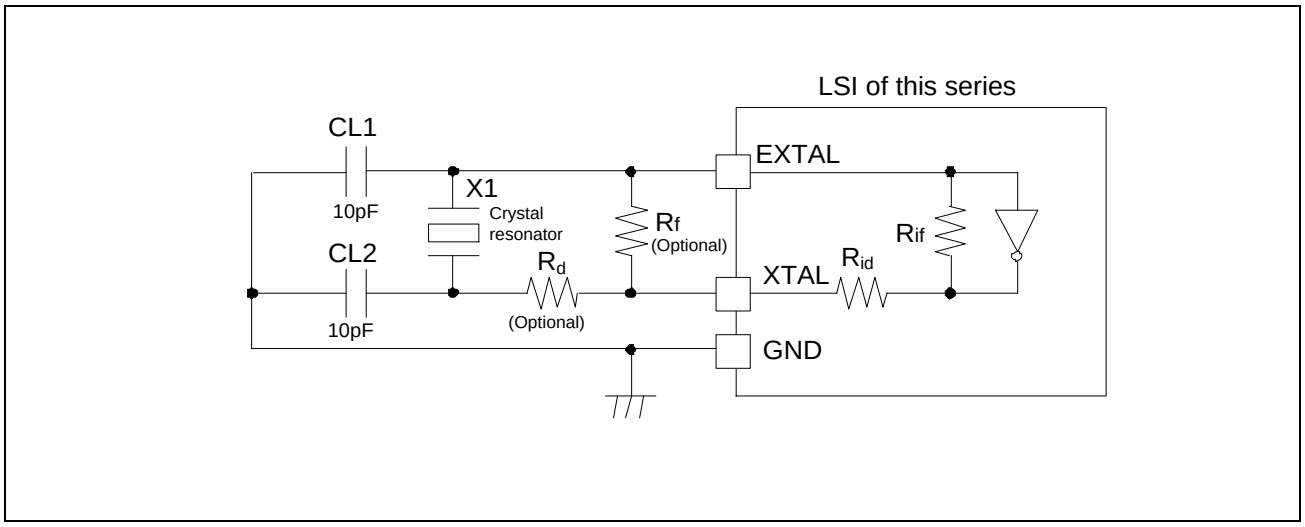

Figure 3.2 Example of crystal resonator connection

3.3.1 Example of P.C.B Layout

This chapter shows a P.C.B layout example of the crystal oscillator peripheral circuit.

If noise enters the clock I/O pins, the clock waveforms may become distorted, possibly causing an MCU malfunction or program runaway.

In addition, accurate clock signals cannot be input to the MCU if there is a potential difference between the VSS inputs to the MCU and oscillators.

Figure 3.3 shows an example PCB layout Layer1 for the crystal connection.

Please note the following points:

- The crystal resonator and capacitors CL1 and CL2 should be placed as close as possible to the Xin (EXTAL) pin and the Xout (XTAL) pin.
- To avoid inductance and to oscillate properly, use a common grounding point for the resonator and additional capacitors, and do not place wiring patterns near these parts.
- Shield the wiring pattern for the clock I/O pins with the GND pattern of the crystal resonator and do not arrange the traces for the clock I/O pins in parallel with or across other traces that have large current flows or rapid level changes.
- The GND traces used for shielding should be at least 0.3 mm wide and there should be a space of 0.3 mm to 2.0 mm between them and adjacent traces.

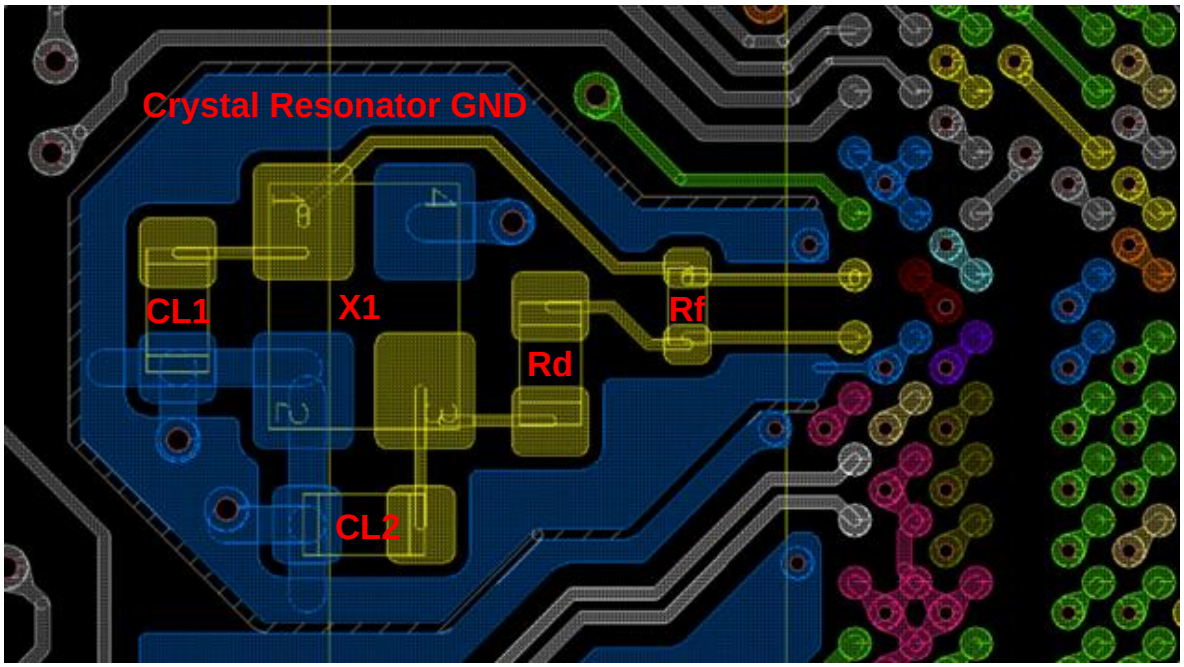

Figure 3.3 Example layout of the first layer (Layer1) of the P.C.B.

Figure 3.4 shows a layout example of the second layer (Layer2) of the PCB.

Pattern wiring to other layers in the area where the crystal oscillator peripheral circuit is arranged is prohibited because it affects other GND and signals. Be sure to make the second layer of the crystal oscillator peripheral circuit the GND of the crystal oscillator peripheral circuit. Also, it is recommended that the third layer be a digital GND (DGND).

- Separate the oscillator circuit GND from the digital GND(DGND).
- Connect the oscillation circuit GND at one point with the GND near the LSI.

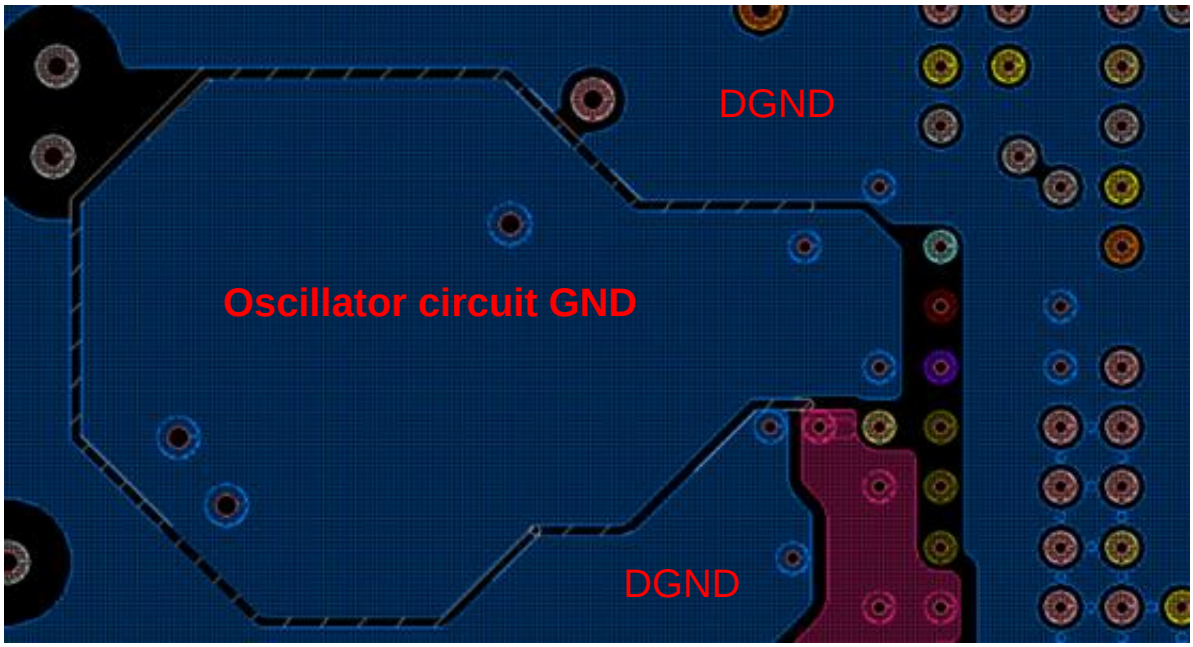

Figure 3.4 Example layout of the second layer (Layer2) of the P.C.B.

Figure 3.5 shows an example of the third layer of the P.C.B. The third layer is DGND, but the through-holes for the oscillation circuit GND are separated so that they do not become a common GND.

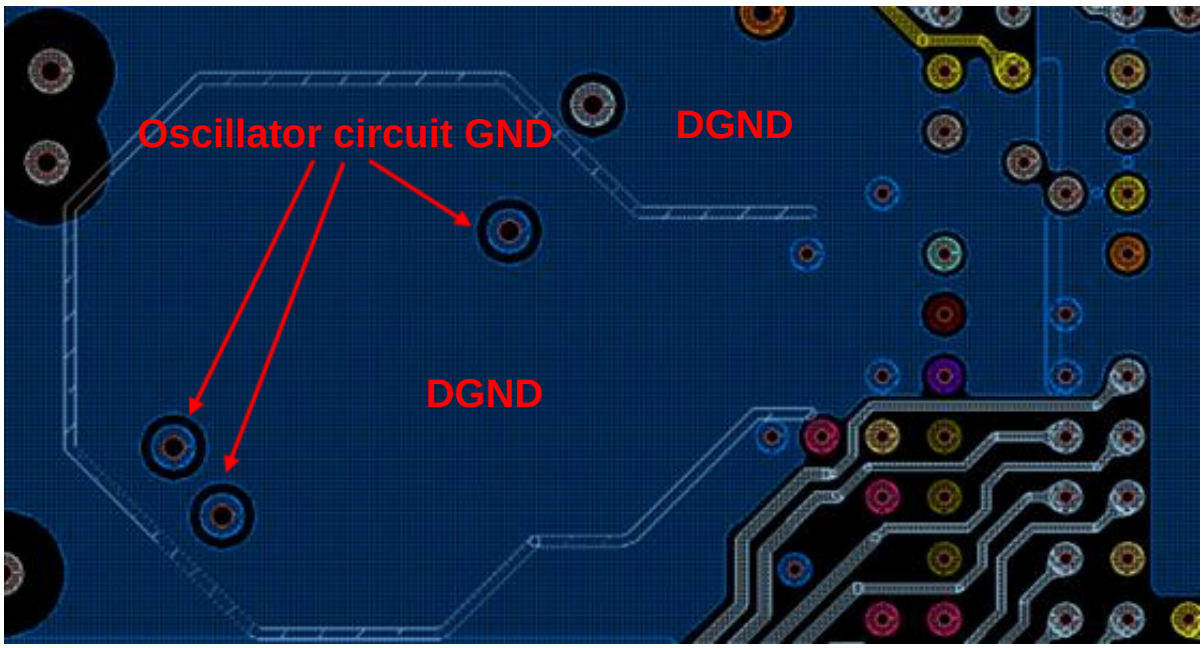

Figure 3.5 Example layout of the third layer (Layer3) of the P.C.B.

4. Flash Memory

4.1 xSPI n (n = 0, 1) boot mode (x1boot serial flash mode)

This series of LSIs has an xSPI controller built-in and is designed so that external serial flash can be booted in either xSPI0 boot or xSPI1 boot (x1 boot serial flash) mode. At startup, the serial flash is accessed in protocol mode 1S-1S-1S and the system software is reset. Please refer to **Table 2.1** and **Table 2.2** for this boot mode setting.

After the reset is released, processing is executed immediately after boot processing starts in xSPI n (n = 0, 1) boot mode (x1 boot serial flash) until the loader parameters are transferred.

NOTE

At x1 boot serial flash mode, if the serial flash protocol mode is switched from 1S-1S-1S to another mode by the application program, it is necessary to pay attention to the serial flash protocol mode setting after reset. If only this LSI is reset, then serial flash cannot receive the 1S command at boot time and cannot boot normally. We will explain the countermeasures below.

4.1.1 For serial flash with hardware reset

When changing the serial flash protocol mode to other than 1S-1S-1S by application program, implement the following software and hardware countermeasures.

(1) Switch the serial flash protocol mode to 1S-xx-xx (the command is 1S mode) before software reset.

(2) Apply a hardware reset to the serial flash when the system is reset.

Figure 4.1 shows a connection example of a Quad serial flash with a reset pin. A hardware reset to the Quad serial flash will also reset the protocol mode setting for the quad serial flash.

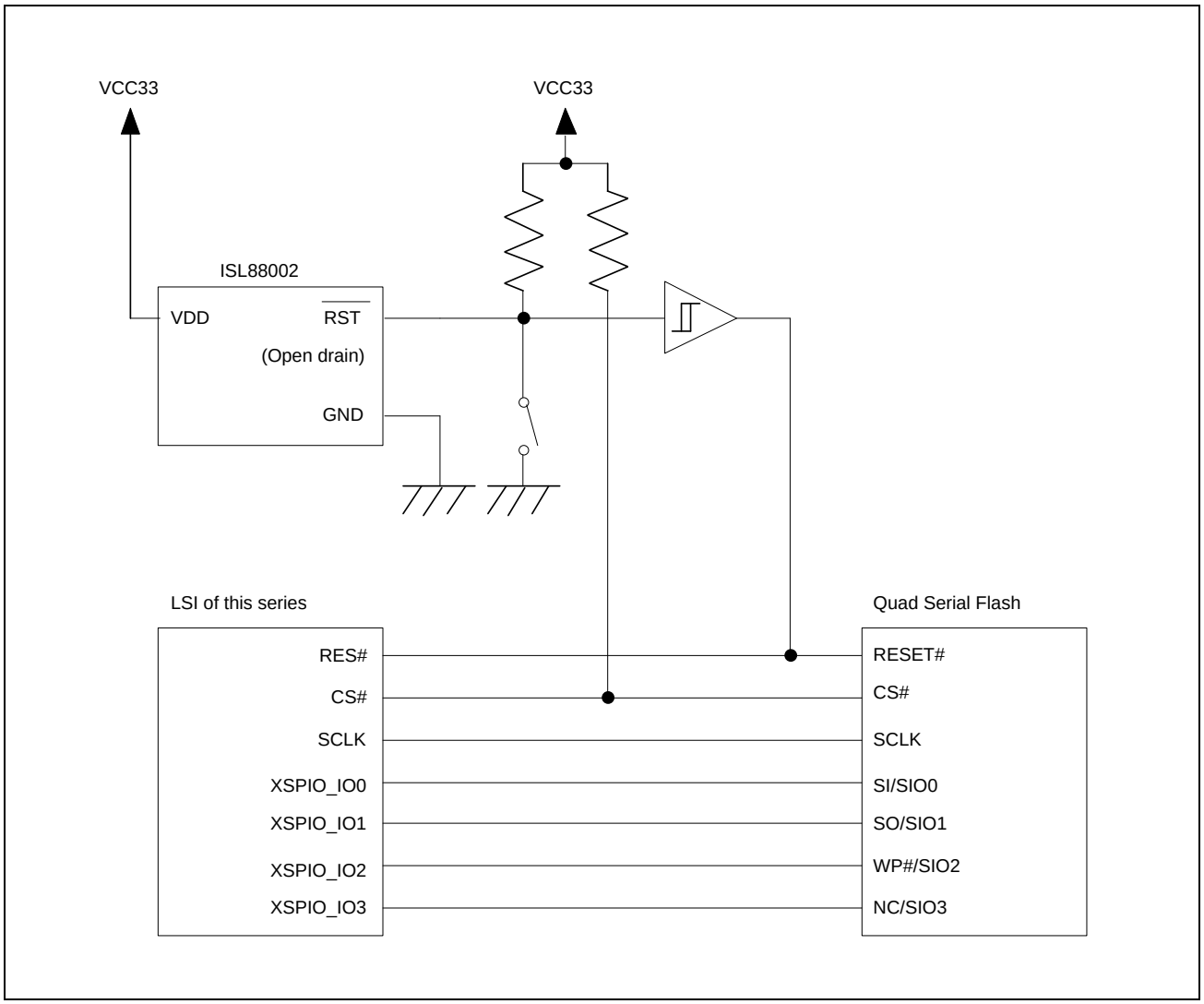

Figure 4.1 Connection example of Quad serial flash with reset pin

4.1.2 For serial flash without hardware reset

Figure 4.2 shows a connection example of a Quad serial flash without a reset pin.

In this case, resetting this LSI after changing the serial flash protocol setting from 1S-1S-1S protocol to another protocol mode in the user program, boot error occurs because the protocol mode of the boot program and the protocol mode of the serial flash do not match. Therefore, use the protocol mode of the serial flash as it is 1S-1S-1S, or use it with 1S-xx-xx (command is 1S).

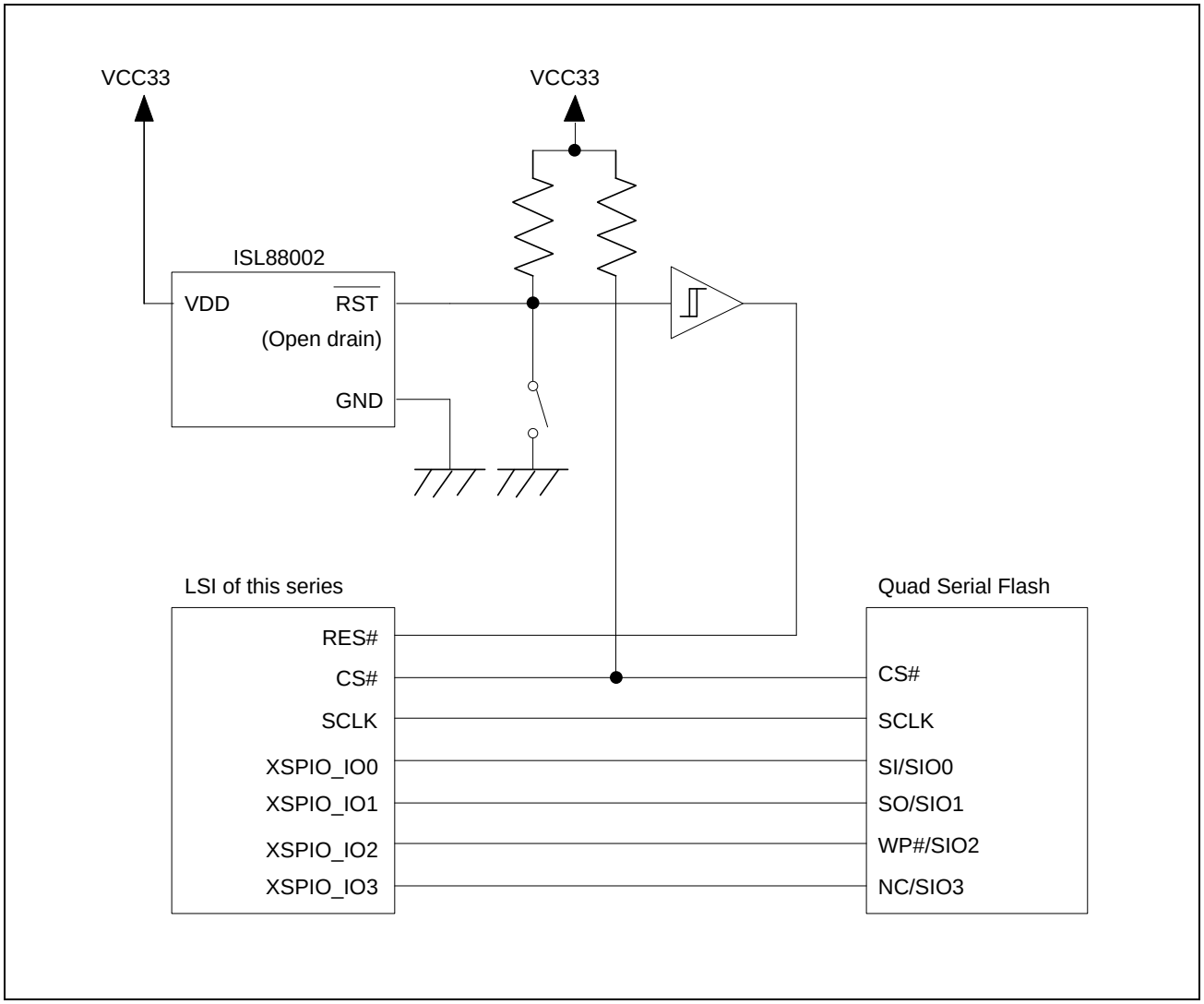

Figure 4.2 Connection example of Quad serial flash without reset pin

4.2 xSPI0 boot mode (x8 boot serial flash mode)

Figure 4.3 shows a connection example for x8 boot serial flash.

In xSPI0 boot (x8 boot serial flash) mode, the serial flash is accessed in protocol mode 8D-8D-8D profile 2.0 at boot time, and hardware reset is performed by the XSPIO_RESET# pin. Please refer to **Table 2.1** and **Table 2.2** for this boot mode setting.

NOTE

Since data is read from HyperFlash with a read latency cycle of 10 at boot, the read latency cycle of HyperFlash must be set to 10 in advance.

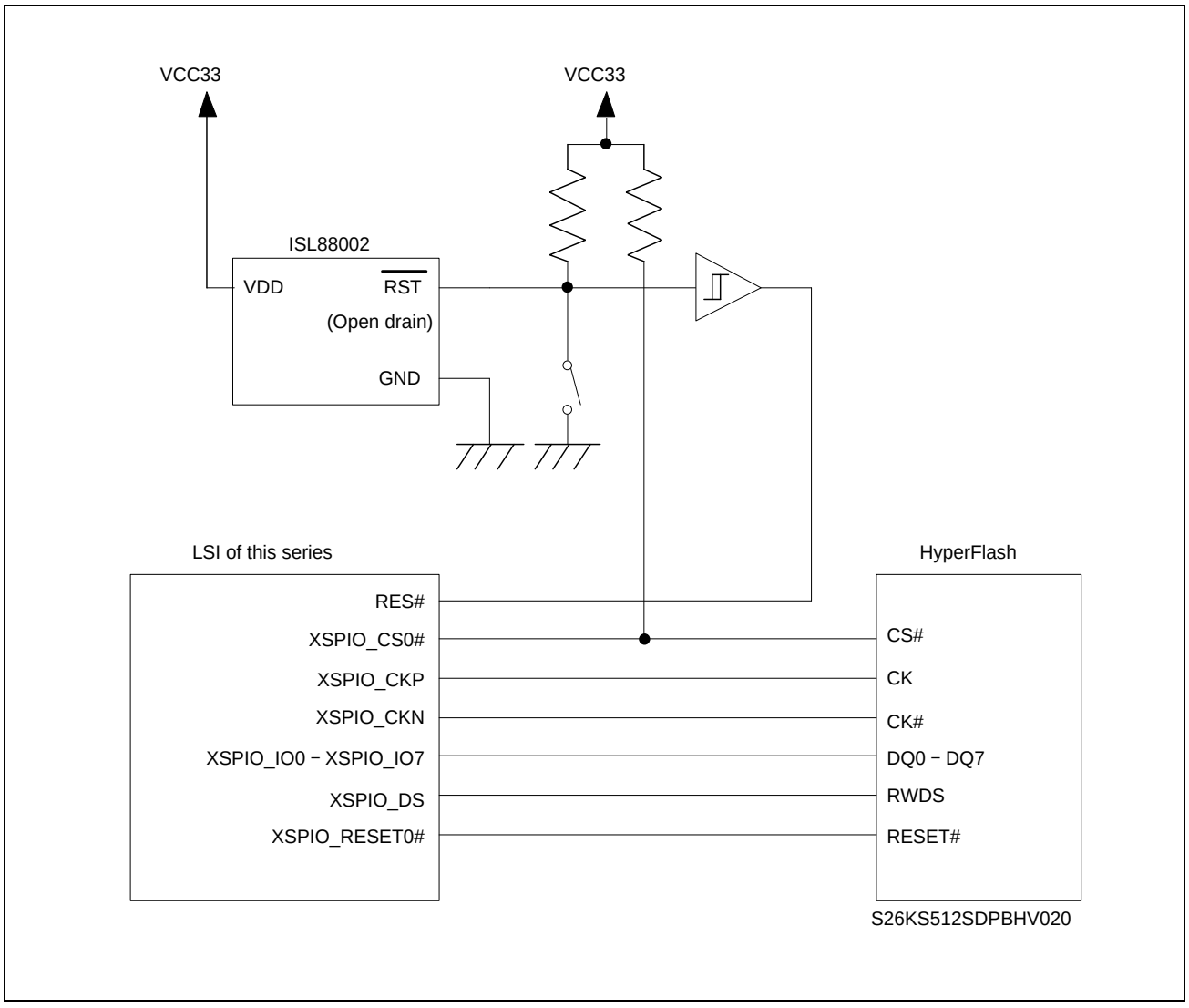

Figure 4.3 Connection example for x8 boot serial flash

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		Page	Summary
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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