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From time to time we are asked to recommend solutions for power supply decoupling and layout. This application note will address these questions by providing solutions which have provided good results and warnings regarding solutions which could produce undesirable results.

Pletronics' oscillators are designed and tested to meet the highest standards of quality and performance. Our oscillators will meet their specifications over variations in power supply voltage and temperature. However, noise at the oscillator's power supply input can degrade jitter and phase noise performance. To get the best performance possible, it is desirable to de-couple high frequency components from the power supply prior to the oscillator.

Power supply bypass design starts with low impedance power and ground connections. This is best provided by a multi-layer PWB incorporating internal power and ground planes. Bulk power supply bypass capacitance is included to reduce power supply ripple and improve the power supply's surge capacity. Bulk bypass capacitance may exist anywhere on the target application board.

Unlike the bulk bypass capacitance, the oscillator's high frequency bypass capacitors are placed as close as possible to the oscillator. Figure 1 shows typical bypass configuration for Pletronics' oscillators. The capacitance values shown in Figure-1 may be used for all product families.

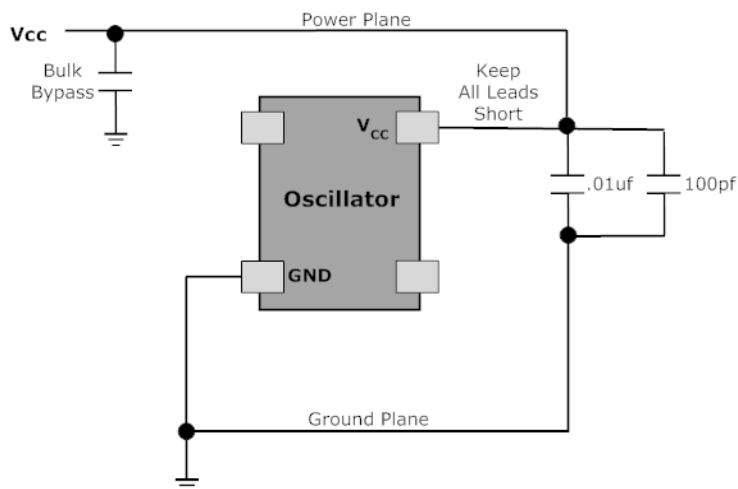


Figure 1 Oscillator with Capacitor Bypass

A bit of comment needs to be added about capacitors. EIA specifies capacitors in four classes. Class-I are the most stable and includes the zero temperature coefficient NPO capacitors used for load capacitors in discrete crystal applications. Class-IV is specified but not commonly available. Class-II and Class-III are the most commonly

used. For oscillator bypass applications, Pletronics recommends at least X5R capacitors. This class of capacitor is specified from -55°C to +80°C, has excellent drift characteristics over this temperature range, excellent high frequency characteristics and good volumetric efficiency. Table 1 summarizes the characteristics of common EIA Class-II and Class-III capacitors.

EIA Class	EIA Designation	Lowest Temperature	Highest Temperature	Capacitor Drift over Temperature
II	X5R	-55°C	+85°C	±15%
II	X7R	-55°C	+125°C	±15%
III	Y5V	-30°C	+85°C	+22%/-82%
III	Z5U	+10°C	+85°C	+22%/-56%

Table 1 Capacitor Characteristics

In addition to the bypass capacitor network shown in Figure 1, some designers also insert a series impedance between the oscillator and power supply to create a low pass filter, further isolating the oscillator. The cutoff frequency for this simple filter is given by:

$$F_{cutoff}(Hz) \approx 1 / (2 * \pi * X_{ser} * C_{bypass})$$

The added impedance, either resistive or inductive, may be in series with the normal capacitive bypass network, or placed between the two bypass capacitors. These connections are shown in Figure 2.

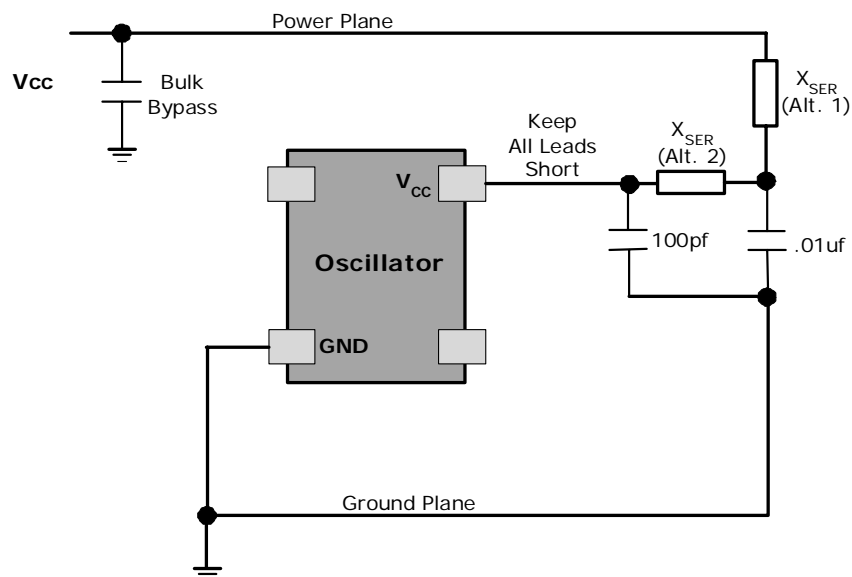


Figure 2 Oscillator with Series Impedance

Care must be taken any time a resistor is placed in series with the power supply. A surprisingly small value of resistance in series with the power supply is sufficient to

reduce V_{CC} below the oscillator's V_{CCmin} . Maximum current values for Pletronics oscillators are specified in the data sheets and range from 5uA for some of our 32.768KHz real-time-clock oscillators to 90mA for higher frequency LVPECL oscillators. Table 2 provides maximum resistor values for combinations of I_{CC} , V_{CC} and power supply tolerance.

I_{CC}	V_{CC}			
	1.8V \pm 5%	2.5V \pm 5%	2.5V \pm 10%	3.3V \pm 10%
5uA	1.8K ohm	25K ohm	50K ohm	66K ohm
25mA	3.6 ohm	5.0 ohm	10 ohm	13.2 ohm
50mA	1.8 ohm	2.5 ohm	5.0 ohm	6.6 ohm
75mA	1.2 ohm	1.7 ohm	3.3 ohm	4.4 ohm
100mA	0.9 ohm	1.3 ohm	2.5 ohm	3.3 ohm

Table 2 Maximum Series Resistance

Inserting a series ferrite bead between the power supply and the oscillator is also acceptable. The designer should select a low-Q, non-resonant ferrite bead (also called lossy or absorptive beads). A high-Q ferrite bead or inductor could create a resonant tank with the bypass and parasitic capacitance. When selecting a ferrite bead for this application, the bead's DC resistance must be considered. It is not uncommon for the DC resistance to be one-Ohm or greater.

Lead lengths and PWB layout are important considerations for optimal performance. Figure 3 shows close spacings, use of ground planes and parallel capacitor decoupling.

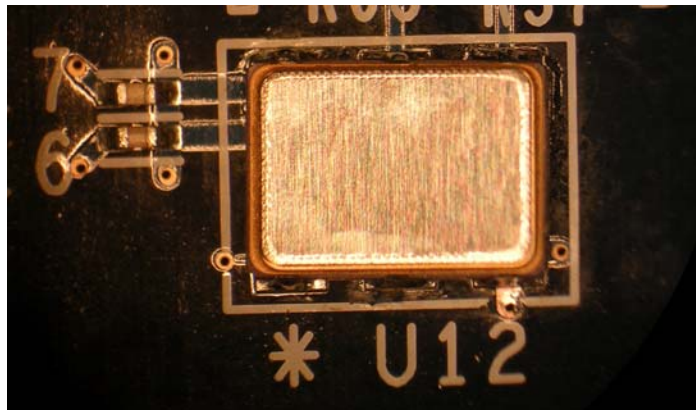


Figure 3 Typical PWB layout with decoupling capacitors

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