AND9089/D

A Guide to Choosing the Right Ultra - Low I_Q Low Dropout Linear Voltage Regulators

ON Semiconductor®

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APPLICATION NOTE

Introduction

One of the most important challenges today in designing electronic applications is to minimize the power consumption of the system. To accomplish this, most systems utilize various low power modes which help to minimize the overall power consumption. When utilizing various modes of operation, system supply currents can easily vary from single μA or even fractions of μA in sleep to tenths or hundreds of mA in full power mode. Low Dropout Linear Voltage Regulators (popularly referred to as LDOs) are common building blocks in any power system and the choice of linear regulator can have an important impact on the overall system power consumption. To complicate this choice, it is often required that the LDO not only feature ultra−low quiescent current but should additionally provide good dynamic performance to assure stable, noise−free voltage rail, suitable for sensitive circuits. These requirements are often mutually exclusive and unveil a real challenge for the IC designers. As a consequence not many LDOs on the market can satisfy both these requirements simultaneously.

The following paper discusses the tradeoffs between achieving low I_Q and good dynamic performance when choosing an LDO, and some techniques that are now used to achieve an acceptable balance.

Factors to Consider

When choosing a linear regulator for a low power application, engineers predominantly search for ultra−low I_Q LDOs[1] meeting their input voltage and output current requirements. Whereas making a selection according to the I_Q specification gives some good initial information about the LDO's current consumption, two devices with equal or very similar I_Q can dramatically differ in terms of dynamic performance. I_Q can become rather a virtual parameter if we recall that it defines the ground current consumption without any load applied. In practical cases it may be more appropriate to look at the ground current consumption at very light loads from single μA to tenths or hundreds of μA. It is interesting to note that after evaluating different LDO products from different manufacturers, it was not uncommon to find that the I_Q specification given in the datasheet was for the perfect no load condition, and not the more realistic output load of 10 μA to 100 μA. Sometimes it may also be relevant to know the ground current behavior with respect to the input voltage or temperature. Apparently the ground current of some regulators available on the market increases considerably if the input voltage decreases and the LDO enters into its dropout region. This may be an important factor in choosing a product for battery operated equipment. Additional unexpected current consumption can have a negative impact on a product by considerably shortening its battery life. These undesired effects can be especially severe if the application spends most of the time in idle or sleep state drawing a minimum current. The designer should always read the datasheet notes for the I_Q specification and where possible, examine the associated graphs of I_Q vs. I_{LOAD} before making the decision to choose a particular LDO.

1. By specifying ultra−low I_Q here we refer to regulators with I_Q < 15μA.

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Dynamic Parameters

There are two main factors which influencing the dynamic performance of an Ultra−Low I_Q LDO regulator. The first is the technology process being used. The majority of ON Semiconductor's Ultra−Low I_Q LDOs are implemented using advanced CMOS or BiCMOS technologies with specific process flow options optimized for low power consumption, high speed Power Management ICs. Although the proper technology choice is essential it obviously doesn't guarantee in itself good dynamic parameters for LDO regulators. The second very important factor determining the final performance are the design techniques implemented in the design of the LDO, and this comes from design experience in this field. ON Semiconductor has over 40 years of experience in this field, and the latest generation of devices features ultra−low noise, good PSRR and ultra−low I_Q at the same time. To dip into the details let us review different types of regulators with respect to the dynamic performance.

Constant Bias LDO Regulators

Traditionally Ultra−Low I_Q CMOS LDOs used constant biasing scheme. This means that ground current consumption was kept relatively constant across the available range of output currents. Examples of such devices are the MC78LC or NCP551 featuring an I_{GND} (or I_Q) of 1.5 μA and 4 μA respectively. These devices are very well suited for battery powered applications with less demanding performance requirements. Their primary disadvantage is relatively poor dynamic performance, namely load and line transients, PSRR or output noise. Often it is possible to tweak this dynamic performance by using larger output capacitors. Figure 1 shows how the MC78LC load transient overshoot and undershoot are improved by increasing the C_{OUT} from 1 μF to 100 μF.

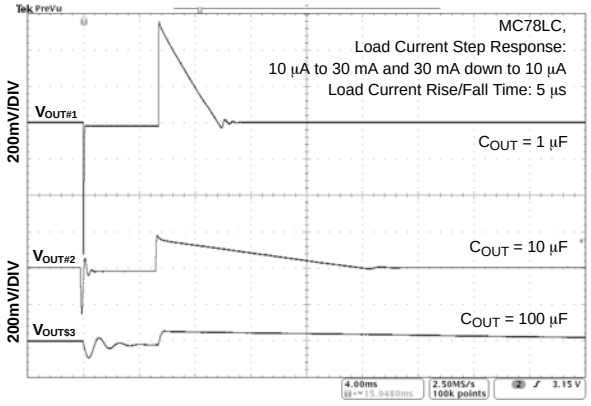

Figure 1. MC78LC Load Transient Improvement

Table 1 below summarizes these results. As can be seen the transient amplitude was greatly reduced due to a larger C_{OUT}.

Table 1. MC78LC LOAD TRANSIENT AMPLITUDE

	Output Capacitor, C_{OUT}		
	1 μF	**10 μF**	**100 μF**
Overshoot	+560 mV	+180 mV	+80 mV
Undershoot	−720 mV	−240 mV	−100 mV

Unfortunately while the transient amplitude decreased, the settling time increased at the same time. It should also be noted that when using large output capacitors it may be necessary to provide an external reverse protection diode between the V_{IN} and V_{OUT} pins. This will protect the regulator from the excessive reverse current which could otherwise flow through internal PMOS body diode during a sudden fall of the input voltage. Increasing C_{OUT} does not always achieve the desired performance. Furthermore it can be troublesome either due to the necessity of including the external protection diode or in applications requiring fast settling time, small solution size or small inrush currents. In such cases it is recommended to use some of the newer LDOs which are presented in the next sections.

Proportional Bias LDO Regulators

To improve the relatively poor dynamic behavior of the constant bias (constant I_{GND}) LDOs, in newer devices ground current changes proportionally to the output current. Examples of such LDOs are the NCP4681 and NCP4624 featuring typical quiescent current of 1 μA and 2 μA respectively. Figure 2 demonstrates the concept used in the proportional I_{GND} LDOs. These devices are designed so that the I_{GND} starts to rise at I_{OUT} > 2 mA.

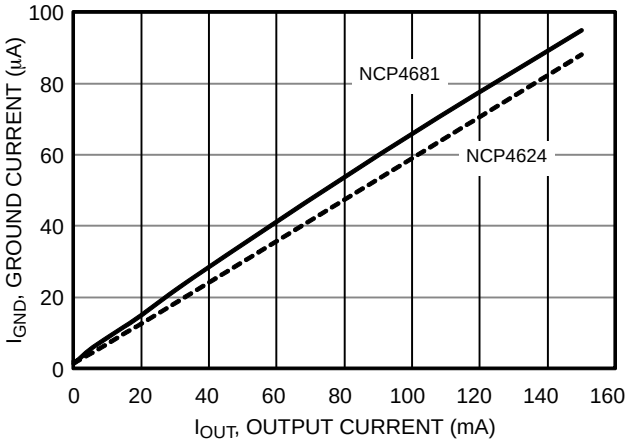

Figure 2. NCP4681, NCP4624 I_{GND} vs. I_{OUT}

It assures that the LDO current consumption at light loads is practically constant and corresponds very well with the I_Q specification given in the datasheet. The comparison between NCP4681 and MC78LC PSRR at 100 Hz and I_{OUT} = 30 mA shows about 15 dB improvement from 38 dB to 53 dB. As will be discussed later, the improvement in load transient response is even more noticeable. Although the proportional bias technique provides improved dynamic parameters with respect to constant I_{GND} LDOs, in highly demanding, precision applications requiring very clean power supply rail and ultra−low I_Q this performance may still be insufficient.

Adaptive Bias LDO Regulators

To provide excellent dynamic parameters and ultra−low I_Q at the same time the newest generation of ON Semiconductor LDOs implement a technique called adaptive ground current. These regulators use special techniques to boost the ground current at a certain level of output current without compromising light load efficiency. Due to this, the end application can benefit from good load/line transients, PSRR and output noise. Examples of ICs featuring the adaptive ground current technique are the NCP4587/9 and NCP702 having an I_Q of 1.5 μA and 9 μA respectively. The NCP702 is additionally optimized in terms of noise featuring typ. 11.5 μV_{RMS} in 100 Hz to 100 kHz noise bandwidth. It is very well suited for powering sensitive Analog, RF circuitry in environments requiring long battery life and small solution size.

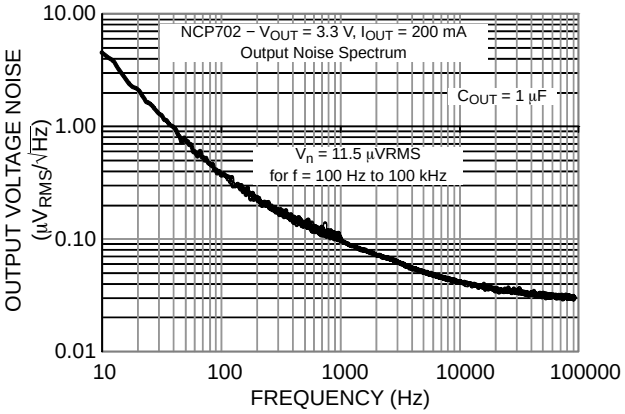

Figure 3. NCP702 Output Noise Density

Comparison of the Three LDO Types

Figure 4 shows the ground current versus output current comparison for the three types of ultra−low I_Q LDOs described above. All regulators used in the comparison feature very similar quiescent current specification of 1 μA to 1.5 μA. Their ground current dependence on the output current is very different. As a consequence the dynamic performance of these regulators also differs considerably.

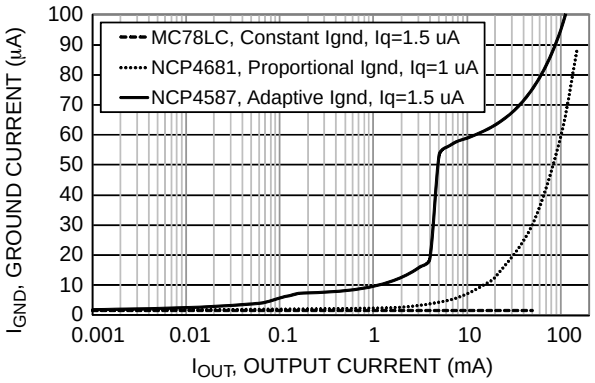

Figure 4. I_{GND} vs. I_{OUT} comparison

The load transient performance advantage of NCP4587, an adaptively biased LDO as illustrated on Figure 5 is evident. The transient amplitudes are summarized in Table 2.

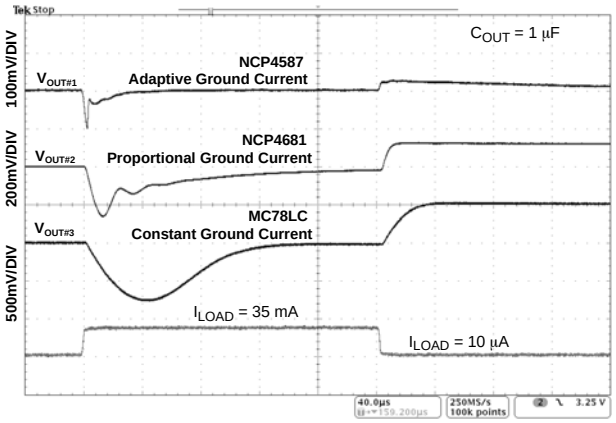

Figure 5. Load Transient Comparison

Table 2. ULTRA−LOW IQ LDO LOAD TRANSIENT AMPLITUDE

	Ultra−Low I_Q LDO		
	MC78LC	**NCP4681**	**NCP4587**
Overshoot	+560 mV	+120 mV	+30 mV
Undershoot	−750 mV	−260 mV	−100 mV

Similarly to the previous comparison Figures 6 and 7 presents I_{GND} and corresponding load transient comparison between NCP702 (an adaptive type LDO) and NCP4641 (a constant bias LDO). Both ICs feature an I_Q of 9 μA but again the transient performance is notably better in the case of the adaptive voltage regulator.

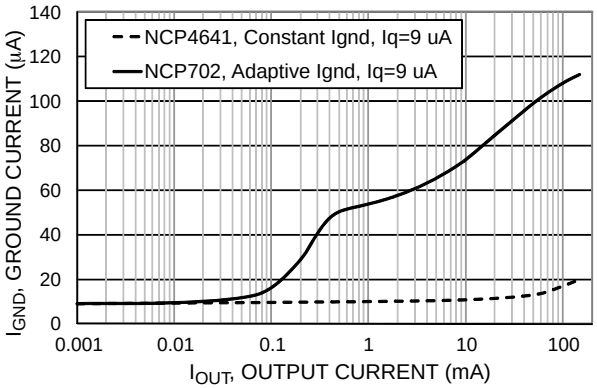

Figure 6. I_{GND} vs. I_{OUT} comparison

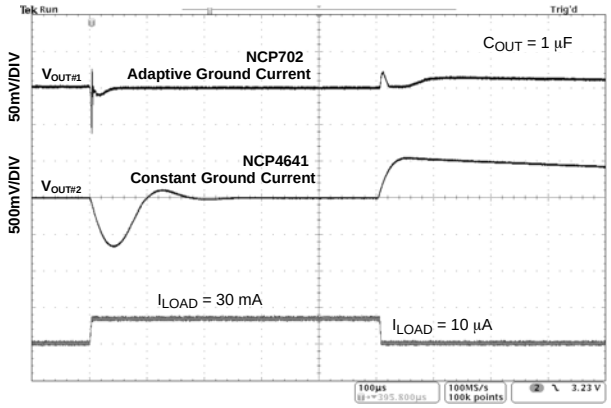

Figure 7. Load Transient Comparison

AE Pin Functionality

Another feature deserving of mention which may be used to improve the dynamic parameters of Ultra−Low I_Q regulators is commonly called Auto−ECO functionality (Figure 8).

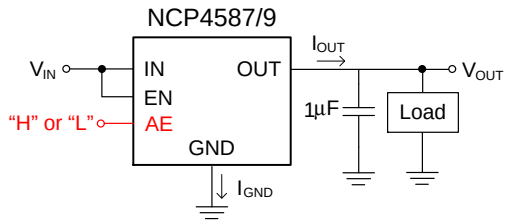

Figure 8. NCP4587/9 LDO with AE pin

Setting the additional AE pin to a logic low level allows the user to configure the regulator as an adaptive ground current Ultra−Low I_Q LDO. Pulling the AE pin to a high logic level the ground current consumption at low output current is raised to approximately 40 μA which substantially improves the load transient response from very light to large loads. At higher load currents the I_{GND} in both modes of operation is approximately equal and there is basically no difference in the dynamic performance. Figure 9 shows how the AE pin state influences the ground current consumption of the regulator.

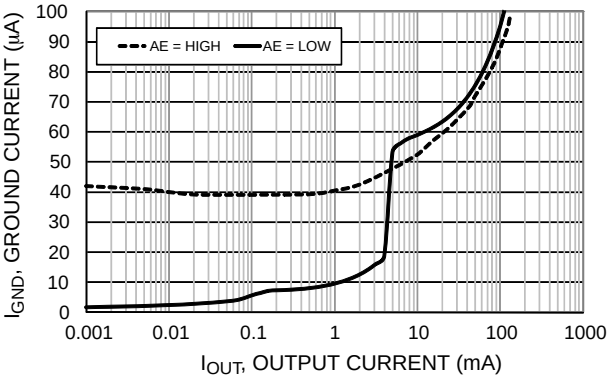

Figure 9. NCP4587/9 LDO with AE pin

The AE pin becomes helpful in applications where the system is periodically brought from sleep mode to full−power mode. If the transition between these two states is very fast, large undershoots could be experienced. Although NCP4587/9 features very good load transient response in comparison to other LDOs, by connecting the AE pin with a MCU I/O line (for example) and then indicating ahead of time an increase in load current demand via the I/O line, the undershoot can be further optimized. As a practical example, many GPS receiver chipsets are equipped with an external WAKEUP signal to indicate ahead of time a switching of the GPS from a hibernate state. This signal is usually connected to an external active antenna supply and can also be used in conjunction with the regulator powering the GPS chipset. In this way the regulator will be manually set to higher ground current consumption mode before the GPS transition from hibernate to full−power mode, improving its dynamic performance.

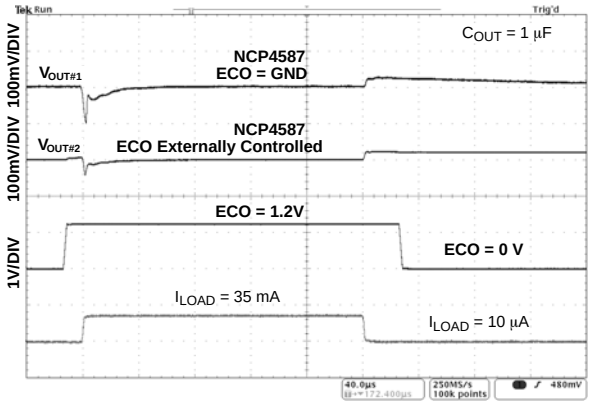

Figure 10. NCP4587 Load Transient improvement

Figure 10 shows the transient improvement by using the AE pin function. The top most waveform ($V_{OUT#1}$) was registered for the condition that AE pin was permanently connected to GND. The waveform below ($V_{OUT#2}$) shows the improved load transient where the AE was manually set to a logic high state approximately 20 μs before the high load current demand occurred. Generally it is sufficient, that the AE logic high is set 1 μs − 2 μs before the load transient event occurs. Yet another situation where the ECO function can prove to be useful is where the application requires ultra−low I_Q for very light load currents but already at 1 mA − 3 mA demands very good PSRR and line/load transient characteristics. Figure 11 shows that more than 40 dB improvement in PSRR at 1 kHz, I_{OUT} = 1 mA to 3 mA is possible, if the AE pin is switched from a low to a high logic state.

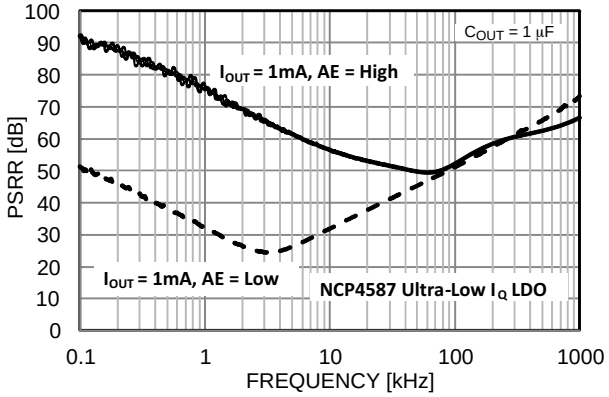

Figure 11. NCP4587 PSRR Improvement

Quiescent Current Specifications

Next, we will take a closer look at datasheet quiescent current specifications vs. actual measurements. As we will see in some cases the number stated on the datasheet title page can be very different from the actual measured value. We will identify some parameters to look at in order to avoid unexpected current consumption.

Quiescent Current − A Case Study

As an example let us consider two very similar LDOs, both with adaptive ground current configurations: the NCP702 with typical I_Q = 10 μA and a competitor LDO with typical I_Q = 11 μA. Tables 3 and 4 show the datasheet value of the quiescent current (I_{OUT} = 0 μA) and actual ground current consumption measured for I_{OUT} = 10 μA and 50 μA.

LDO1: NCP702 − V_{OUT} = 3.3 V, V_{IN} = 3.6 V

Table 3. NCP702 MEASUREMENT VS. SPECIFICATION

Datasheet: I_Q, I_{OUT} = 0 μA	Measured: I_{GND} at I_{OUT} = 10 μA	Measured: I_{GND} at I_{OUT} = 50 μA
Typ. 10 μA	9.2 μA	11.5 μA

LDO2: Competitor LDO − V_{OUT} = 3.3 V, V_{IN} = 3.6 V

Table 4. COMPETITOR MEASUREMENT VS. DATASHEET

Datasheet: I_Q, I_{OUT} = 0 μA	Measured: I_{GND} at I_{OUT} = 10μ A	Measured: I_{GND} at I_{OUT} = 50 μA
Typ. 11 μA	16.4 μA	22.1 μA

In the case of the NCP702 the measured I_{GND} at I_{OUT} = 10 μA matches very closely to the datasheet value of I_Q. In the case of the competitor LDO at I_{OUT} = 10 μA the actual result is 49% higher than what we could predict from the datasheet. There are two reasons for that. The first is that the competitor I_Q specification does not include the EN (Enable) pin input current which flows through an internal pull−down resistor to ground. Measurements show that this internal pull−down resistance is in the order of 1 MΩ. If the EN pin is connected to the V_{in} pin, the ground current will be heavily influenced by the input voltage. In this case the input voltage is 3.6 V so there is additional 3.6 μA of current consumption due to pull−down resistance. By contrast, the NCP702 has internal 100 nA pull−down current source and the enable current is independent on the input voltage.

The second reason why the I_Q spec. doesn't match with reality is that the adaptive ground current used in the competitive LDO is set in such a way that the I_{GND} starts to increase at very low output currents, much lower than the NCP702 threshold

It may be of interest to designers to note that the NCP702 can be offered with a customized adaptive ground current curve. On request, the NCP702 can be configured at the factory so that the I_{GND} consumption is held at ultra−low level, matching the I_Q specification up to $I_{OUT} \approx 2$ mA. For the available options please contact your local sales office.

Quiescent Current Differences and the Impact on Battery Life

We could ask ourselves if the ground current difference measured and discussed previously really matters and could seriously impact the battery life performance. Unfortunately the answer to this question isn't straightforward and it depends on the specific end application where the LDO is being used.

As an example let us consider the basic application shown on Figures 12 and 13 where the LDO is used to down−convert the battery voltage and provide a current to the load.

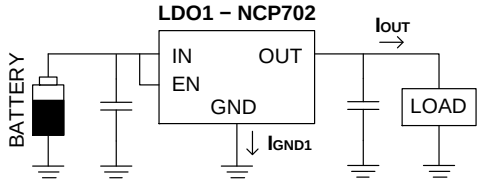

Figure 12. Basic Application using the NCP702

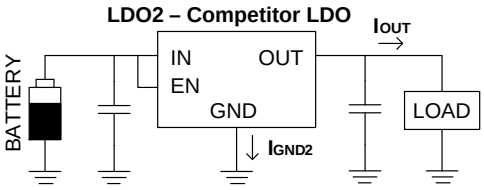

Figure 13. Basic Application Using the Competitor LDO

The battery life for the application shown on Figures 12 and 13 can be described by a general formula:

$$\text{Battery Life (h)} = \frac{\text{Battery Capacity (mAh)}}{\text{Average Current (mA)}}$$

Examining the case of the NCP702 (LDO1) we have:

$$\text{Battery Life 1} = \frac{\text{Battery Capacity}}{I_{OUT} + I_{GND1}}$$

For the competitor LDO (LDO2) we have:

$$\text{Battery Life 2} = \frac{\text{Battery Capacity}}{I_{OUT} + I_{GND2}}$$

From the two equations shown above we can calculate the battery life saving offered by NCP702 over the competitive solution:

$$\text{Battery Life Saving \%} = \frac{I_{GND2} - I_{GND1}}{I_{OUT} + I_{GND1}}$$

The resulting equation becomes meaningful after plugging−in the measured ground current vs. output current values for the two LDOs considered. Figure 14 illustrates the Battery Life Saving and the two LDO I_{GND} plotted against the output current.

What we can see is that the savings will be roughly 20% for light load, I_{OUT} = 40 μA. At larger loads, as the LDO ground current becomes less prominent in comparison with the output current drawn from the battery there is no evident advantage in the battery life between the two solutions.

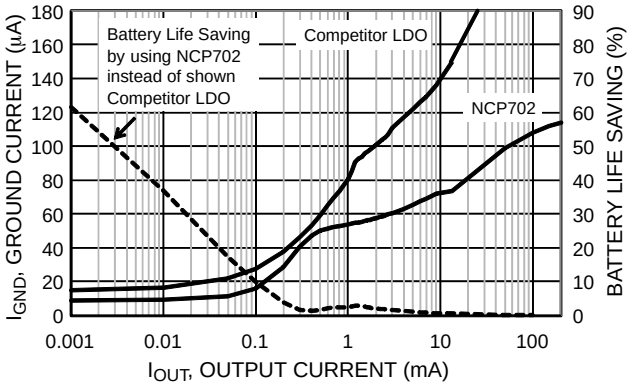

Figure 14. Basic Application Using the Competitor LDO

Generally in applications where other large current contributions exist, the battery life saving can be less severe than the calculated one. Nevertheless it may pay−off to apply the basic calculations and check the results before making the final selection of an Ultra−Low I_Q LDO.

Battery Life Impact of a Variable Load Current

Since it is quite seldom that the LDO output current is constant (as we assumed in the above example) we may want to extend the considerations and include the case of a changing load. Usually it is much more often the case that the circuitry being powered by the regulator transitions between sleep and operation. As an example Figure 15 shows the load current profile of an application working with a 10% duty cycle. The load draws 40 μA in sleep and 100 mA in operation. At I_{OUT} = 40 μA the NCP702 will add 11.1 μA of its own ground current yielding a total battery current of 51.1 μA. In the case of competitor LDO it will add 21.4 μA yielding a total current of 61.4 μA. If we express this current difference in percents the result shows−up 20.2%. This number represents the battery life saving in the sleep mode.

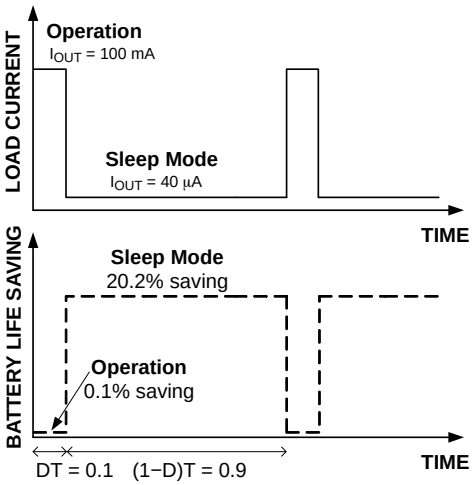

Figure 15. Example Load Current Profile

Figure 16 shows the battery life saving vs. the duty cycle. For the particular case of 10% duty cycle there is still 18.2% lifetime benefit of NCP702.

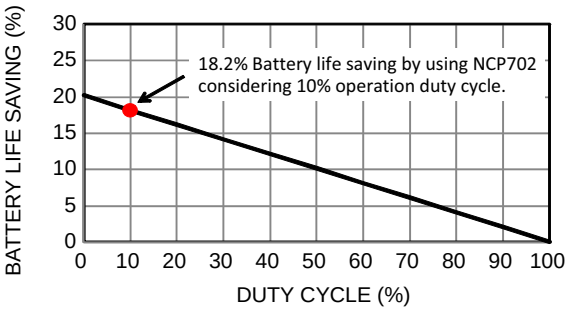

Figure 16. Battery Life Saving vs. Duty Cycle

Ground Current in the Dropout Region

Another important, but often overlooked parameter of the LDO is the ground current consumption if it enters a dropout condition. In Li−Ion or Li−Poly battery powered products it is common to regulate the power supply with reasonably high efficiency using LDOs to produce a 3.3 V or 3.1 V output voltage. However, as the battery discharges and its' voltage decays, the V_{IN} of the LDO may approach V_{OUT} to the point where the regulator enters its dropout region. In such cases, most of the Ultra−Low I_Q LDOs available on the market will start to draw significantly higher ground current than what could be expected relying solely on the datasheet values stated in the electrical table. To illustrate the problem, Figure 17 shows the I_{GND} vs. V_{IN} for a typical Ultra−Low I_Q LDO

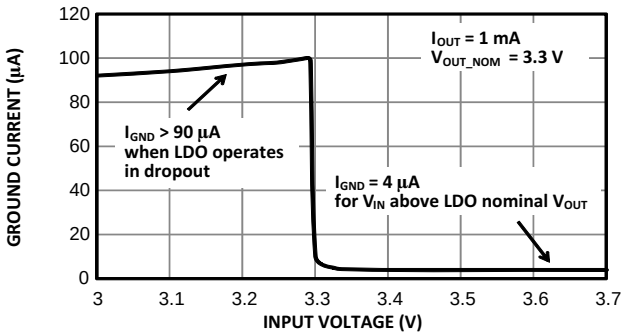

Figure 17. I_{GND} vs. V_{IN} Example

In the dropout region the regulator starts to draw up to 100 μA. To tackle this problem in power conscious applications it may be advisable to add a very low power supervisor with adjustable hysteresis to account for the battery voltage recovery after the load is removed. In some cases where the hysteresis is insufficient other voltage detectors with a latched output may be better suited. This will however result in the necessity to clear the latch using either a push button or the information from the battery charge controller.

The latest generation of ON Semiconductor Ultra−Low I_Q LDOs incorporates an integrated dropout condition detector which will prevent the ground current increase during low input voltage conditions. Examples of devices incorporating this idea are the NCP702 and the NCP4681.

Summary

Traditionally, improving the current consumption of an LDO meant sacrificing dynamic performance. With newer process technologies and design techniques, there are now LDOs available which now make these compromises less dramatic. However, the application designer needs to pay careful attention to the LDO datasheet to understand the operation of the device and to select their solution according to the key requirements of their application.

Table 5. ON SEMICONDUCTOR ULTRA−LOW I_Q LDO PRODUCTS OFFERING:

Part Number	Ground Current	Typ. I_Q	Max. V_{IN}	Rated I_{OUT}	Package	Special Feature	Note
NCP4681/2/4/5	Proportional	1 μA	6 V	150 mA	SC−88A−5 , SC−70−5, SOT−323−5 SC−82AB-4, UDFN4	Soft−Start, Enable Pin	Obsolete
MC78LC	Constant	1.5 μA	12 V	80 mA	SOT−89, TSOP−5	−	
NCP4587/9*	Adaptive/Constant	1.5 μA	6 V	150/300 mA	SOT−23−5, XDFN6	Foldback current limit, Enable Pin	Obsolete
NCP4624	Proportional	2 μA	12 V	150 mA	SC−88A−5, SC−70−5, SOT−323−5 SOT−23−5, UDFN4	Reverse current protection	Obsolete
NCP698	Constant	2.5 μA	6 V	150 mA	SC−82AB-4	Enable Pin	
NCV662/3	Constant	2.5 μA	6 V	100 mA	SC−82AB-4	Enable Pin	
NCV553	Constant	2.8 μA	12 V	80 mA	SC−82AB-4	Enable Pin	
NCP551	Constant	4 μA	12 V	150 mA	TSOP−5, SOT23−5	Enable Pin	
NCP4623	Constant	5 μA	24 V	150 mA	SOT23−5, XDFN6	Foldback current limit, Enable Pin	Obsolete
NCP4626*	Proportional Low/High	6 μA	18 V	300 mA	SOT23−5, XDFN6	Reverse current protection, Enable Pin	Obsolete
NCP702	Adaptive	9 μA	5.5V	200 mA	SOT23−5, XDFN6, TSOP−5	Ultra−Low Noise, Soft−Start, Enable Pin	
NCP4640/1	Constant	9 μA	50 V	50/150 mA	SOT−89−5	Enable pin	Obsolete
NCP4588	Proportional	9.5 μA	5.3 V	200 mA	SC−88A−5, SC−70−5,SOT−323−5 XDFN6	Capacitor−less LDO, Enable Pin	Obsolete
NCP715	Constant	4.7 μA	24 V	50 mA	XDFN6, SC−88A	Fixed output voltage, current limit	New
NCP716	Constant	4.7 μA	24 V	80 mA	WDFN6	Fixed output voltage, current limit	New
NCP718	Proportional	4 μA	24 V	300 mA	SOT23−5, WDFN6	Adjustable output voltage	New
NCP170	Proportional	0.5 μA	5.5 V	150 mA	SOT−563, XDFN4	Enable Pin	New

*Modes of operation are selectable through the external AE pin.

PUBLICATION ORDERING INFORMATION

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