AN11160

Designing RC snubbers

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Document information

Information	Content
Keywords	RC snubber, commutation, reverse recovery, leakage inductance, parasitic capacitance, RLC circuit and damping, MOSFET
Abstract	This document describes the design of a simple RC snubber circuit.

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1. Introduction

This document describes the design of a simple “RC snubber circuit”. The snubber is used to suppress high-frequency oscillations associated with reverse recovery effects in power semiconductor applications.

2. Designing the snubber - theory

The basic circuit is a half-bridge and shown in Fig. 1

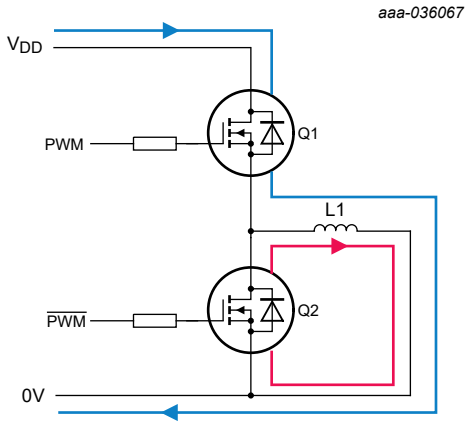

Fig. 1. The half-bridge circuit

In this application note, Q1 and Q2 are BUK7Y2R0-40H devices. Other devices could be considered. Inductor L1 could be connected to V_{DD} rather than 0 V.

Inductor current is established in the red loop; Q1 is off. Before turning Q1 on, Q2 should be turned off to prevent shoot-through current. During the time when both switches are off, current flows through the body diode of Q2 and reverse recovery charge, Q_{rr}, is accumulated in the PN junction. When Q1 is turned on, the body diode of Q2 becomes reverse biased and the stored Q_{rr} depletes through Q1. This causes an additional current in Q1 called the reverse recovery current, I_{rr}. We observe the effect of reverse recovery in the V_{DS} waveform of Q2; see Fig. 2. Time intervals, t1 and t2 shown in this figure will be used to estimate the peak reverse recovery current; see equation (22).

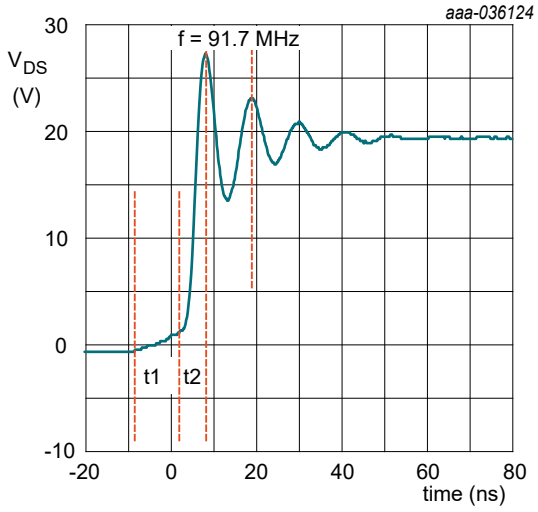

Fig. 2. Reverse recovery-induced oscillation in Q2 V_{DS}

The equivalent circuit is shown in Fig. 3

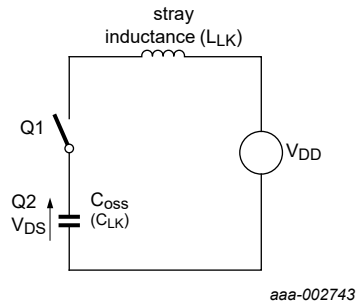

Fig. 3. Equivalent circuit

We are primarily interested in the parasitic elements in the circuit:

- L_{LK} is the total stray or “leakage” inductance comprised of PCB trace inductance, device package inductance, etc.
- The parasitic capacitance C_{LK} is mainly due to C_{oss} of the bottom (Q2) device

Q1 is treated as a simple switch. L1 is omitted here because of its high impedance at the frequency range of interest.

The oscillation caused by reverse recovery of Q2 can be eliminated (snubbed) by placing an RC circuit across Q2 drain-source; see Fig. 4.

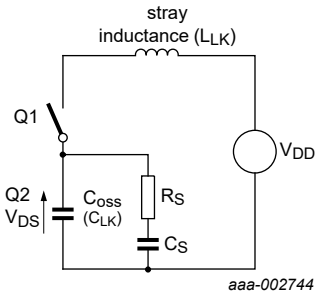

Fig. 4. Equivalent circuit with snubber components R_S and C_S

Before Q2 body diode goes into blocking state, current builds up in the leakage inductance in Fig. 4 due to the reverse recovery charge of Q2. Assuming Q2 blocks the current in a short time, the reverse recovery current in the inductor is forced to flow through the snubber network formed by C_S and R_S. The transition of energy from inductor to snubber capacitor causes the oscillations if the network is not well damped. Behavior of this circuit is analyzed in [1] and the energy loss in the snubber resistor during turn off is found as:

$$W_{RS} = \frac{1}{2} C_S V_{DD}^2 + \frac{1}{2} L_{LK} I_{RM}^2 \quad (1)$$

where I_{RM} is the peak recovery current.

In addition to the energy loss in the resistor, stored energy in C_S will be dissipated in the next turn on of Q2. So, the total energy loss due to snubber network is

$$W_{total} = W_{C_S} + W_{R_S} = C_S V_{DD}^2 + \frac{1}{2} L_{LK} I_{RM}^2 \quad (2)$$

In Equation 2, the first term is due to addition of snubber network, but the second term is inevitable even if a snubber is not used. So, the average power loss due to snubber is:

$$P_{snubber} = C_S V_{DD}^2 f_{sw} \quad (3)$$

The analysis done in [1] shows that there is an optimum snubber resistor value that minimizes the peak voltage during oscillations once C_S is fixed. Using a higher C_S value decreases the minimum peak voltage that can be achieved by using the optimum R_S corresponding to that capacitance. However, C_S linearly affects the power loss according to Equation 3. So, the selection of C_S is a trade-off between efficiency and peak voltage on the MOSFET. Another benefit of dampening oscillations, as shown in the next section, is reduced emission levels.

Choosing C_S capacitor should follow two conditions. First, it should be big enough to be able to store more energy than the leakage inductance's initial energy. This condition is to keep the peak voltage less than 2 x V_{DD}. Second, it should be small enough to fully discharge during the on time so that it is ready for the next turn off event. To be on the safe side, maximum time constant, tau, can be selected as one tenth of the on time. These conditions yield following limits for C_S:

$$\frac{1}{2} C_S V_{DD}^2 > \frac{1}{2} L_{LK} I_{RM}^2 \tag{4}$$

$$C_S > \frac{L_{LK} I_{RM}^2}{V_{DD}^2} \tag{5}$$

$$R_S C_S < \frac{t_{on}}{10} \tag{6}$$

$$C_S < \frac{t_{on}}{(10 \times R_S)} \tag{7}$$

Hence, the range for C_S is:

$$\frac{L_{LK} I_{RM}^2}{V_{DD}^2} < C_S < \frac{t_{on}}{(10 \times R_S)} \tag{8}$$

The damping factor, ζ, for this circuit is defined as:

$$\zeta = \frac{R_S}{2} \sqrt{\frac{C_S}{L_{LK}}} = \frac{R_S}{2 \times Z_0} \tag{9}$$

Once C_S value is chosen in the given range according to concerns mentioned above, the damping factor should be set to somewhere between 0.5 to 1 to achieve minimum peak voltage.

$$0.5 < \frac{R_S}{2 \times Z_0} < 1 \tag{10}$$

Then, the optimum R_S value should be in the following range:

$$Z_0 < R_S < 2 Z_0 \tag{11}$$

3. Determining C_{LK} and L_{LK}

Before designing the snubber network, we must first determine the values of C_{LK} and L_{LK}. We could attempt to measure them directly, but a more elegant method can be used. For the LC circuit in Fig. 3, we know that:

$$f_{RING0} = \frac{1}{2\pi\sqrt{L_{LK}\,C_{LK}}} \tag{12}$$

Where f_{RING0} is the frequency of oscillation without a snubber in place; see Figure 2.

If we put an additional capacitor (C_{add}) in parallel with Q1, the oscillation frequency shifts from f_{RING0} to a lower frequency, f_{RING1}. It can be shown that:

$$C_{LK} = \frac{C_{add}}{x^2 - 1} \tag{13}$$

$$\text{where, } x = \frac{f_{RING0}}{f_{RING1}}$$

See Appendix A.

So, if we measure the oscillation frequency with and without C_{add} in place, we can get f_{RING1} and f_{RING0}, respectively. Then, we can determine C_{LK} and L_{LK} by using equations (12) and (13).

In our example, initial oscillation frequency (f_{RING0}) is found to be 91.74 MHz; see Fig. 2. Then, C_{add} = 1 nF is added to the circuit and f_{RING1} is measured as 61.3 MHz; see Fig. 5.

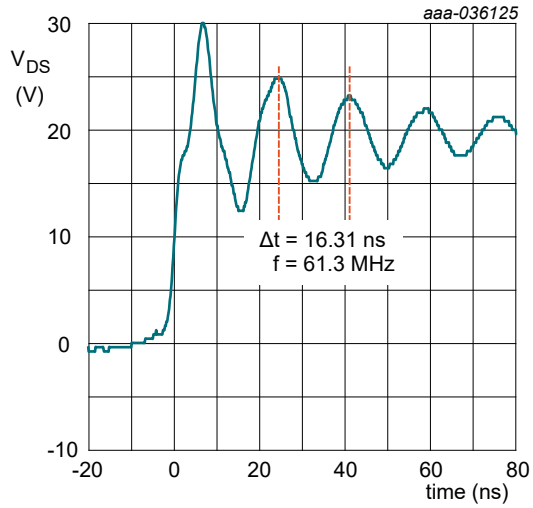

Fig. 5. Reverse recovery-induced oscillation in Q2 V_{DS}; with snubber cap added

From Equation 13:

$$x = \frac{91.74}{61.3} = 1.497 \tag{14}$$

$$C_{LK} = \frac{1000\,pF}{1.497^2 - 1} = 807\,pF \tag{15}$$

Rearranging Equation 12:

$$L_{LK} = \frac{1}{(2\pi f_{RING0})^2 C_{LK}} \quad (16)$$

Substituting f_{RING0} = 91.74 MHz and C_{LK} = 807 pF yields:

$$L_{LK} = \frac{1}{(2 \times \pi \times 9.174 \times 10^7)^2 \times 8.07 \times 10^{-10}} = 3.73\ nH \quad (17)$$

We can double-check that the new oscillation frequency with the added capacitor gives the same L_{LK} value when used in Equation 12:

$$C_{total} = C_{LK} + C_{add0} = 1807\ pF \quad (18)$$

$$L_{LK} = \frac{1}{(2\pi \times f_{RING1})^2 C_{total}} = \frac{1}{(2 \times \pi \times 6.13 \times 10^7)^2 \times 1.807 \times 10^{-9}} = 3.73\ nH \quad (19)$$

4. Designing the snubber - in practice

We now have sufficient information to design a snubber for the waveform shown in Figure 2. To recap:

V_{DD} = 20 V
I_O = 8 A
f_{SW} = 300 kHz
C_{LK} = 807 pF
L_{LK} = 3.73 nH

As mentioned before, there is no perfect value for C_S. Designers must choose a value according to their performance requirements. Equation 8 should still hold but it generally gives a very wide range for C_S to start with. It has been found that selecting C_S in the range of 1 to 2 times C_{LK} is a good starting point in terms of the compromise between power loss and peak voltage. In the example, it is aimed to almost eliminate the oscillation which would also help us observe the EMI effect clearly. Therefore, C_S is selected as:

$$C_S = 2 \times C_{LK} = 1.614\ nF \quad (20)$$

The closest standard value of 1.6 nF is preferred. Using higher values of C_S would not reduce the peak further since almost no overshoot is achieved with 1.6 nF and the optimum R_S. However, a lower capacitance could be used if peak voltages can be tolerated, and EMI is a lesser concern than efficiency.

Once C_S value is fixed, determining the optimum R_S resulting the minimum peak voltage requires a couple of trials in the range given by Equation 11. For C_S = 1.6 nF, optimum R_S turned out to be:

$$R_{S,opt} = 1.5 \times Z_0 = 1.5 \times \sqrt{\frac{L_{LK}}{C_S}} = 1.5 \times \sqrt{\frac{3.73}{1.6}} = 2.28\ \Omega \quad (21)$$

The closest standard value of 2.2 Ω is used.

Now we need to check if the chosen C_S value is in the allowed range. From the V_{DS} waveform in Fig. 2, I_{RM} can be calculated roughly as follows:

$$I_{RM} = \frac{di}{dt} \times t_2 = \frac{I_0}{t_1} \times t_2 = \frac{8\,A}{11\,ns} \times 4\,ns = 3.64\,A \quad (22)$$

Taking minimum duty cycle D_{min} = 10%, we get:

$$t_{on(min)} = \frac{D_{min}}{f_{SW}} = \frac{0.1}{300 \times 10^3} = 33\,\mu s \quad (23)$$

Evaluating Equation 8 yields:

$$\frac{3.73 \times 10^{-9} \times 3.64^2}{20^2} < C_S < \frac{0.33 \times 10^{-6}}{(10 \times 2.2)} \quad (24)$$

$$124\,pF < C_S < 15\,nF \quad (25)$$

Verifying that the selected C_S value falls in this range completes the snubber design. As can be seen in Fig. 6, placing the snubber across Q2 eliminated the oscillation in the V_{DS} waveform. Power dissipation in the snubber resistor should be taken into consideration when selecting the components. By using Equation 1, it can be calculated as:

$$P_{RS} = f_{sw} W_{RS} = \frac{f_{sw}}{2} \times \left(C_S V_{DD}^2 + L_{LK} I_{RM}^2\right) \quad (26)$$

For the worked example:

$$P_{RS} = 1.5 \times 10^{-4} \times \left(1.6 \times 20^2 + 3.37 \times 3.64^2\right) \approx 103\,mW \quad (27)$$

So, an SMD resistor of 0805 size with 0.125W power rating or higher should be fine if no significant derating is needed.

In AC applications of the half-bridge topology, such as 3-phase BLDC, current can obviously flow in both directions unlike the buck converter presented in this note where it only flows towards the output. In that case, RC snubbers may be needed for both devices because when the current is flowing towards the input, the bottom MOSFET is the active switch and the top MOSFET is freewheeling. So, oscillation may occur due to the reverse recovery of the top MOSFET as well. The snubber design technique presented here can be applied to the top (Q1) MOSFET as well.

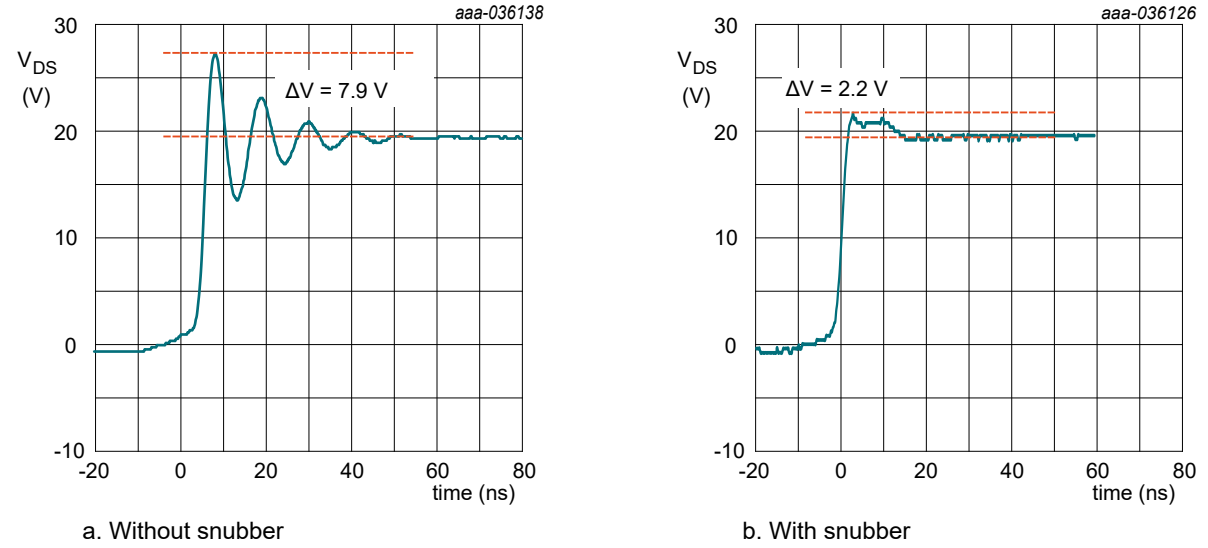

Fig. 6. Q2 V_{DS} waveform with and without snubber

To investigate the EMI effect of using a snubber, conducted emission tests in the range of 150 kHz to 150 MHz are done on the example buck converter in accordance with CISPR 25 standard. Fig. 7 shows the resulting emission levels with and without snubber in green and orange, respectively. In the low frequency region, peaks are observed at the switching frequency, f_{sw} = 300 kHz and its harmonics as expected. In this case, there is no external EMI filter because the purpose of this exercise is to show the effect of the snubber on conducted emissions at high frequency. In the high frequency region, reverse recovery oscillation causes elevated emission levels around f_{RING0} = 91.74 MHz. It is clearly seen that emissions can be decreased significantly with a snubber design which is optimized for damping.

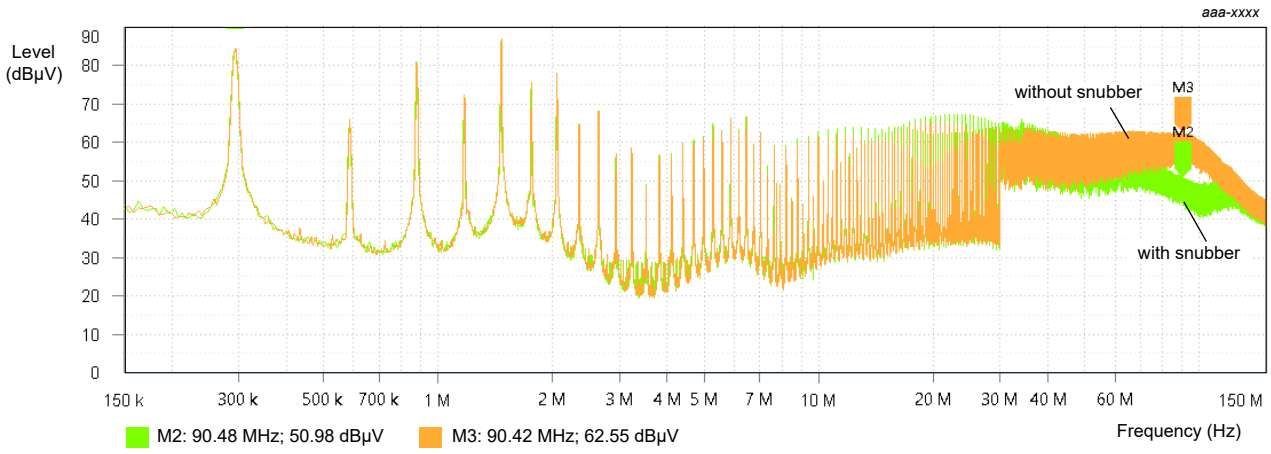

Fig. 7. Effect of snubber on conducted emission

In some cases, adding a snubber across the semiconductor device can cause another oscillation with a higher frequency than the original one. An example of this situation is presented in Fig. 8. Studies showed that this behavior is caused by the parasitic inductance of the loop formed by Q2 MOSFET and the snubber network especially when they are placed far from each other. Added inductance in this loop increases the order of the circuit causing a new ringing.

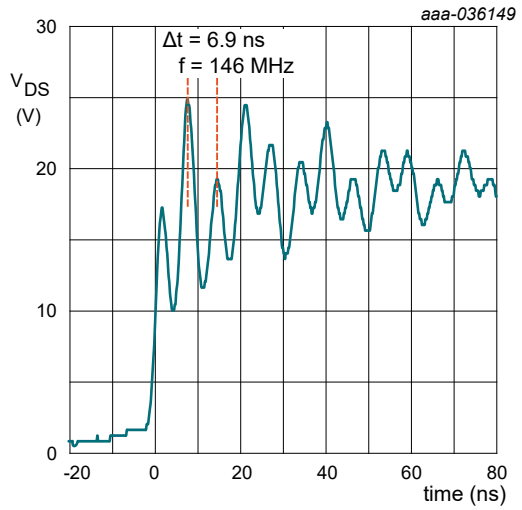

Fig. 8. Effect of snubber on conducted emission; snubber network is placed far from MOSFET

To prevent the occurrence of a second high-frequency oscillation, the designer should pay special attention to placing snubber as close as possible to the switching device during the PCB design stage. Also, components with low internal inductances should be used. This problem is less likely to occur with Nexperia's LFPAK copper clip technology which provides lower parasitic inductance compared to wire bond technology. As regarding the snubber resistor, thin film chip resistors are preferred which have lower inductances compared to thick film type and leaded ones like metal film, carbon film or wire wound. In this application note, surface mount Class I (C0G type) ceramic capacitors are preferred. These capacitors are well suited for snubber applications because they present low ESR and ESL compared to leaded ceramic capacitors and electrolytic capacitor types. Furthermore, Class 1 ceramic capacitors have better capacitance stability than other ceramic classes and they are not susceptible to aging. Surface mount film capacitors are also a good choice for snubber applications especially at high voltage levels. If it is too late to make any changes in the design and such waveform is observed during testing when snubber is placed, the two ringing frequencies should be measured first. Then, the method described in this note can be applied for the low frequency component. High frequency one can be eliminated by adding a series element to the gate of the MOSFET. A small value resistor or a ferrite bead with a high impedance at the ringing frequency can help solving this issue with the cost of increasing switching losses.

5. Summary

- Reverse recovery effects in power devices can induce high frequency oscillations.
- A common technique for suppressing the oscillations is the use of an RC snubber.
- Design of an effective snubber requires the extraction of the circuit parasitic capacitance and inductance. A method has been demonstrated for doing this.
- The snubbed circuit has been shown to be a variation on the classic RLC circuit with an initial condition.
- It has been explained that there is no perfect snubber design. It is a matter of compromise between damping the oscillations and keeping the energy loss low.
- A method of determining values of snubber components has been demonstrated. The method has been shown to work well, using the example of BUK7Y2R0-40H MOSFETs.
- Effects of snubber on EMI has been demonstrated with an example CISPR25 conducted emission measurement.
- Importance of correct component selection and good PCB design in term of snubber effectiveness has been discussed.

6. Appendix A; determining C_{LK} from C_{add}, f_{RING0} and f_{RING1}

We know that:

$$f_{RING0} = \frac{1}{2\pi\sqrt{L_{LK}\,C_{LK}}} \tag{28}$$

where f_{RING0} is the frequency of oscillation without a snubber in place and L_{LK} and C_{LK} are the parasitic inductances and capacitances respectively.

If we add capacitor C_{add} across Q2 drain-source, f_{RING0} is reduced by an amount "x" where:

$$\frac{f_{RING0}}{x} = \frac{1}{2\pi\sqrt{L_{LK}\left(C_{LK}+C_{add}\right)}} \tag{29}$$

therefore:

$$\frac{1}{2\pi\sqrt{L_{LK}\,C_{LK}}} = \frac{x}{2\pi\sqrt{L_{LK}\left(C_{LK}+C_{add}\right)}} \tag{30}$$

$$\frac{1}{\sqrt{L_{LK}\,C_{LK}}} = \frac{x}{\sqrt{L_{LK}\left(C_{LK}+C_{add}\right)}} \tag{31}$$

$$\sqrt{L_{LK}\,C_{LK}} = \frac{\sqrt{L_{LK}\left(C_{LK}+C_{add}\right)}}{x} \tag{32}$$

$$C_{LK} = \frac{C_{LK}+C_{add}}{x^2} \tag{33}$$

$$C_{LK}\,x^2 - C_{LK} = C_{add} \tag{34}$$

$$C_{LK}\,(x^2-1) = C_{add} \tag{35}$$

$$C_{LK} = \frac{C_{add}}{x^2-1} \tag{36}$$

where:

$$x = \frac{f_{RING0}}{f_{RING1}} \tag{37}$$

7. References

1. W. McMurray, "Optimum Snubbers for Power Semiconductors," in IEEE Transactions on Industry Applications, vol. IA-8, no. 5, pp. 593-600, Sept. 1972, doi: 10.1109/TIA.1972.349788.

8. Revision history

Table 1. Revision history

Revision number	Date	Description
3.0	2023-02-03	Various updates.
2.0	2021-05-18	Document revised to use latest Nexperia branding and legal information.
1.0	2012-04-25	Initial version.

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List of Tables

List of Figures

Contents

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Date of release: 3 February 2023