ND1160

IO-Link Device Transceiver

FEATURES

- IO-Link Compliant: COM1/2/3 available
- High-side, low-side, and push-pull operation can be configured
- Output Current 200 mA (min.)
- Operating Voltage Range 8.5 V to 36 V
- Over Current Protection < 500 mA
- Thermal Shutdown (TSD)
- Reverse Current Protection
- Package DFN3030-8-GG
  WLCSP-12-ZA1(UD)

GENERAL DESCRIPTION

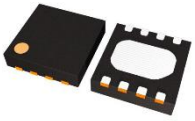
ND1160 is an IO-Link device transceiver using Bi-CMOS process.

The current capacity is 200 mA and the operating voltage range is guaranteed from 8.5 V to 36 V.

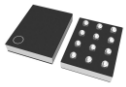
High-side, low-side, and push-pull operation can be set depending on the logic of the input terminal.

Compliant with IO-Link standard and can detect the status of connected devices.

In addition, the ND1160 is integrated the over current protection, the thermal shutdown and reverse current protection.



DFN3030-8-GG
3.0 mm × 3.0 mm × 0.75 mm

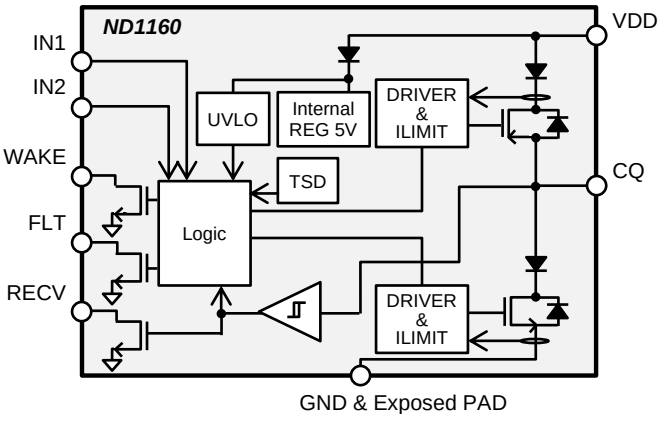


WLCSP-12-ZA1
1.76 mm × 2.26 mm × 0.65 mm

APPLICATIONS

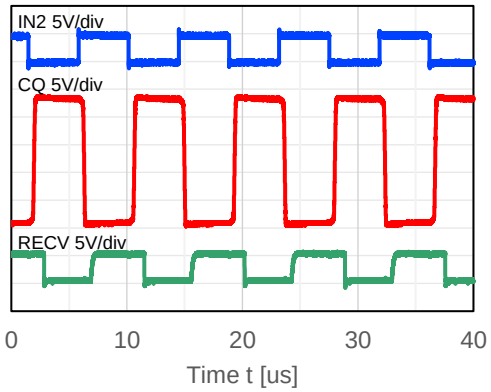
- Various sensors
- Programable logic controller
- Light curtain
- Actuator
- Others

BLOCK DIAGRAM



OPERATION EXAMPLE

VDD = 24 V, IN1 = 5.0 V, RL = 2 kΩ, CL = 5 nF
RECV Pulled up via 10kΩ to 5.0V



■ PRODUCT NAME INFORMATION

ND1160 aa c dd e

Description of Configuration

Composition	Item	Description
aa	Package Code	Indicates the package. GG : DFN3030-8-GG、ZA：WLCSP-12-ZA1
c	Version	Product version A: Specified value
dd	Packing	Taping direction. Refer to the packing specifications.
e	Grade	Indicates the quality grade.

Package code

aa	
GG	DFN3030-8-GG
ZA	WLCSP-12-ZA1

Version

c	
A	Specified value

Packaging

dd	
E4	Refer to the packing specifications.
E2	Refer to the packing specifications.

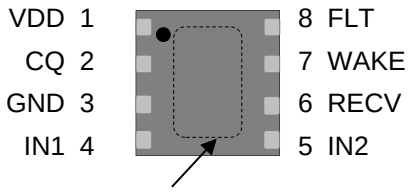
Grade

e	Applications	Operating Temperature Range	Test Temperature
D	Industrial equipment and Social infrastructures	− 40°C to 125°C	25°C, 125°C

■ ORDER INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	PLATING COMPOSITION	WEIGHT (mg)	QUANTITY (pcs/reel)
ND1160GGAE4D	DFN3030-8-GG	✓	✓	Sn2Bi	7.2	3000
ND1160ZAAE2D	WLCSP-12-ZA1	✓	✓	−	TBD	3000

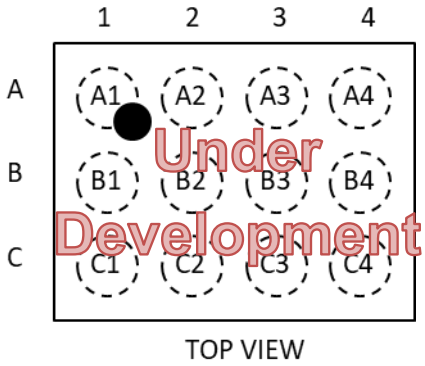
■ PIN DESCRIPTIONS (ND1160GG)



∗TAB on the bottom of the package is the silicon substrate level. Please be sure to connect to GND on the mounting board.

Pin No.	Pin Name	I/O	Description
DFN3030-8-GG			
1	VDD	Power	Power Supply Input Pin
2	CQ	I/O	CQ Driver Input/Output Pin
3	GND	-	Ground Pin
4	IN1	I	Input Pin 1
5	IN2	I	Input Pin 2
6	RECV	O	Receiver Pin, Open-Drain Output
7	WAKE	O	Wake-up Detection Pin, Open-Drain Output
8	FLT	O	Fault Output Pin, Open-Drain Output

■ PIN DESCRIPTIONS (ND1160ZA)



TOP VIEW

Pin No.	Pin Name	I/O	Description
WLCSP-12-ZA1			
A1	VDD	Power	Power Supply Input Pin
A2	CQ	I/O	CQ Driver Input/Output Pin
A3	GND	-	Ground Pin
A4	IN1	I	Input Pin 1
B1	GND	-	Ground Pin
B2	GND	-	Ground Pin
B3	GND	-	Ground Pin
B4	GND	-	Ground Pin
C1	FLT	O	Fault Output Pin, Open-Drain Output
C2	WAKE	O	Wake-up Detection Pin, Open-Drain Output
C3	RECV	O	Receiver Pin, Open-Drain Output
C4	IN2	I	Input Pin 2

■ ABSOLUTE MAXIMUM RATINGS

	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	− 60[*1] to + 60	V
CQ Pin Voltage	V_{CQ}	− 60[*1] to + 60	V
Input Pin Voltage	$V_{IN1/IN2}$	− 0.3 to + 7	V
RECV/WAKE/FLT Pin Voltage	$V_{RECV/WAKE/FLT}$	− 0.3 to + 7	V
Junction Temperature Range	Tj	− 40 to + 150	°C
Storage Temperature Range	T_{stg}	− 50 to + 150	°C

[*1] This is the guaranteed value when the power supply terminal, CQ terminal, and GND terminal are reversely connected.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

■ THERMAL CHARACTERISTICS

Package	Parameter	Measurement Result	Unit
DFN3030-8-GG	Thermal Resistance (θja)	190 at 2layer 58 at 4layer	°C / W
	Thermal Characterization Parameter (ψjt)	20 at 2layer 7 at 4layer	

θja : Junction-to-Ambient Thermal Resistance
ψjt : Junction-to-Top Thermal Characterization Parameter

4Layer Mounted on glass epoxy board (101.5 mm × 114.5 mm × 1.6 mm: based on EIA/JEDEC standard, 4-layer FR-4) with exposed pad.
(For 4-layer, applying 99.5 mm × 99.5 mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5.)

■ ELECTROSTATIC DISCHARGE RATINGS

	Conditions	Protection Voltage
HBM	C = 100pF, R = 1.5kΩ	±2000V
CDM		±1000V

ELECTROSTATIC DISCHARGE RATINGS
The electrostatic discharge test is done based on JEDEC JS001 and JS002. In the HBM method, ESD is applied using the power supply pin and GND pin as reference pins.

■ RECOMMENDED OPERATING CONDITIONS

	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	8.5 to 36	V
CQ Pin Voltage	V_{CQ}	0 to 36	V
Input Pin Voltage	$V_{IN1/IN2}$	0 to 5.5	V
RECV/WAKE/FLT Pin Voltage	$V_{RECV/WAKE/FLT}$	0 to 5.5	V
Output Current	I_{CQ}	0 to 200	mA
Operating Temperature Range	T_a	− 40 to + 125	°C

RECOMMENDED OPERATING CONDITIONS
All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

■ ELECTRICAL CHARACTERISTICS

V_{DD} = 24 V, C_{IN} = 1.0 µF, Ta = 25°C unless otherwise specified.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
General						
Supply Voltage	V_{DD}		8.5	24	36	V
Quiescent Current	I_{Q1}	IN1 = 0 V, IN2 = 0 V	–	1.5	2.3	mA
	I_{Q2}	IN1 = 5.0 V, IN2 = 0 V	–	1.5	2.3	mA
	I_{Q3}	IN1 = 5.0 V, IN2 = 5.0 V	–	1.5	2.3	mA
Driver Output Block						
Output Residual Voltage	V_{RCQH}	$I_{CQ\text{-}SOURCE}$ = 100 mA, IN1 = 5.0 V, IN2 = 0 V Ta = –40°C to +125°C	–	1.1	1.5	V
	V_{RCQL}	$I_{CQ\text{-}SINK}$ = 100 mA, IN1 = 5.0 V, IN2 = 5.0 V Ta = –40°C to +125°C	–	1.0	1.5	V
High-side Current Limit	I_{LIMITH}	V_{CQ} = 0 V, IN1 = 5.0 V, IN2 = 0 V Ta = –40°C to +125°C	200	350	500	mA
Low-side Current Limit	I_{LIMITL}	V_{CQ} = 24 V, IN1 = IN2 = 5.0 V Ta = –40°C to +125°C	-200	-350	-500	mA
Output Leak Current	$I_{LEAKCQH}$	V_{CQ} = 0 V, IN1 = IN2 = 0 V	–	–	3	µA
	$I_{LEAKCQL}$	V_{CQ} = 23 V, IN1 = IN2 = 0 V	–	–	50	µA
Driver Input Block						
IN1/IN2 Pin High Voltage	$V_{IH\_IN1/IH2}$		2.0	–	5.5	V
IN1/IN2 Pin Low Voltage	$V_{IL\_IN1/IH2}$		0	–	0.8	V
Input Pulldown Resistance	R_{INPD}		60	100	140	kΩ
Driver Under Voltage Lock Out (UVLO) Block						
UVLO Release Voltage	V_{UVLO2}	V_{DD} = L → H	6.0	7.3	8.5	V
UVLO Operating Voltage	V_{UVLO1}	V_{DD} = H → L	5.6	6.9	8.1	V
UVLO Hysteresis Voltage	ΔV_{UVLO}	$V_{UVLO2} - V_{UVLO1}$	–	0.4	–	V
Driver Output Rise / Fall Time						
Output Rise Time	tr	R_L = 2 kΩ, C_L = 5 nF	–	100	–	ns
Output Fall Time	tf	R_L = 2 kΩ, C_L = 5 nF	–	100	–	ns
Output Rise Propagation Delay Time	t_{td_ON}	R_L = 2 kΩ, C_L = 5 nF	–	630	–	ns
Output Fall Propagation Delay Time	t_{td_OFF}	R_L = 2 kΩ, C_L = 5 nF	–	630	–	ns
Receiver Block						
RECV H Threshold Voltage	V_{THH}	IN1 = IN2 = 0 V Ta = –40°C to +125°C	10.5	12.0	13.0	V
RECV L Threshold Voltage	V_{THL}	IN1 = IN2 = 0 V Ta = –40°C to +125°C	8.0	9.75	11.5	V
RECV Hysteresis Voltage	V_{HYS}	*2	–	2.25	–	V
RECV Rise Propagation Delay Time	t_{rd_ON}	*2	–	650	–	ns
RECV Fall Propagation Delay Time	t_{rd_OFF}	*2	–	850	–	ns
RECV Pin Low Level Voltage	V_{L_RV}	I_{RECV} = 500 µA, V_{CQ} = 24 V	–	55	500	mV
RECV Pin Leak Current at OFF status	I_{LEAK_RV}	V_{RECV} = 5.5 V, V_{CQ} = 0 V	–	–	1	µA
WAKE-UP Block						
WAKE-UP Detection Minimum Pulse Width	t_{WMIN}	*2 Ta = –40°C to +125°C	30	40	75	µs
WAKE-UP Detection Maximum Pulse Width	t_{WMAX}	*2 Ta = –40°C to +125°C	85	100	138	µs
WAKE-UP Flag Time	t_W	*2	200	270	300	µs
WAKE Pin Low Level Voltage	V_{L_WK}	I_{WAKE} = 500 µA, V_{OUT} = 24V, 80 µs Pulse	–	55	380	mV
WAKE Pin Leak Current at OFF status	I_{LEAK_WK}	V_{WAKE} = 5.5 V	–	–	1	µA

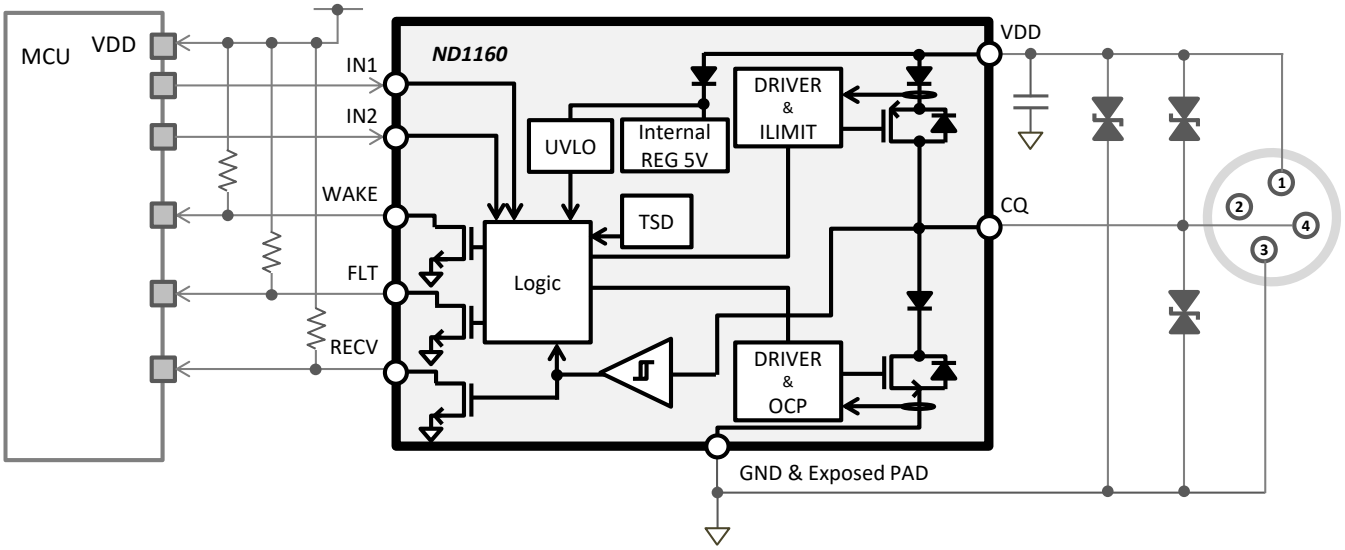
■ ELECTRICAL CHARACTERISTICS

V_{DD} = 24 V, C_{IN} = 1.0 µF, Ta = 25°C unless otherwise specified.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Fault Block						
Over Current Detection Blanking Time	t_{OCPD}	*2	0.9	1.2	1.5	ms
Over Current Detection Auto Recovery Time	t_{OCPR}	*2	2.8	3.7	4.6	ms
FLT Pin Low Level Voltage	I_{LEAK_FL}	I_{FLT} = 500 µA	–	55	110	mV
FLT Pin Leak Current at OFF status	V_{L_FL}	V_{FLT} = 5.5 V, V_{DD} = 5.5 V	–	–	1	µA

*2: Refer to Timing Chart

■ TYPICAL APPLICATION CIRCUIT



ND1160 Typical Application Circuit

■ **PIN OPERATIONAL FUNCTION TABLE (TRUTH TABLE)**

RECV/WAKE/FLT Pin Pulled up via 10kΩ to 5.0V

Output Block

	INPUT		OUTPUT		
Operating Status	**IN1**	**IN2**	**High Side Switch**	**Low Side Switch**	**CQ**
Low side (N-ch) Output					
Normal	L	H	OFF	OFF	Z*3
	H	H	OFF	ON	L
High side (P-ch) Output					
Normal	L	L	OFF	OFF	Z*3
	H	L	ON	OFF	H
Push pull Output					
Normal	H	L	ON	OFF	H
	H	H	OFF	ON	L
	L	X	OFF	OFF	Z*3
At Error Detection					
TSD	X	X	OFF	OFF	Z*3
UVLO	X	X	OFF	OFF	Z*3
OCP*4	X	X	OFF	OFF	Z*3

Receiver Block

	INPUT			OUTPUT		
Operating Status	**IN1**	**IN2**	**CQ**	**RECV**	**WAKE**	**FLT**
Normal	X	X	L	Z	Z	L
	X	X	H	L	Z	L
WAKE-UP Pulse *4	H	L	L Pulse	Z Pulse	L Pulse	L
	H	H	H Pulse	L Pulse	L Pulse	L
TSD	X	X	X	X	Z	Z
UVLO	X	X	X	X	Z	Z
OCP *4	X	X	X	X	Z	Z

X: Don't care

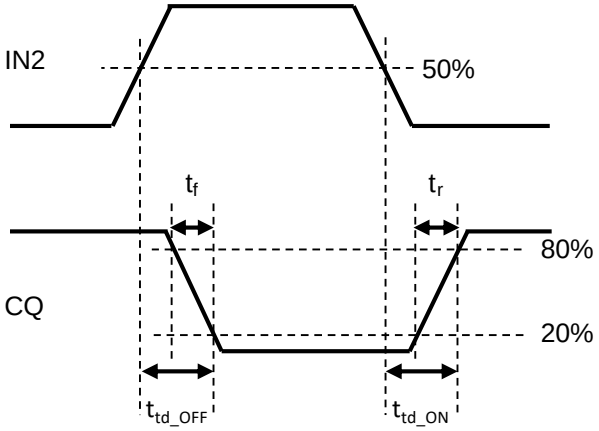
*3: Weak Pull Down

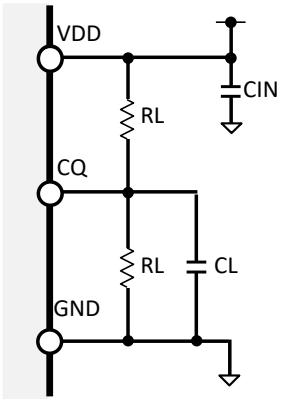
*4: Refer to Timing Chart

■ **TIMING CHART**

Unless other noted, RECV/WAKE/FLT Pin Pulled up via 10kΩ to 5.0V

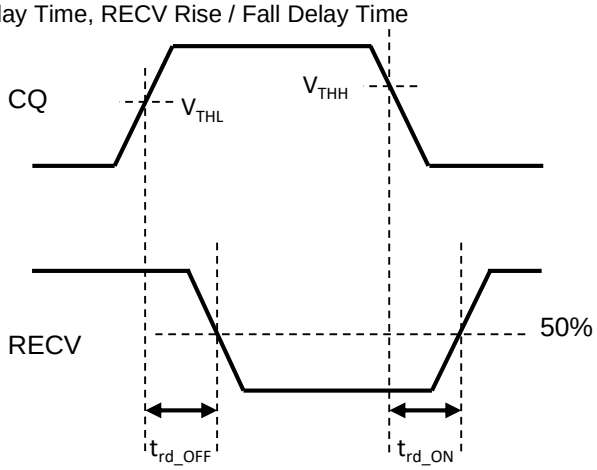
・Output Rise / Fall Time, Output Rise / Fall Propagation Delay Time
Condition: IN1 = H





Measurement Circuit

・RECV Rise / Fall Propagation Delay Time, RECV Rise / Fall Delay Time

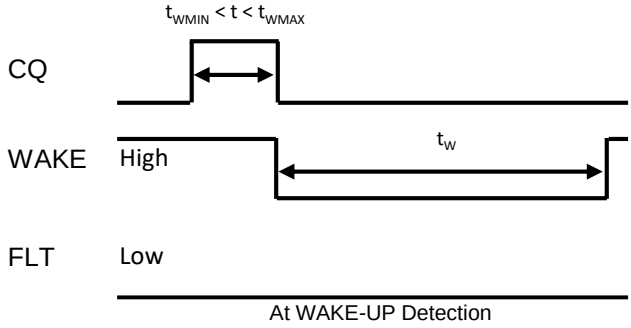


■ **TIMING CHART**

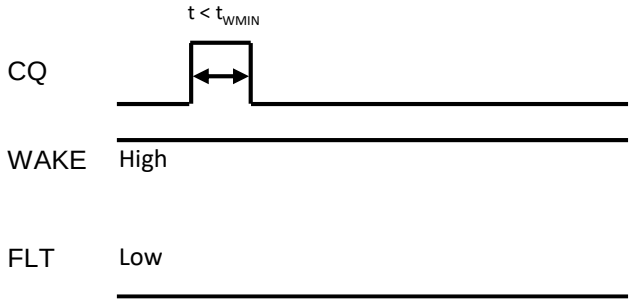
・WAKE-UP Detection

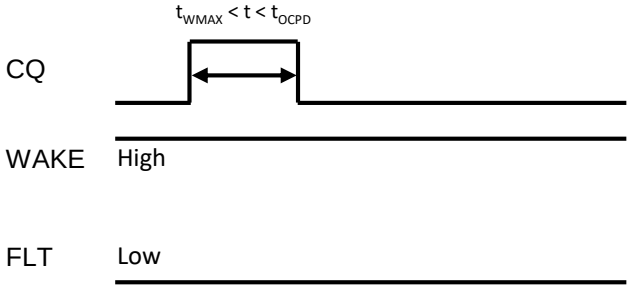
IN1 = H, IN2 = H

(In case of IN1 = H, IN2 = L, The CQ pin in the figure below operates in inverse logic.)



At WAKE-UP Detection



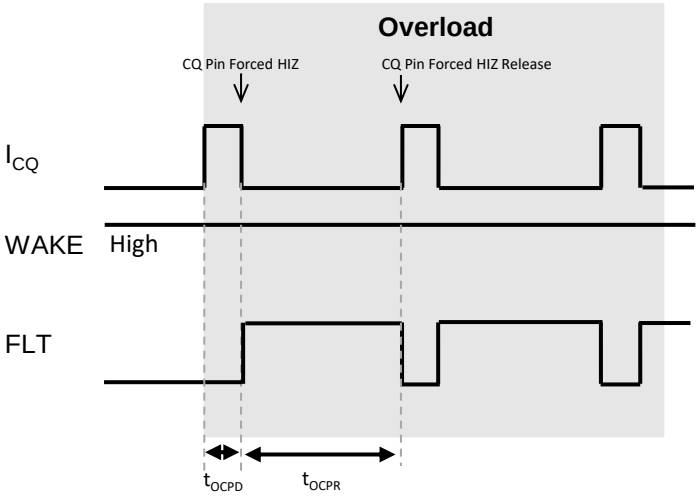


WAKE-UP` Non Detection

・Over Current Detection

IN1 = H, IN2 = H

(In case of IN1 = H, IN2 = L, The I_{CQ} in the figure below is reversed.)



■ APPLICATION NOTE

・Driver output block

Depending on the combination of IN1 and IN2, the ND1160 can support three output methods from the CQ terminal: low side (N-ch), high side (P-ch), and push-pull. Please refer to the PIN OPERATIONAL FUNCTION TABLE (TRUTH TABLE) for details.

When IN1 is L, both the high side switch and low side switch are OFF, resulting in Hi-Z output. During Hi-Z output, the CQ pin is weakly pulled down inside the IC. The pull-down current is defined by the low-side output leakage current ($I_{LEAKCQL}$).

・Receiver block

ND1160 has a built-in receiver to monitor the logic of the CQ pin with the RECV pin. The RECV pin is an open drain output, so please pull it up to an external power supply. By pulling up the RECV pin with the MCU's power supply voltage, it is possible to input the logic of the CQ pin to the MCU via the RECV pin. Please note that the logic between RECV and CQ pins is inverted. The logic threshold of the CQ terminal is defined by the receive H/L threshold voltage (V_{THH}, V_{THL}). The threshold decreases proportionally with the VDD terminal voltage in regions where the VDD terminal voltage is 18V (typ.) or lower.

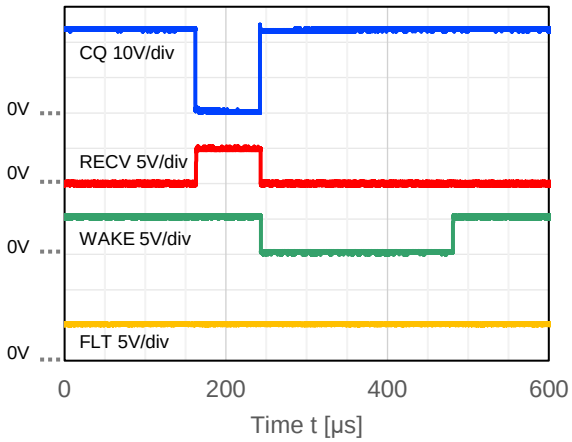
・Reverse current protection

To prevent damage to the IC and peripheral components due to incorrect connection of the IO-Link M5, M8, and M12 connectors, the ND1160 is equipped with reverse polarity protection. As shown in the block diagram, a reverse current blocking diodes are inserted to prevent current from flowing when the VDD, CQ, and GND pins are reversely connected. The leakage current is less than 20μA (typ.) when the voltage between pins is 36V.

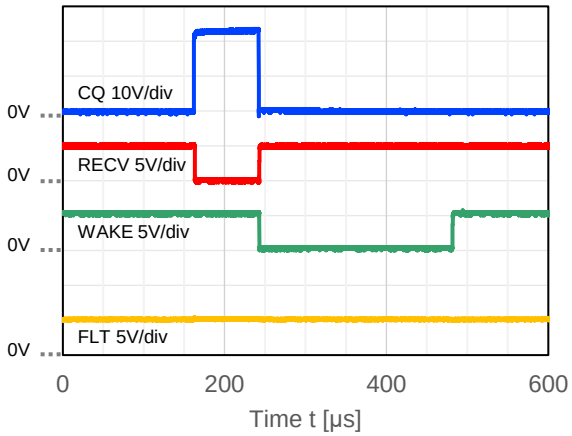
・Wake-up detection

ND1160 can detect wake-up through the WAKE pin in any case of low-side, high-side and push-pull. The WAKE pin is an open drain output, so please pull it up to an external power supply. The Wake-Up signal is a signal sent by the master that requests the start of IO-Link communication. When receiving the Wake-Up signal from the IO-Link master, the FET of the WAKE pin turns on and outputs a low-level pulse with a width of 270μs (typ.).

The Wake-Up signal is a single current pulse of ±500mA or more and 80us wide. When the potential of CQ pin is reversed by the current pulse, the ND1160 measures the width of this pulse. If the pulse width is greater than or equal to the minimum pulse width for wake-up detection (t_{WMIN}) and less than or equal to the maximum pulse width for wake-up detection (t_{WMAX}), it is determined that a wake-up signal has been received.



At CQ = H Wake-Up signal detection waveform
IN1 = 5 V, IN2 = 0 V
RECV,WAKE,FLT Pulled up via 10kΩ to 5.0V



At CQ = L Wake-Up signal detection waveform
IN1 = 5 V, IN2 = 5 V
RECV,WAKE,FLT Pulled up via 10kΩ to 5.0V

■ **APPLICATION NOTE**

・Overcurrent protection

ND1160 has constant current and automatic resetauto-recovery type overcurrent protection. When the current flowing to the CQ terminal increases due to a load short circuit, the value is limited to below the high-side overcurrent limit (I_{LIMITH}) or the low-side overcurrent limit (I_{LIMITL}). If the current limit state continues for longer than the overcurrent detection blanking time (t_{OCPD}), both the high-side switch and low-side switch are turned OFF, resulting in Hi-Z output. If the overcurrent detection auto-matic recovery time (t_{OCPR}) or more elapses after the output becomes HI-Z, the Hi-Z state is released canceled and normal operation is resumedresumes. If the overload condition continues even after recovery, the above operation will be repeated.

・Thermal shutdown (TSD)

When the ND1160 chip temperature exceeds 165°C (typ.), the thermal shutdown function activates and the CQ pin becomes Hi-Z output. To restore operation, lower the chip temperature to 150°C (typ.) or lower. The thermal shutdown function is a backup circuit to prevent IC thermal runaway at high temperatures, and does not compensate for improper thermal design. It is recommended to provide sufficient margin to operate within the IC junction temperature (~150°C) range.

・Under voltage lock out (UVLO)

When the power supply voltage is low, the IC operation is stopped by the UVLO circuit, and when VDD=7.3V (typ.) or higher, the UVLO circuit is released and the IC starts operating. A hysteresis voltageof 0.4V (typ.) is provided for the rise and fall of the power supply voltage. This prevents the fluctuation of UVLO release and operation, ensuring stable operation of the ND1160.

・External TVS diode

To comply with EMC standards such as IEC61004-2, IEC61004-4, IEC61004-5 and impulse noise testing, connect protection elements such as TVS between the CQ, VDD, and GND pins. Please refer to TYPICAL APPLICATION CIRCUIT for connection examples. In order to support a wide range of TVS, the VDD and CQ pins of the ND1160 have a high withstand voltage, but when selecting a TVS, please be careful that the clamp voltage during surge application does not exceed the maximum rating of the ND1160.

・FAULT signal output

If there is an abnormality in the operation of ND1160, a signal will be output from the FLT terminal. The FLT pin is an open drain output, so please pull it up to an external power supply. During normal operation, the FET tuens ON and the voltage is low, while during abnormal operation, the FET is OFF and the voltage is high.

The information reflected as a FAULT signal is as follows.

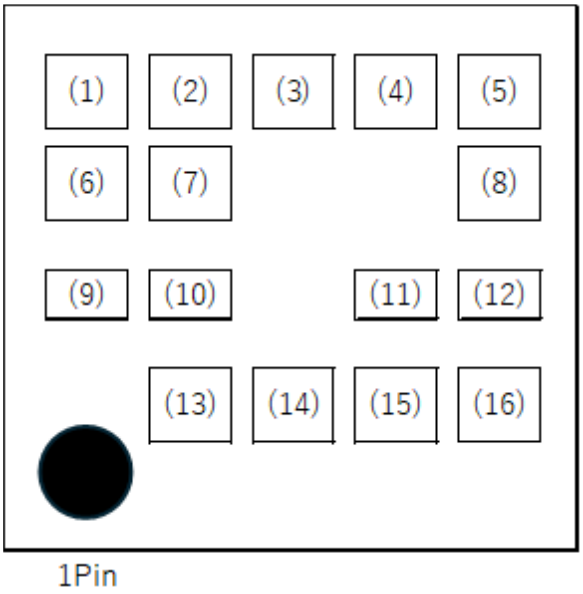
- Operation stop due to under voltage lockout (UVLO)
- CQ pin Hi-Z output due to overcurrent protection
- Thermal shutdown

・Implementation and Use of Components

Connect the back pad of the DFN package to the GND pin as short as possible. Place the bypass capacitor for the power supply terminal close to the VDD terminal and connect it to ensure the shortest current loop with GND. The standard bypass capacitor is a 1.0μF/100V MLCC, but ensure a larger capacity according to the load characteristics and application environment.
Since the WAKE, FLT, and RECV pins are open-drain outputs, the waveform may become blunt due to parasitic capacitance between them and the ground plane. We recommend that the wiring for each terminal as short as possible.

■ MARKING SPECIFICATION

(1)(2)(3)(4)(5)(6)(7): Product Code ⋯ **Refer to the following table**
(8) to (16): Lot Number ⋯ Alphanumeric Serial Number



ND1160GGAE4D Marking Specification

NOTICE
There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

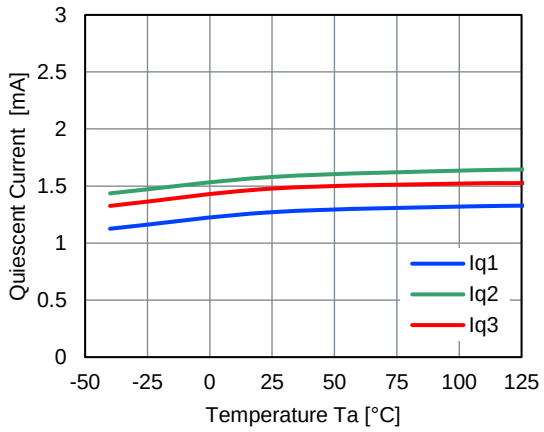
ND1160 Marking List (DFN3030-8-GG)

Product Name	(1)	(2)	(3)	(4)	(5)	(6)	(7)
ND1160GGAE4D	D	1	1	6	0	A	D

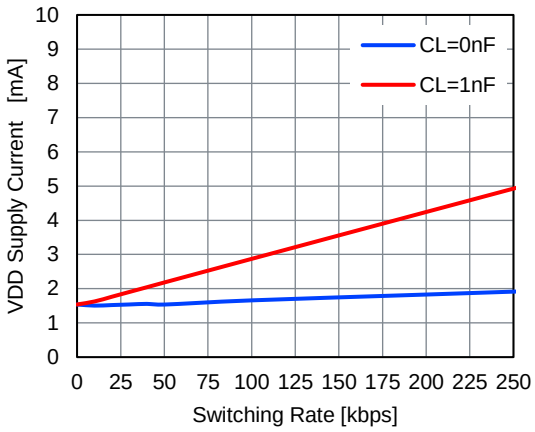
■ TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.
V_{DD} = 24 V, Ta = 25 °C

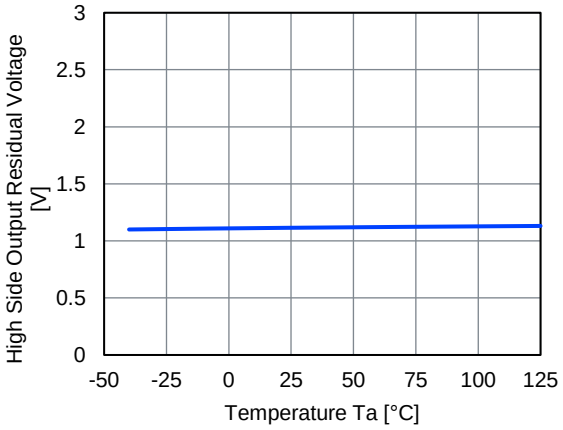
Quiescent Current vs VDD Input Voltage



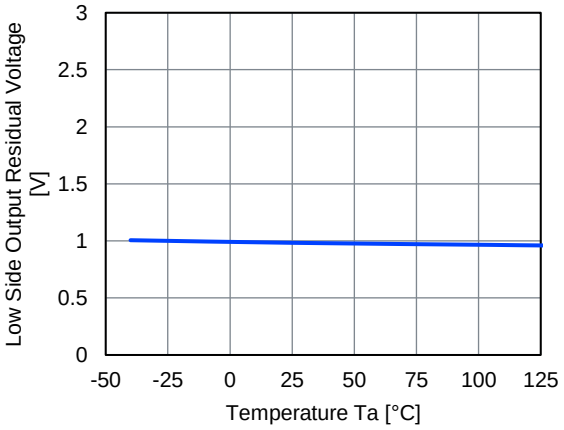
VDD Supply Current vs Switching Rate
IN1=5.0V, IN2 = 0 to 5.0 Switching



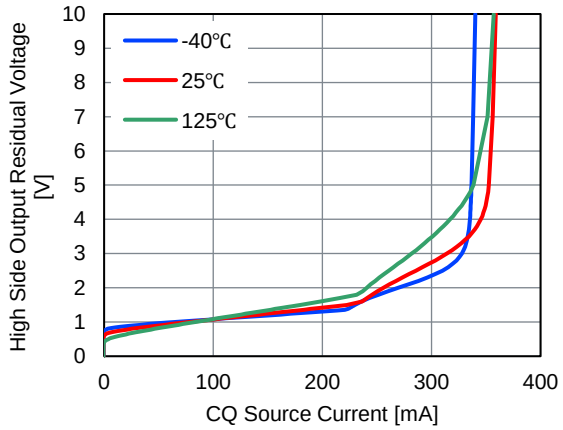
High Side Output Residual Voltage vs Temperature
IN1=5.0V, IN2=0V $I_{CQ\text{-}SOURCE}$=100 mA



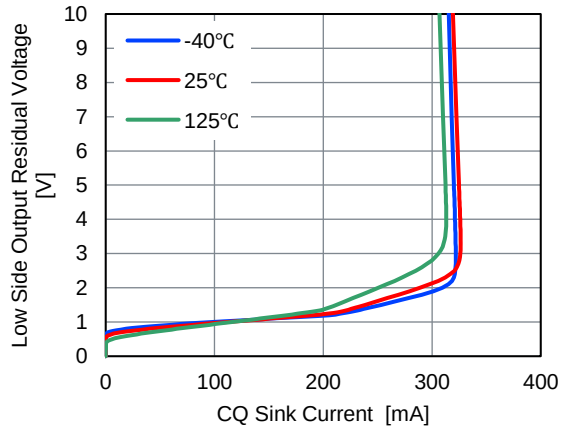
Low Side Output Residual Voltage vs Temperature
IN1=5.0V, IN2=5.0V $I_{CQ\text{-}SINK}$=100 mA



High Side Output Residual Voltage vs CQ Source Current
IN1=5.0V, IN2=0V



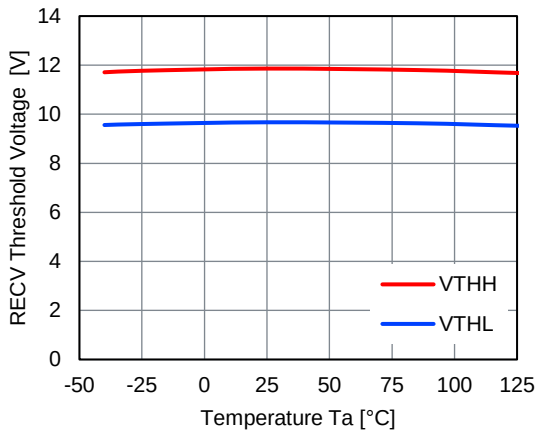
Low Side Output Residual Voltage vs CQ Sink Current
IN1=5.0V, IN2=5.0V



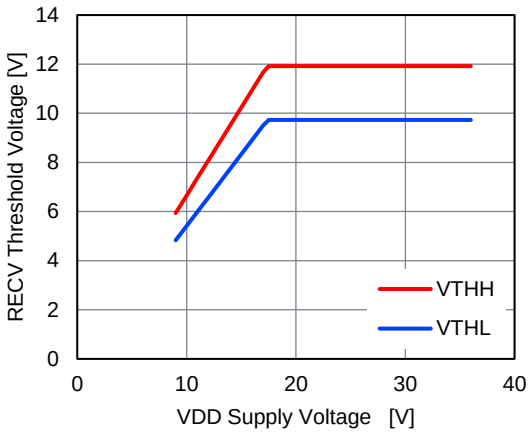
■ TYPICAL CHARACTERISTICS

Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.
V_{DD} = 24 V, Ta = 25 °C

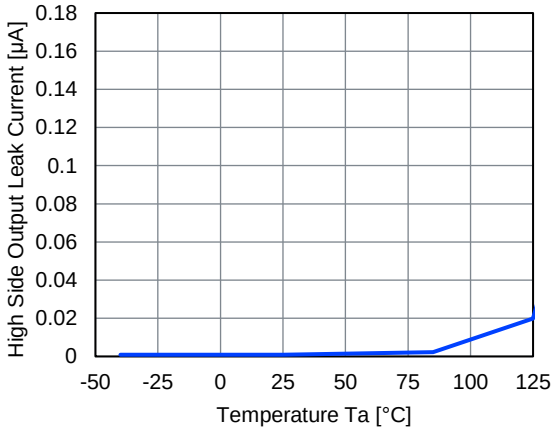
RECV Threshold Voltage vs Temperature
IN1=IN2=0V



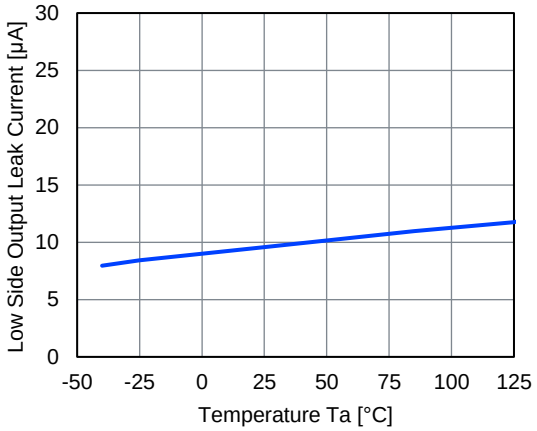
RECV Threshold Voltage vs VDD Supply Voltage
IN1=IN2=0V



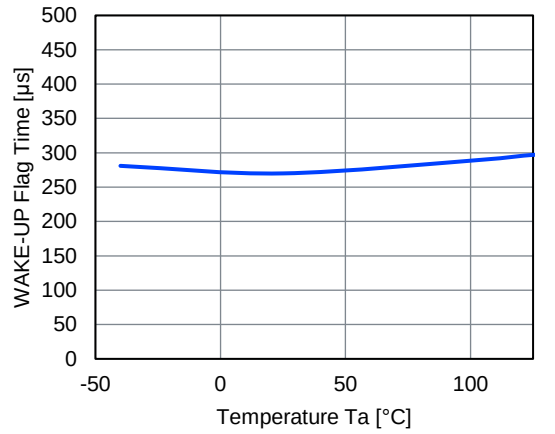
High Side Output Leak Current vs Temperature
V_{CQ}=0V IN1=IN2=0V



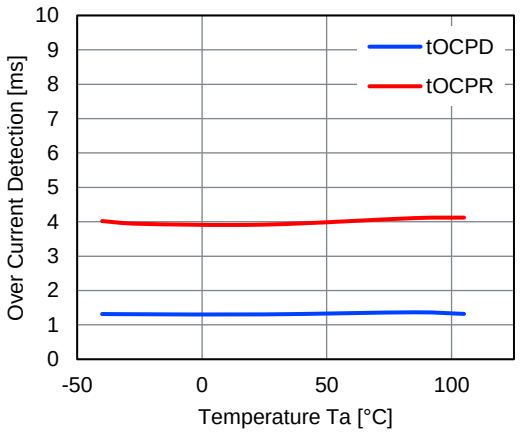
Low Side Output Leak Current vs Temperature
V_{CQ}=23V, IN1= IN2=0V



WAKE-UP Flag Time vs Temperature



Over Current Detection Time vs Temperature



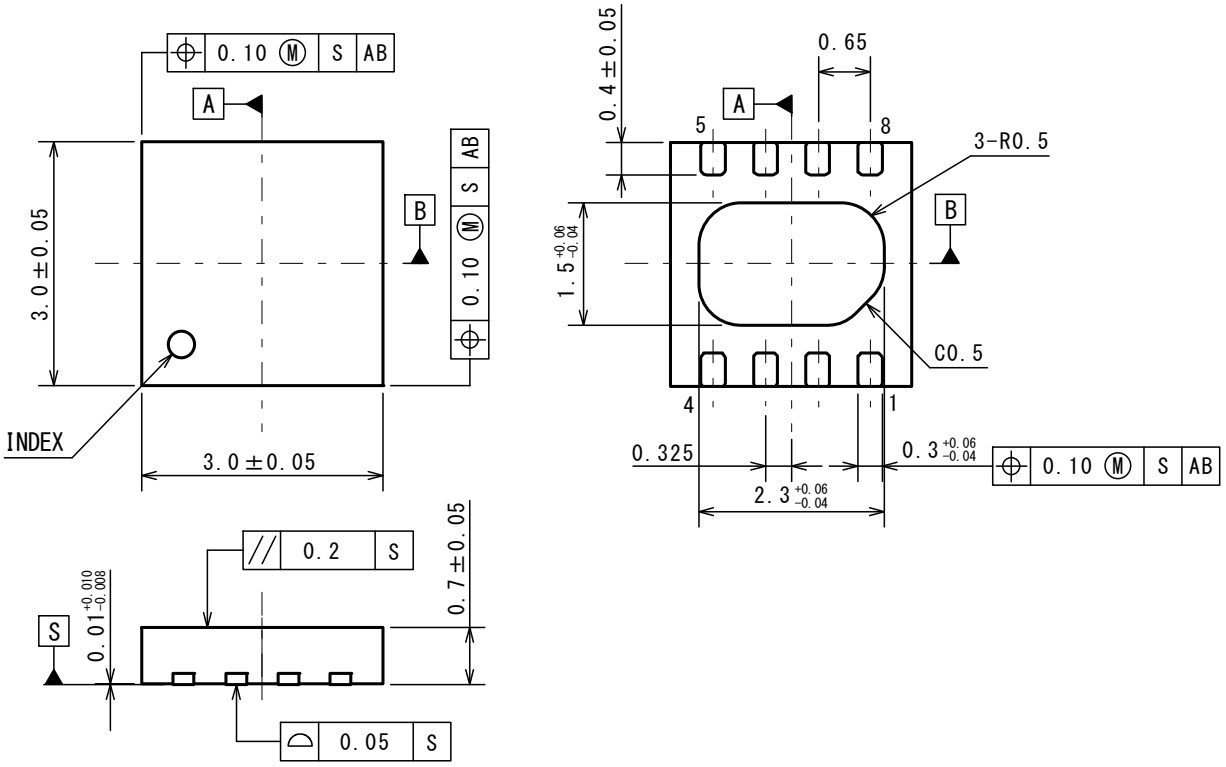
Nisshinbo Micro Devices Inc.

DFN3030-8-GG

PI-DFN3030-8-GG-E-B

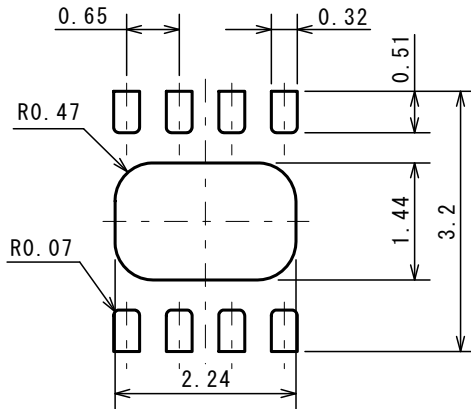
■ PACKAGE DIMENSIONS

UNIT: mm



■ EXAMPLE OF SOLDER PADS DIMENSIONS

UNIT: mm



Nisshinbo Micro Devices Inc.

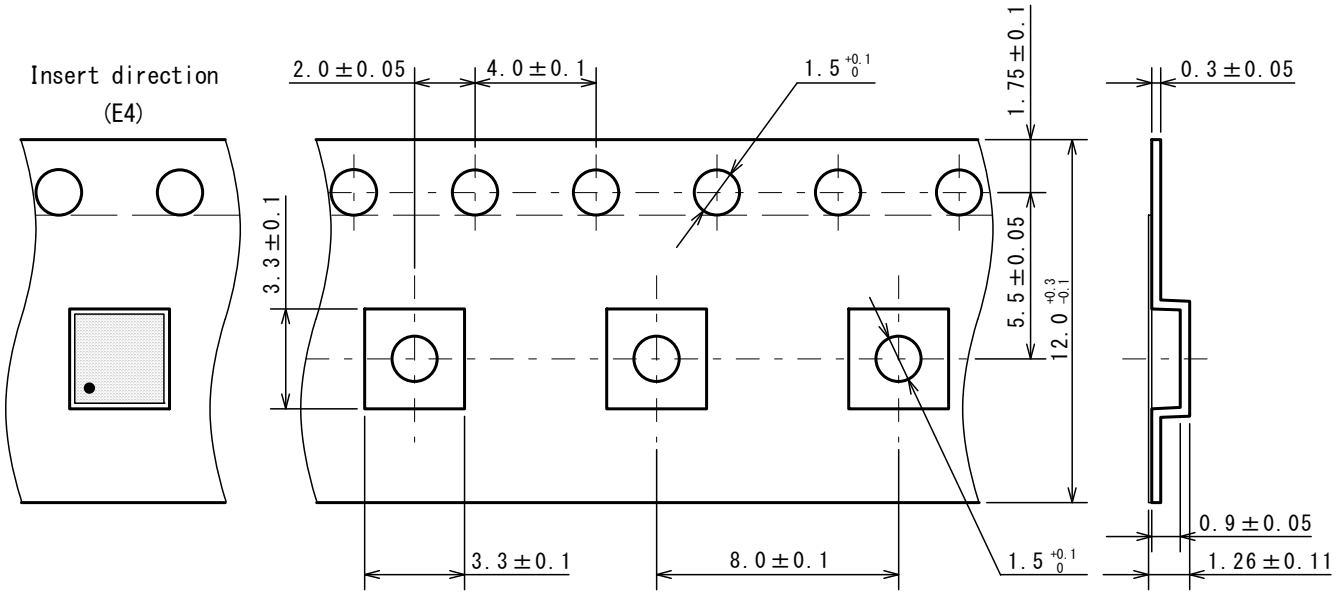
DFN3030-8-GG

PI-DFN3030-8-GG-E-B

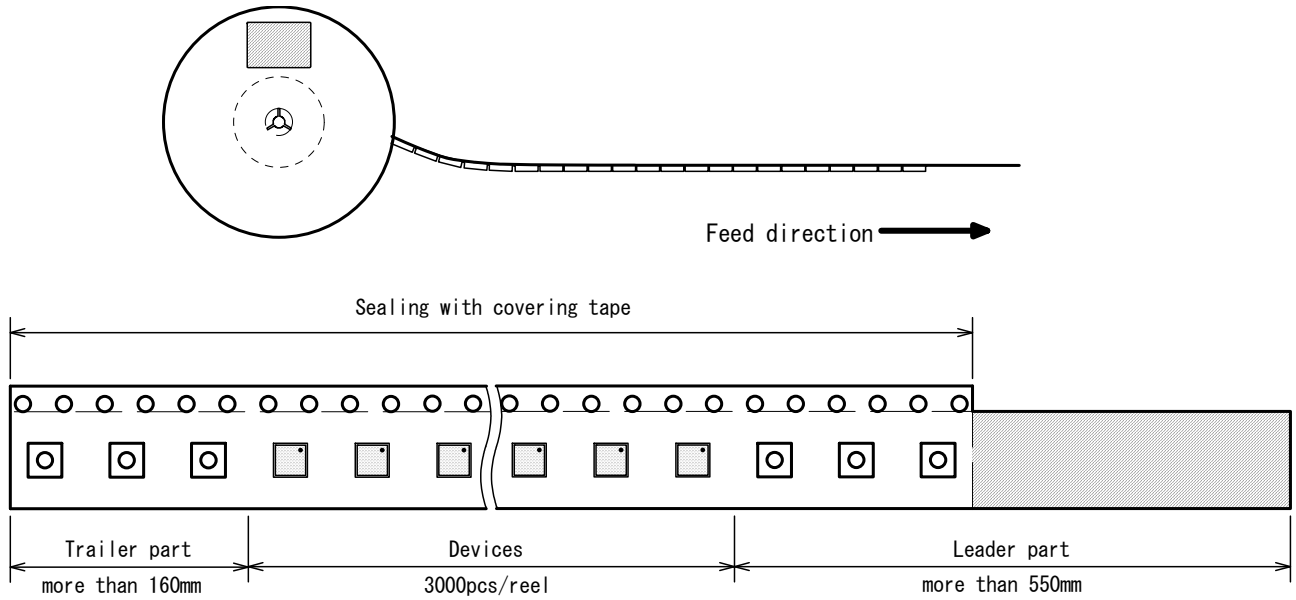
■ PACKING SPEC

UNIT: mm

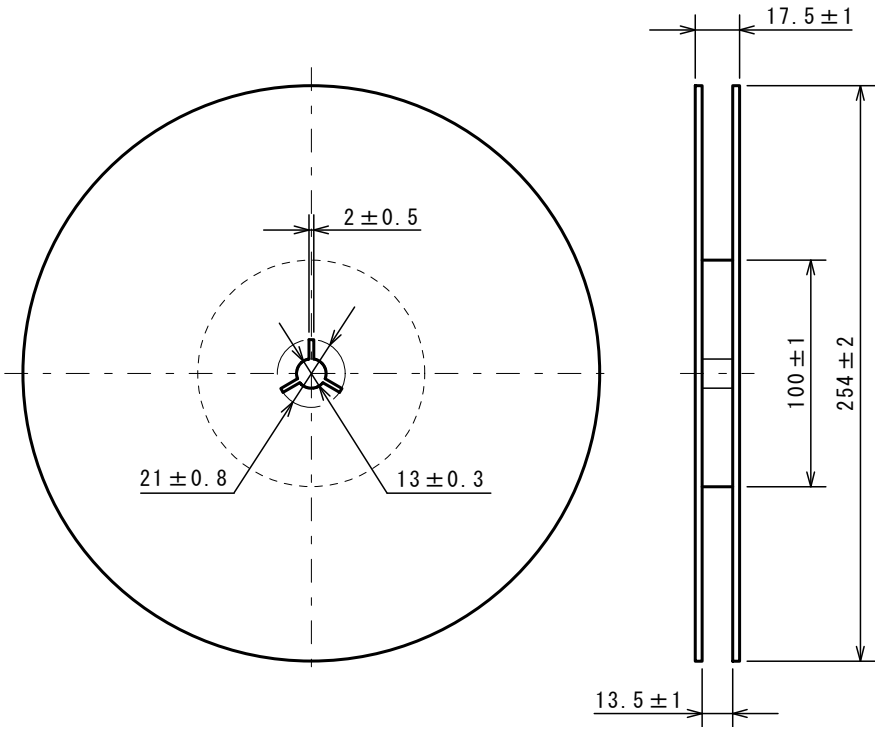
(1) Taping dimensions / Insert direction



(2) Taping state



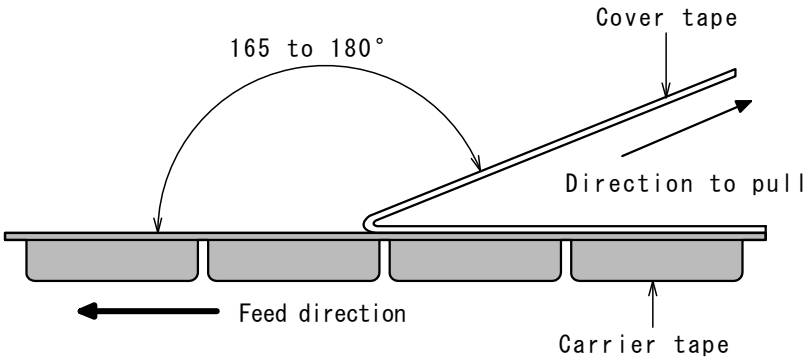
(3) Reel dimensions



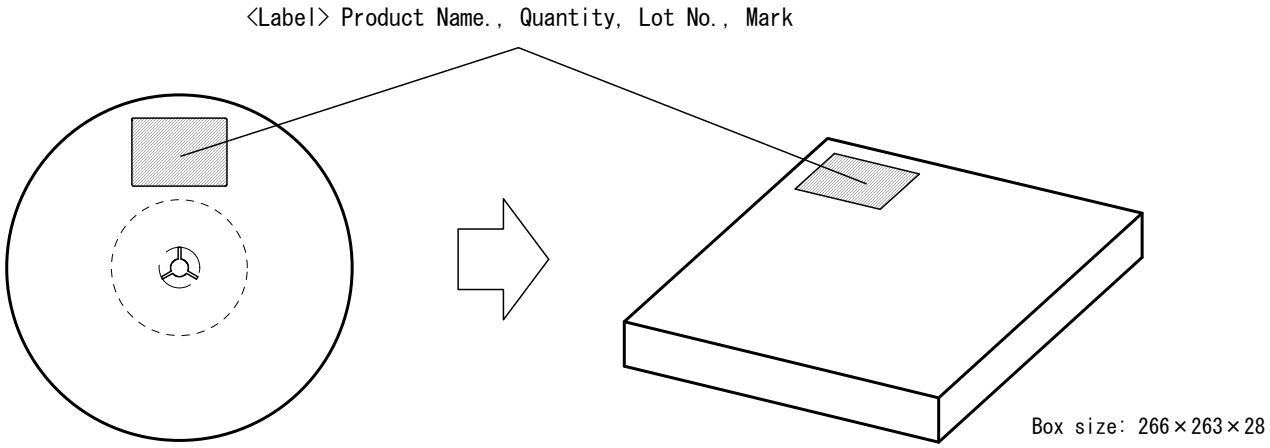
(4) Peeling strength

Peeling strength of cover tape

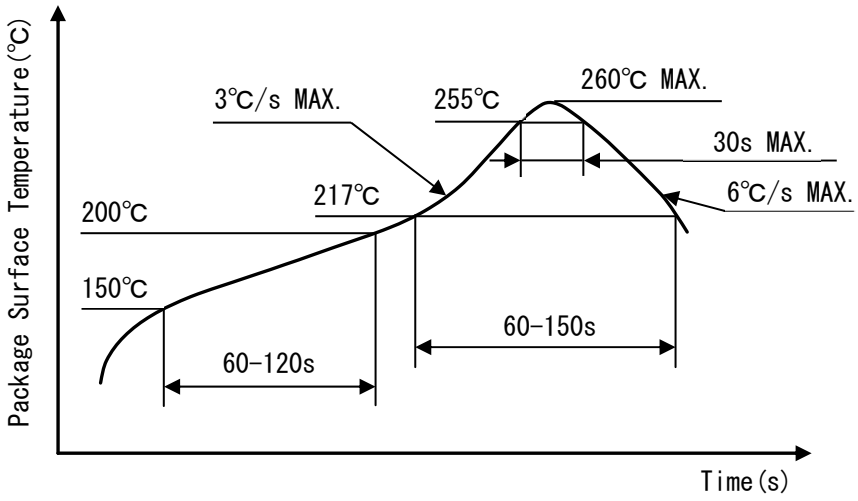
- Peeling angle 165 to 180° degrees to the taped surface.
- Peeling speed 300mm/min
- Peeling strength 0.1 to 1.3N



(5) Packing state



■ **HEAT-RESISTANCE PROFILES**



Reflow profile

■ Revision History

Date	Revision	Changes
June 18, 2024	Ver. 1.0	Initial release

1. The products and the product specifications described in this document are subject to change or discontinuation of production without notice for reasons such as improvement. Therefore, before deciding to use the products, please refer to our sales representatives for the latest information thereon.
2. The materials in this document may not be copied or otherwise reproduced in whole or in part without the prior written consent of us.
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    - Aerospace Equipment
    - Equipment Used in the Deep Sea
    - Power Generator Control Equipment (nuclear, steam, hydraulic, etc.)
    - Life Maintenance Medical Equipment
    - Fire Alarms / Intruder Detectors
    - Vehicle Control Equipment (automotive, airplane, railroad, ship, etc.)
    - Various Safety Devices
    - Traffic control system
    - Combustion equipment

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6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order to prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
7. The products have been designed and tested to function within controlled environmental conditions. Do not use products under conditions that deviate from methods or applications specified in this datasheet. Failure to employ the products in the proper applications can lead to deterioration, destruction or failure of the products. We shall not be responsible for any bodily injury, fires or accident, property damage or any consequential damages resulting from misuse or misapplication of the products.
8. Quality Warranty
    8-1. Quality Warranty Period
    In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.
    8-2. Quality Warranty Remedies
    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
    8-3. Remedies after Quality Warranty Period
    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
9. Anti-radiation design is not implemented in the products described in this document.
10. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
11. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
12. Warning for handling Gallium and Arsenic (GaAs) products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
13. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.

NISSHINBO

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