MSA303 • MSA303A

High Voltage Integrated Power Module

RoHS COMPLIANT

FEATURES

- 40 A Continuous Output Current
- Up to 1 MHz Switching Frequency
- 600 V Supply Voltage
- Internal Bootstrap Operation
- Under-Voltage Lockout
- Active Miller Clamping

APPLICATIONS

- Motor Control
- Variable Frequency Drives
- DC/AC converters
- Power Inverters
- Test Equipment

DESCRIPTION

The MSA303 is a fully integrated three-phase driver designed primarily to drive Brush-Less DC (BLDC), Permanent Magnet Synchronous (PMSM) motors or, DC/AC converters. The module uses Silicon Carbide MOSFET technology to improve efficiency over other devices in its class. Three fully independent half-bridges provide 40 A of continuous current. MSA303 is built on a thermally conductive, but electrically isolated substrate to provide the most versatility and ease in heatsinking.

Protection features include under-voltage lockout (UVLO) function and active Miller clamping to improve reliability. Also included in the module are Silicon Carbide Schottky Barrier free-wheeling diodes in parallel to the body diode of each MOSFET. No external output protection diodes are required.

MSA303's integrated gate drivers provide isolation between the inputs and high-voltage outputs. By integrating the gate drive with the output MOSFETs, parasitics that impact the switching behavior are kept at a minimum, improving the switching characteristics while reducing potential oscillations.

Figure 1: Equivalent Schematic

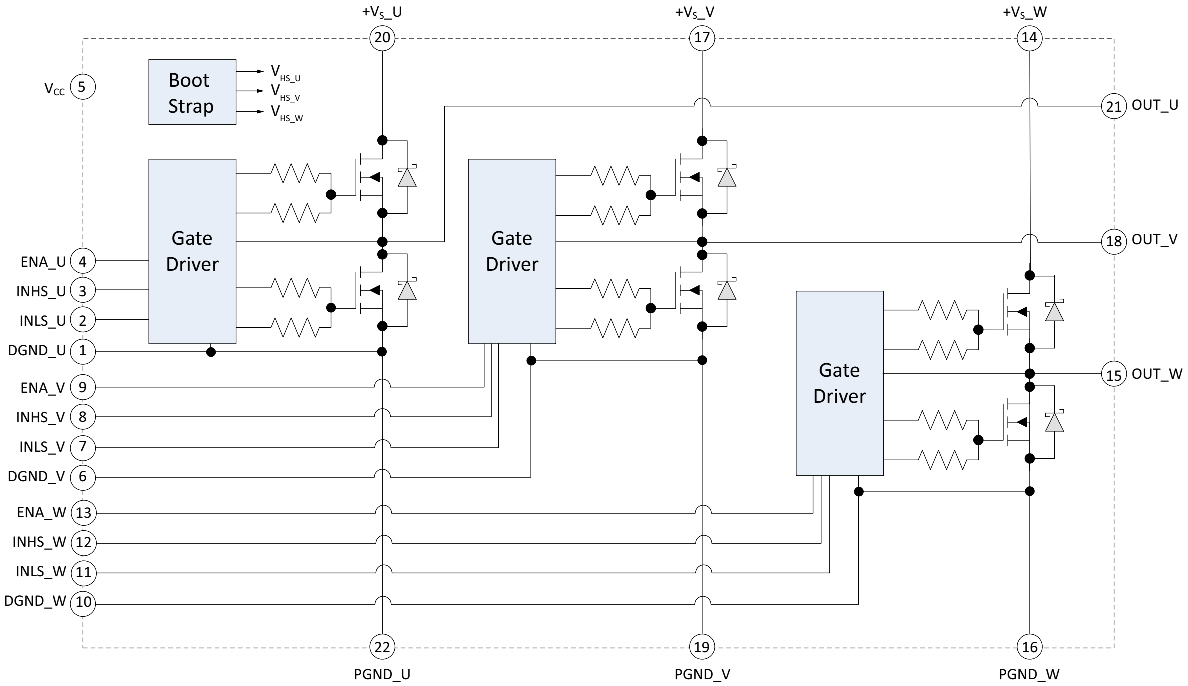
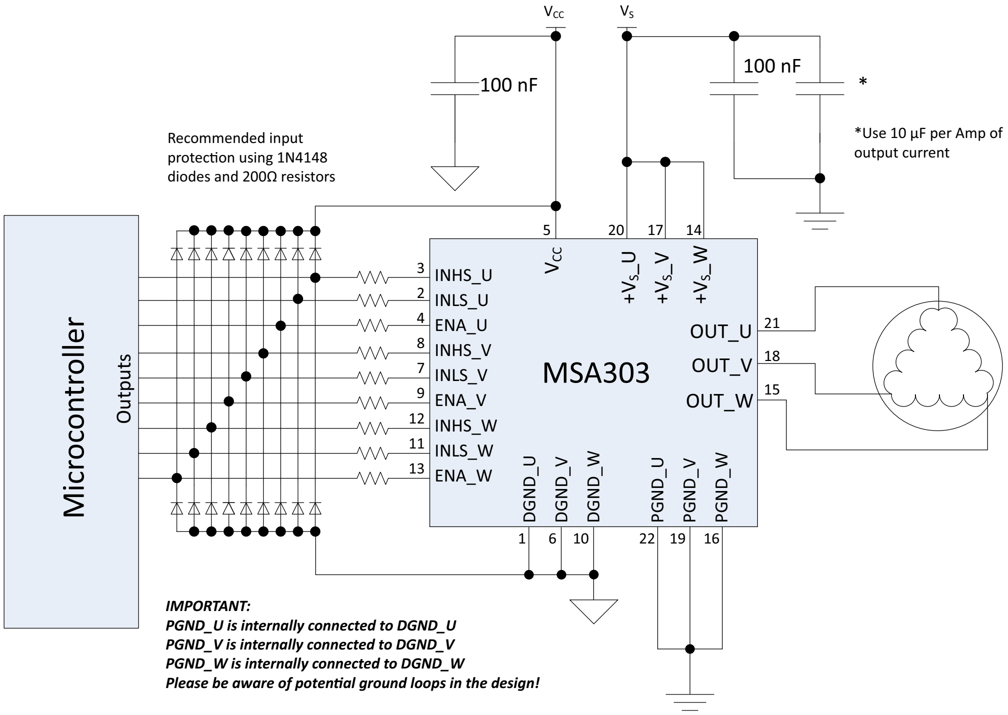


Figure 2: Typical Connection



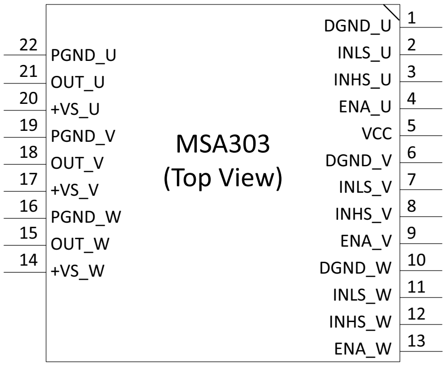
*Use 10 µF per Amp of output current

Recommended input protection using 1N4148 diodes and 200Ω resistors

IMPORTANT:
PGND_U is internally connected to DGND_U
PGND_V is internally connected to DGND_V
PGND_W is internally connected to DGND_W
Please be aware of potential ground loops in the design!

PINOUT AND DESCRIPTION TABLE

Figure 3: Pinout Diagram



Pin Number	Name	Description
1	DGND_U	Return path for digital circuit. Connected internally to PGND_U
2	INLS_U	Input signal to command channel U low-side FET
3	INHS_U	Input signal to command channel U high-side FET
4	ENA_U	Output enable channel U. Drive HIGH to enable. A LOW signal will cause the output of channel U to be high impedance
5	V_{CC}	Voltage supply for logic circuit. The ground terminal of the supply must be connected to at least one of the DGND pins
6	DGND_V	Return path for digital circuit. Connected internally to PGND_V
7	INLS_V	Input signal to command channel V low-side FET
8	INHS_V	Input signal to command channel V high-side FET
9	ENA_V	Output enable channel V. Drive HIGH to enable. A LOW signal will cause the output of channel V to be high impedance
10	DGND_W	Return path for digital circuit. Connected internally to PGND_W
11	INLS_W	Input signal to command channel W low-side FET. Drive pin HIGH to sink current through OUT_W.
12	INHS_W	Input signal to command channel W high-side FET. Drive pin HIGH to source current through OUT_V.
13	ENA_W	Output enable channel W. Drive HIGH to enable. A LOW signal will cause the output of channel W to be high impedance
14	$+V_S$_W	High-voltage supply for channel W
15	OUT_W	Output of channel W
16	PGND_W	Return path for channel W. Signal is internally connected to DGND.
17	$+V_S$_V	High-voltage supply for channel V
18	OUT_V	Output of channel V
19	PGND_V	Return path for channel V. Signal is internally connected to DGND.
20	$+V_S$_U	High-voltage supply for channel U
21	OUT_U	Output of channel U
22	PGND_U	Return path for channel U. Signal is internally connected to DGND.

SPECIFICATIONS

Unless otherwise noted: T_C = 25 °C. Power supply voltages are typical ratings.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Total Supply Voltage	$+V_S$ to PGND		650	V
Logic Supply Voltage	V_{CC}		22	V
Logic Supply Surge Voltage, t_{SURGE} < 300 ns			26	V
Current, peak, SiC MOSFET [1,2]	$I_{PEAK,MOSFET}$		170	A
Current, peak, up to 1 second, within SOA	I_{PEAK}		40	A
Output Current, continuous, within SOA, MSA303	I_{OUT}		30	A
Output Current, continuous, within SOA, MSA303A	I_{OUT}		40	A
Switching frequency, soft switching	$f_{SW,SOFT}$		1	MHz
Switching frequency	f_{SW}		500	kHz
Input Voltage, Logic Level	V_{IN}	-0.3	V_{CC}+0.3	V
Temperature, pin solder, 10s			260	°C
Temperature, junction[3]	T_J		175	°C
Temperature, storage		-55	150	°C
Operating Temperature Range, case	T_C	-55	125	°C

1. Does not consider temperature rise of the device pins
2. Maximum pulse width 10µs, duty cycle less than 1%. Repetition rate might be limited by the temperature rise of device pins.
3. Long term operation at the maximum junction temperature will result in reduced product life. De-rate internal power dissipation to achieve high MTTF

INPUT LOGIC

Parameter	Test Conditions	MSA303			MSA303A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Low		0		0.8	*		*	V
Input High		2.0		V_{CC}	*		*	V
Isolation			650			*		V

OUTPUT

Parameter	Test Conditions	MSA303			MSA303A			Units
		Min	Typ	Max	Min	Typ	Max	
Current, Continuous[1]	25°C Case Temperature			30			40	A
Rise Time			45			*		ns
Fall Time			30			*		ns
Turn-on Delay (module, gate driver input to module output)			85			*		ns
Turn-off Delay (module, gate driver input to module output)			120			*		ns
ON Resistance (Each Switch)[2]	27A Load, T_J = 25 °C		35			30		mΩ
ON Resistance (Each Switch)[2]	27A Load, T_J = 125 °C		50			40		mΩ
Switching Frequency [3]	50% duty cycle, 1A output current			400			*	kHz
Duty Cycle [4]		0		98	*		*	%
High-side Switch On				1			*	ms
Minimum Pulse Time		500			*			ns

1. The MSA303 is rated for 40A of continuous current by design but tested up to 35A on ATE.
2. Does not include parasitic resistance of internal wirebonds.
3. If the load is greater than 100 Ω, the maximum switching frequency might be reduced due to the required discharge of the parasitic capacitances of the SiC MOSFETs through the load.
4. Device supports 100% duty cycle events up to the maximum “High-side Switch On” time.

POWER SUPPLY AND UVLO

Parameter	Test Conditions	MSA303			MSA303A			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage, $+V_S$				600			*	V
Supply Voltage, V_{CC}[1]		14	18	22	*	*	*	V
Supply Current, V_{CC}	All channels idle		8	14		*	*	mA
UVLO, kick-in[2]	for reference only - see footnotes 1 and 2 for details	8.0	8.5	9.0	*	*	*	V
UVLO, release[2]	for reference only - see footnotes 1 and 2 for details	9.0	9.5	10.0	*	*	*	V

1. MSA303 can operate with logic supply voltages below 14 V, up to the UVLO kick-in, but with some operating parameters no longer being applicable. See also typical performance graphs. Apex recommends to never operate MSA303 below 12 V.
2. MSA303 uses a bootstrap circuit for the high-side gate supply. Thus, the high side gate drive supply voltage needs to be considered to be around 1V lower than the provided supply voltage VCC. In addition, the high side supply voltage will drop while the high-side FET is on, further lowering the high-side gate voltage supply.

THERMAL

Parameter	Test Conditions	MSA303			MSA303A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, Junction to Case, each MOSFET	$f_{SW} > 60$ Hz		1.35			*		°C/W
Resistance, Junction to Case, Schottky-Barrier Diode	$f_{SW} > 60$ Hz		2.0			*		°C/W
Temperature Range, Case[1]		-40		125	*		*	°C

1. Case temperature must be derated with switching frequency

Note: *The specification of MSA303A is identical to the specification for MSA303 in applicable column to the left.

SILICON CARBIDE MOSFET PARAMETERS

T_J = 25°C unless otherwise specified. MSA303 has a Schottky Barrier diode in parallel per switch. See Figure 1 for illustration.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0V, V_{DS} = 650V, T_j = 25°C		1	10	μA
		V_{GS} = 0V, V_{DS} = 650V, T_j = 125°C		2		μA
Gate-Source leakage current	I_{GSS+}	V_{GS} = 0V, V_{DS} = 0V			100	nA
	I_{GSS-}	V_{GS} = -4V, V_{DS} = 0V			100	nA
Gate input resistance[1]	R_G	f = 1 MHz, open drain		7		Ω
MOSFET transductance	g_{fs}	V_{DS} = 10V, I_D=27A		9.4		S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=500V, f=1 MHz		1526		pF
Output capacitance	C_{oss}			89		pF
Reverse transfer capacitance	C_{rss}			42		pF
Effective output capacitance	$C_{o(er)}$	V_{GS}=0V, V_{DS}=0V to 300V		230		pF
Turn-on switching loss	E_{ON}	VDS=300V, VGS=0V/18V, ID=27A, RG=0Ω, L=250μH. E_{ON} includes diode reverse recovery L_σ=50nH, C_σ=200pF		168		μJ
Turn-off switching loss	E_{OFF}			112		μJ
Total gate charge	Q_g	V_{DS}=300V, V_{GS}=18V, I_D=27A		104		nC
Gate-Source charge	Q_{gs}			19		nC
Gate-Drain charge	Q_{gd}			55		nC
Gate plateau voltage				9.6		V
Body diode, forward current, peak[2]	I_{SM}				175	A
Body diode, forward voltage[2]	V_{SD}	V_{GS}=0V, I_S=27A		3.2		V
Reverse recovery time[2]	t_{rr}	I_F=27A, V_R=300V, di/dt=1100A/μs, L_σ=50nH, C_σ=200pF		26		ns
Reverse recovery charge[2]	Q_{rr}			130		nC
Reverse recovery current[2]	I_{rrm}			10		A

1. For reference only. MSA303 uses additional resistors between the gate driver and the MOSFET to optimize the switching behavior of the module.
2. Under normal operation, the body diode of MSA303 will not be conducting, as the Schottky Barrier Diode put in parallel to the MOSFET conducts at a lower forward voltage.

SILICON CARBIDE SCHOTTKY-BARRIER DIODE PARAMETERS

T_J = 25°C unless otherwise specified. All parameters are per die. MSA303 has a Schottky Barrier diode in parallel per switch. See Figure 1 for illustration.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse voltage (repetitive peak)	V_{RM}				650	V
Continuous forward current	I_F	Limited by T_j			20	A
Surge forward current	I_{FSM}	PW=10µs square			260	A
		10% duty cycle			76	A
Forward voltage	V_F	I_F=20A, T_j=25°C		1.35	1.55	V
		I_F=20A, T_j=150°C		1.55		V
Reverse current	I_R	V_R=600V, T_j=25°C		4		µA
		V_R=600V, T_j=150°C		60		µA
Total capacitance	C	V_R=1V, f=1MHz		730		pF
		V_R=600V, f=1MHz		74		pF
Total capacitance charge	Q_C	V_R=400V, di/dt=350A/µs		31		nC
Switching time	t_C	V_R=400V, di/dt=350A/µs		19		ns

TYPICAL PERFORMANCE GRAPHS

All MOSFET performance graphs are per MOSFET. MSA303 has one MOSFET die and a Schottky Barrier diode in parallel per switch. See Figure 1 for illustration.

Figure 4: I_{CC} vs. Switching Frequency

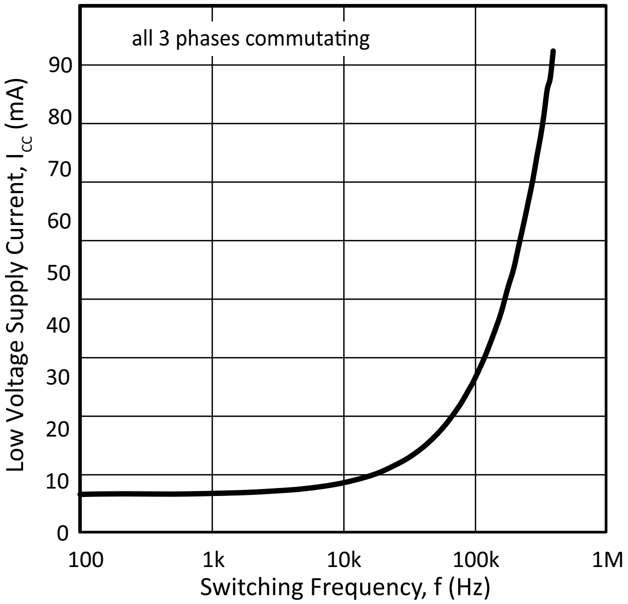


Figure 5: MOSFET Output Characteristics 1

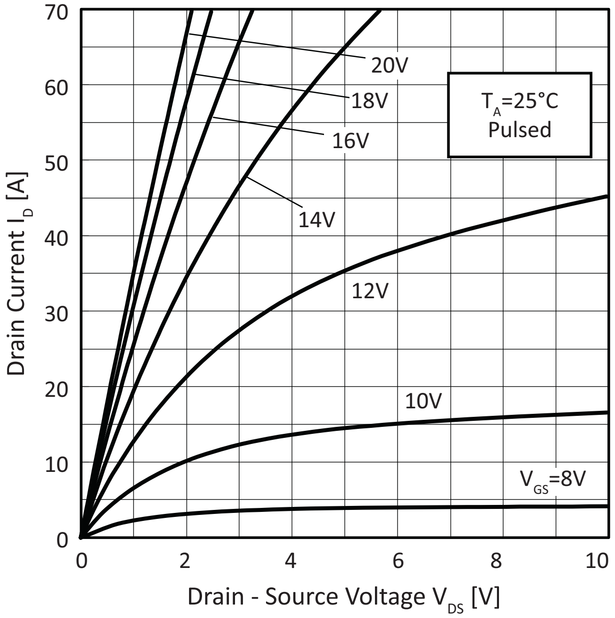


Figure 6: MOSFET Output Characteristics 2

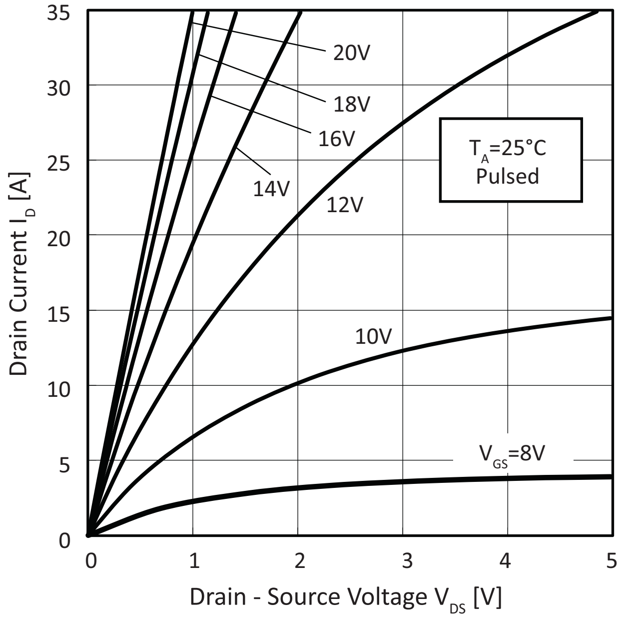


Figure 7: MOSFET Output Characteristics 3

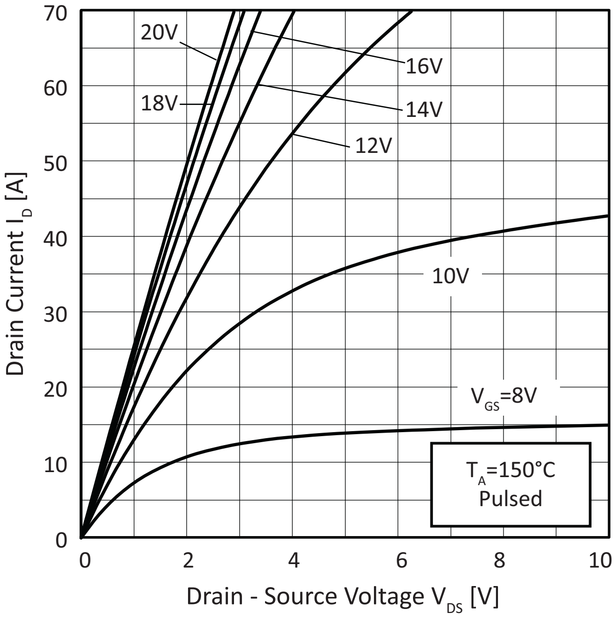


Figure 8: MOSFET Output Characteristics 4

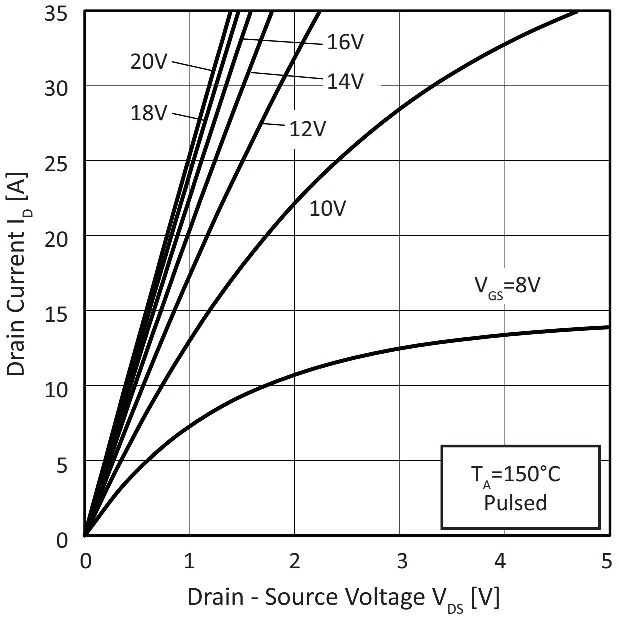


Figure 9: MOSFET VGS vs ID (1)

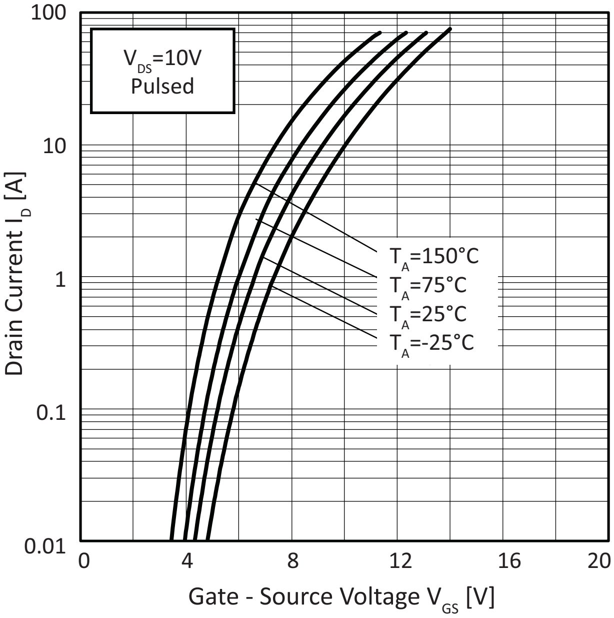


Figure 10: MOSFET VGS vs ID (2)

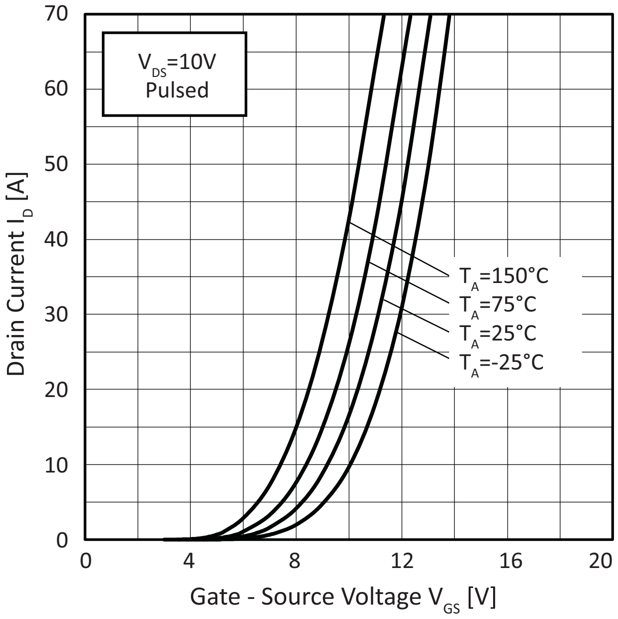


Figure 11: Gate Threshold vs TJ

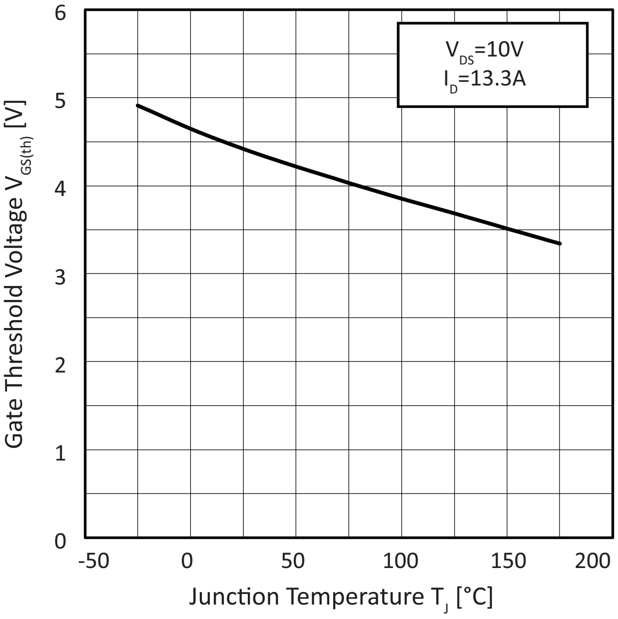


Figure 12: Transconductance vs ID

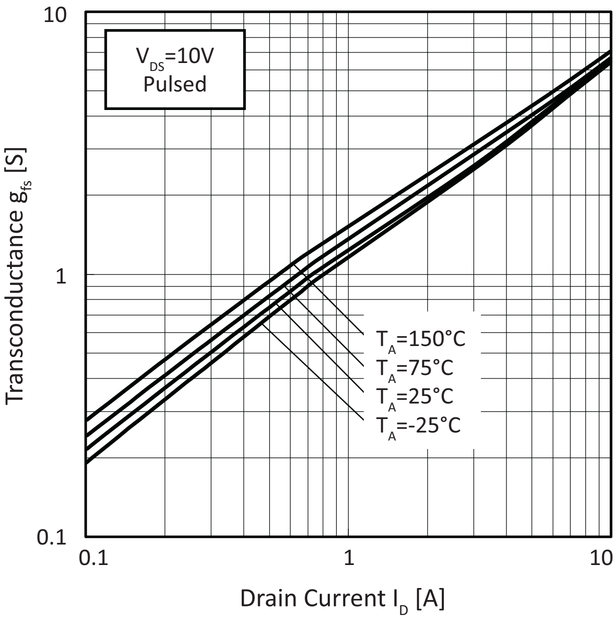


Figure 13: RDS(on) vs VGS

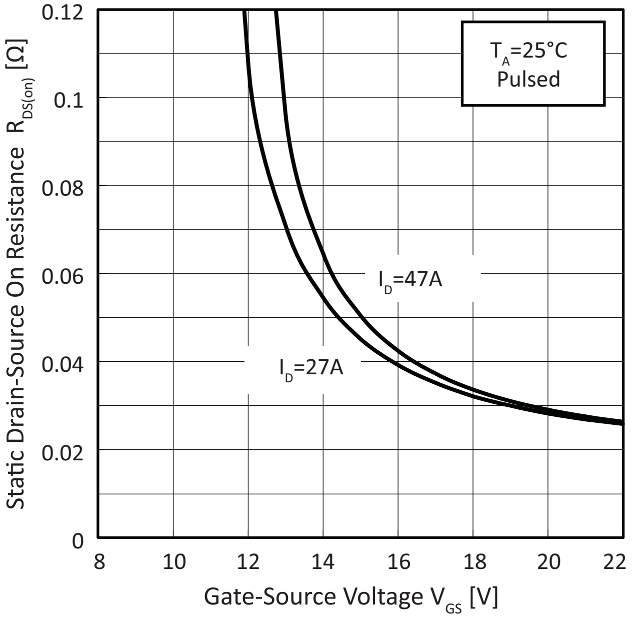


Figure 14: RDS(on) vs TJ

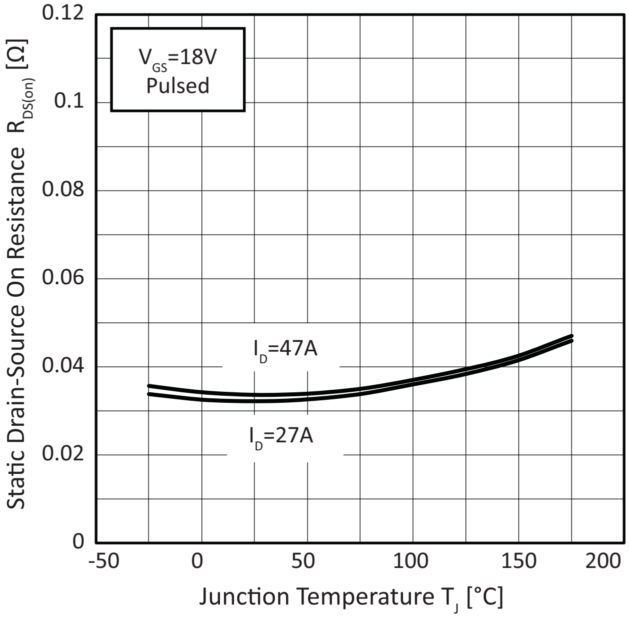


Figure 15: RDS(on) vs ID

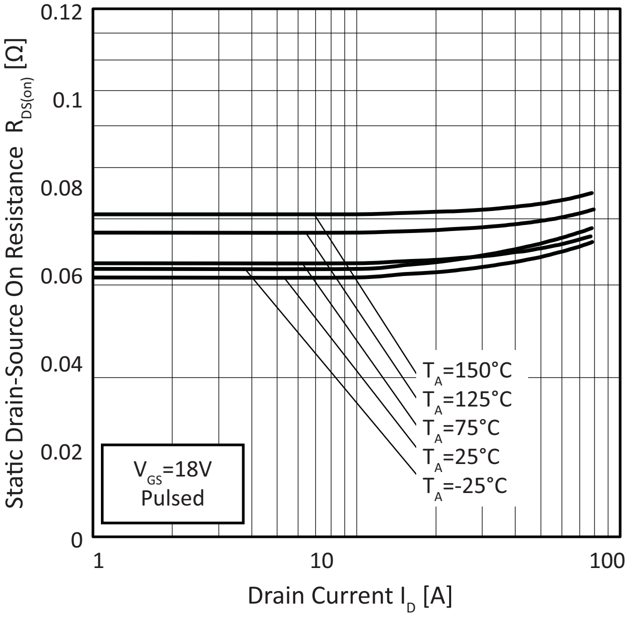


Figure 16: Capacitance vs VDS

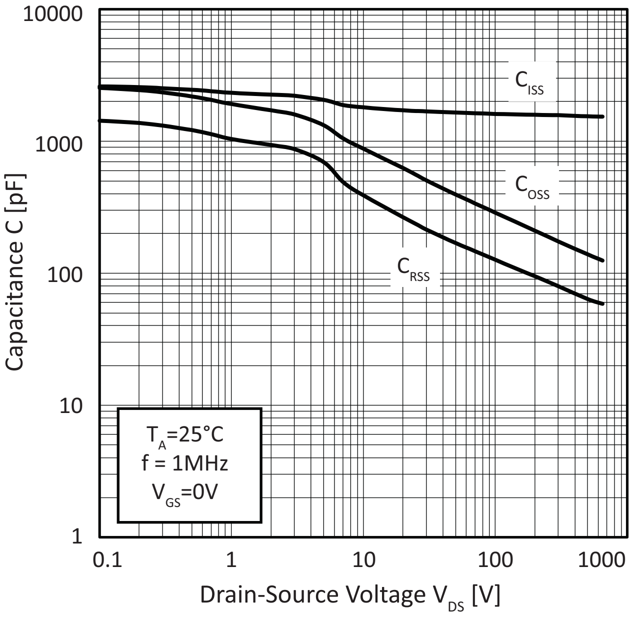


Figure 17: Switching Time vs ID

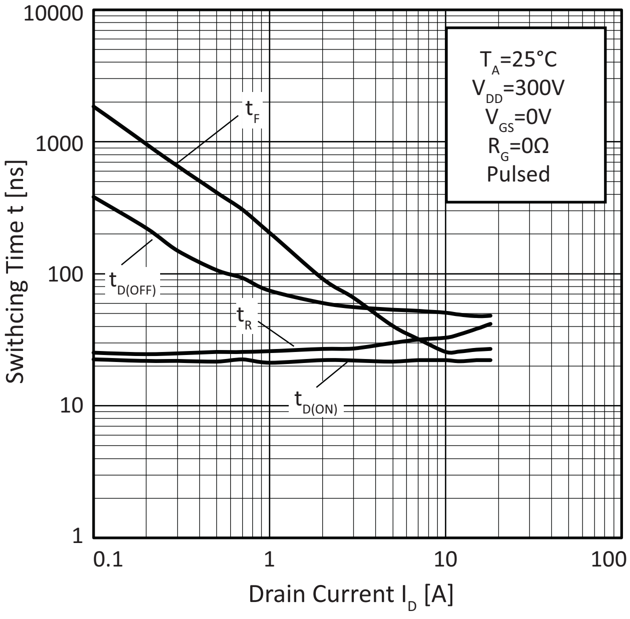


Figure 18: Gate Charge vs VGS

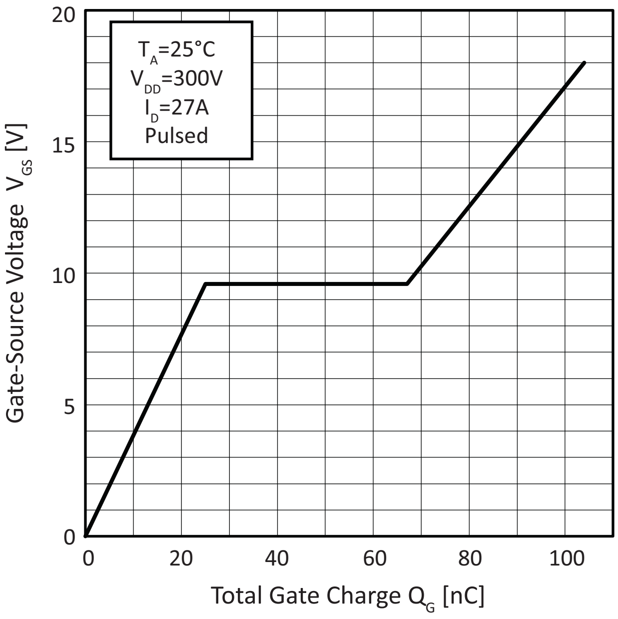


Figure 19: Cross-Stored Energy vs VDS

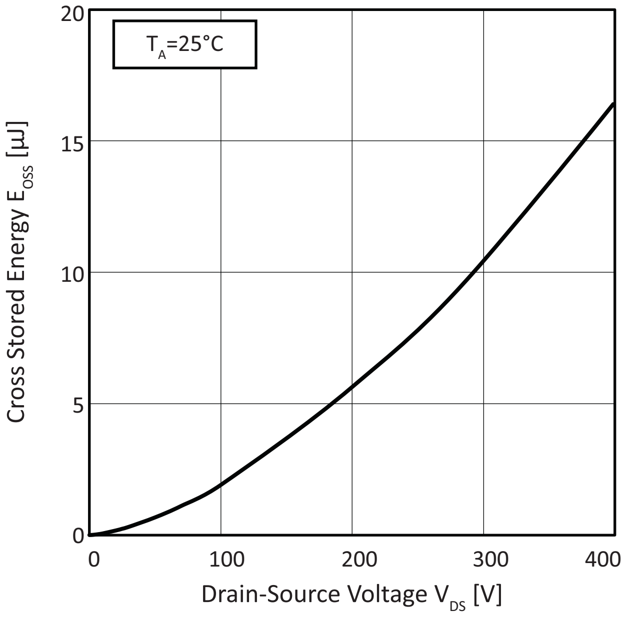


Figure 20: Switching Energy vs VDS

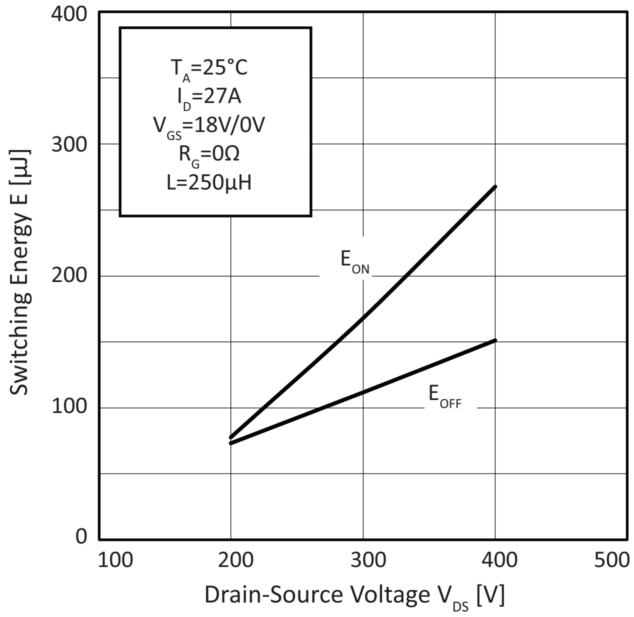


Figure 21: Switching Energy vs ID

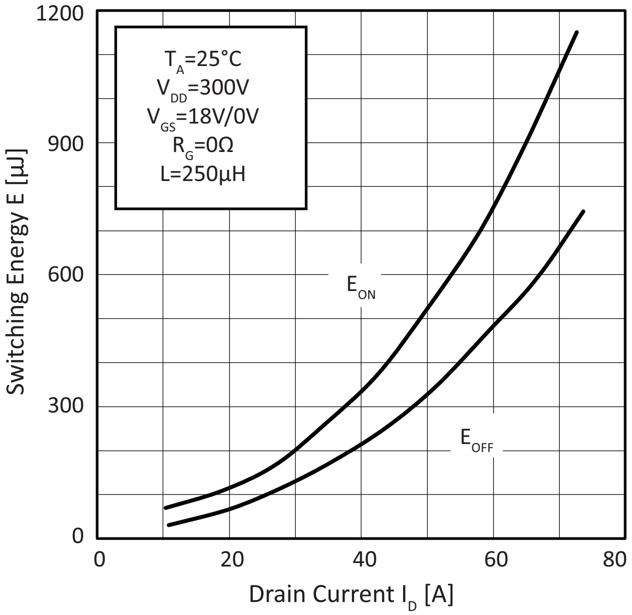


Figure 22: Switching Energy vs RG

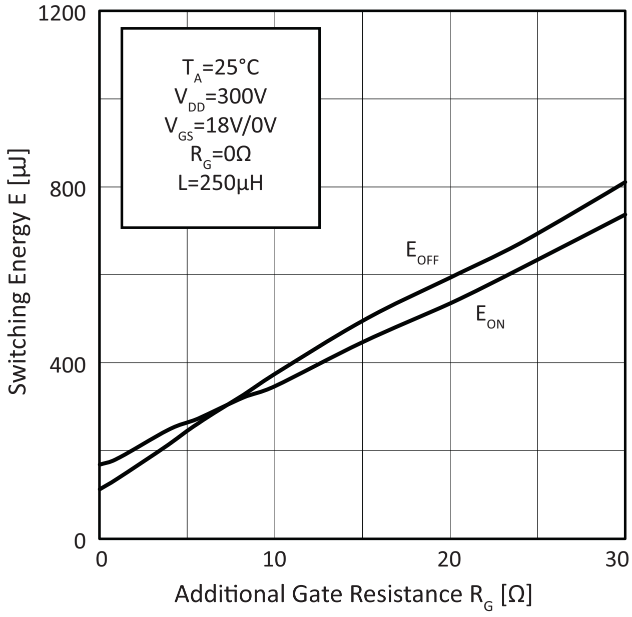


Figure 23: SBD IF vs VF (1)

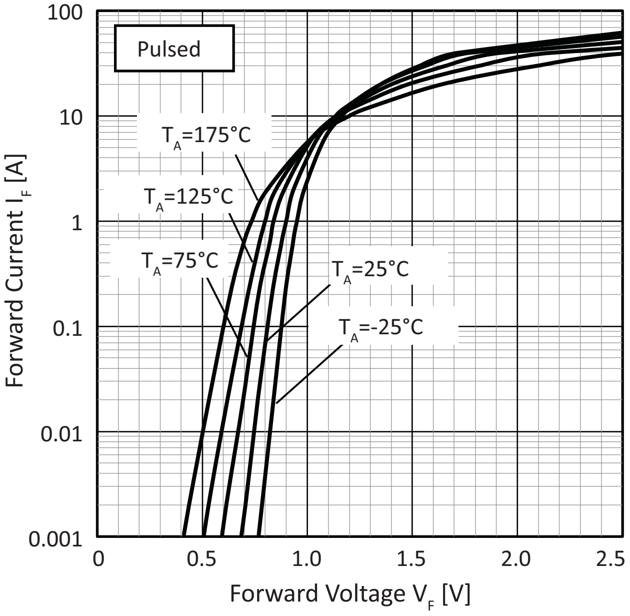


Figure 24: SBD IF vs IF (2)

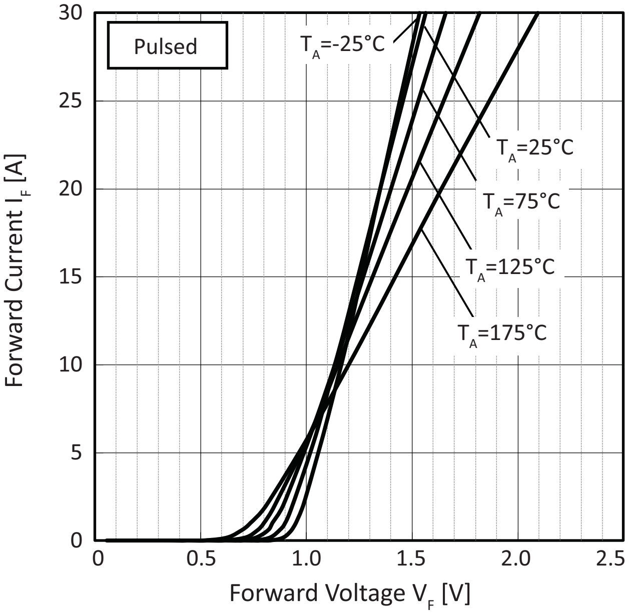


Figure 25: SBD IR vs VR

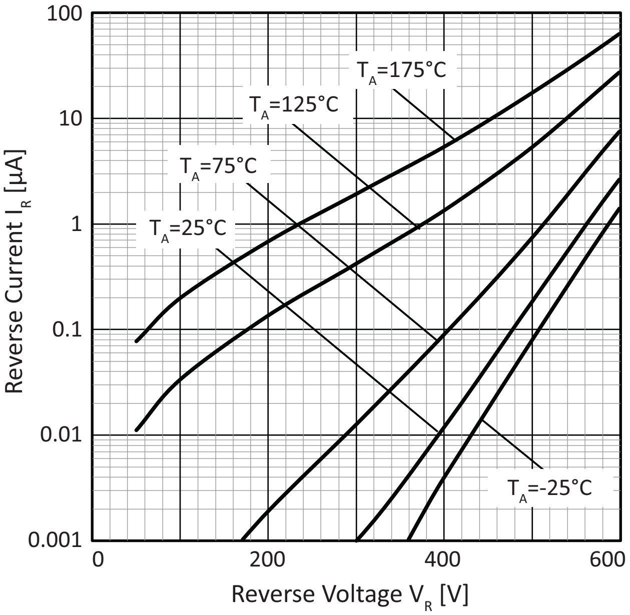
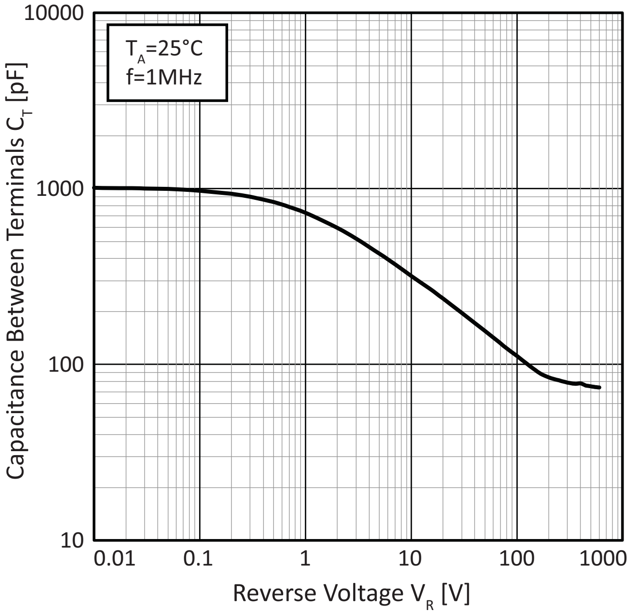


Figure 26: SBD CT vs VR



GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology's complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

CALCULATING POWER DISSIPATION

Power dissipation internal to MSA303 consists mostly of 2 elements, which may be calculated as follows:

1. Conduction Losses

$$P_{CONDUCTION} = (I_S)^2 \times R_{DS(ON)} \times X[W]$$

X = 1.5 for Wye or Delta loads
X = 2 for Single Ended loads having sinking AND sourcing current
X = 1 for Single Ended loads having sinking OR sourcing current

2. Switching Losses

$$P_{SWITCHING} = \frac{3}{2} \times V_S \times I_S \times f_{SWITCHING} \times (t_{RISE} + t_{FALL})[W]$$

Given in above specification tables and performance graphs:
$R_{DS(ON)}$ =ON Resistance (for the paralleled FETs) [Ω]
t_{RISE}=Rise Time [s]
t_{FALL}=Fall Time [s]

Application Specific:
I_S=Average Supply Current from V_S Power Supply [A]
V_S=Supply Voltage [V]
$f_{SWITCHING}$=Switching Frequency of Input Signal [Hz]

UNDER-VOLTAGE LOCKOUT FUNCTION

MSA303 has a built-in under-voltage lockout function. When V_{CC} drops below approximately 9V, the outputs will be high impedance. When V_{CC} rises above approximately 10V, the outputs will return to normal operating mode. In addition, to prevent malfunctions due to noise, a mask time of approximately 2.5µs is set on V_{CC}.

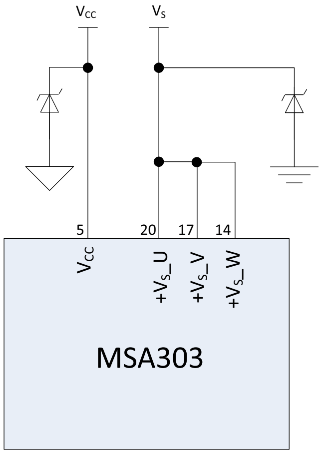
BYPASSING

Adequate bypassing of the power supplies is required for proper operation. Failure to do so can cause erratic and low efficiency operation as well as excessive ringing at the outputs. The V_S supply should be bypassed with at least a 1µF ceramic capacitor in parallel with another low ESR capacitor of a least 10µF per amp of output current. Capacitor types rated for switching applications are the only types that should be considered. The 1µF ceramic capacitor must be physically connected directly to the $+V_S$ and PGND nodes. Even one inch of lead length will cause excessive ringing at the outputs. This is due to the very fast switching times and the inductance of the lead connection. The bypassing requirements of the V_{CC} supply are less stringent, but still necessary. A 0.1µF to 0.47µF ceramic capacitor connected directly from the V_{CC} pin to DGND close to MSA303 will suffice.

POWER SUPPLY PROTECTION

Unidirectional transient Voltage suppressors are recommended as protection on the supply pins as shown in Figure 27. TVS diodes clamp transients to voltages within the power supply rating and clamp power supply reversals to ground. Whether the TVS diodes are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation. Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Unidirectional TVS diodes prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

Figure 27: TVS Diodes



INPUT PROTECTION

It is recommended to connect two small-signal diodes at each of the input signals to provide external protection for MSA303, as shown in the typical connection diagram. A 100pF capacitor can be connected from each input to ground to provide ESD protection from coaxial cables and other ESD sources. A series resistor (approximately 200 Ω) may be added in series with the input pins to limit excessive current going into the pins. Without these protection features, MSA303 is susceptible to permanent input stage failure.

Each INX_LS and INX_HS has an internal pull-down resistance to DGND of 50 kΩ typical.

DEAD TIME

Dead time is entirely user-selectable and must be considered when generating an input signal. Generally, dead time is chosen as a multiple of clock-cycles from the system controller; this makes the coordination of _HS and _LS inputs easy. The absolute minimum dead time is 60ns. A dead time of 120ns is recommended for margin.

OUTPUT LOGIC

MSA303 follows the following truth table for each phase:

ENA_X	INX_LS	INX_HS	OUT_X
L	X	X	High-Impedance
H	L	L	High-Impedance
H	L	H	H
H	H	L	L
H	H	H	High-Impedance

POWER SUPPLY SEQUENCING

During power-on of MSA303, turn on power supplies in the following order:
1. VCC
2. +VS
During power-off of the MSA303, turn off power supplies in the reverse order.

BOOTSTRAP CONSIDERATIONS

The high side drives inside MSA303 each relies on a bootstrap circuit. It consists of a capacitor that is charged when the low-side is active through a diode circuit and operates as a floating supply when the high side is turned on. To ensure that the internal capacitance is properly charged, the device needs to be supplied with an active INX_L signal for several microseconds after power-on prior to starting any PWM operation.

The high-side capacitor will discharge while the high-side is actively driven. When operating MSA303, any output sequence needs to have the low side enabled periodically to allow for the capacitor to be re-charged. Thus, the maximum PWM duty cycle can’t be 100% for an extended operating period.

The voltage drop through the diode when charging the high side supply capacitor and the discharge of the capacitor while the high side is turned-on need to be considered when operating the device at low supply voltages, as it can cause the under-voltage lock-out to kick-in at voltage level above the values in the specification tables.

DIGITAL AND ANALOG GROUND CONNECTIONS

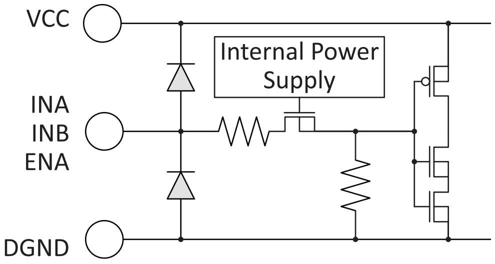
The digital ground (DGND_X) and power (PGND_X) ground pins are connected inside MSA303. When designing the external circuitry, ground loops should be avoided.

If low-side current sensing is used, it is recommended to use a current sense circuit with a ultra-low voltage drop to avoid any accidental low-side turn-off during peak currents.

DIGITAL INPUTS EQUIVALENT CIRCUIT

The equivalent circuit for the digital inputs is shown in Figure 28. In case of a failure of the internal power supply or the inputs not connected, the signals are pulled to the digital ground through an internal resistor.

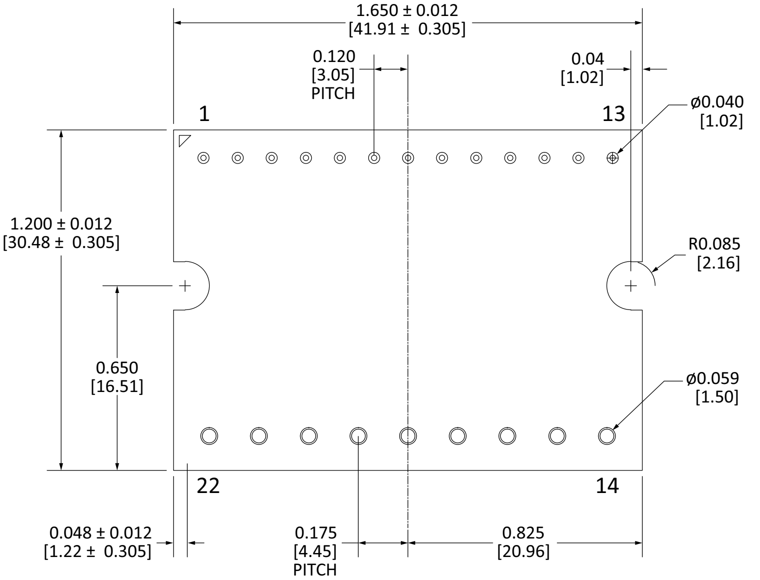
Figure 28: Digital Input Equivalent Circuit

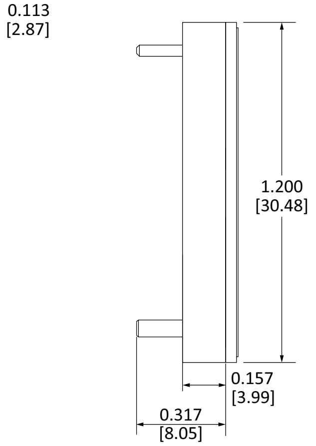


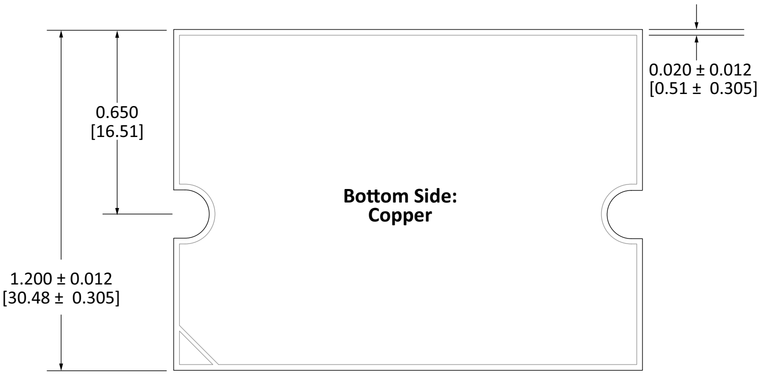
PACKAGE OPTIONS

Part Number	Apex Package Style	Description
MSA303	KU	22-pin with vertical mounting pins

PACKAGE OUTLINE







Substrate Thickness: .0498 ± 10%

Notes:

1. Dimensions are in inches [mm]
2. Unless otherwise specified, tolerances are ±0.005 [0.127]
3. Mininum Distance between high voltage traces 0.031 [0.79]
4. Pins (Ø 0.040): nickel-plated brass alloy (100-150 micro-inch)
5. Pins (Ø 0.059): nickel-plated copper (125 micro-inch)
6. Mount with #4 (M3) fasteners

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