

Features

Operating Conditions

- 1.8–5.5V, -40°C to +85°C, DC to 24 MHz
- 1.8–5.5V, -40°C to +125°C, DC to 24 MHz

Qualification

- AEC-Q100 Grade 1 (-40°C to +125°C)

Core: Arm® Cortex®-M0+ CPU Running at up to 24 MHz

- Single-cycle hardware multiplier

Memories

- Up to 128 KB in-system self-programmable Flash
- Up to 16 KB SRAM main memory

System

- Power-on Reset (POR) and Brown-out Detection (BOD)
- Internal and external clock options
- External Interrupt Controller (EIC)
- One non-maskable interrupt

Low Power

- Idle and Standby sleep modes
- SleepWalking peripherals

Input/Output (I/O)

- Up to 55 programmable I/O pins
- Up to 16 external interrupts
- Multi-Voltage I/O (MVIO)

Clock System

- Main Clock Controller (MCLK)
- Generic Clock Controller (GCLK)
- Clock sources:
 - Internal 1-24 MHz High Frequency Oscillator (OSCHF)
 - Internal 32.768 kHz Oscillator (OSC32K)
 - External 32.768 kHz Oscillator input (XOSC32K)

Debugger Development Support

- In-circuit and in-application programming
- 2-wire Serial Wire Debug Port Interface
- Four hardware breakpoints, one data watchpoint
- Micro Trace Buffer (MTB) for instruction trace in SRAM
- Programming and Debugging Interface Disable (PDID) functionality

Advanced Analog

- One 12-bit, 800 kps Analog-to-Digital Converter (ADC)
 - Differential and single-ended input
 - Automatic offset and gain error compensation
 - Oversampling and decimation in hardware to support up to 5 extra bits of resolution
- Two Analog Comparators (AC) with window compare function
- Peripheral Touch Controller (PTC) with up to 29 self-capacitance touch channels
- Internal and external voltage reference options

Peripherals

- 2-channel Direct Memory Access Controller (DMAC) with CRC Function
- 4-channel Event System
- Four 16-bit Timer/Counters:
 - Three 16-bit basic timers (TC0-2)
 - One 16-bit Timer/Counter for Control with four PWM channels (TCC0)
- 32-bit Real Time Counter (RTC) with clock/calendar function
- Watchdog Timer (WDT)
- Two Serial Communication Interfaces (SERCOM), configurable to operate as:
 - USART with full-duplex and single-wire half-duplex configuration

- ISO7816 UART
- I²C up to 1 MHz (SERCOM0)
- SPI
- LIN Host/Client
- RS-485
- Configurable Custom Logic (CCL) with four Look-Up Tables (LUT)
- Integrated Temperature Sensor

Available Packages

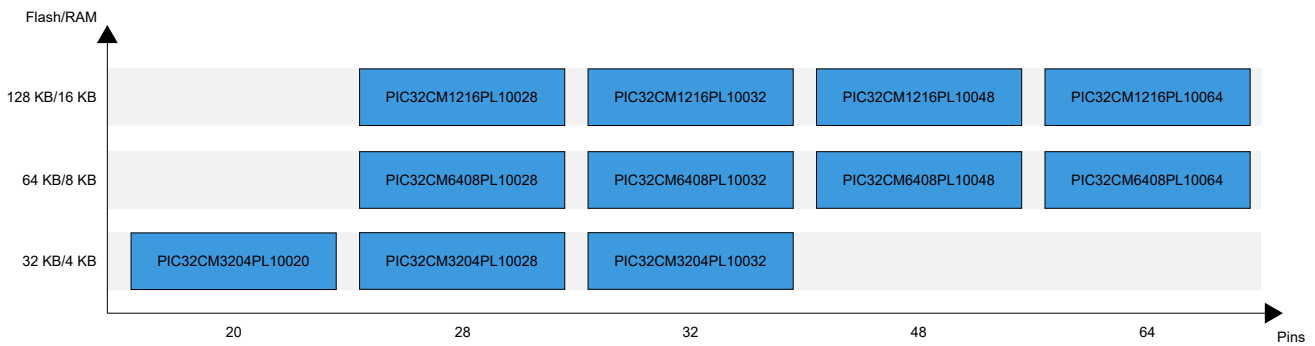
- 20-pin SSOP and VQFN
- 28-pin SSOP, SPDIP and VQFN
- 32-pin TQFP and VQFN
- 48-pin TQFP and VQFN
- 64-pin TQFP and VQFN

Family Overview

The figure below shows the PIC32CM PL10 Family devices and illustrates the pin count variants and memory sizes:

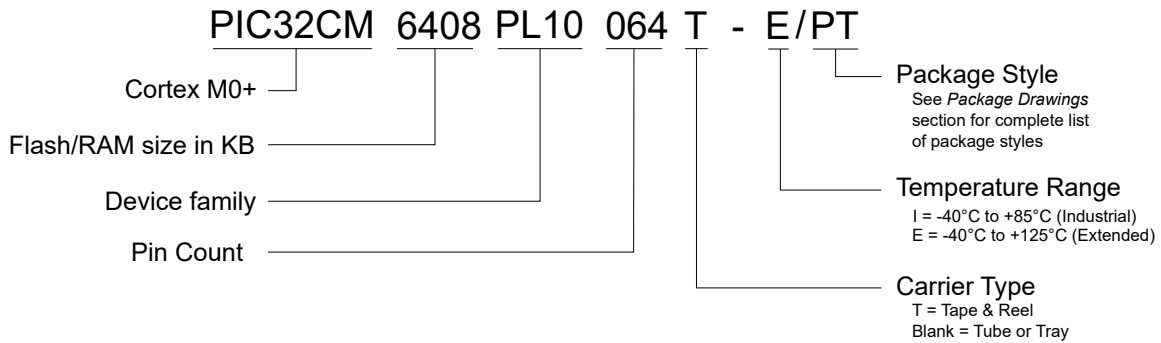
- Vertical migration is possible without code modification, as these devices are fully pin- and feature-compatible
- Horizontal migration to the left reduces the pin count and, therefore, the available features

Figure 1. PIC32CM PL10 Family Overview



The name of a device in the PIC32CM PL10 Family is decoded as follows:

Figure 2. PIC32CM PL10 Family Family Device Designations



Note:

1. VQFN packages have wettable flanks.

Memory Overview

Table 1. Memory Overview

| Devices | CM3204-20 CM3204-28 CM3204-32 | CM6408-28 CM6408-32 CM6408-48 CM6408-64 | CM1216-28 CM1216-32 CM1216-48 CM1216-64 |
|--------------------|-------------------------------------|--|--|
| Flash memory | 32 KB | 64 KB | 128 KB |
| SRAM | 4 KB | 8 KB | 16 KB |
| Boot ROM (BOOTROM) | 8 KB | 8 KB | 8 KB |
| User row (USERROW) | 512B | 512B | 512B |

Peripheral Overview

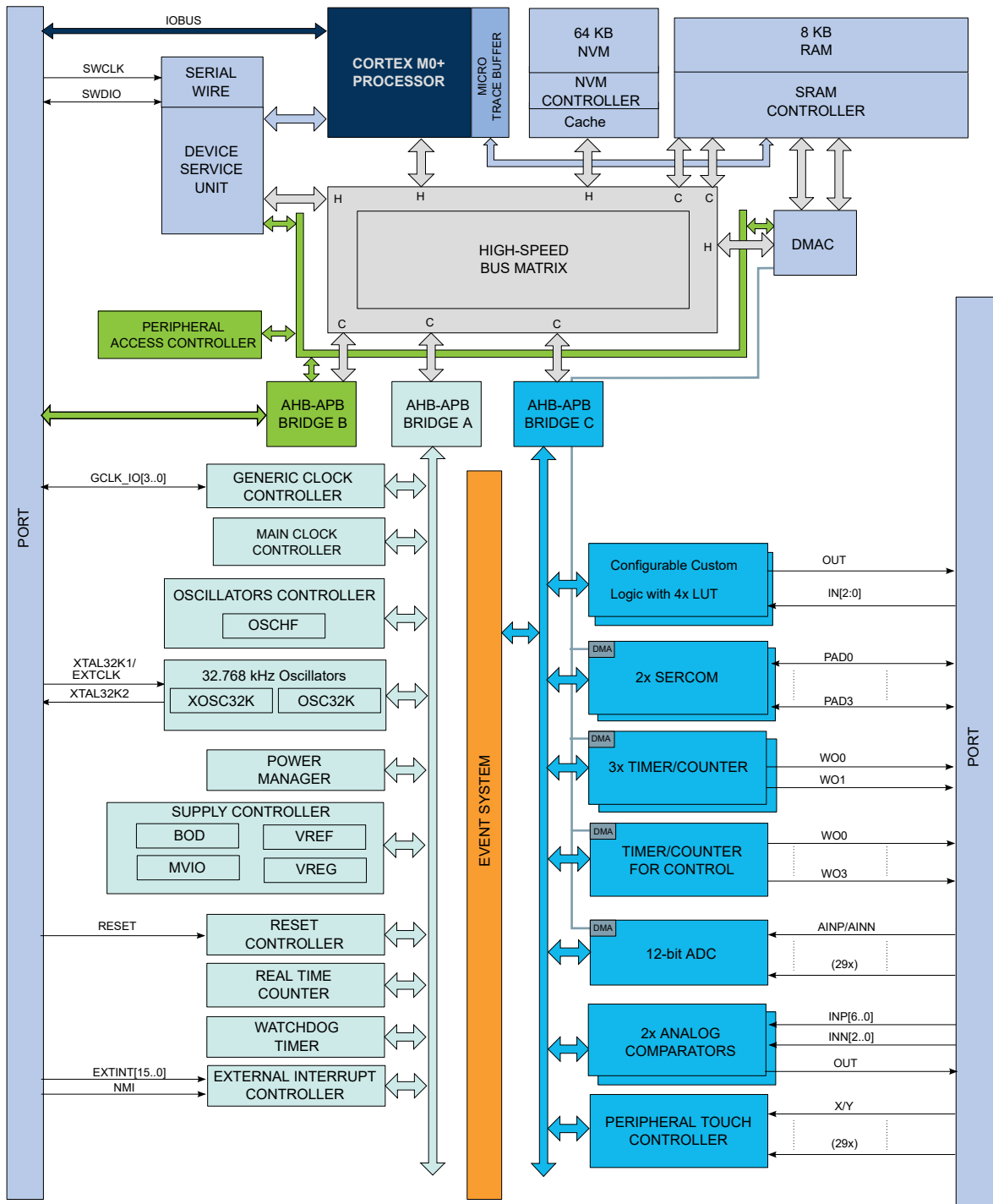
Table 2. Peripheral Overview

| Feature | CM3204-20 | CM3204-28 CM6408-28 CM1216-28 | CM3204-32 CM6408-32 CM1216-32 | CM6408-48 CM1216-48 | CM6408-64 CM1216-64 |
|---|-----------|-------------------------------------|-------------------------------------|------------------------|------------------------|
| Pins | 20 | 28 | 32 | 48 | 64 |
| Max. frequency (MHz) | 24 | 24 | 24 | 24 | 24 |
| Generic Clock Controller (GCLK) | 4 | 4 | 4 | 4 | 4 |
| External High-Frequency Oscillator (XOSCHF) | 0 | 0 | 0 | 0 | 0 |
| External 32.768 kHz Oscillator | 1 | 1 | 1 | 1 | 1 |
| Timer/Counter (TC) | 3 | 3 | 3 | 3 | 3 |
| Timer/Counter for Control Applications (TCC) | 1 | 1 | 1 | 1 | 1 |
| Real-Time Counter (RTC) | 1 | 1 | 1 | 1 | 1 |
| Serial Communication Interface (SERCOM) | 2 | 2 | 2 | 2 | 2 |
| ADC (channels) | 1 (11) | 1 (16) | 1 (20) | 1 (25) | 1 (29) |
| DAC | 0 | 0 | 0 | 0 | 0 |
| Analog Comparator (AC) | 2 | 2 | 2 | 2 | 2 |
| Peripheral Touch Controller (PTC) and (channels) | 1 (11) | 1 (16) | 1 (20) | 1 (25) | 1 (29) |
| Operational Amplifier (OPAMP) | 0 | 0 | 0 | 0 | 0 |
| Configurable Custom Logic Look-up Table (CCL LUT) | 3 | 4 | 4 | 4 | 4 |
| Watchdog Timer (WDT) | 1 | 1 | 1 | 1 | 1 |
| Direct Memory Access Channels (DMA) | 2 | 2 | 2 | 2 | 2 |
| Event System channels (EVSYS) | 4 | 4 | 4 | 4 | 4 |
| General Purpose I/O ⁽¹⁾ | 17/16 | 23/22 | 27/26 | 42/41 | 56/55 |
| Multi-Voltage I/O (MVIO) | 3 | 4 | 4 | 8 | 8 |
| External Interrupts | 11 | 13 | 15 | 16 | 16 |

Note:

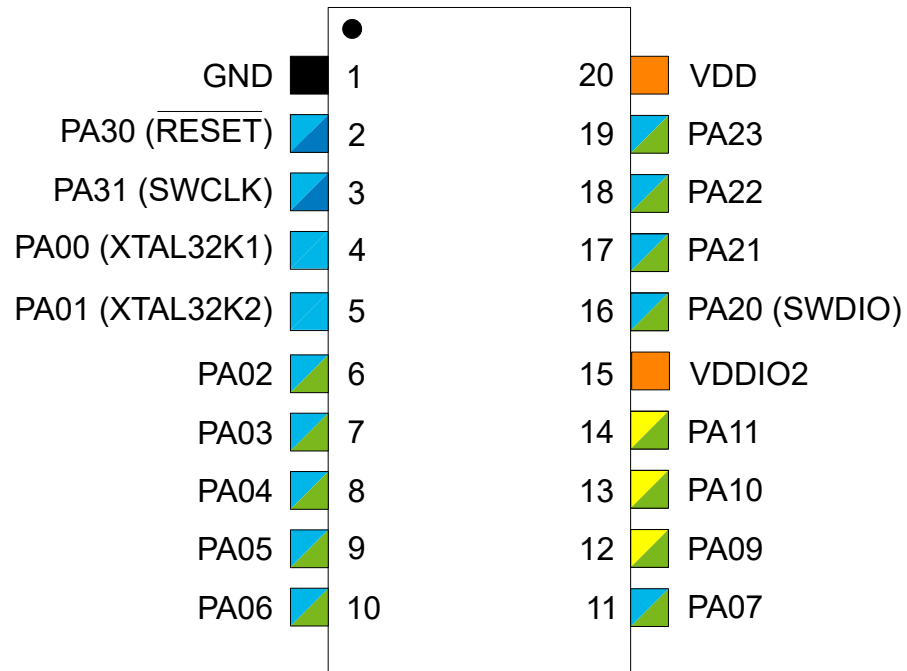
1. The PA30/RESET pin is input only.

1. Block Diagram








2. Pinout





2.1. 20-pin SSOP



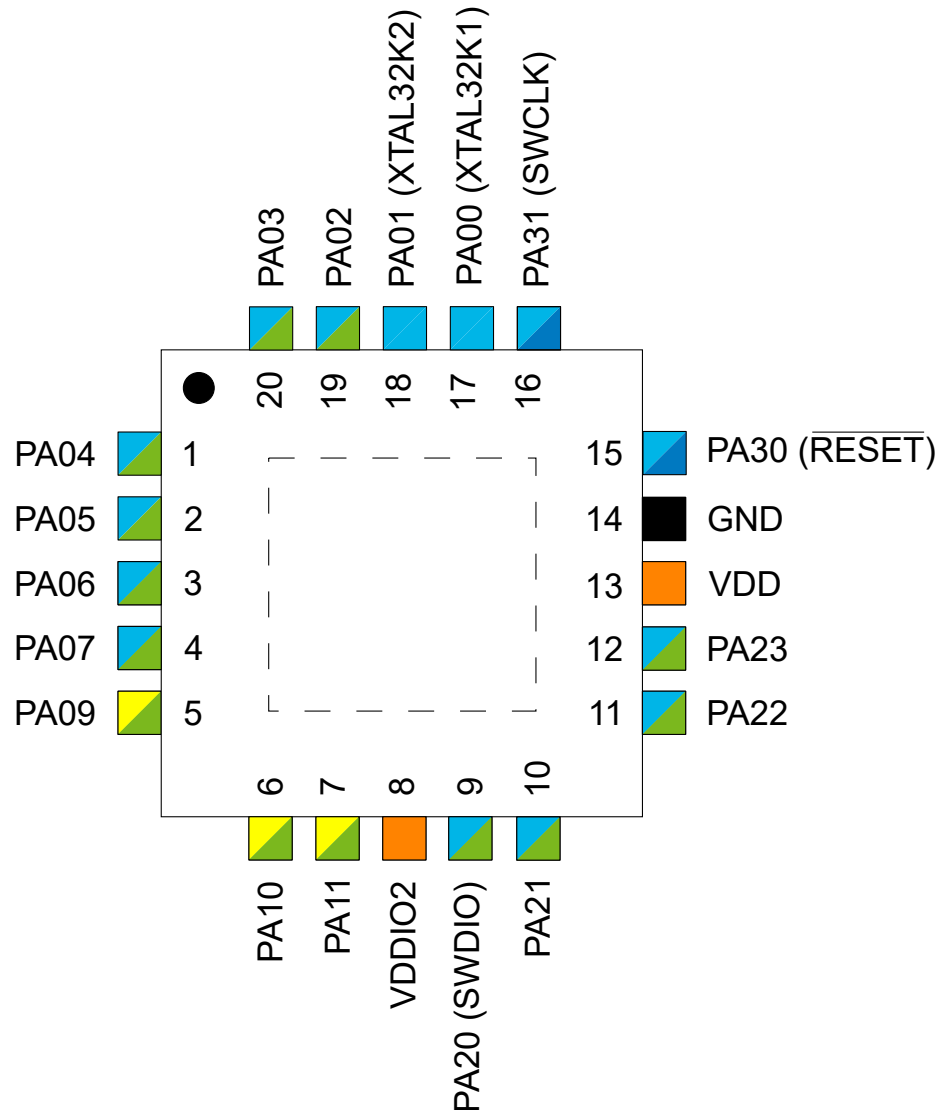
Power

-  Power Supply
-  Ground
-  Pin on VDD Power Domain
-  Pin on AVDD Power Domain
-  Pin on VDDIO2 Power Domain






Functionality

-  Programming/Debug
-  Clock/Crystal
-  Digital Function Only
-  Analog Function





2.2. 20-pin VQFN



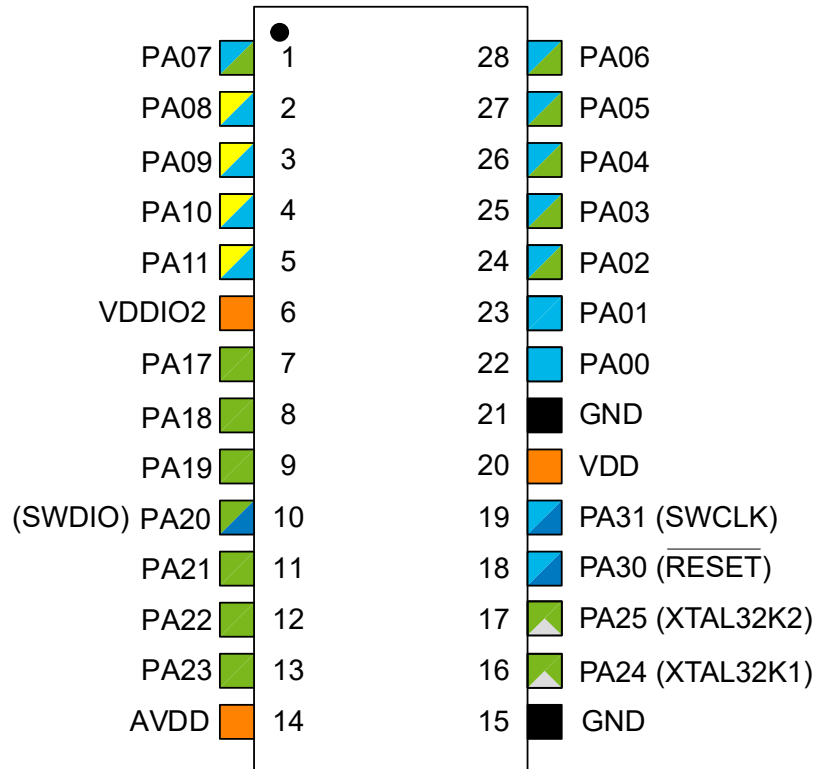
Power

-  Power Supply
-  Ground
-  Pin on VDD Power Domain
-  Pin on AVDD Power Domain
-  Pin on VDDIO2 Power Domain






Functionality

-  Programming/Debug
-  Clock/Crystal
-  Digital Function Only
-  Analog Function





2.3. 28-pin SPDIP and SSOP



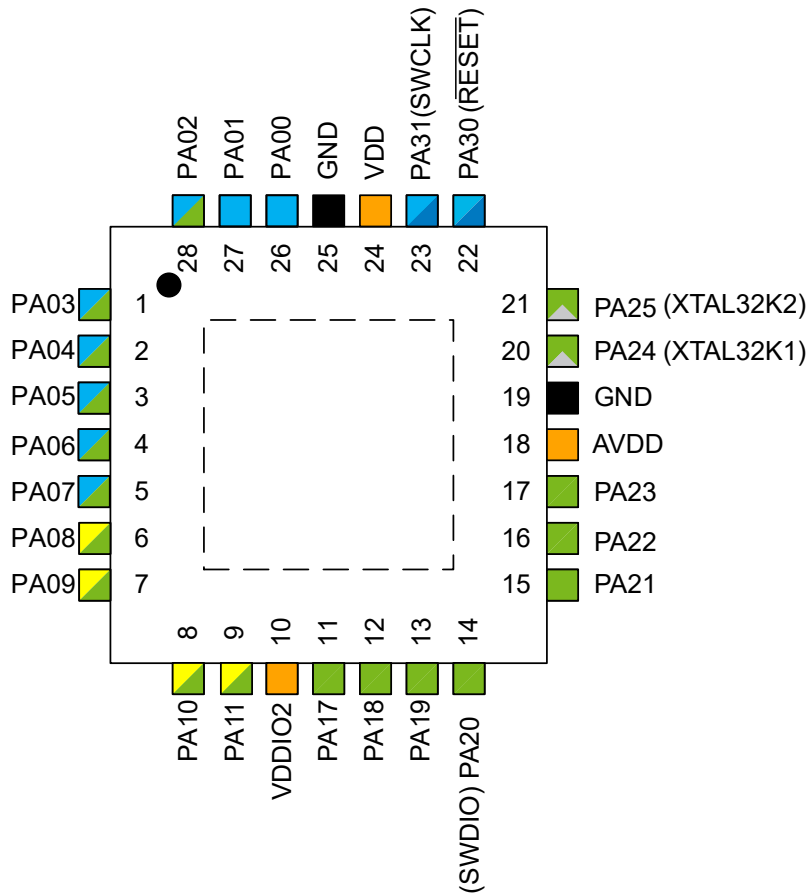
Power

-  Power Supply
-  Ground
-  Pin on VDD Power Domain
-  Pin on AVDD Power Domain
-  Pin on VDDIO2 Power Domain

Functionality

-  Programming/Debug
-  Clock/Crystal
-  Digital Function Only
-  Analog Function

2.4. 28-pin VQFN



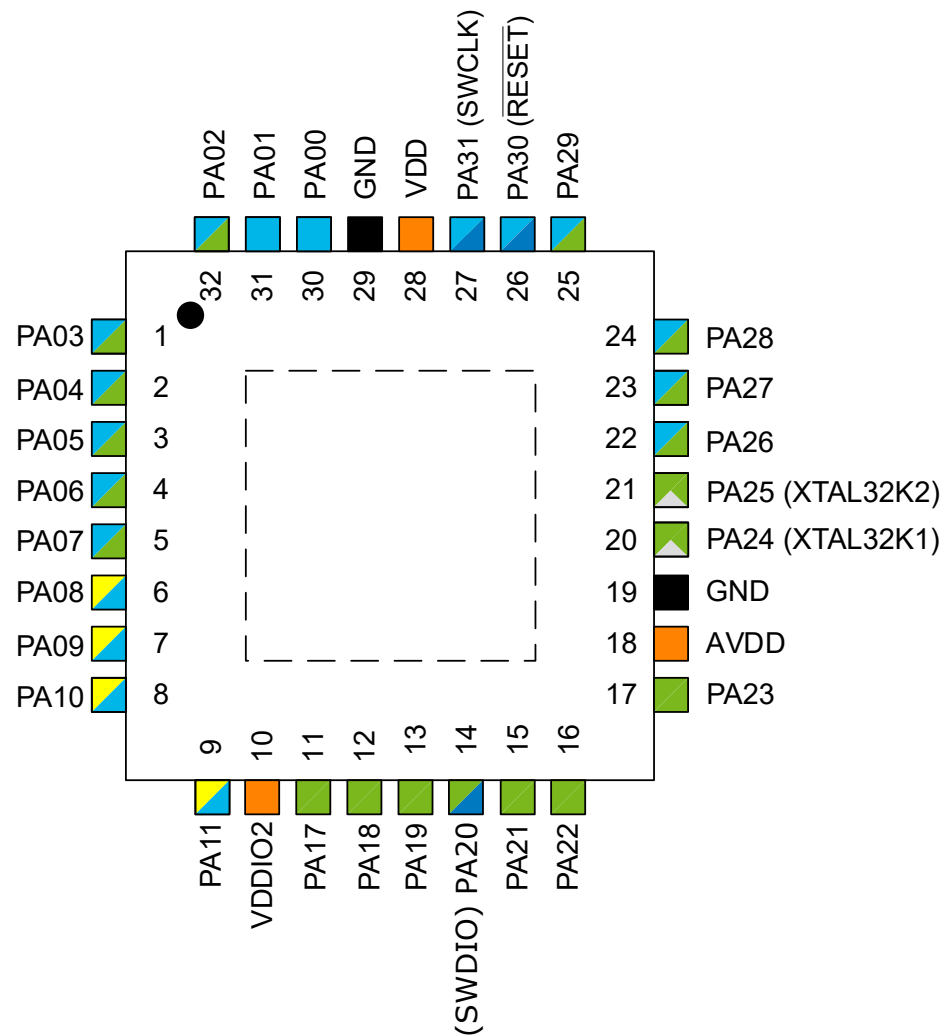
Power










- Power Supply
- Ground
- Pin on VDD Power Domain
- Pin on AVDD Power Domain
- Pin on VDDIO2 Power Domain

Functionality

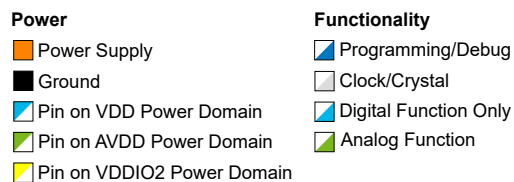
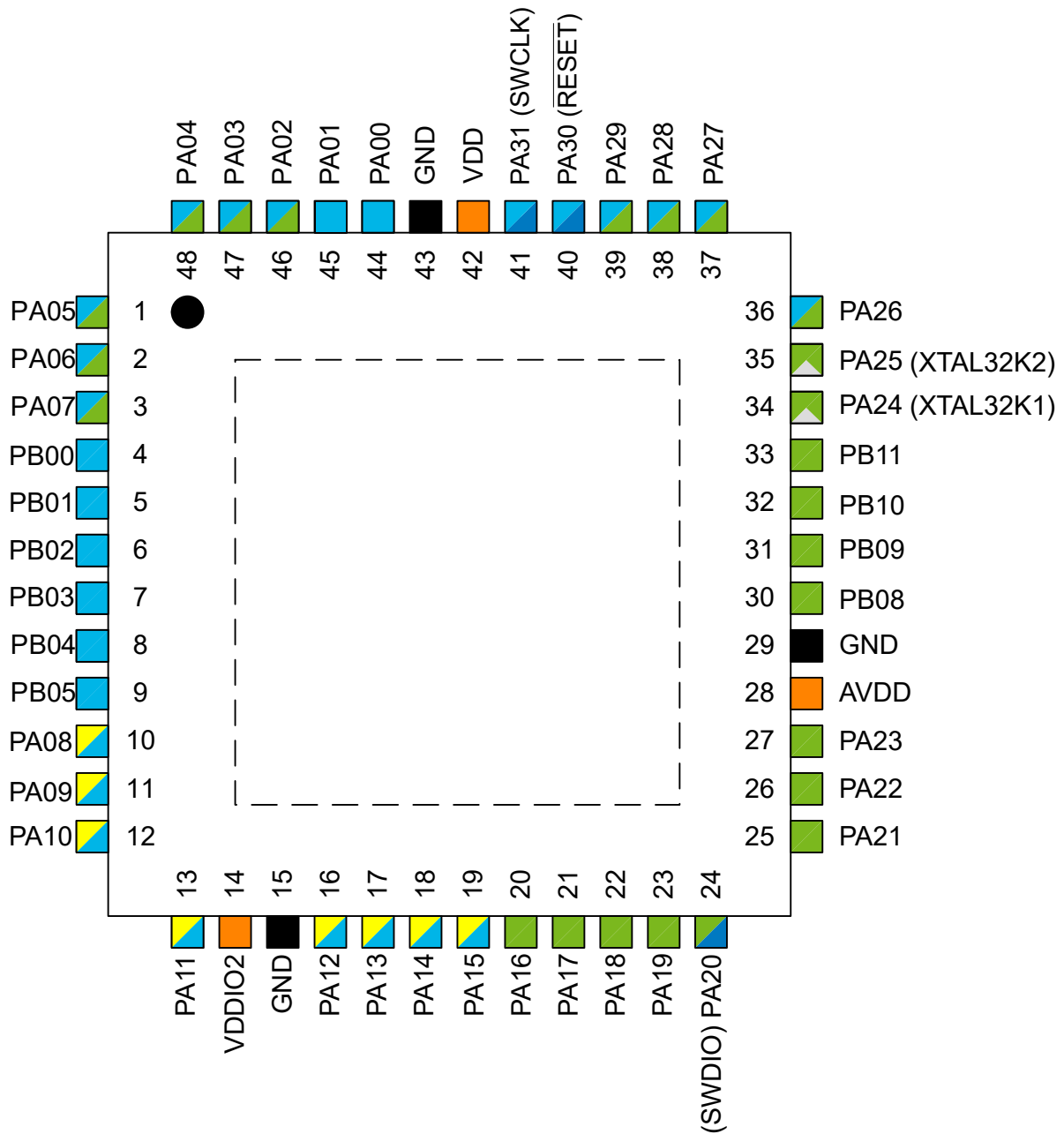
- Programming/Debug
- Clock/Crystal
- Digital Function Only
- Analog Function

2.5. 32-pin VQFN and TQFP

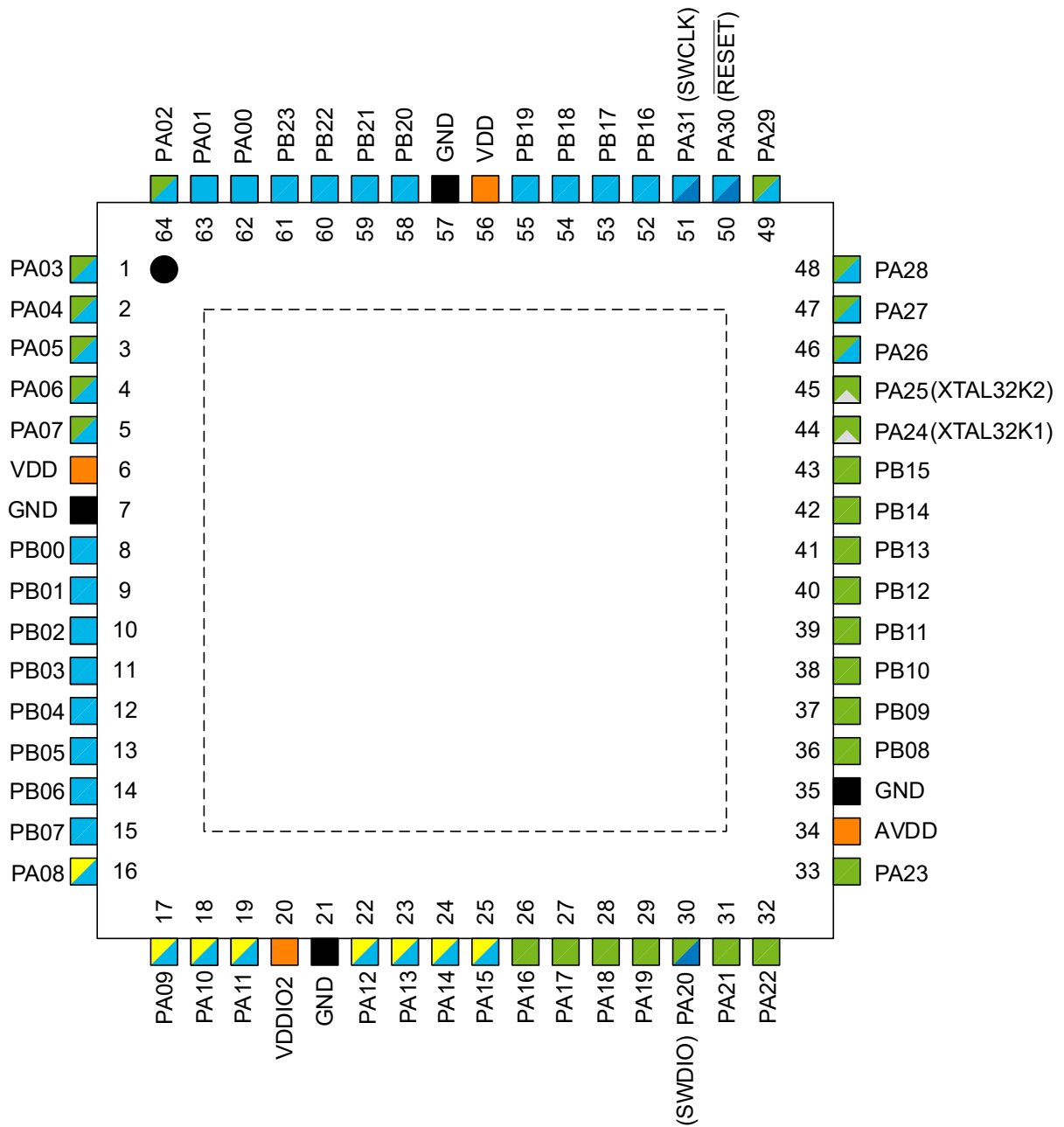


| Power | | Functionality | |
|---|----------------------------|---|-----------------------|
|  | Power Supply |  | Programming/Debug |
|  | Ground |  | Clock/Crystal |
|  | Pin on VDD Power Domain |  | Digital Function Only |
|  | Pin on AVDD Power Domain |  | Analog Function |
|  | Pin on VDDIO2 Power Domain | | |

2.6. 48-pin VQFN and TQFP



2.7. 64-pin VQFN and TQFP



- | Power | Functionality |
|----------------------------|-----------------------|
| Power Supply | Programming/Debug |
| Ground | Clock/Crystal |
| Pin on VDD Power Domain | Digital Function Only |
| Pin on AVDD Power Domain | Analog Function |
| Pin on VDDIO2 Power Domain | |

3. I/O Multiplexing and Considerations

3.1. Pinout and Multiplexing

| Package/Pin Number | | | | | | | | A | | B | | | C | D | E | F | G | H | I | P | | | |
|--------------------|--------|--------|--------|--------|--------|--------|--------|-------------------------|------------|--------|--------|----------|-----------------|-------------------------|---------------------------|---------------------------|----------------------|--------------------|----------------------|----------------------|---------------------|---------|---------|
| 64-pin | 48-pin | 32-pin | 28-pin | 28-pin | 20-pin | 20-pin | SSOP | Pin name | Special | EXTINT | ADC0 | | PTC | ACn | SERCOMn | | TCn | TCC0 | | CCLn, ACn OUT | GCLKn | PTC X/Y | |
| | | | | | | | | | | | Pos | Neg | EXTCINT | | def. and alt. | alt. | | def. and alt. | SWCLK | | | | |
| 62 | 44 | 30 | 26 | 22 | 17 | 4 | PA00 | XTAL32K1 ⁽⁵⁾ | EXTINT[0] | | | | | | 0,PAD[0] ⁽²⁾ | 1,PAD[0] ⁽¹⁾ | 0,W00 ⁽¹⁾ | W00 | | 0,IN0 | 1,IO | | |
| 63 | 45 | 31 | 27 | 23 | 18 | 5 | PA01 | XTAL32K2 ⁽⁵⁾ | NMI | | | | | | 0,PAD[1] ⁽²⁾ | 1,PAD[1] ⁽¹⁾ | 0,W01 ⁽¹⁾ | W01 | | 0,IN1 | 2,IO | | |
| 64 | 46 | 32 | 28 | 24 | 19 | 6 | PA02 | | EXTINT[2] | AINP2 | AINN2 | | | | 0,PAD[2] | 1,PAD[2] ⁽¹⁾ | 1,W00 ⁽¹⁾ | W02 | | 0,IN2 | 3,IO | X2/Y2 | |
| 1 | 47 | 1 | 1 | 25 | 20 | 7 | PA03 | | EXTINT[3] | AINP3 | AINN3 | | | | 0,PAD[3] | 1,PAD[3] ⁽¹⁾ | 1,W01 ⁽¹⁾ | W03 | | 0,IO | 1,IO | X3/Y3 | |
| 2 | 48 | 2 | 2 | 26 | 1 | 8 | PA04 | | EXTINT[4] | AINP4 | AINN4 | | | | 0,PAD[0] ^(1,2) | | | | | | 1,IO ⁽¹⁾ | X4/Y4 | |
| 3 | 1 | 3 | 3 | 27 | 2 | 9 | PA05 | | EXTINT[5] | AINP5 | AINN5 | | | | 0,PAD[1] ^(1,2) | | | | | AC1 ⁽⁴⁾ | 2,IO ⁽¹⁾ | X5/Y5 | |
| 4 | 2 | 4 | 4 | 28 | 3 | 10 | PA06 | | EXTINT[6] | AINP6 | AINN6 | | | | 0,PAD[2] ⁽¹⁾ | | | | | 0,OUT ⁽¹⁾ | 3,IO ⁽¹⁾ | X6/Y6 | |
| 5 | 3 | 5 | 5 | 1 | 4 | 11 | PA07 | | NMI | AINP7 | AINN7 | | | | 0,PAD[3] ⁽¹⁾ | | | | | AC0 ⁽⁴⁾ | 0,IO ⁽¹⁾ | X7/Y7 | |
| 6 | | | | | | | | VDD | | | | | | | | | | | | | | | |
| 7 | | | | | | | | GND | | | | | | | | | | | | | | | |
| 8 | 4 | | | | | | PB00 | | EXTINT[0] | | | | | | | 1,PAD[0] ⁽¹⁾ | | W00 ⁽¹⁾ | | | | | |
| 9 | 5 | | | | | | PB01 | | EXTINT[1] | | | | | | | 1,PAD[1] ⁽¹⁾ | | W01 ⁽¹⁾ | | | | | |
| 10 | 6 | | | | | | PB02 | | EXTINT[2] | | | | | | | 1,PAD[2] ⁽¹⁾ | | W02 ⁽¹⁾ | | | | | |
| 11 | 7 | | | | | | PB03 | | EXTINT[3] | | | | | | | 1,PAD[3] ⁽¹⁾ | | W03 ⁽¹⁾ | | | | | |
| 12 | 8 | | | | | | PB04 | | EXTINT[4] | | | | | | | | | | | | | | |
| 13 | 9 | | | | | | PB05 | | EXTINT[5] | | | | | | | | | | | | | | |
| 14 | | | | | | | PB06 | | EXTINT[6] | | | | | | | | | | | | | | |
| 15 | | | | | | | PB07 | | EXTINT[7] | | | | | | | | | | | | | | |
| 16 | 10 | 6 | 6 | 2 | | | PA08 | VDDIO2 ⁽³⁾ | EXTINT[8] | | | | | | 1,PAD[2] | 0,PAD[2] ⁽¹⁾ | 1,W00 | W00 ⁽¹⁾ | | 1,IN0 | 1,IO ⁽¹⁾ | | |
| 17 | 11 | 7 | 7 | 3 | 5 | 12 | PA09 | VDDIO2 ⁽³⁾ | EXTINT[9] | | | | | | 1,PAD[3] | 0,PAD[3] ⁽¹⁾ | 1,W01 | W01 ⁽¹⁾ | | 1,IN1 | 2,IO ⁽¹⁾ | | |
| 18 | 12 | 8 | 8 | 4 | 6 | 13 | PA10 | VDDIO2 ⁽³⁾ | EXTINT[10] | | | | | | 1,PAD[0] | 0,PAD[0] ^(1,2) | 0,W00 | W02 ⁽¹⁾ | | 1,IN2 | 3,IO ⁽¹⁾ | | |
| 19 | 13 | 9 | 9 | 5 | 7 | 14 | PA11 | VDDIO2 ⁽³⁾ | EXTINT[11] | | | | | | 1,PAD[1] | 0,PAD[1] ^(1,2) | 0,W01 | W03 ⁽¹⁾ | | 1,OUT | 1,IO ⁽¹⁾ | | |
| 20 | 14 | 10 | 10 | 6 | 8 | 15 | VDDIO2 | | | | | | | | | | | | | | | | |
| 21 | 15 | | | | | | GND | | | | | | | | | | | | | | | | |
| 22 | 16 | | | | | | PA12 | VDDIO2 ⁽³⁾ | EXTINT[12] | | | | | | 1,PAD[2] ⁽¹⁾ | | | | | | | | |
| 23 | 17 | | | | | | PA13 | VDDIO2 ⁽³⁾ | EXTINT[13] | | | | | | 1,PAD[3] ⁽¹⁾ | | | | | AC1 ^(1,4) | | | |
| 24 | 18 | | | | | | PA14 | VDDIO2 ⁽³⁾ | EXTINT[14] | | | | | | 1,PAD[0] ⁽¹⁾ | | | | | 1,OUT ⁽¹⁾ | | | |
| 25 | 19 | | | | | | PA15 | VDDIO2 ⁽³⁾ | EXTINT[15] | | | | | | 1,PAD[1] ⁽¹⁾ | | | | | AC0 ^(1,4) | | | |
| 26 | 20 | | | | | | PA16 | | EXTINT[0] | AINP16 | AINN16 | | 0,N1 1,N1 | | | | W00 ⁽¹⁾ | | 2,IN0 | | | X16/Y16 | |
| 27 | 21 | 11 | 11 | 7 | | | PA17 | | EXTINT[1] | AINP17 | AINN17 | | | | | | W01 ⁽¹⁾ | | 2,IN1 | | | X17/Y17 | |
| 28 | 22 | 12 | 12 | 8 | | | PA18 | | EXTINT[2] | AINP18 | AINN18 | | 0,P0 1,P0 | | | | W02 ⁽¹⁾ | | 2,IN2 | | | X18/Y18 | |
| 29 | 23 | 13 | 13 | 9 | | | PA19 | | EXTINT[3] | AINP19 | AINN19 | | 0,N0 1,P1 | | | | W03 ⁽¹⁾ | | 2,OUT | | | X19/Y19 | |
| 30 | 24 | 14 | 14 | 10 | 9 | 16 | PA20 | SWDIO | EXTINT[4] | AINP20 | AINN20 | | 0,P5 1,P2 | 1,PAD[0] ⁽¹⁾ | | 2,W00 | | | | 2,IO ⁽¹⁾ | | X20/Y20 | |
| 31 | 25 | 15 | 15 | 11 | 10 | 17 | PA21 | | EXTINT[5] | AINP21 | AINN21 | EXTCINT0 | 0,P6 1,N0/P5 | 1,PAD[1] ⁽¹⁾ | | 2,W01 | | | | 3,IO ⁽¹⁾ | | X21/Y21 | |
| 32 | 26 | 16 | 16 | 12 | 11 | 18 | PA22 | | EXTINT[6] | AINP22 | AINN22 | EXTCINT1 | 0,P3 1,P3 | 1,PAD[2] ⁽¹⁾ | | | | | 2,OUT ⁽¹⁾ | 1,IO ⁽¹⁾ | | X22/Y22 | |
| 33 | 27 | 17 | 17 | 13 | 12 | 19 | PA23 | VREFA | EXTINT[7] | AINP23 | AINN23 | | 0,N2 1,N2 | 1,PAD[3] ⁽¹⁾ | | | | | | 0,IO ⁽¹⁾ | | X23/Y23 | |
| 34 | 28 | 18 | 18 | 14 | 13 | 20 | AVDD | | | | | | | | | | | | | | | | |
| 35 | 29 | 19 | 19 | 15 | 14 | 1 | AGND | | | | | | | | | | | | | | | | |
| 36 | 30 | | | | | | PB08 | | EXTINT[8] | AINP40 | AINN40 | | | | | | W00 ⁽¹⁾ | | | | | X40/Y40 | |
| 37 | 31 | | | | | | PB09 | | EXTINT[9] | AINP41 | AINN41 | | | | | | W01 ⁽¹⁾ | | | | | X41/Y41 | |
| 38 | 32 | | | | | | PB10 | | EXTINT[10] | AINP42 | AINN42 | | | | | | W02 ⁽¹⁾ | | | | | X42/Y42 | |
| 39 | 33 | | | | | | PB11 | | EXTINT[11] | AINP43 | AINN43 | | | | | | W03 ⁽¹⁾ | | | | | X43/Y43 | |
| 40 | | | | | | | PB12 | | EXTINT[12] | AINP44 | AINN44 | | | | | | | | | | | X44/Y44 | |
| 41 | | | | | | | PB13 | | EXTINT[13] | AINP45 | AINN45 | | | | | | | | | | | X45/Y45 | |
| 42 | | | | | | | PB14 | | EXTINT[14] | AINP46 | AINN46 | | | | | | | | | | | X46/Y46 | |
| 43 | | | | | | | PB15 | | EXTINT[15] | AINP47 | AINN47 | | | | | | | | | | | X47/Y47 | |
| 44 | 34 | 20 | 20 | 16 | | | PA24 | XTAL32K1 ⁽⁶⁾ | EXTINT[8] | AINP24 | AINN24 | | | | 1,PAD[2] ⁽¹⁾ | | W00 ⁽¹⁾ | | 3,IN0 | 1,IO ⁽¹⁾ | | X24/Y24 | |
| 45 | 35 | 21 | 21 | 17 | | | PA25 | XTAL32K2 ⁽⁶⁾ | EXTINT[9] | AINP25 | AINN25 | | | | 1,PAD[3] ⁽¹⁾ | | W01 ⁽¹⁾ | | 3,IN1 | 2,IO ⁽¹⁾ | | X25/Y25 | |
| 46 | 36 | 22 | | | | | PA26 | | EXTINT[10] | AINP26 | AINN26 | | | | 1,PAD[0] ⁽¹⁾ | | W02 ⁽¹⁾ | | 3,IN2 | 3,IO ⁽¹⁾ | | X26/Y26 | |
| 47 | 37 | 23 | | | | | PA27 | | EXTINT[11] | AINP27 | AINN27 | | | | 1,PAD[1] ⁽¹⁾ | | W03 ⁽¹⁾ | | 3,OUT | | | X27/Y27 | |
| 48 | 38 | 24 | | | | | PA28 | | EXTINT[12] | AINP28 | AINN28 | | | | | | | | | | | | X28/Y28 |
| 49 | 39 | 25 | | | | | PA29 | | EXTINT[13] | AINP29 | AINN29 | | | | | | | | | | 1,IO ⁽¹⁾ | | X29/Y29 |
| 50 | 40 | 26 | 22 | 18 | 15 | 2 | PA30 | RESET | NMI | | | | | | | | | | | | | | |
| 51 | 41 | 27 | 23 | 19 | 16 | 3 | PA31 | SWCLK | EXTINT[15] | AINP31 | AINN31 | | | 1,PAD[0] ⁽¹⁾ | 0,PAD[2] ⁽¹⁾ | | | SWCLK | | 0,IO ⁽¹⁾ | | X31/Y31 | |
| 52 | | | | | | | PB16 | | EXTINT[0] | | | | | | | | W00 ⁽¹⁾ | | | | | | |
| 53 | | | | | | | PB17 | | EXTINT[1] | | | | | | | | W01 ⁽¹⁾ | | | | | | |
| 54 | | | | | | | PB18 | | EXTINT[2] | | | | | | | | W02 ⁽¹⁾ | | | | | | |
| 55 | | | | | | | PB19 | | EXTINT[3] | | | | | | | | W03 ⁽¹⁾ | | | | | | |
| 56 | 42 | 28 | 24 | 20 | | | VDD | | | | | | | | | | | | | | | | |
| 57 | 43 | 29 | 25 | 21 | | | GND | | | | | | | | | | | | | | | | |

| Package/Pin Number | | | | | | | | | | A | | B | | | C | D | E | F | G | H | I | P |
|--------------------|--------|--------|--------|----------------|--------|--------|-----|-------------|---------|-----------|------|---------|------------------|-----|---------|------------------|----------------------|-------|-----|------------------|-------|-----|
| VQFN/ TQFP | | VQFN | | SSOP/ SPDIP | | VQFN | | Pin name | Special | EXTINT | ADC0 | | PTC | ACn | SERCOMn | | TCn | TCC0 | | CCLn, ACn OUT | GCLKn | PTC |
| 64-pin | 48-pin | 32-pin | 28-pin | 28-pin | 20-pin | 20-pin | Pos | | | | Neg | EXTCINT | def. and alt. | | alt. | def. and alt. | | SWCLK | X/Y | | | |
| | | | | | | | | PB20 | | EXTINT[4] | | | | | | | 2,W00 ⁽¹⁾ | | | | | |
| | | | | | | | | PB21 | | EXTINT[5] | | | | | | | 2,W01 ⁽¹⁾ | | | | | |
| | | | | | | | | PB22 | | EXTINT[6] | | | | | | | | | | | | |
| | | | | | | | | PB23 | | EXTINT[7] | | | | | | | | | | | | |

1. Alternative pin position. To select alternative pin positions, refer to the *Port Multiplexer* chapter.
2. This pin supports I²C with SERCOM0.
3. This pin is on the VDDIO2 power domain. For usage and properties, refer to the MVIO description in the *SUPC - Supply Controller* and in the *Electrical Characteristics* sections.
4. The output of the Analog Comparator to the pin can be used as input to the CCL. Refer also to the *CCL - Configurable Custom Logic* section.
5. Applicable only for 20-pin devices.
6. Not applicable for 20-pin devices.

4. Product Brief Revision History

Note: The product brief revision is independent of the die revision and the device variant (the last letter of the ordering number).

4.1. Rev. B - 02/2026

| Section | Description |
|-----------------|--|
| Document | Removed the 16 kB variant |
| Features | Minor updates and clarifications to the text |
| Family Overview | Updated figure; the 16 kB variant has been removed |

4.2. Rev. A - 09/2025

| Section | Description |
|----------|--------------------------|
| Document | Initial document release |

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