Data Sheet

LT8350S

40V$_{IN}$, 18V$_{OUT}$, 6A Synchronous Buck-Boost Silent Switcher® 2

FEATURES

- 4-Switch Single Inductor Architecture Allows V$_{IN}$ Above, Below or Equal to V$_{OUT}$
- Silent Switcher® 2 Architecture for Low EMI
- Up to 95% Efficiency at 2MHz
- Proprietary Peak Current Mode
- 3V to 40V Input Voltage Range
- 1V to 18V Output Voltage Range
- ±1.5% Output Voltage Regulation
- Output/Input Current Regulation and Monitor
- Constant-voltage/Constant-current Regulation
- High-Side PMOS Load Switch Driver
- No Top MOSFET Refresh Noise in Buck or Boost
- 200kHz to 2MHz Fixed Switching Frequency with External Frequency Synchronization and SSFM
- V$_{OUT}$ Disconnected from V$_{IN}$ During Shutdown
- Small 4mm x 6mm 32-Pin LQFN Package
- AEC-Q100 Qualified

APPLICATIONS

- Automotive, Industrial, Telecom Systems
- Voltage Regulator with Accurate Current Limit
- High-Frequency Battery-Powered System
- USB Power Delivery (USB-PD) Source

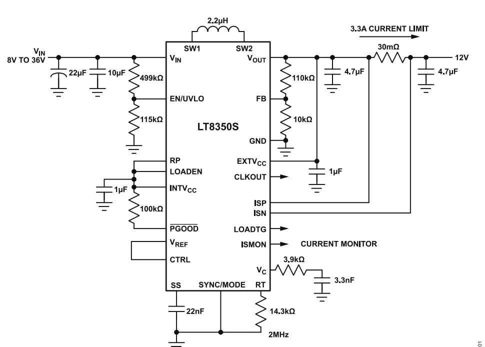
GENERAL DESCRIPTION

The LT8350S is a monolithic 4-switch synchronous buck-boost converter with second-generation Silent Switcher architecture to minimize electromagnetic interference (EMI) emissions while delivering high efficiency at high switching frequency. The switcher can regulate the output voltage, input or output current from input voltages above, below, or equal to the output voltage. The proprietary peak current mode control scheme allows for the synchronization and adjustment of 200kHz to 2MHz fixed frequency operation or spread spectrum frequency modulation (SSFM) operation. With a 3V to 40V input voltage range, 1V to 18V output voltage capability, and seamless low noise transitions between operation regions, the LT8350S is ideal for voltage regulator, battery, and super-capacitor charger applications in automotive, industrial, telecom, and battery-powered systems.

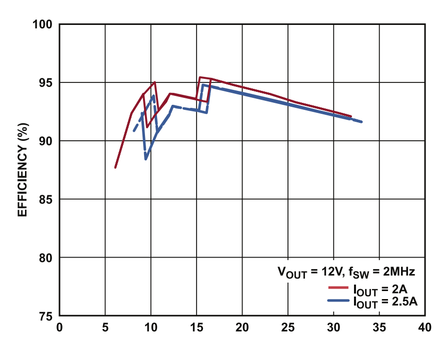
The LT8350S provide an input or output current monitor and power good flag. Robust fault protection is provided to detect output short-circuit conditions, during which the LT8350S retries, latches off, or keeps running.

	Maximum Junction Temperature	Internal Caps
LT8350	150°C	No
LT8350S	125°C	Yes

SIMPLIFIED APPLICATION DIAGRAM



95% Efficient 24W (12V, 2A) 2MHz Buck-Boost Voltage Regulator with Output Current Limit



EFFICIENCY vs V$_{IN}$

TABLE OF CONTENTS

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/24	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = 25°C, unless otherwise specified, where conditions must be at full operating temperature range. V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V, unless otherwise noted.)

PARAMETER	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Input and Output						
Input Voltage Range		T_A = -40°C to 125°C	3		40	V
V_{IN} Shutdown Current	$V_{EN/UVLO}$ = 0.3V			2	5	µA
V_{IN} Active Current (Not Switching)	$V_{EN/UVLO}$ = 1.5V, $EXTV_{CC}$ = 0V			3.5	5	mA
	$V_{EN/UVLO}$ = 1.5V, $EXTV_{CC}$ = 5V			400	650	mA
$EXTV_{CC}$ Voltage Range		T_A = -40°C to 125°C	1		18	V
Output Voltage Range		T_A = -40°C to 125°C	0		18	V
EN/UVLO Shutdown Threshold	Falling		0.3	0.6	0.9	V
EN/UVLO Enable Threshold	Falling	T_A = -40°C to 125°C	1.196	1.220	1.244	V
EN/UVLO Enable Hysteresis				15		mV
EN/UVLO Enable Hysteresis Current	$V_{EN/UVLO}$ = 1.1V		2.1	2.5	2.9	µA
	$V_{EN/UVLO}$ = 1.5V		-0.1	0	0.1	µA
Linear Regulators						
$INTV_{CC}$ Regulation Voltage	$IINTV_{CC}$ = 20mA		3.4	3.6	3.8	V
V_{REF} Regulation Voltage	I_{VREF} = 100µA	T_A = -40°C to 125°C	1.99	2.00	2.03	V
Current Regulation Loop						
Full-Scale Current Regulation	V_{CTRL} = 2V, V_{ISP} = 12V	T_A = -40°C to 125°C	97	100	103	mV
	V_{CTRL} = 2V, V_{ISP} = 0V	T_A = -40°C to 125°C	97	100	103	mV
ISP/ISN Input Common Mode Range		T_A = -40°C to 125°C	0		40	V
ISP/ISN Current Regulation Amplifier g_m				2300		µS
Voltage Regulation Loop						
FB Pin Current	FB in Regulation, Current Out of Pin			35	80	nA

(T_A = 25°C, unless otherwise specified, where conditions must be at full operating temperature range. V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V, unless otherwise noted.)

PARAMETER	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
FB Regulation Voltage	V_C = 0.8V	T_A = -40°C to 125°C	0.985	1.00	1.015	V
FB Line Regulation	V_{IN} = 3V to 40V			0.02	0.2	%
FB Load Regulation				0.02	0.1	%
FB Voltage Regulation Amplifier g_m				580		uS
V_C Output Impedance				10		MΩ
Power Switches						
Maximum Switch Current Limit	Peak-Boost Current Mode		6.3	7.0	7.7	A
	Peak-Buck Current Mode		5.8	7.0	8.0	A
Switch A On-Resistance (From V_{IN} to SW1)	I_{SW} = 1A			50		mΩ
Switch B On-Resistance (From SW1 to GND)	I_{SW} = 1A			50		mΩ
Switch C On-Resistance (From SW2 to GND)	I_{SW} = 1A			30		mΩ
Switch D On-Resistance (From V_{OUT} to SW2)	I_{SW} = 1A			30		mΩ
Oscillator						
Switching Frequency	$V_{SYNC/MODE}$ = 0V, R_T = 14.3kΩ	T_A = -40°C to 125°C	1930	2000	2070	kHz
	$V_{SYNC/MODE}$ = 0V, R_T = 178kΩ	T_A = -40°C to 125°C	260	290	320	kHz
SYNC Frequency			200		2000	kHz
SYNC/MODE Threshold Voltage			0.4		1.5	V
Spread Spectrum Above Oscillator Frequency	$V_{SYNC/MODE}$ = 3.6V		20	23	26	%
Fault						
FB Short Threshold (V_{FB})	Falling		0.23	0.23	0.27	V

(T_A = 25°C, unless otherwise specified, where conditions must be at full operating temperature range. V_{IN} = 12V, $V_{EN/UVLO}$ = 1.5V, unless otherwise noted.)

PARAMETER	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
FB Short Hysteresis			38	50	62	mV
ISP/ISN Over Current Threshold $V_{(ISP-ISN)}$	V_{ISP} = 12V			750		mV
$\overline{PGOOD}$ Upper Threshold Offset from V_{FB}	Rising		8	10	12	%
$\overline{PGOOD}$ Lower Threshold Offset from V_{FB}	Falling		-12	-10	-8	%
$\overline{PGOOD}$ Pull-Down Resistance				130	200	Ω
SS Hard Pull-Down Resistance				130	200	Ω
SS Pull-Up Current	V_{FB} = 0.8V, V_{SS} = 0V		10.5	12.5	14.5	µA
SS Pull-Down Current	V_{FB} = 1V, V_{SS} = 2V		1.0	1.25	1.5	µA
SS Fault Latch-Off Threshold				1.75		V
SS Fault Reset Threshold				0.2		V
Output Current Monitor						
ISMON Voltage	$V_{(ISP-ISN)}$ = 100mV, V_{ISP} = 12V/0V		1.21	1.25	1.29	V
ISMON Voltage	$V_{(ISP-ISN)}$ = 0mV, V_{ISP} = 12V/0V		0.22	0.25	0.28	V
Load Switch Driver						
LOADEN Threshold	Rising			1.5		V
LOADEN Hysteresis				540		mV
Minimum V_{OUT} for LOADTG to be ON	V_{LOADEN} = 5V			3	4.0	V
LOADTG ON Voltage $V_{(VOUT-LOADTG)}$	V_{OUT} = 12V		4.5	5	5.5	V
LOADTG OFF Voltage $V_{(VOUT-LOADTG)}$	V_{OUT} = 12V		-0.1	0	0.1	V

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}, EN/UVLO, ISP, ISN	-0.3V to 42V
V_{OUT}, $EXTV_{CC}$	-0.3V to 20V
SW1	-0.3V to 42V
SW2	-0.3V to 20V
BST1	47V
BST2	25V
BST1–SW1, BST2–SW2, $INTV_{cc}$	-0.3V to 5V
CTRL, FB, LOADEN, SYNC/MODE, $\overline{PGOOD}$	-0.3V to 5V
ISMON, V_C, R_T	-0.3V to 5V
SS, VREF	-0.3V to 4V
ISP-ISN	-1V to 1V
CLKOUT, LOADTG	([1])
Operating Junction Temperature Range ([2, 3])	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C

1 Do not apply a positive or negative voltage source to these pins, otherwise permanent damage may occur.

2 The LT8350S is specified over the –40°C to 125°C operating junction temperature range. High Junction temperatures degrade operating lifetimes. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors.

3 The LT8350S includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Electrostatic Discharge (ESD)

The following ESD information is provided for the handling of ESD-sensitive devices in an ESD-protected area only Human body model (HBM) per ANSI/ESDA/JEDEC JS-001 and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings

Table 3. ESD Ratings for LT8350S

ESD Model	Withstand Threshold (V)
HBM	±4000
CDM	±1250

ESD Caution

	**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

Table 4. Thermal Resistance on EVAL-LT8350S-AZ

Thermal Resistance, Four-Layer Board	
Junction-to-Ambient (θ_{JA})	19°C/W
Junction-to-Case (θ_{JCtop})	28°C/W
Junction-to-Case Thermal Resistance (Ψ_{JT})	0.6°C/W

Table 5. Thermal Resistance on JEDEC Board

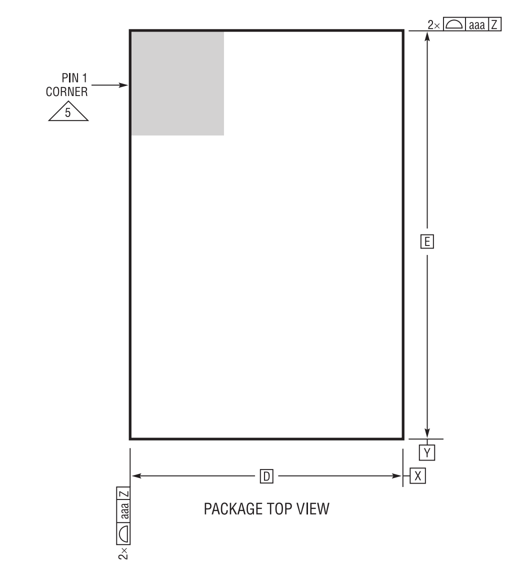
Thermal Resistance, Four-Layer Board[4]	
Junction-to-Ambient (θ_{JA})	30°C/W
Junction-to-Case (θ_{JCtop})	28°C/W
Junction-to-Case (Ψ_{JT})	0.7°C/W

[4] Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.

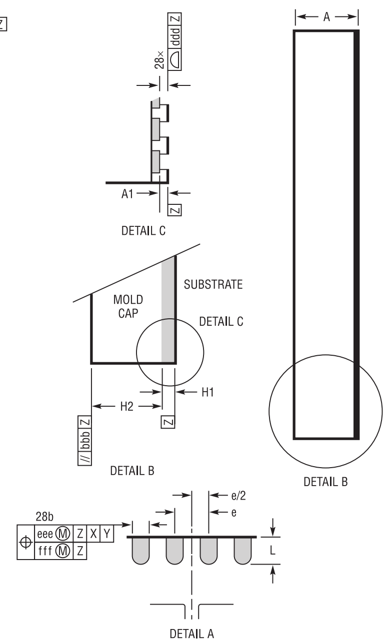
For the latest package outline information and land patterns (footprints), go to **https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

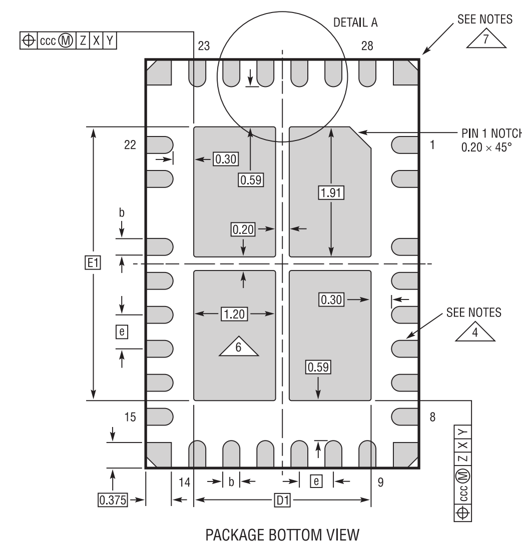
Package thermal resistances were obtained using the evaluation kit, a four-layer board. For detailed information on package thermal considerations, refer **https://www.analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages.html**.

LQFN Package
32(28)-Lead (6mm × 4mm × 0.94mm)
(Reference LTC DWG # 05-08-1676 Rev Ø)

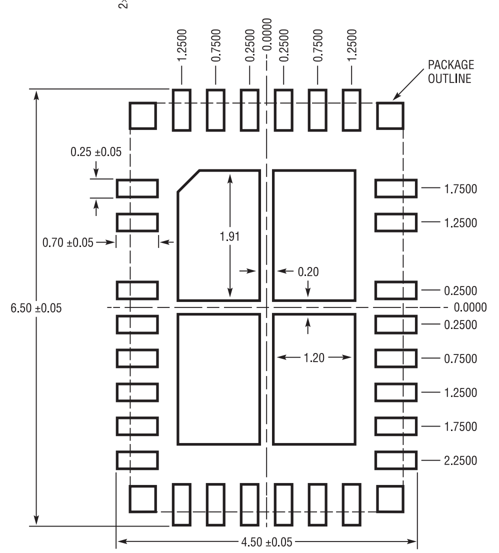


PACKAGE TOP VIEW





PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

	DIMENSIONS			
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	0.85	0.94	1.03	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		4.00		
E		6.00		
e		0.50		
D1		2.60		
E1		4.02		
H1		0.24 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

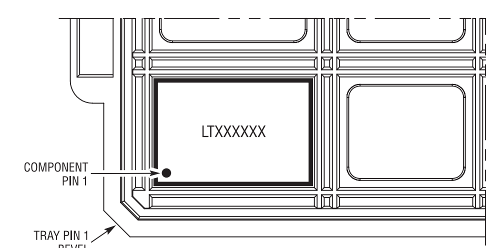
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE

4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES

5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE

6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT

7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL



PACKAGE IN TRAY LOADING ORIENTATION

LQFN 32(28) 0818 REV Ø

TYPICAL OPERATING CHARACTERISTICS

T_A = 25°C, Unless otherwise noted.

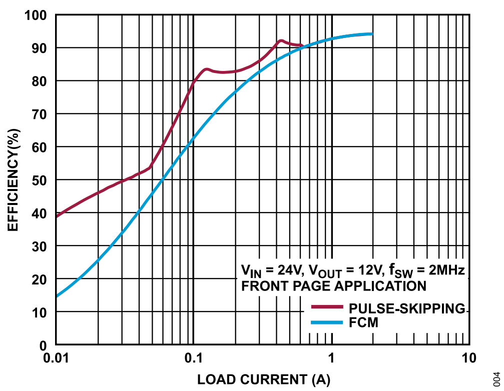


Figure 1. Efficiency vs Load Current (Buck Region)

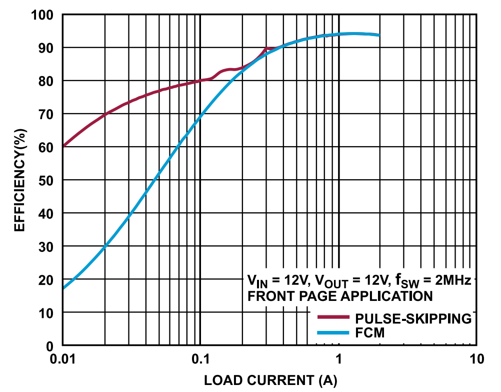


Figure 2. Efficiency vs Load Current (Buck-Boost Region)

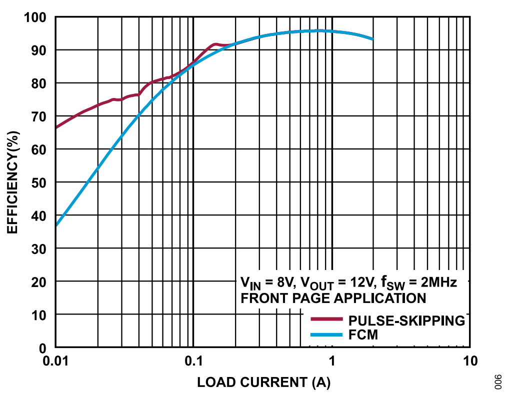


Figure 3. Efficiency vs Load Current (Boost Region)

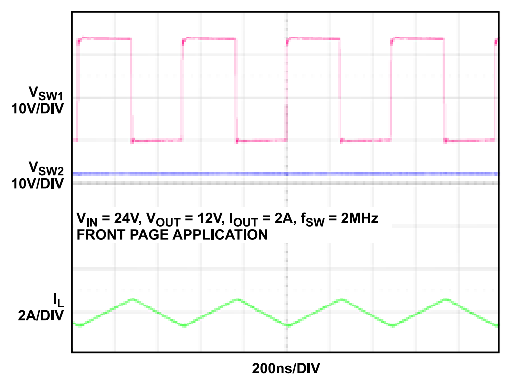


Figure 4. Switching Waveforms (Buck Region)

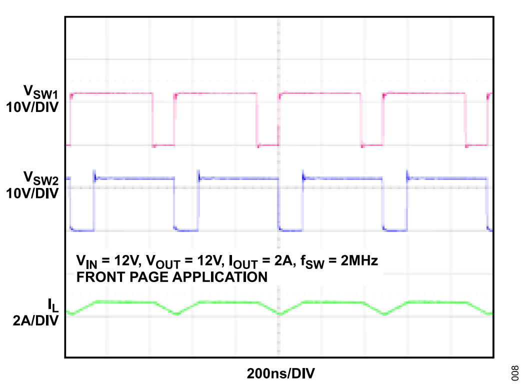


Figure 5. Switching Waveforms (Buck-Boost Region)

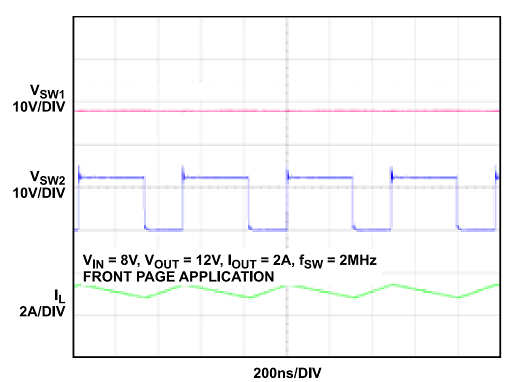


Figure 6. Switching Waveforms (Boost Region)

T_A = 25°C, Unless otherwise noted.

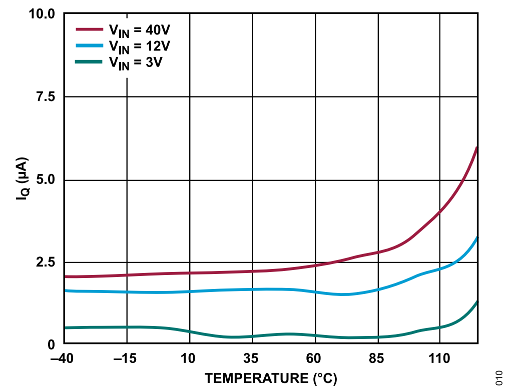


Figure 7. V_{IN} Shutdown Current

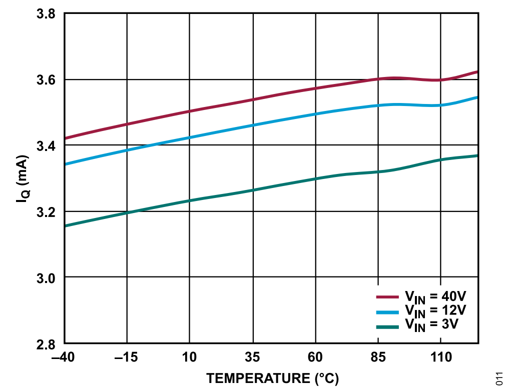


Figure 8. V_{IN} Active Current

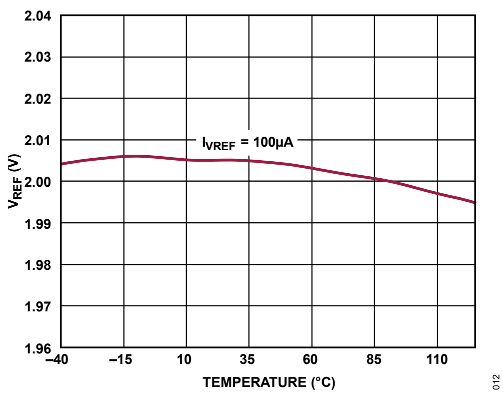


Figure 9. V_{REF} Voltage vs Temperature

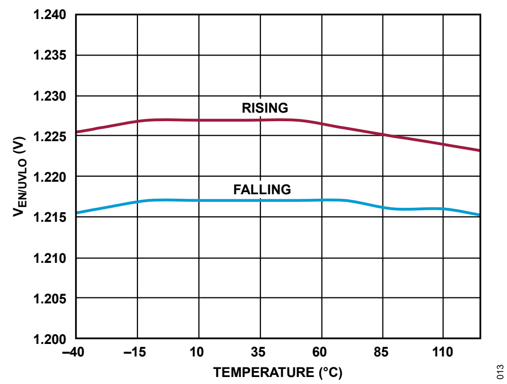


Figure 10. EN/UVLO Enable Threshold

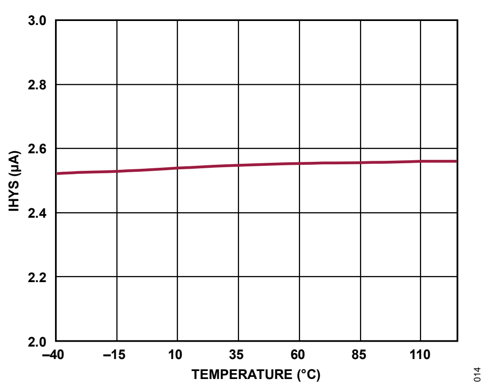


Figure 11. EN/UVLO Hysteresis Current

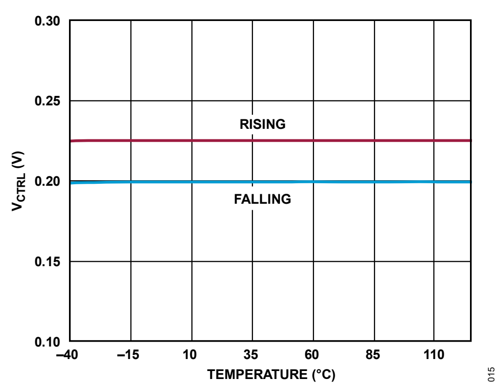


Figure 12. CTRL Off Threshold

T_A = 25°C, Unless otherwise noted.

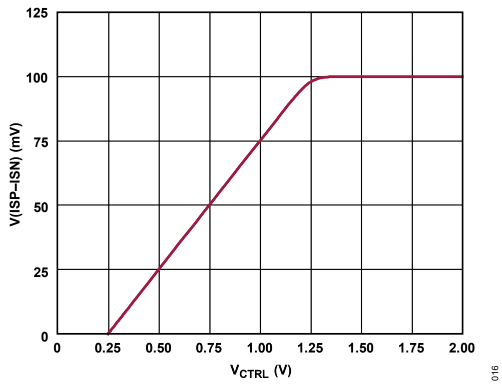


Figure 13. $V_{(ISP-ISN)}$ Regulation vs V_{CTRL}

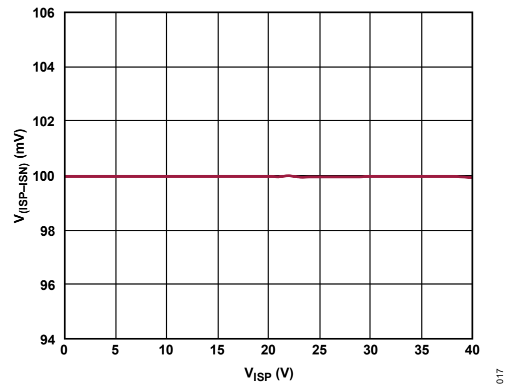


Figure 14. $V_{(ISP-ISN)}$ Regulation vs V_{ISP}

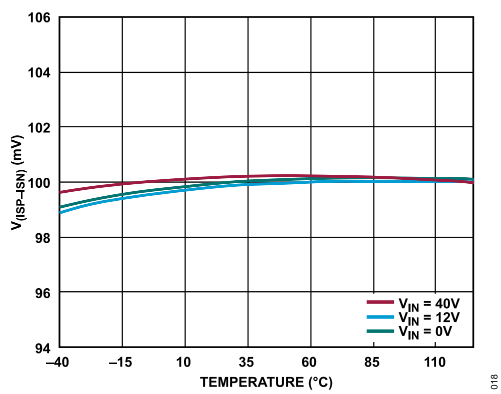


Figure 15. $V_{(ISP-ISN)}$ Regulation vs Temperature

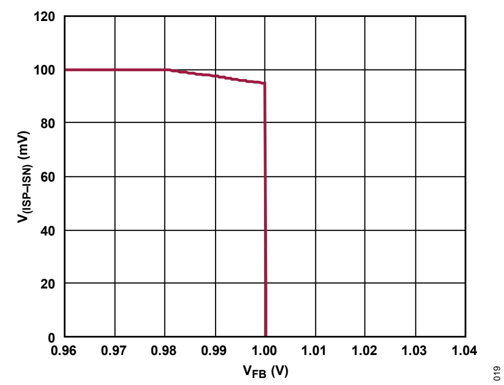


Figure 16. $V_{(ISP-ISN)}$ Regulation vs $V_{(FB)}$

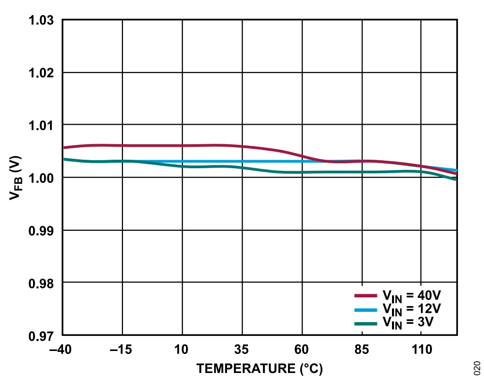


Figure 17. FB Regulation vs Temperature

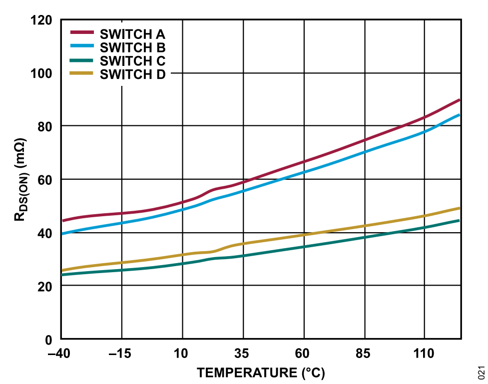


Figure 18. Power Switch $R_{DS(ON)}$

T_A = 25°C, Unless otherwise noted.

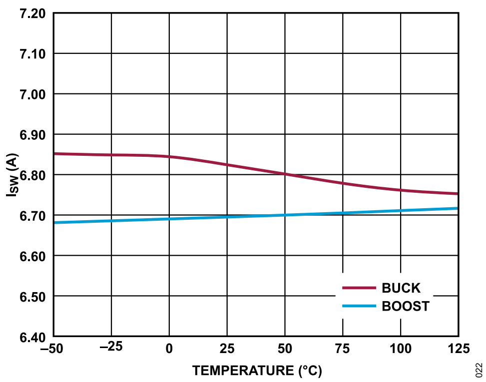


Figure 19. Peak Current vs Temperature

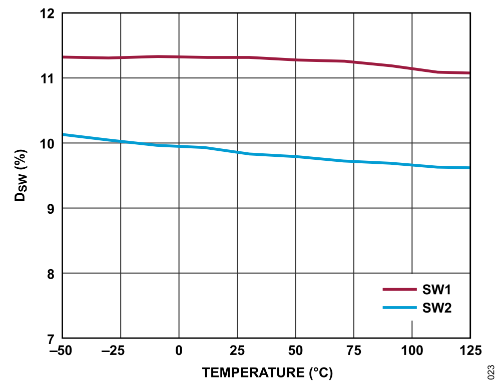


Figure 20. Minimum On-Time vs Temperature

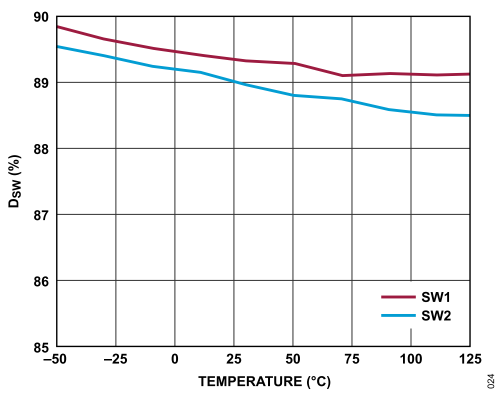


Figure 21. Maximum On-Time vs Temperature

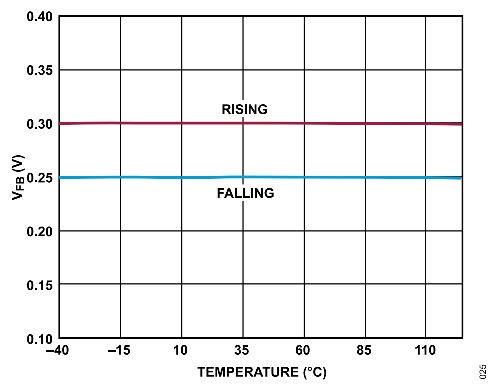


Figure 22. FB Short-Circuit Threshold

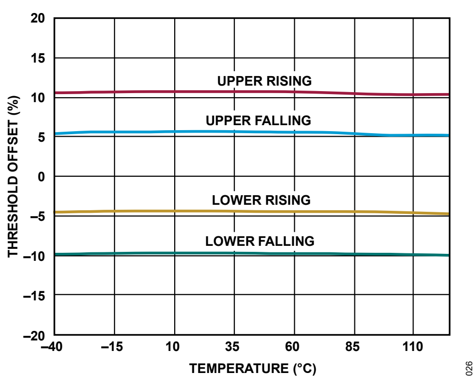


Figure 23. $\overline{PGOOD}$ Threshold

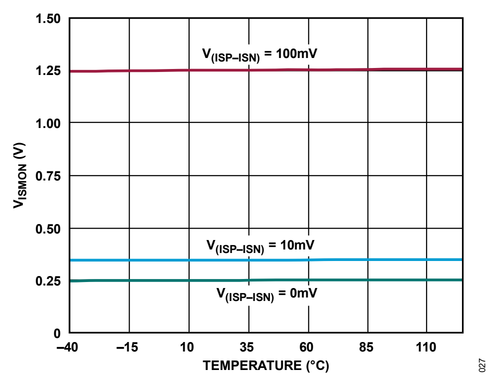


Figure 24. ISMON vs Temperature

T_A = 25°C, Unless otherwise noted.

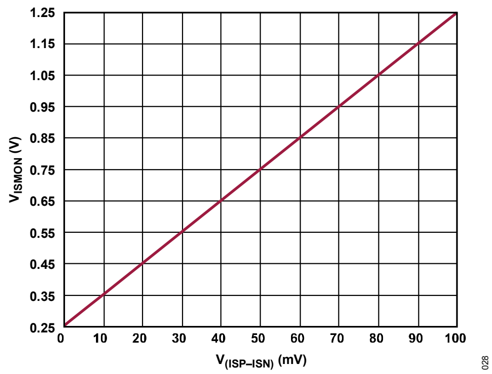


Figure 25. ISMON vs Temperature

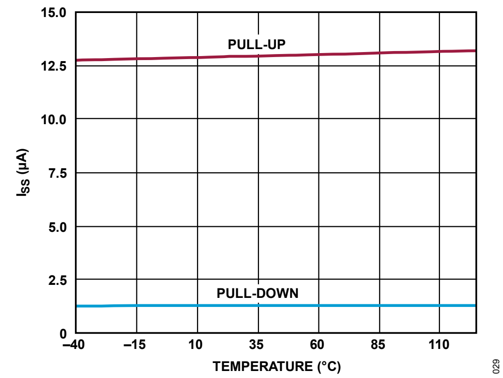


Figure 26. SS Current Temperature

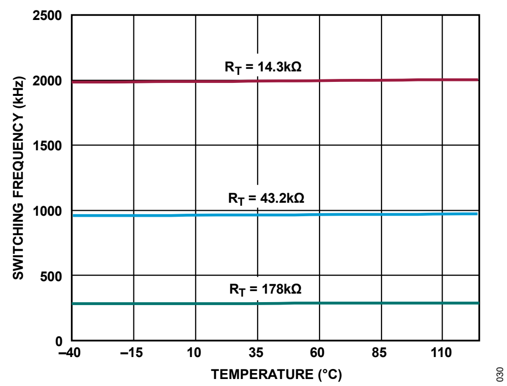
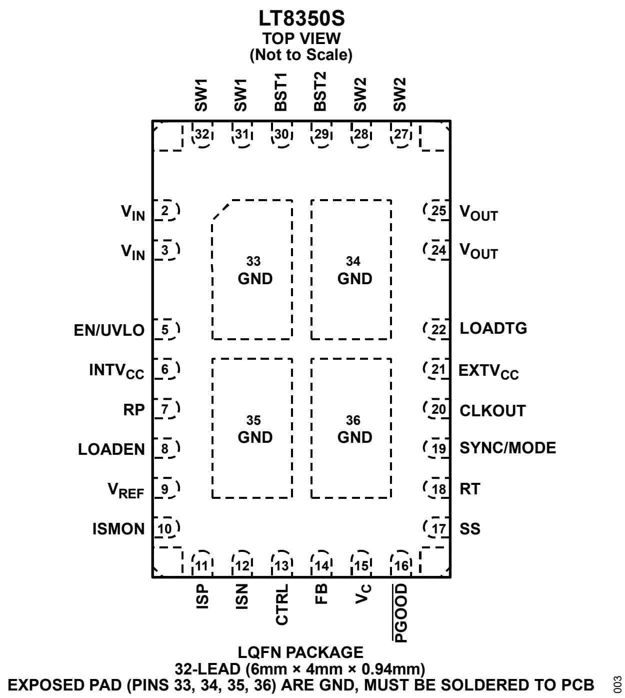


Figure 27. Frequency vs Temperature

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



PIN DESCRIPTIONS

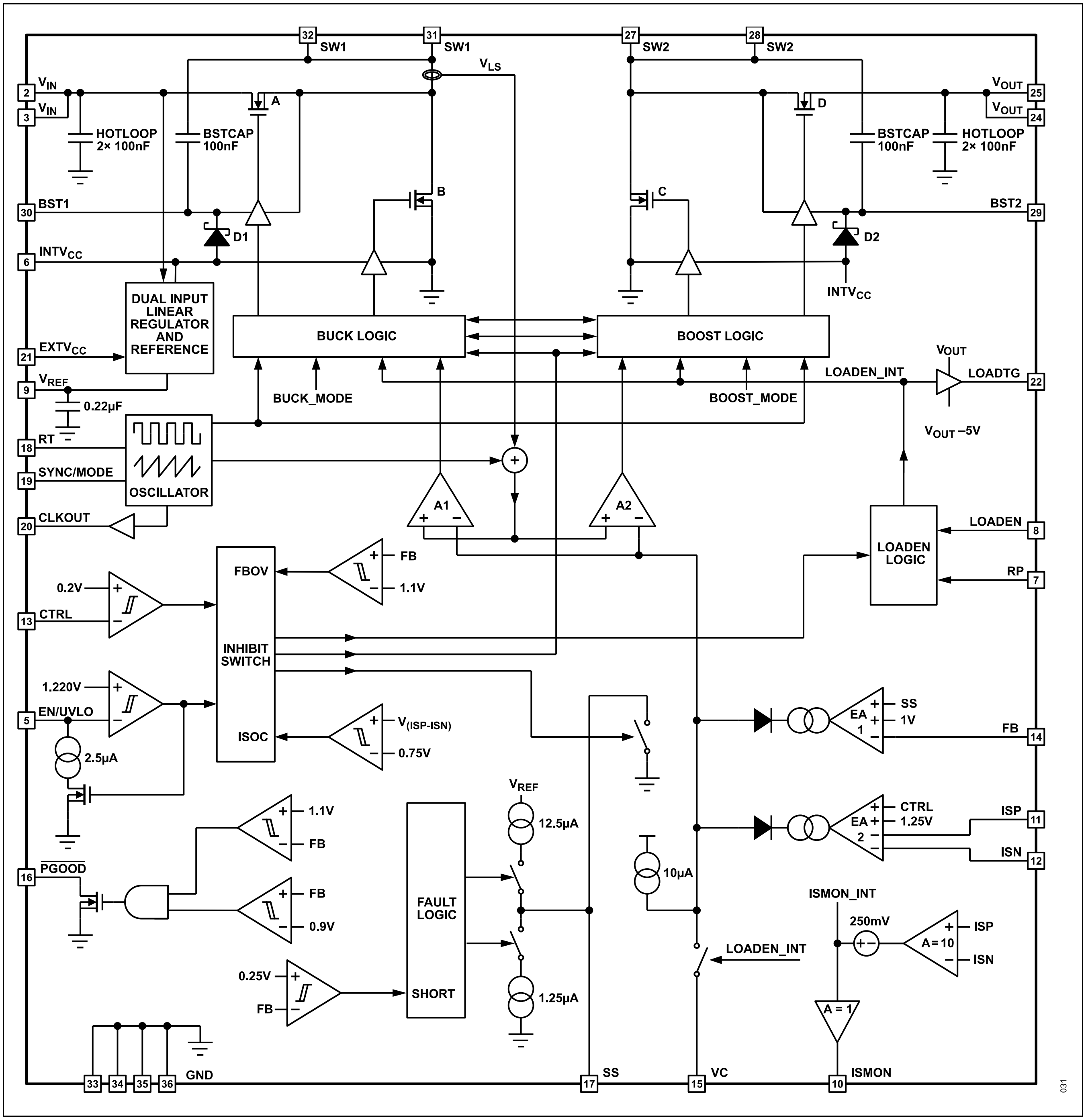
Table 6. Pin Descriptions

PIN	NAME	DESCRIPTION
2, 3	V_{IN}	Input Voltage Pin. The V_{IN} pin supplies the internal circuitry and connects to the power input of the converter. Bypass this pin to ground with a ceramic capacitor. The bypass capacitor should be placed as close to the chip as possible with vias directly down to the ground plane.
5	EN/UVLO	Enable and Undervoltage Lockout Pin. Force the pin below 0.3V to shut down the chip. Force the pin above 1.235V (typical) for normal operation. If neither function is used, connect this pin directly to V_{IN}. See the *Applications Information* section for *Programming VIN UVLO*.
6	$INTV_{CC}$	Internal 3.6V Linear Regulator Output Pin. Powered from the V_{IN} pin, the $INTV_{CC}$ supplies the internal control circuitry and gate drivers. Do not force any voltage on this pin. Place a 1µF bypass capacitor to GND close to the package.
7	RP	Factory Test Pin. Always connect this pin to $INTV_{CC}$.
8	LOADEN	Load Switch Enable Input. The LOADEN pin controls the ON/OFF of the high-side PMOS load switch. If the load switch control is not used, connect this pin to V_{REF} or $INTV_{CC}$. Forcing the pin low turns off all power switches, disconnects the V_C pin from all internal loads, and turns off LOADTG.

PIN	NAME	DESCRIPTION
9	V_{REF}	Voltage Reference Output Pin. The V_{REF} pin provides an accurate 2V reference capable of supplying up to 2mA current. It can be used to supply resistor networks to set the voltages at the CTRL pin. An optional bypass capacitor to GND can be placed on this pin close to the package.
10	ISMON	ISP/ISN Current Monitor Output Pin. The ISMON pin generates a buffered voltage that is equal to ten times $V_{(ISP-ISN)}$ plus 0.25V offset voltage. The voltage on the ISMON pin will be 1.25V when $V_{(ISP-ISN)}$ is equal to 100mV full-scale.
11	ISP	Positive Terminal of ISP/ISN Current Sense Resistor (RIS). Ensure accurate current sense with Kelvin connection.
12	ISN	Negative Terminal of ISP/ISN Current Sense Resistor (RIS). Ensure accurate current sense with Kelvin connection.
13	CTRL	Control Input for ISP/ISN Current Sense Threshold. The CTRL pin is used to program the ISP/ISN regulation current. The V_{CTRL} can be set by an external voltage reference or a resistor divider from V_{REF} to ground. Connect the CTRL pin to V_{REF} for a 100mV full-scale threshold or force below 0.1V to stop switching. See the *Applications Information* section for the *Programming Input or Output Current Limit*.
14	FB	Voltage Loop Feedback Input. The FB pin is used for constant voltage regulation and output fault protection. See the *Applications Information* section for *Programming Output Voltage and Thresholds*.
15	V_C	Error Amplifier Output to Set Inductor Current Comparator Threshold. The VC pin is used to compensate the control loop with an external resistor–capacitor (RC) network. During the LOADEN low state, the VC pin is disconnected from all internal loads to store its voltage information.
16	$\overline{\text{PGOOD}}$	Power Good Open Drain Output. The $\overline{\text{PGOOD}}$ pin is pulled low when the FB pin is within ±10% of the final regulation voltage. To function, this pin requires an external pull-up resistor.
17	SS	The SS pin is used to set a soft-start timer by connecting a capacitor to ground. An internal 12.5µA pull-up current charging the external SS capacitor gradually ramps up FB regulation voltage. Any UVLO or thermal shutdown immediately pulls this pin to ground to stop switching. See the *Applications Information* section for *Start-Up and Fault Protection*.
18	RT	Switching Frequency Setting. Connect a resistor from this pin to ground to set the internal oscillator frequency from 200kHz to 2MHz.
19	SYNC/MODE	External Switching Frequency Synchronization and Operation Mode Selection. This pin allows five selectable modes for optimizing performance. See the *Applications Information* section for *Frequency Synchronization and Operation Mode Selection*.
20	CLKOUT	Clock output. The CLKOUT pin provides a 50% duty cycle square wave with 180° out of phase with the system clock. This allows synchronization with other regulators. Float this pin if the CLKOUT function is not used.
21	$EXTV_{CC}$	Second Input Supply for Powering $INTV_{CC}$. The part intelligently chooses either V_{IN} or $EXTV_{CC}$ for $INTV_{CC}$ LDO to improve efficiency. Connect this pin to GND if not used.

PIN	NAME	DESCRIPTION
22	LOADTG	High-Side PMOS Load Switch Top Gate Drive. The LOADTG pin produces a buffered and inverted version of the LOADEN input signal and drives an external high-side PMOS load switch with a voltage swing from the higher voltage between (V_{OUT}−5V) and 1.2V to V_{OUT}. Leave this pin open if not used.
24, 25	V_{OUT}	Power Output. The V_{OUT} pins connect to the power output of the converter, and also serve as the positive rail for the LOADTG drive. Bypass this pin to ground with a ceramic capacitor. The bypass capacitor should be placed as close to the chip as possible with vias directly down to the ground plane.
27, 28	SW2	Boost Side Switch Node. The SW2 pins connect to the internal power switches, and swing from ground to a diode voltage above V_{OUT}. Do not force any voltage on these pins.
29	BST2	Boost Side Bootstrap Floating Driver Supply. The BST2 pin connects to an integrated bootstrap diode and capacitor from the $INTV_{CC}$ pin and supplies the boost side top power switch gate driver. Do not connect anything to this pin.
30	BST1	Buck Side Bootstrap Floating Driver Supply. The BST1 pin connects to an integrated bootstrap diode and capacitor from the $INTV_{CC}$ pin and supplies the buck side top power switch gate drive. Do not connect anything to this pin.
31, 32	SW1	Buck Side Switch Node. The SW1 pins connect to the internal power switches, and swing from a diode voltage drop below ground up to V_{IN}. Do not force any voltage on these pins.
33, 34, 35, 36	GND	Ground. Solder the exposed pads directly to the ground plane.
	Corner Pins	These pins are for mechanical support only and can be connected anywhere on the Printed Circuit Board (PCB).

BLOCK DIAGRAM



OPERATION

The LT8350S is a current mode DC/DC converter that can regulate output voltage from input voltage above, below, or equal to the output voltage. Four internal low-resistance N-channel double-diffused Metal-Oxide-Semiconductor (DMOS) switches minimize the size of the application circuit and reduce power losses to maximize efficiency. Internal high-side gate drivers further simplify the design process. The ADI proprietary peak current mode control scheme directly senses the inductor current across the internal power switches. It provides a smooth transition between buck region, buck-boost region, and boost region. The LT8350S can be configured to operate over a wide range of switching frequencies, from 200kHz to 2MHz, allowing applications to be optimized for broad area and efficiency. See the *Block Diagram* for the best understanding of the operation.

Power Switch Control

Figure 28 shows the topology of the LT8350S power stage, which is comprised of four N-channel DMOS switches and their associated gate drivers. *Figure 29* shows the current mode control as a function of the V_{IN}/V_{OUT} ratio, and *Figure 30* shows the operation region as a function of the V_{IN}/V_{OUT} ratio. The power switches are properly controlled to transition smoothly between modes and regions. Hysteresis is added to prevent chattering between modes and regions.

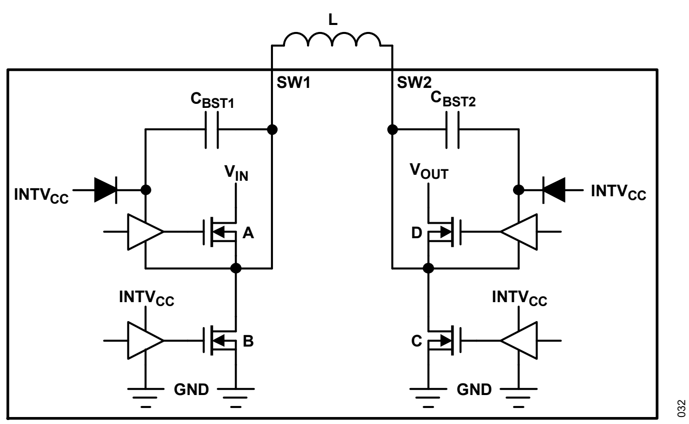


Figure 28. Power Stage Schematic

There are a total of four states:

(1) Peak-Buck current mode control in Buck region.

(2) Peak-Buck current mode control in the Buck-Boost region.

(3) Peak-Boost current mode control in the Buck-Boost region, and

(4) Peak-Boost current mode control in Boost region.

The following sections provide detailed descriptions for each state with waveforms, in which the shoot-through protection dead time between switches A and B and between switches C and D are ignored for simplification.

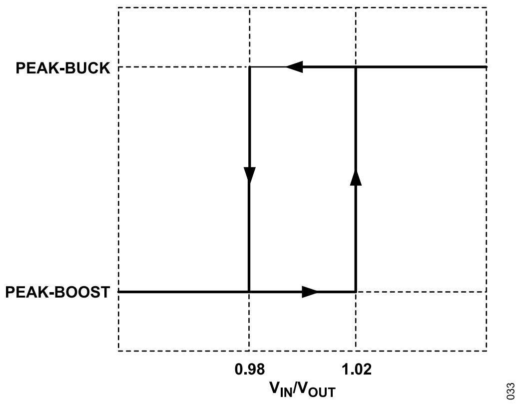


Figure 29. Current Mode vs V_{IN}/V_{OUT} Ratio

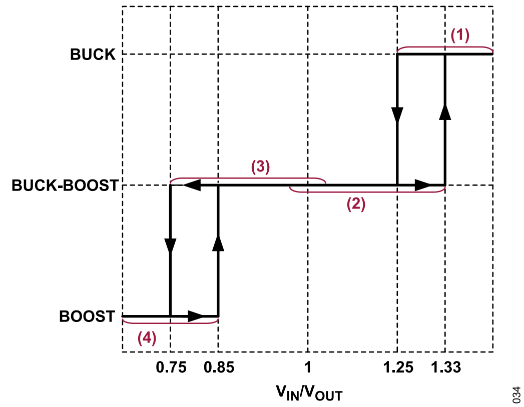


Figure 30. Operation Region vs V_{IN}/V_{OUT} Ratio

(1) Peak-Buck in Buck Region (V_{IN} >> V_{OUT})

When VIN is much higher than VOUT, the LT8350S uses peak-buck current mode control in the buck region (See *Figure 31*). Switch C is always off, and switch D is always on. At the beginning of every cycle, switch A is turned on, and the inductor current ramps up. When the inductor current hits the peak-buck current threshold commanded by VC voltage at buck current comparator A1 during the (A + D) phase, switch A is turned off and switch B is turned on for the rest of the cycle. Switches A and B will alternate, behaving like a typical synchronous buck regulator.

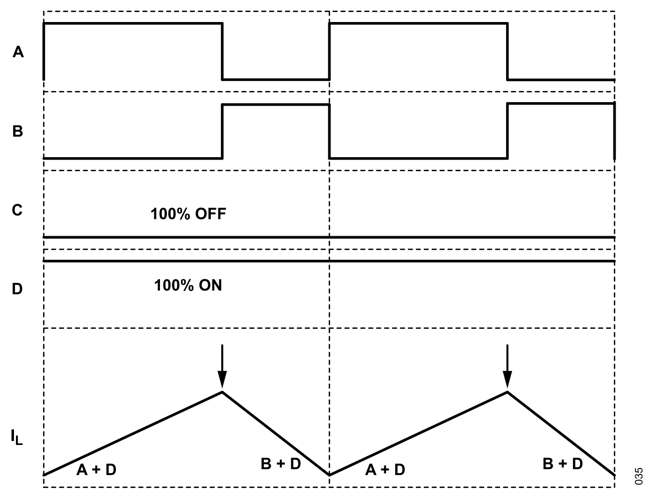


Figure 31. Peak-Buck in Buck Region (VIN>>VOUT)

(2) Peak-Buck in Buck-Boost Region (V_{IN} ~> V_{OUT})

When V_{IN} is slightly higher than V_{OUT}, the LT8350S uses peak-buck current mode control in the buck-boost region (See *Figure 32*). In each switching cycle, switch C is turned on for the beginning 20% of the cycle and switch D is turned on for the remaining 80% of the cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. After a 20% cycle, switch C is turned off, switch D is turned on, and the inductor keeps ramping up. When the inductor current hits the peak buck current threshold commanded by V_C voltage at buck current comparator A1 during the (A + D) phase, switch A is turned off and switch B is turned on for the rest of the cycle.

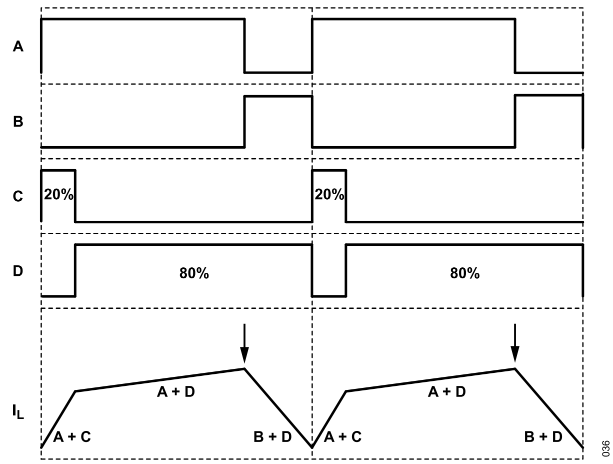


Figure 32. Peak-Buck in Buck-Boost Region (V_{IN}~>V_{OUT})

(3) Peak-Boost in Buck-Boost Region (V_{IN} <~ V_{OUT})

When V_{IN} is slightly lower than V_{OUT}, the LT8350S uses peak-boost current mode control in the buck-boost region (See *Figure 33*). In each switching cycle, switch A is turned on for the beginning 80% of the cycle and switch B is turned on for the remaining 20% of the cycle. At the beginning of every cycle, switches A and C are turned on and the inductor current ramps up. When the inductor current hits the peak-boost current threshold commanded by V_C voltage at boost current comparator A2 during the (A + C) phase, switch C is turned off, and switch D is turned on for the rest of the cycle. After the 80% cycle, switch A is turned off and switch B is turned on for the rest of the cycle.

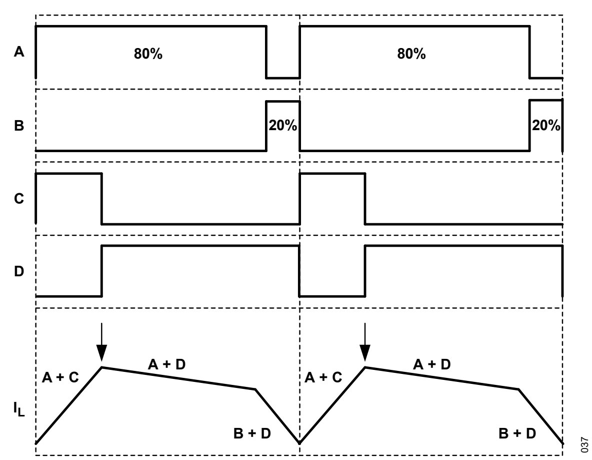


Figure 33. Peak-Boost in Buck-Boost Region (V_{IN}<~V_{OUT})

(4) Peak-Boost in Boost Region (V_{IN} << V_{OUT})

When V_{IN} is much lower than V_{OUT}, the LT8350S uses peak-boost current mode control in the boost region (See *Figure 34*). Switch A is always on, and switch B is always off. At the beginning of every cycle, switch C is turned on, and the inductor current ramps up. When the inductor current hits the peak-boost current threshold commanded by V_C voltage at boost current comparator A2 during the (A + C) phase, switch C is turned off, and switch D is turned on for the rest of the cycle. Switches C and D will alternate, behaving like a typical synchronous boost regulator.

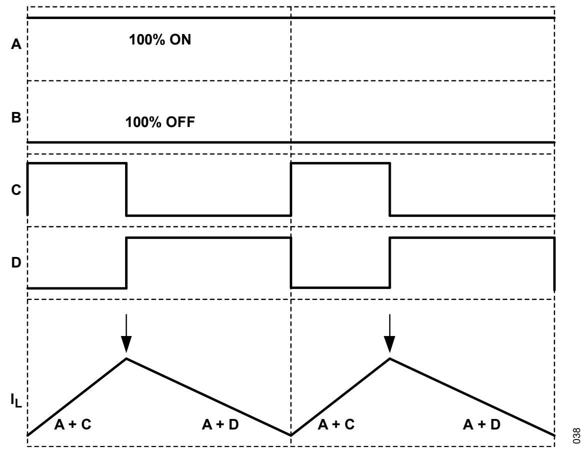


Figure 34.Peak-Boost in Boost Region (V_{IN}<<V_{OUT})

Main Control Loop

The LT8350S is a fixed frequency current mode DC/DC converter. The inductor current is directly sensed across the internal switch A. The current sense voltage is added to a slope compensation ramp signal from the internal oscillator. The summing signal is then fed into the positive terminals of the buck current comparator A1 and boost current comparator A2. The negative terminals of A1 and A2 are controlled by the voltage on the V_C pin, which is the diode-OR of error amplifiers EA1 and EA2.

Depending on the state of the peak-buck peak-boost current mode control, either the buck logic or the boost logic is controlling the four power switches so that either the FB voltage is regulated to 1V or the current sense voltage between the ISP and ISN pins is regulated by the CTRL pin during normal operation. The gains of EA1 and EA2 have been balanced to ensure a smooth transition between constant-voltage and constant-current operation with the same compensation network.

Light Load Current Operation

At light load, the LT8350S can be configured to operate in forced continuous conduction mode or discontinuous conduction mode. The LT8350S runs at their full switching frequency in force continuous conduction mode.

In discontinuous conduction mode, both buck and boost reverse current sense thresholds are set to be positive, thus preventing any reverse current flowing from the output to the input. In the buck region, switch B is turned off whenever the buck reverse current threshold is triggered during the (B + D) phase. In the boost region, switch D is turned off whenever the boost reverse current threshold is triggered during the (A + D) phase. In the buck-boost region, switch D is turned off whenever the boost reverse current threshold is triggered during the (A + D) phase, and both switches B and D are turned off whenever the buck reverse current threshold is triggered during the (B + D) phase. As the load becomes lower and lower, or when a smaller value inductor is used and the inductor current ripple is bigger, the LT8350S may run in pulse-skipping mode, where the switches are held off for multiple cycles (i.e., skipping pulses) to maintain the regulation.

Internal Charge Path

Each of the two high-side gate drivers is biased from its floating bootstrap capacitor C_{BST1} and C_{BST2}, which is usually recharged by $INTV_{CC}$ through the integrated bootstrap diode D1 and D2 when the bottom power switches are turned on. When the LT8350S operates exclusively in the buck or boost regions, one of the top power switches is constantly on. Internal charge paths, from V_{OUT} and BST2 to BST1, or from V_{IN} and BST1 to BST2, charge the bootstrap capacitors to above 3.3V so that the top power switch can be kept on.

Shutdown and Power-On-Reset

The LT8350S enters shutdown mode and drains less than 2µA (typical) quiescent current when the EN/UVLO pin is below its shutdown threshold (0.3V minimum). Once the EN/UVLO pin is above its shutdown threshold (0.9V maximum), the LT8350S wakes up startup circuitry, generates bandgap reference, and powers up the internal $INTV_{CC}$ LDO. The $INTV_{CC}$ LDO supplies the internal control circuitry and gate drivers. Now, LT8350S enters undervoltage lockout (UVLO) mode with a hysteresis current (2.5µA typical) pulled into the EN/UVLO pin. When the $INTV_{CC}$ pin is charged above its rising UVLO threshold (2.52V typical), the EN/UVLO pin passes its rising enable threshold (1.235V typical), and the junction temperature is less than its thermal shutdown (165°C typical), the LT8350S enters enable mode, in which the EN/UVLO hysteresis current is turned off, and V_{REF} is being charged up from ground. From the time of entering enable mode to the time of V_{REF} passing its rising UVLO threshold (1.89V typical), the LT8350S goes through a power-on-reset (POR), waking up the entire internal control circuitry and settling to the right initial conditions. After the POR, the LT8350S is ready and waiting for the signals on the CTRL and LOADEN pins to start switching.

Start-Up and Fault Protection

Figure 35 shows the start-up and fault sequence for the LT8350S. During the POR state, the SS pin is hard pulled down with a 130Ω to ground. In a pre-biased condition, the SS pin must be pulled below 0.2V to enter the INIT state, where the LT8350S waits for 10µs to discharge the SS pin to the ground completely. After the 10µs, the LT8350S enters the UP/PRE state when the LOADON signal goes high. The LOADON high signal happens when the CTRL pin is above its CTRL OFF thresholds (0.225V typical) and the LOADEN is high.

During the UP/PRE state, the SS pin is charged up by a 12.5µA pull-up current while the switching is disabled and the LOADTG is turned off. Once the SS pin is charged above 0.25V, the LT8350S enters the UP/TRY state, where the LOADTG is turned on first while the switching is still disabled. If an excessive current flowing through the current sense resistor triggers the ISP/ISN overcurrent (ISOC) signal, it will reset the LT8350S back into the POR state. After 10µs in the UP/TRY state without triggering the ISOC signal, the LT8350S enters the UP/RUN state.

During the UP/RUN state, the switching is enabled, and the start-up of the output voltage V_{OUT} is controlled by the voltage on the SS pin. When the SS pin voltage is less than 1V, the LT8350S regulates the FB pin voltage to the SS pin voltage instead of the 1V reference. This allows the SS pin to program soft start by connecting an external capacitor from the SS pin to the GND. The internal 12.5µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage V_{OUT} rises smoothly to its final regulation voltage.

Once the SS pin is charged above 1.75V, the LT8350S enters the OK/RUN state, where the output short detection is activated. The output short means that V_{FB} < 0.25V. When the output short happens, the LT8350S enters the FAULT/RUN state, where a 1.25µA pull-down current slowly discharges the SS pin with the other conditions the same as the OK/RUN state. Once the SS pin is discharged below 1.7V, the LT8350S enters the DOWN/STOP state, and the short detection is deactivated with the previous fault latched. Once the SS pin is discharged below 0.2V and the LOADON signal is still high, the LT8350S goes back to the UP/RUN state.

In output short conditions, the LT8350S can be set to hiccup, latch-off, or keep-running fault protection mode with a resistor between the SS and V_{REF} pins. Without any resistor, the LT8350S will hiccup between 0.2V and 1.75V and go around the UP/RUN, OK/RUN, FAULT/RUN, and DOWN/STOP states until the fault condition is cleared. With a 499kΩ resistor, the LT8350S will latch off until the EN/UVLO is toggled. With a 100kΩ resistor, the LT8350S will keep running regardless of the fault.

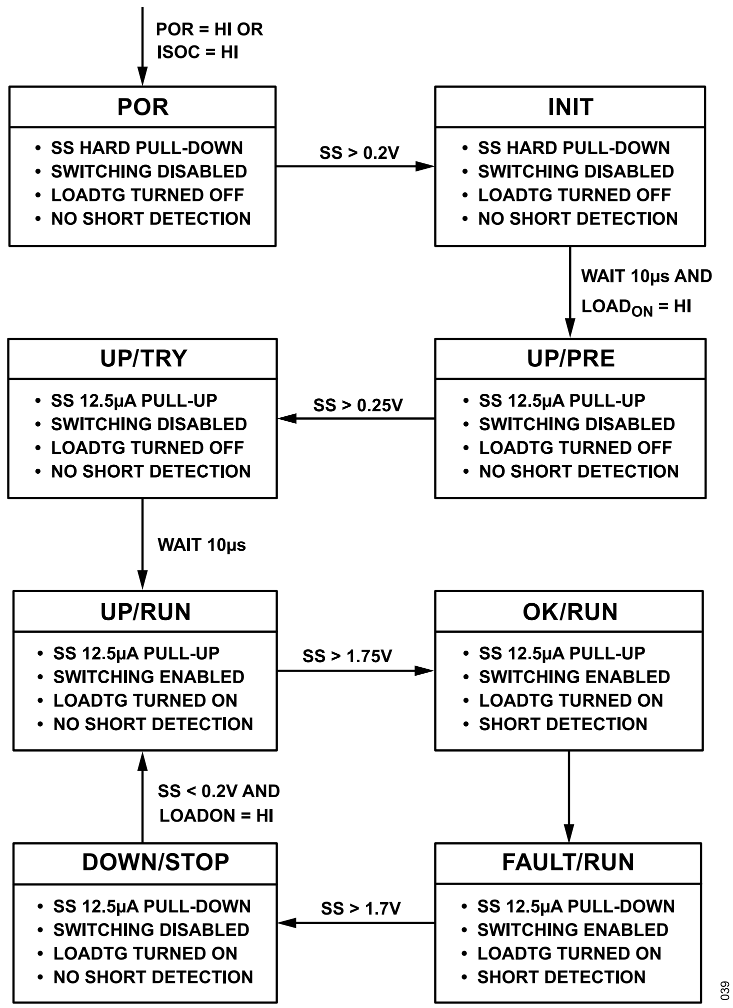


Figure 35. Start-Up and Fault Sequence

APPLICATIONS INFORMATION

This section serves as a guideline for selecting external components for typical applications. See the *Simplified Application Diagram* for more details. Unless otherwise specified, the examples and equations in this section assume continuous conduction mode.

Switching Frequency Selection

The LT8350S uses a constant frequency control scheme between 200kHz and 2MHz. The selection of the switching frequency is a trade-off between efficiency and component size. Low-frequency operation improves efficiency by reducing MOSFET switching losses but requires larger inductor and capacitor values. Consider operating at lower frequencies for high-power applications to minimize MOSFET heating from switching losses. Consider operating at higher frequencies for low-power applications to minimize the total solution size. In addition, the specific application also plays an important role in switching frequency selection. In a noise-sensitive system, the switching frequency is usually selected to keep the switching noise out of a sensitive frequency band.

Switching Frequency Setting

The internal oscillator can set the LT8350S's switching frequency. With the SYNC/MODE pin pulled to ground, a resistor from the RT pin to ground sets the switching frequency. *Table 7* shows R_T resistor values for common switching frequencies.

Table 7. Switching Frequency vs R_T Value (1% Resistor)

F_{OSC} (kHz)	R_T (kΩ)
200	249
400	124
600	78.7
800	56.2
1000	43.2
1200	33.2
1400	26.1
1600	21.5
1800	17.4
2000	14.3

Spread Spectrum Frequency Modulation

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. The LT8350S implements a triangle spread spectrum frequency modulation scheme to improve EMI performance. With the SYNC/MODE pin connected to $INTV_{CC}$, the LT8350S spreads its switching frequency 23% (typical) above the internal oscillator frequency. *Figure 36* and *Figure 37* show the noise spectrum of the typical application (See *Figure 41*) when the part operates at $12V_{OUT}$, 2.5A, and 350kHz with ferrite bead EMI filter and spread spectrum enabled.

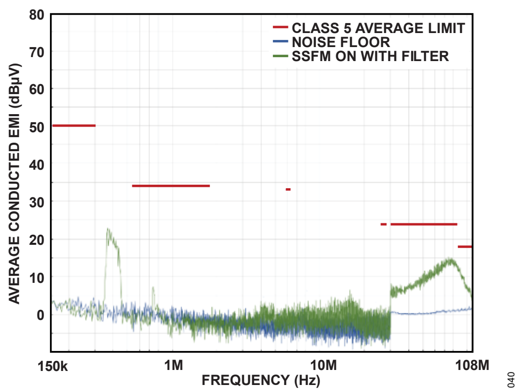


Figure 36. Conducted Average EMI (CISPR25)

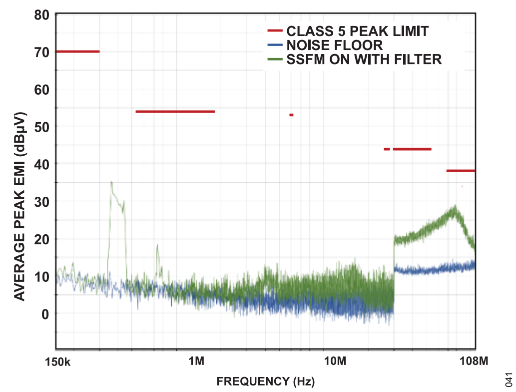


Figure 37. Conducted Peak EMI (CISPR25)

Frequency Synchronization and Operation Mode Selection

The LT8350S switching frequency can be synchronized to an external clock using the SYNC/MODE pin. It is recommended to drive the SYNC/MODE with a 10% to 90% duty cycle waveform. Due to the use of a phase-locked loop (PLL) inside, there is no restriction between the synchronization frequency and the internal oscillator frequency. The rising edge of the synchronization clock represents the beginning of a switching cycle, turning on switches A and C or switches A and D.

SYNC/MODE pin also has four selectable modes for optimization of performance:

1) Connect to $INTV_{CC}$: For spread spectrum frequency modulation and force continuous mode at light load.
2) Connect to V_{REF}: For spread spectrum frequency modulation and pulse-skipping mode at light load.
3) Float: For internal oscillator frequency and force continuous mode at light load.
4) Connect to GND: For internal oscillator frequency and pulse-skipping mode at light load.

Maximum Output Current

The LT8350S is a constant-voltage, constant-current, and buck-boost converter. The output voltage is regulated up to the current limit threshold, which is set by the CTRL pin voltage and the current sense resistor across the ISP/ ISN pins. If the accurate current limit is not required in the application, connect the CTRL pin to V_{REF} and short the ISP and ISN pins to disable this accurate current limit function. See the *Programming Input or Output Current Limit* section for more details. In practice, the maximum output current can be limited by the thermal constraints of the application. *Figure 38* shows the measured output currents over V_{IN} that increase the case temperature by 60°C. The output is regulated at 12V, and the ambient temperature is 25°C. The measurements were done using the LT8350S demo board. See *Figure 38* to estimate how much output current and power the LT8350S can provide under the temperature constraint for a given application.

Another factor that can limit the output current and power from the LT8350S is the maximum switch current limit. The typical maximum switch current limit is 6.8A. When the output current and power increase for a given input voltage, the input current will increase until the peak of the inductor current reaches the maximum switch current limit. If the load demands more current, the output voltage may decrease as the converter will regulate the peak of the inductor current to be less than the maximum switch current limit.

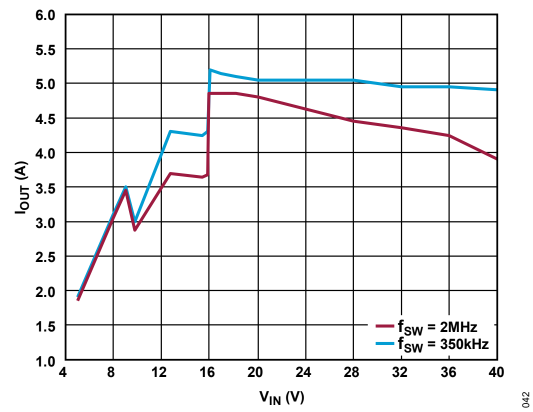


Figure 38. LT8350S Output Currents Resulting 60°C Case Temperature Increase

Inductor Selection

The switching frequency and inductor selection are interrelated in that higher switching frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on the ripple current. The highest current ripple $\Delta I_L\%$ happens in the buck region at $PV_{IN(MAX)}$, and the lowest current ripple $\Delta I_L\%$ happens in the boost region at $V_{IN(MIN)}$. For any given ripple allowance, the minimum inductance can be calculated as:

$$L_{BUCK} > \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{f_{SW} \times I_{OUT(MAX)} \times \Delta I_L\% \times V_{IN(MAX)}} \qquad L_{BOOST} > \frac{V_{IN(MIN)}^2 \times (V_{OUT} - V_{IN(MIN)})}{f_{SW} \times I_{OUT(MAX)} \times \Delta I_L\% \times V_{OUT}^2}$$

where:

f_{SW} is switching frequency

$\Delta I_L\%$ is allowable inductor current ripple

$V_{IN(MIN)}$ is minimum input voltage

$V_{IN(MAX)}$ is maximum input voltage

$I_{OUT(MAX)}$ is maximum output current

Slope compensation provides stability in constant frequency current mode control by preventing subharmonic oscillations at certain duty cycles. The minimum inductance required for stability can be calculated as:

$$L > \frac{V_{OUT}}{2 \times f_{SW} \times I_{SW(MAX)}}$$

where:

f_{SW} is switching frequency

$I_{SW(MAX)}$ is maximum maximum switch current limit = 6.8A (typical)

For high-efficiency, choose an inductor with low core loss, such as ferrite. The inductor should also have low DC resistance to reduce the I^2R losses and must be able to handle the peak inductor current without saturating. Use a shielded inductor to minimize radiated noise.

C_{IN} and C_{OUT} Selection

Input and output capacitance are necessary to suppress voltage ripple caused by discontinuous current moving in and out of the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low equivalent series resistance (ESR). Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP, are also available.

Ceramic capacitors should be placed near the regulator input and output to suppress high-frequency switching spikes. Ceramic capacitors of at least 1µF should also be placed from VIN to GND and VOUT to GND as close to the LT8350 pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce input ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

Input Capacitance (C_{IN})

Discontinuous input current is highest in the buck region due to switch A toggling on and off. Make sure that the C_{IN} capacitor network has low enough ESR and is sized to handle the maximum RMS current. In buck region, the input RMS current is given by:

$$I_{I\_inputRMS} \approx I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

The formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{I\_inputRMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Output Capacitance (C_{OUT})

Discontinuous current shifts from the input to the output in the boost region. Make sure that the C_{OUT} capacitor network can reduce the output voltage ripple. The effects of ESR and bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The maximum steady state ripple due to charging and discharging the bulk capacitance is given by:

$$\Delta V_{CAP(BOOST)} = \frac{I_{OUT} \times (V_{OUT} - V_{IN(MIN)})}{C_{OUT} \times V_{OUT} \times f_{SW}}$$

$$\Delta V_{CAP(BUCK)} = \frac{V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN(MIN)}})}{8 \times L \times f_{SW}^2 \times C_{OUT}}$$

The maximum steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ERS(BOOST)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{V_{IN(MIN)}} \times ESR$$

$$\Delta V_{ERS(BUCK)} = \frac{V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN(MIN)}})}{L \times f_{SW}} \times ESR$$

Programming V_{IN} UVLO

A resistor divider from V_{IN} to the EN/UVLO pin implements V_{IN} undervoltage lockout (UVLO). The EN/UVLO enable falling threshold is set at 1.220V with 15mV hysteresis. In addition, the EN/UVLO pin sinks 2.5µA when the voltage on the pin is below 1.220V. This current provides user-programmable hysteresis based on the value of R1. A resistor divider from V_{IN} to ground can be used to program UVLO. The programmable UVLO thresholds are:

$$V_{IN(UVLO^+)} = 1.235V \times \frac{R1 + R2}{R2} + (2.5\mu A \times R1)$$

$$V_{IN(UVLO^-)} = 1.220V \times \frac{R1 + R2}{R2}$$

Figure 39 shows the implementation of external shutdown control while still using the UVLO function. The NMOS grounds the EN/UVLO pin when turned on and puts the LT8350S in shutdown with a quiescent current of less than 2µA (typical).

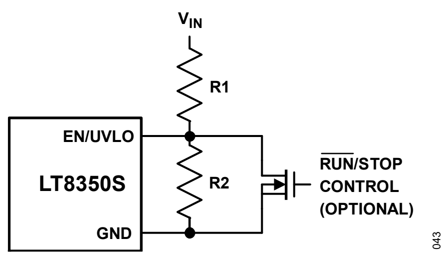


Figure 39. V_{IN} Undervoltage Lockout

Programming Input or Output Current Limit

The input or output current limit is programmed by placing an appropriate value current sense resistor, RIS, in the input or output power path. The voltage drop across RIS is Kelvin sensed by the ISP and ISN pins. The CTRL pin should be connected to a voltage higher than 1.35V to get the full-scale 100mV (typical) threshold across the sense resistor. The CTRL pin can be used to reduce the input or output current to zero, although relative accuracy decreases with the decreasing sense threshold. For 0.25V ≤ VCTRL ≤ 1.15V, the current sense threshold linearly goes up from 0mV to 90mV. For 1.15V ≤ VCTRL ≤ 1.35V, the current sense threshold smoothly transitions from the linear function of VCTRL to the 100mV constant value. When the CTRL pin voltage, VCTRL, is less than 1.15V, the current limit is:

$$I_{IS(MAX)} = \frac{V_{CTRL} - 0.25V}{10 \times R_{IS}}$$

When VCTRL is higher than 1.35V, the current threshold is regulated to:

$$I_{IS(MAX)} = \frac{100mV}{R_{IS}}$$

The CTRL pin should not be left open (tie to VREF if not used). The CTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the output load, or with a resistor divider to VIN to reduce output power and switching current when VIN is low.

The presence of a time varying differential voltage ripple signal across ISP and ISN at the switching frequency is expected. The amplitude of this signal is increased by a higher load current, lower switching frequency, or smaller value output filter capacitor. Some level of ripple signal is acceptable, and the compensation capacitor on the VC pin filters the signal so the average difference between ISP and ISN is regulated to the user-programmed value. The ripple voltage amplitude (peak-to-peak) in excess of 20mV should not cause misoperation but may lead to a noticeable offset between the average value and the user-programmed value.

ISMON Current Monitor

The ISMON pin provides a buffered monitor output of the current flowing through the ISP/ISN current sense resistor, R_{IS}. The ISMON voltage is calculated as:

$$V_{ISMON} = 10 \times V_{(ISP\text{-}ISN)} + 250mV$$

Since the ISMON pin has the same 0.25V offset as the CTRL pin, the primary LT8350S ISMON pin can be directly connected to the secondary LT8350S pin for equal current sharing in parallel applications.

LOAD Switch control

The LOADEN and LOADTG pins provide high-side p-channel metal-oxide semiconductor (PMOS) load switch control. The LOADEN pin accepts a logic level ON/OFF signal and then drives the LOADTG pin to turn on or off the high-side PMOS load switch, thereby connecting or disconnecting the LT8350S power output from the system output. When the LOADEN pin is forced low, the LT8350S turns off power switches, disconnects the V_C pin from all internal loads, and turn off LOADTG. The LOADEN pin should not be open (connect to $INTV_{CC}$ or V_{REF} if not used).

High Side PMOS Load Switch Selection

A high-side PMOS load switch is recommended in some LT8350S applications requiring load switch control. The high-side PMOS load switch is typically selected for drain-source voltage V_{DS}, gate-source threshold voltage $V_{GS(TH)}$, and continuous drain current I_D. For proper operations, V_{DS} rating should exceed the maximum output voltage set by the FB pin, the absolute value of $V_{GS(TH)}$ should be less than 3V, and I_D rating should be above $I_{OUT(MAX)}$.

Programming Output Voltage and Thresholds

The LT8350 has a voltage feedback pin FB that can be used to program a constant-voltage output. The internal error amplifier with its output V_C regulates V_{FB} to 1V through the DC/DC converter.

The output voltage can be set by selecting the values of R3 and R4 (*Figure 40*) according to the following equation:

$$V_{OUT} = 1V \times \frac{R3 + R4}{R4}$$

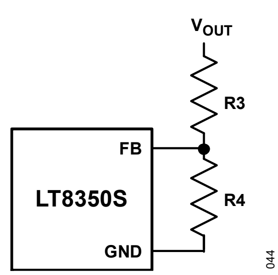


Figure 40. Feedback Resistor Connection

In addition, the FB pin also sets the output overvoltage threshold, output power good thresholds, and output short threshold. For an application with small output capacitors, the output voltage may exhibit considerable overshoots during a load transient event. Once the FB pin hits its overvoltage threshold of 1.1V, the LT8350S stops switching by turning off all four power switches and turns off LOADTG to disconnect the output load for protection.

The output overvoltage threshold can be set as follows:

$$V_{OUT(OVP)} = 1.1V \times \frac{R3 + R4}{R4}$$

To provide the output short-circuit detection and protection, when the FB pin hits $V_{FB} < 0.25V$, the output short threshold can be set as follows:

$$V_{OUT(SHORT)} = 0.25V \times \frac{R3 + R4}{R4}$$

Power Good ($\overline{\text{PGOOD}}$) Pin

The LT8350S provides an open-drain status pin, $\overline{\text{PGOOD}}$, which is pulled low when V_{FB} is within ±10% of the 1V regulation voltage. The $\overline{\text{PGOOD}}$ pin is allowed to be pulled up by an external resistor to $INTV_{CC}$ or an external voltage source of up to 5V.

Soft-Start and Fault Protection

As shown in *Figure 35* and explained in the *Operation* section, the SS pin can be used to program soft-start by connecting an external capacitor from the SS pin to ground. The internal 12.5µA pull-up current charges up the capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises linearly from 0.25V to 1V (and beyond), the output voltage rises smoothly and transitions into its final voltage regulation. The soft-start time can be calculated as:

$$t_{SS} = 1V \times \frac{C_{SS}}{12.5\mu A}$$

Ensure the C_{SS} is at least five to ten times larger than the compensation capacitor on the V_C pin for a well-controlled output voltage soft-start. A 22nF ceramic capacitor is a good starting point.

The SS pin is also used as a fault timer. Once a short-circuit fault is detected, a 1.25µA pull-down current source is activated. Using a single resistor from the SS pin to the V_{REF} pin, the LT8350S can be set to three different fault protection modes: hiccup (no resistor), latch-off (499kΩ), and keep-running (100kΩ).

With a 100kΩ resistor in keep-running mode, the LT8350S continues switching normally and regulates the current into ground. With a 499kΩ resistor in latch-off mode, the LT8350S stops switching until the EN/UVLO pin is pulled low and high to restart. With no resistor in hiccup mode, the LT8350S enters low-duty cycle auto-retry operation. The 1.25µA pull-down current discharges the SS pin to 0.2V, and then the 12.5µA pull-up current charges the SS pin up. If the short-circuit condition has not been removed when the SS pin reaches 1.75V, the 1.25µA pull-down current turns on again, initiating a new hiccup cycle. This will continue until the fault is removed. Once the output short-circuit condition is removed, the output will have a smooth short-circuit recovery due to soft-start.

Loop Compensation

The LT8350S uses an internal transconductance error amplifier, the output of which, V_C, compensates the control loop. The external inductor, output capacitor, and compensation resistor and capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor on the V_C pin are set to optimize control loop response and stability. For a typical application, a 2.2nF compensation capacitor on the V_C pin is adequate, and a series resistor should always be used to increase the slew rate on the V_C pin to maintain tighter output voltage regulation during fast transients on the input supply of the converter.

Efficiency Considerations

The power efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is useful to analyze individual losses to determine what limits the efficiency and which change would produce the most improvement. Although all dissipative elements in circuits produce losses, four main sources account for most of the losses in the LT8350S circuit:

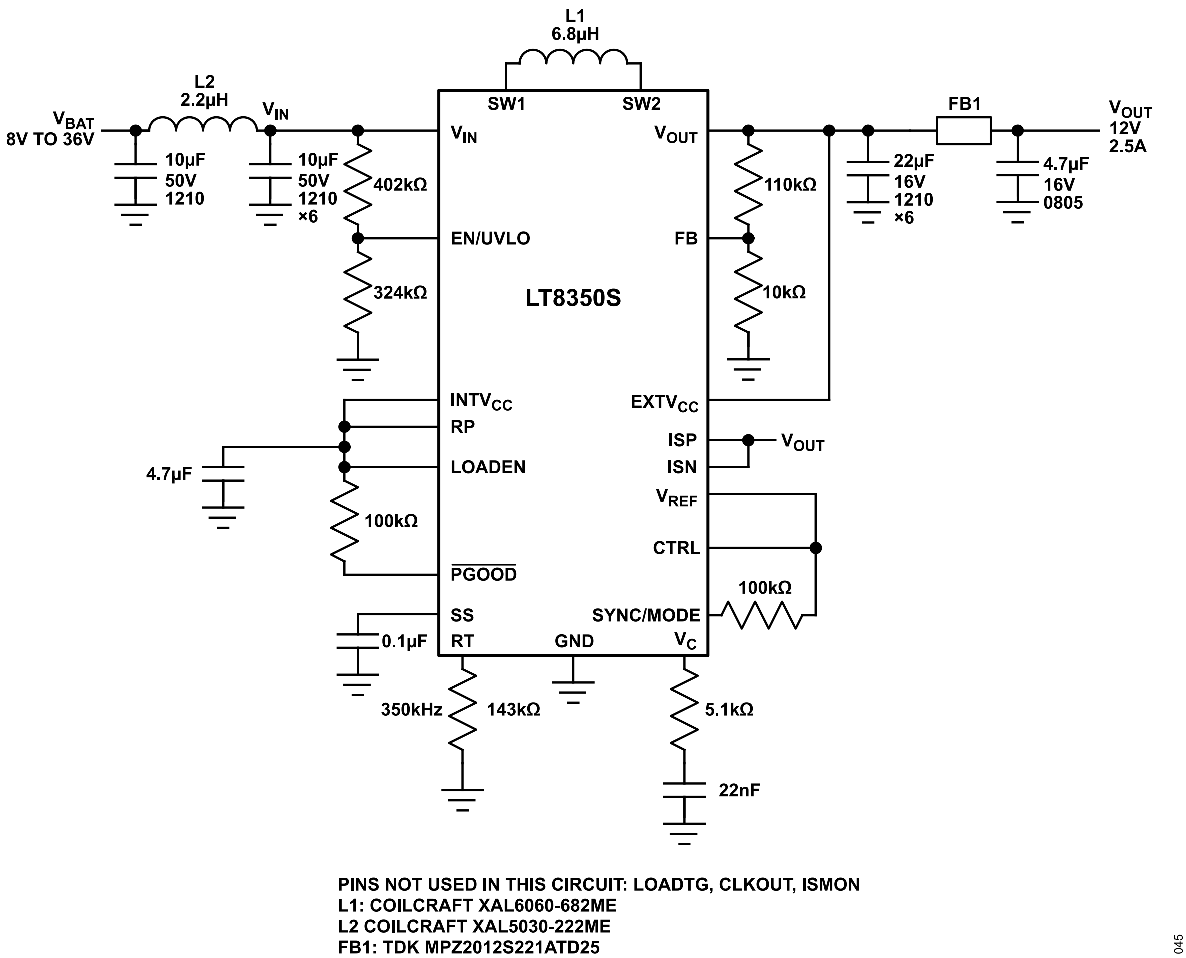
1) DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor, and PC board traces and cause the efficiency to drop at high output currents.

2) Transition loss. This loss arises from the brief amount of time switch A or switch C spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors.

3) $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents.

4) C_{IN} and C_{OUT} loss. The input capacitor has the difficult job of filtering the large Root Mean Square (RMS) input current to the regulator in buck region. The output capacitor has the difficult job of filtering the large RMS output current in boost region. Both C_{IN} and C_{OUT} are required to have low Equivalent series resistance (ESR) to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.

TYPICAL APPLICATION CIRCUITS



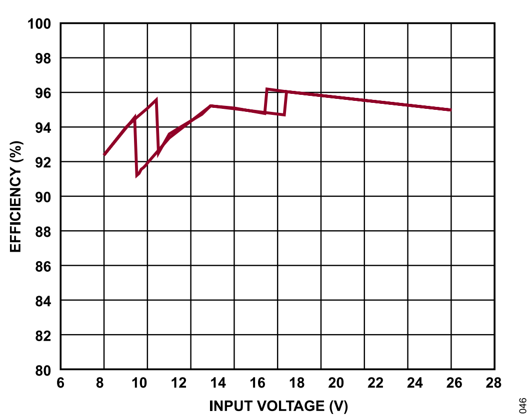


Figure 41. 96% Efficient 30W (12V, 2.5A), 350kHz Buck-Boost Voltage Regulator

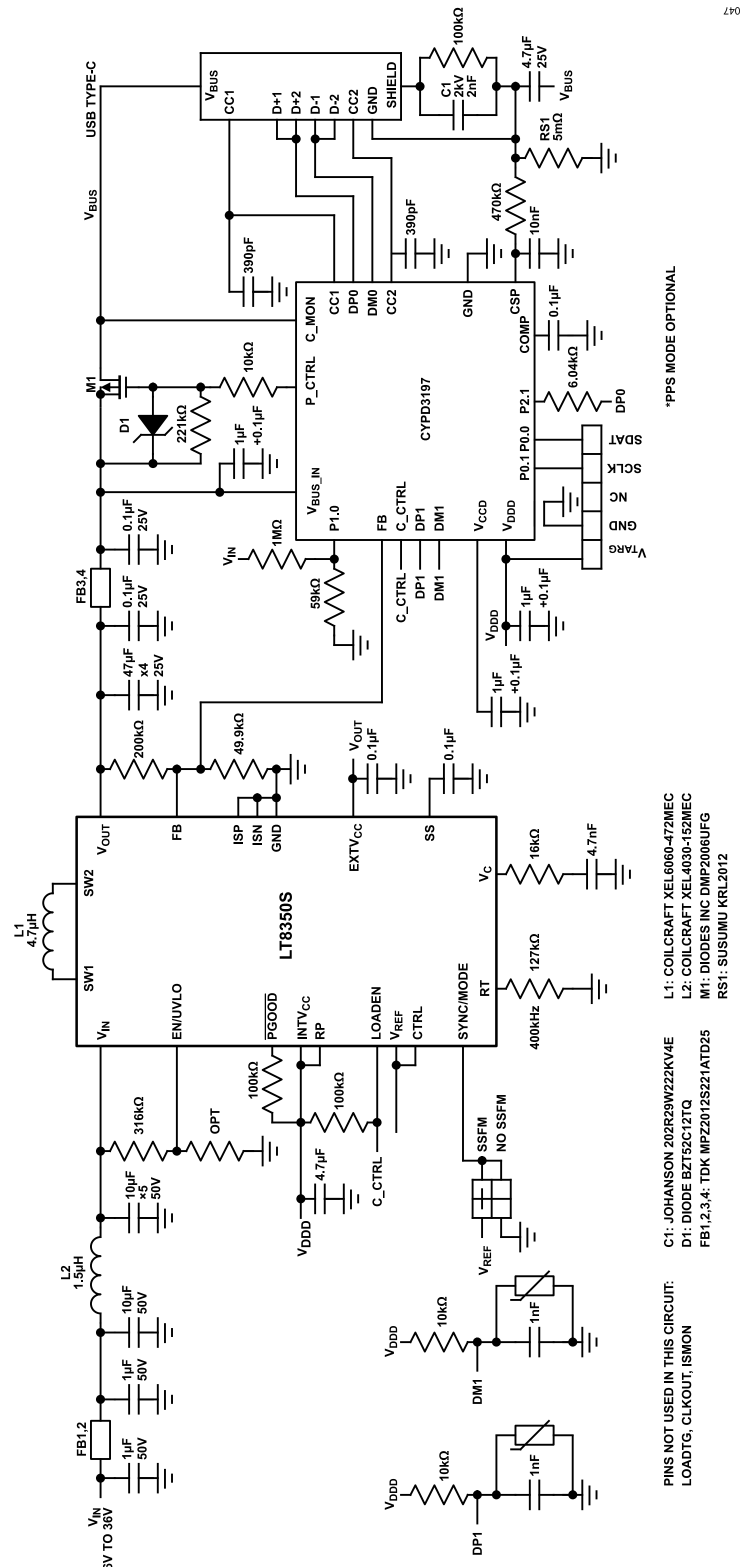


Figure 42. USB-PD Source – 27W 5V, 9V/3A Fixed PDO Mode

ORDERING INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE**	MSL RATING	TEMPERATURE RANGE
		DEVICE	FINISH CODE			
LT8350SAV#PBF	Au (RoHS)	8350S	e4	LQFN (Laminate Package with QFN Footprint)	3	-40°C to 125°C
AUTOMOTIVE PRODUCTS						
LT8350SAV#WPBF	Au (RoHS)	8350S	e4	LQFN (Laminate Package with QFN Footprint)	3	-40°C to 125°C

- **Recommended LGA and BGA PCB Assembly and Manufacturing Procedures**
- **LGA and BGA Package and Tray Drawings**
- *Pad or ball finish code is per IPC/JEDEC J-STD-609. Parts ending with PBF are RoHS and WEEE compliant.
- **The LT8350S package has the same footprint as a standard 4mm x 6mm QFN package and is pin to pin compatible with LT8350.
- ***Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.