



Design-In SSDs

ECC and Spare Blocks help to keep Kingston SSD data protected from errors

End-to-End Data Protection

All Kingston SSDs incorporate End-to-End Data Protection, which protects customer data as soon as it is transferred by the host system to the SSD, and then back from the SSD to the host computer.

Data Transfers within an SSD

All SSDs contain controllers that allow them to communicate with the host system to which they are attached. Data written to or read from the SSD occurs via this SSD controller, regardless of SSD form factor (2.5-inch, Add-In-Card, M.2, etc.) or protocol used (example SATA or NVMe).

There are numerous SSD controller designs currently available. While some SSD controllers incorporate a built-in cache (typically SRAM) as part of the controller design, others may utilize a discrete DRAM chip (or chips), used to temporarily store internal Flash mapping tables and user data being processed. Some controller designs do not use discrete DRAM, but instead use a portion of the NAND Flash as storage for their mapping tables.

SSDs rely on NAND Flash chips for data storage. NAND chips are non-volatile storage devices that store data even after they are powered off. When the SSD controller needs to store or retrieve data, it has to write to or read from the NAND Flash chips.

Error Detection and Correction

SSDs must maintain data integrity as data moves from the host PC to the NAND storage, via the SSD controller. The data transfers from the host to the SSD are often referred to as “data in flight” or “data in transit” before they are actually written to the NAND Flash storage. SSD controllers incorporate Error Correction technology (called ECC for Error Correction Code) to detect and correct the vast majority of errors that can affect data along this trajectory. Flash memory chips incorporate additional error correction information, along with every block of data that is written; this information allows the SSD controller to simultaneously correct many errors when reading a data block. NAND Flash memory, like hard disk drives, will encounter bit errors during normal operation that it will correct on the fly with its ECC data.

In rare cases, data errors in a block being read cannot be corrected; the SSD Controller will recognize this occurrence as an Uncorrectable ECC Error (UECC) and report the error to the host computer. SSDs are designed to be extremely reliable. For Client SSDs,

UECCs are typically rated as one in 10^{15} bits read, and enterprise SSDs are rated as one in 10^{16} bits read. Using the JEDEC JEDS218A and JESD219 UBER requirement for enterprise versus client SSDs, an enterprise class SSD is expected to only experience 1 unrecoverable bit error at a ratio of 1 bit error for every 10 quadrillion bits (~1.11 Petabytes) compared to a client SSD at 1 bit error for every 1 quadrillion bits (~0.11 Petabytes) read.

Kingston SSDs also incorporate Spare Blocks in the NAND Flash devices. These storage areas are usually in the Over-Provisioned (OP) space of a drive, and are not user-accessible. If a NAND device has excessive errors in a data block, then that block will be marked as a Bad Block, retired and one of the spare blocks will be rotated into service. During this process, the data will be corrected if needed using ECC. The use of Spare Blocks extends the useful life and endurance of SSD drives.

