

# TLD4020-3STD\_KIT

## User guide

LITIX™ Interior  
RGB LED driver  
Z8F80405455

## About this document

### Scope and purpose

The TLD4020-3STD\_KIT evaluation platform is designed to facilitate the development and testing of the LITIX™ TLD4020-3ET device, which features three integrated, independent and protected low-side current sinks and an embedded 32-bit Arm® Cortex®-M23 core, particularly suited for controlling RGB LEDs.

It is possible to debug a custom application software running on TLD4020-3ET by connecting a micro-[universal serial bus \(USB\)](#) cable between the PC and the TLD4020-3STD\_EVAL board or by using an external debugger probe such as a SEGGER J-link BASE.

The scope of this user guide is to provide instructions on the use of the TLD4020-3ET evaluation kit.

**Note:** *PCBs and schematics are NOT optimized for final customer design.*

### Intended audience

Hardware engineers, software engineers

## Important notice

**“Evaluation Boards and Reference Boards” shall mean products embedded on a printed circuit board (PCB) for demonstration and/or evaluation purposes, which include, without limitation, demonstration, reference and evaluation boards, kits and design (collectively referred to as “Reference Board”).**

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## Safety precautions

### Safety precautions

**Note:** Please note the following warnings regarding the hazards associated with development systems.

**Table 1** Safety precautions

	<b>Warning:</b> The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.
	<b>Warning:</b> Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.
	<b>Caution:</b> Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.
	<b>Caution:</b> The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.
	<b>Caution:</b> A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.
	<b>Caution:</b> The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.

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## 1 Evaluation kit composition

### 1 Evaluation kit composition

The TLD4020-3STD\_KIT is composed by a main board TLD4020-3STD\_EVAL and a daughter board TLD4020-3DB. It is important to note that the factory assembly of TLD4020-3STD\_EVAL does not include the LITIX™ TLD4020-3ET device.

Therefore, in order to start the evaluation activities, the component needs to be manually soldered on the main board, or quickly added through the usage of the TLD4020-3DB companion board.

A complete description of the boards functionalities are reported in the following chapters.

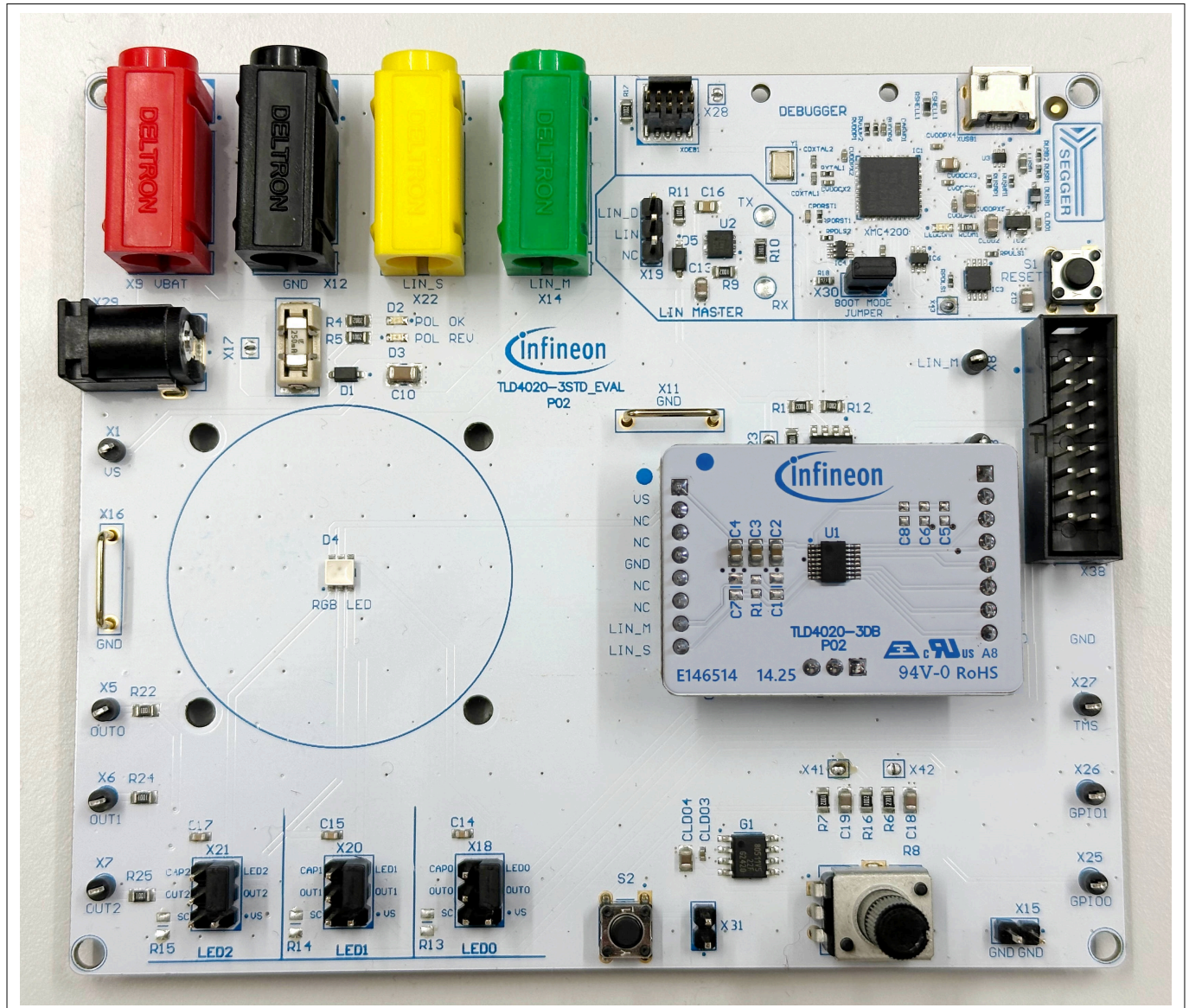


Figure 1 TLD4020-3STD\_KIT - Top side view



## 2 TLD4020-3STD\_EVAL – main board

## 2 TLD4020-3STD\_EVAL – main board

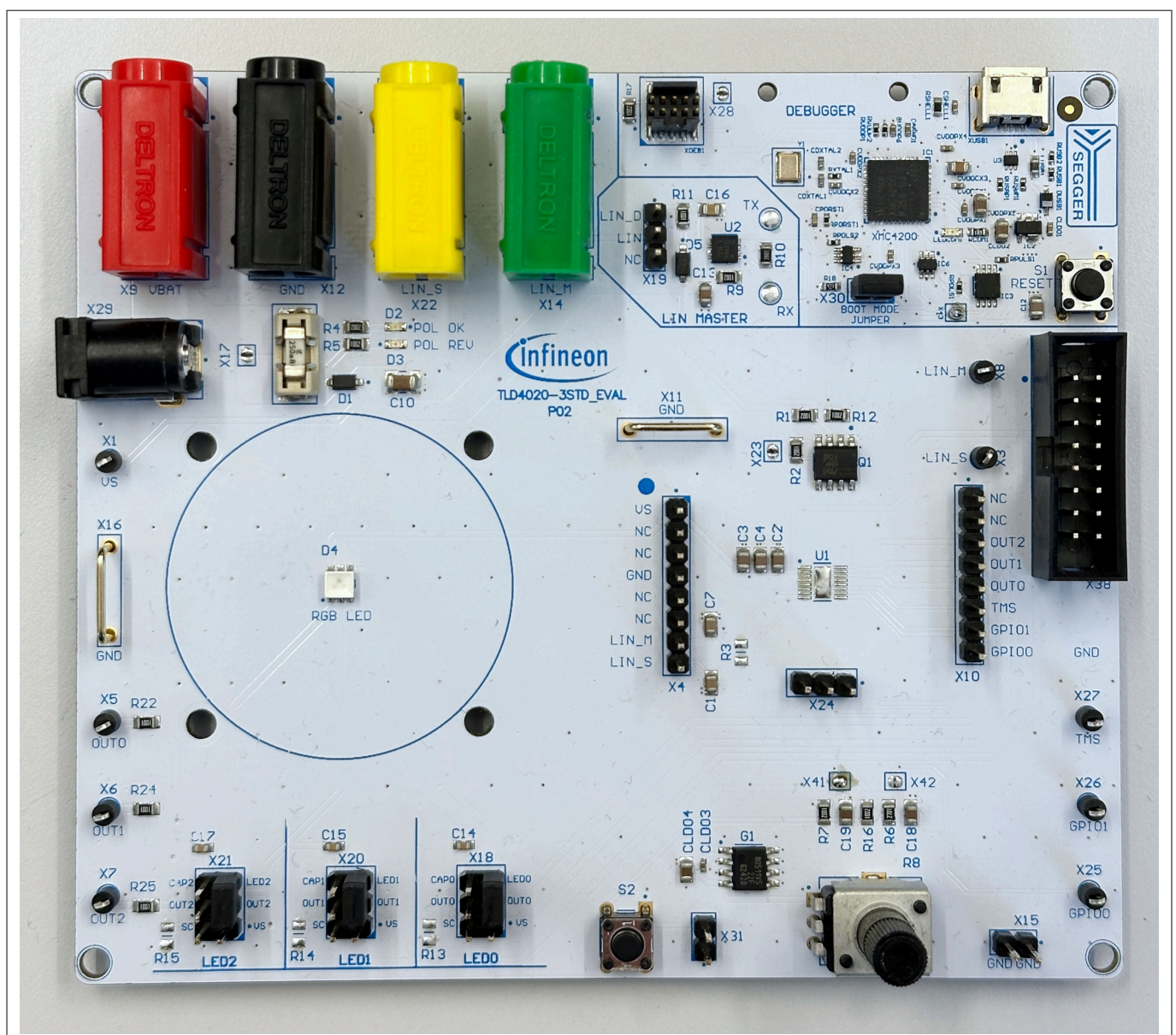
### 2.1 The board at a glance

The TLD4020-3STD\_EVAL provides a complete set of functionalities to enable the user to evaluate the TLD4020-3ET device.

The board can be supplied from the banana type red/black connectors (X9/X12) or by using the jack connector (X29). The recommended supply voltage range is 7 V to 29 V (see [Chapter 2.3](#)).

An integrated reverse polarity protection is present on the board to avoid any component damage in case of incorrect supply connections. In addition, an input supply fuse is present for overcurrent protection.

The load is composed by one RGB *light-emitting diode (LED)*.



**Figure 2** TLD4020-3STD\_EVAL - Top side view

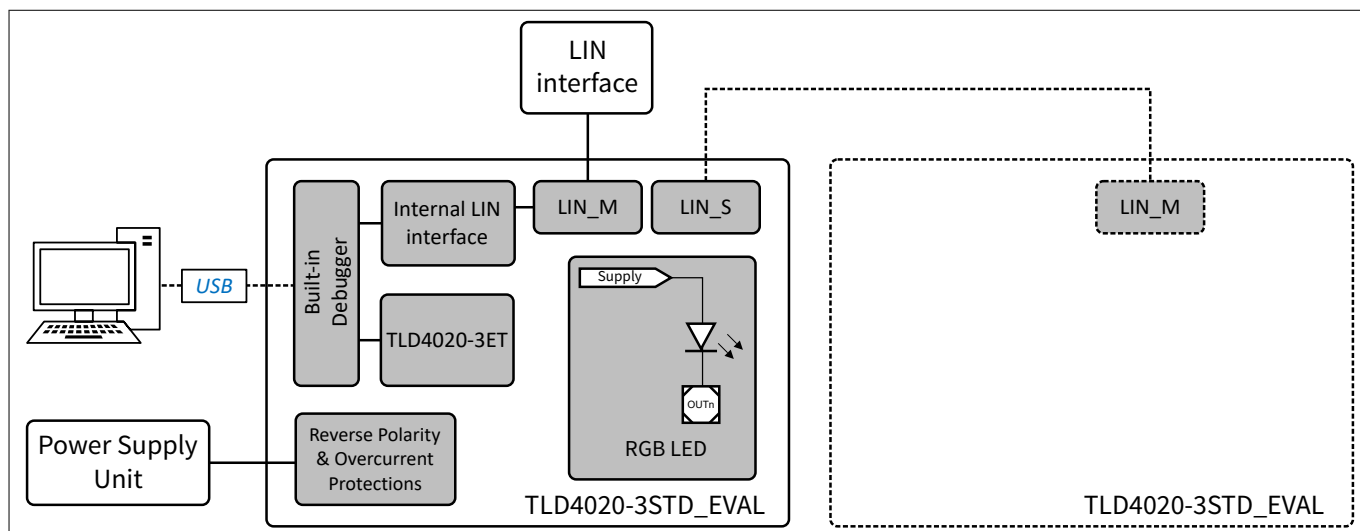
The board features a built-in XMC™ Link debugger, and can be connected to a PC through a micro-[USB cable](#)<sup>1)</sup>.

<sup>1</sup> At first power up of the TLD4020-3STD\_EVAL it is recommended to update the firmware of the SEGGER J-Link on-board debugger

## 2 TLD4020-3STD\_EVAL – main board

The additional banana type yellow/green connectors (X22/X14) make it possible to concatenate multiple boards in "bus mode". This is useful, for example, in case the user wants to evaluate the behavior of multiple devices connected within the same [local interconnect network \(LIN\)](#) network, or to test animations effects and light patterns scenarios.

The system block diagram for "bus mode" operation is reported in [Figure 3](#).



**Figure 3** TLD4020-3STD\_EVAL - Bus mode operation

## 2.2 Main features

- Built-in XMC™ Link debugger<sup>2)</sup>
- Pin stripes for TLD4020-3DB daughter board connection
- On-board [LIN bootstrap loader \(BSL\)](#) connector for uIO stick v2
- General purpose input/output (GPIO) interfaces
- Reverse polarity and overcurrent protected input
- Test points for main signals probing

## 2.3 Board parameters

**Table 2** TLD4020-3STD\_EVAL – board parameters

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input voltage	$V_{IN}$	7	12	29	V	Maintain $V_{IN}$ as low as possible to limit the power dissipation on the LED driver
Input current	$I_{IN}$	5	–	160	mA	$V_{IN} = 13.5\text{ V}$
LIN baud rate	$LIN_{BRATE}$	2.4	–	115.2	kbit/s	Standard LIN limited to 20 kbit/s, higher speed for <a href="#">BSL</a>
Ambient Temperature	$T_{AMB}$	-20	25	85	°C	–

<sup>2)</sup> Based on SEGGER J-Link debugger [\[6\]](#)

## 2 TLD4020-3STD\_EVAL – main board

## 2.4 Output stage configuration

The output stage is equipped with three integrated low-side current sink channels, with output currents ranging from 0 mA to 51.5 mA.

The pin headers offer multiple connection options, allowing the user to customize and test different output configurations. It is for example possible to short the output stages to VS, or to add a 10nF capacitor in parallel with the LEDs. Output stage configuration options are reported in the schematic of [Figure 4](#).

In order to connect the RGB LED to the output stages of the TLD4020-3ET device, the pin headers need to be configured as in [Figure 5](#), by shorting the OUTn pin with the correspondent LEDn pin.

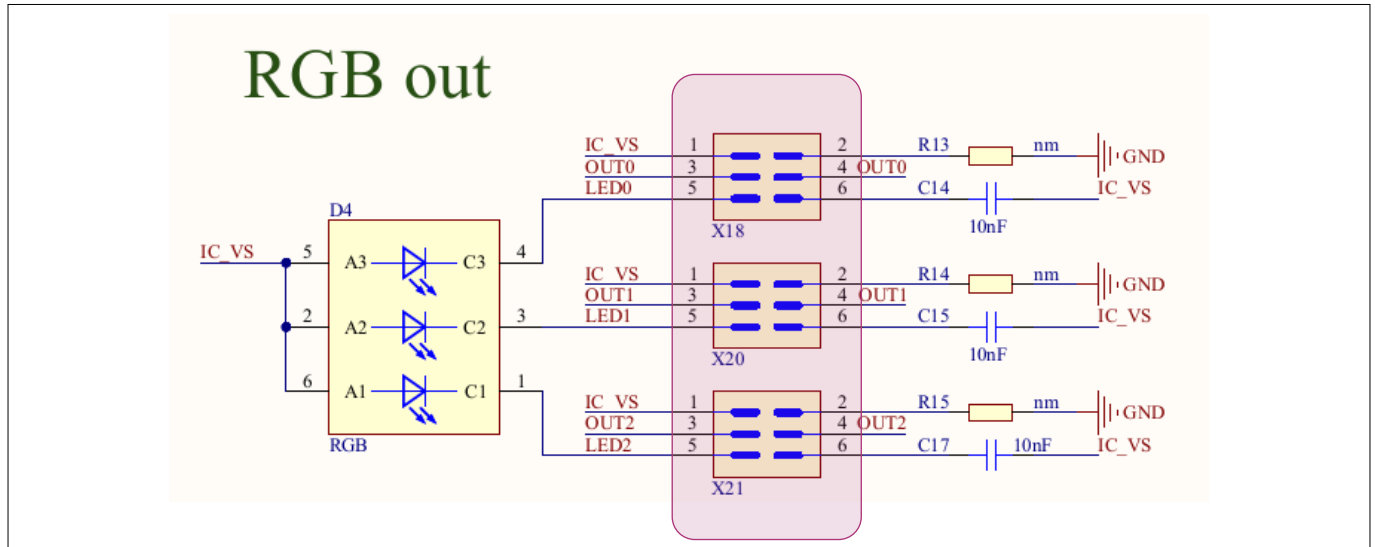


Figure 4 Output stage configuration - schematic

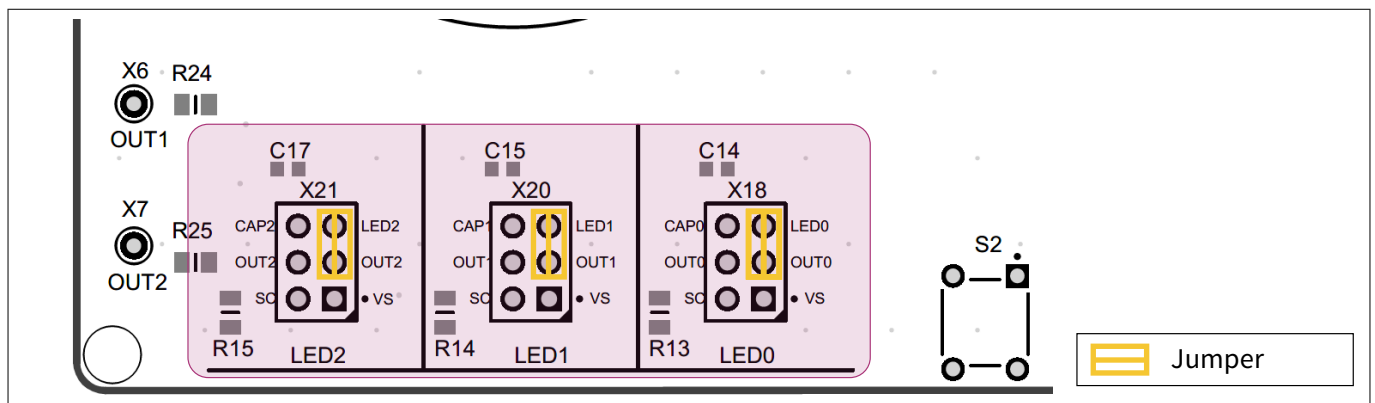


Figure 5 Output stage configuration - OUTn connected to LEDn



## 2 TLD4020-3STD\_EVAL – main board

### 2.5 Operation modes

The device features two different operation modes:

- Debug mode
- User mode

#### Debug mode

In this operation mode debug is enabled and the device can be accessed by *serial wire debug (SWD)*. The SWD functions (SWDIO and SWDCLK) are assigned to the following pins:

**Table 3** Debug Pins

Pin	Functions
TMS	SWDIO
GPIO1	SWDCLK

The entry and exit of the debug mode is controlled by the *boot code in ROM (bootROM)* firmware which is reading the TMS and SWDCLK pins during the boot-up after a cold or warm reset. Therefore, to switch between the user and the debug mode, a device reset in conjunction with controlling the pins is needed.

To enter the debug mode, TMS and SWDCLK both need to be driven "high" externally after device reset. If this condition occurs, the bootROM firmware proceeds with the device start-up in debug mode instead of user mode.

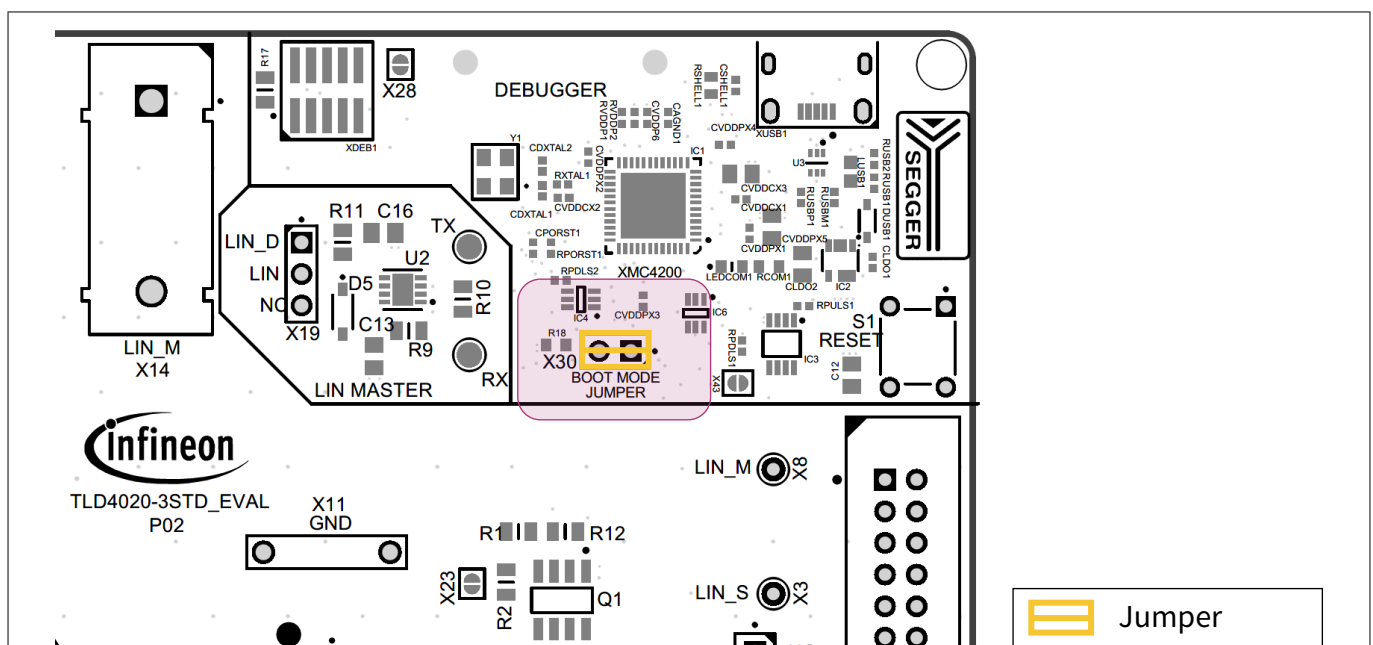
An "high" level on the TMS pin is recognized by the device when the jumper X30 is left open during start-up. By doing this, the pin will be pulled "high" via a high-ohmic pull-up resistor (R17).

Logic level changes of the SWDCLK pin and device resets are handled by the debugger when entering debug mode.

For a detailed description of the *Debug system* refer to the device *User manual* [2].

#### User mode

While operating in user mode, connection to the debugger is not possible. This mode is the standard operation mode and occurs when TMS pin is kept "low" during device start-up. In order to do so, it is sufficient to set the jumper X30. A current limiting resistor (R18) is present on the board for short circuit protection.



**Figure 6** Operation mode setting

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## 2 TLD4020-3STD\_EVAL – main board

The bootup flow of the device is summarized in the following table:

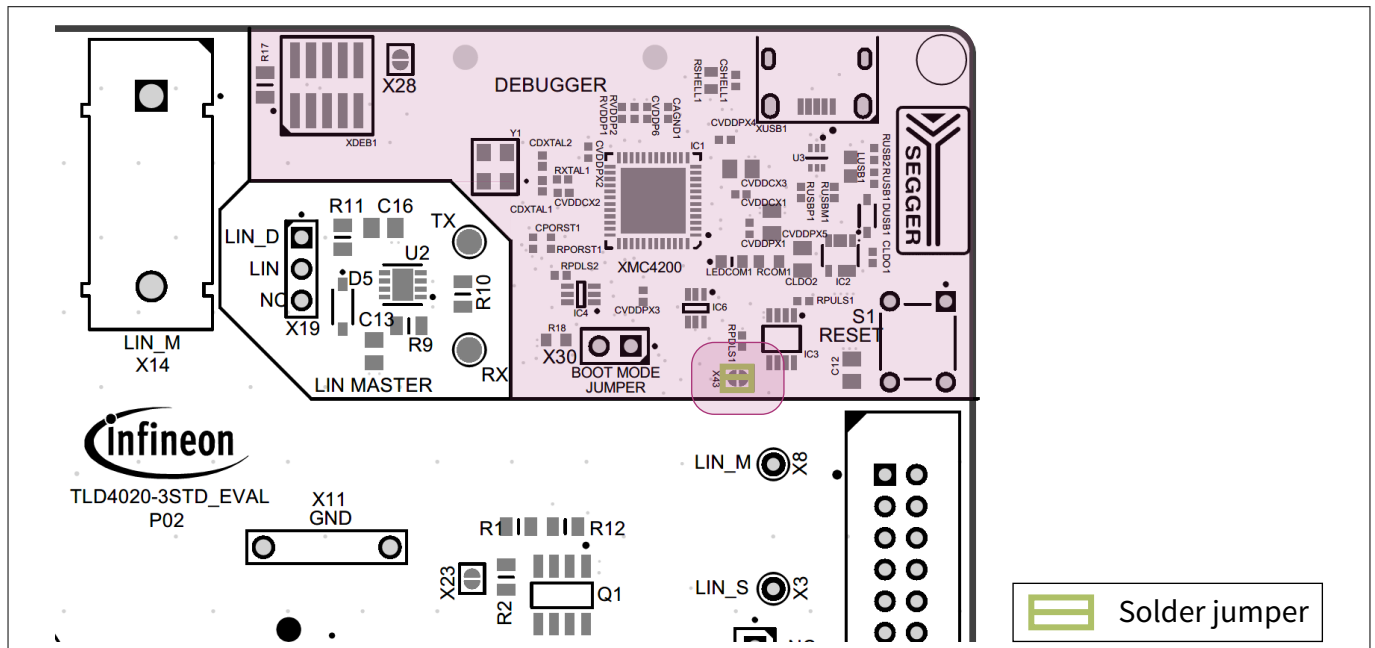
**Table 4**                      **Bootup flow**

Mode	TMS	GPIO1	Note
User	Low	x	X30 in place
Debug	High	High	X30 open

## 2 TLD4020-3STD\_EVAL – main board

### 2.5.1 Debugger connection

The on-board debugger circuitry of the TLD4020-3STD\_EVAL is shown in the figure below.



**Figure 7** TLD4020-3STD\_EVAL - Debugger section

The debugger is an indispensable tool not only for programming the TLD4020-3ET, but also for debugging and verifying the application's functionality in real-time. To utilize the debugger and develop firmware for the TLD4020-3ET, download the PC installation of Keil  $\mu$ Vision<sup>3)</sup> or IAR Embedded Workbench<sup>4)</sup> and the dedicated software driver for the debugger<sup>5)</sup>.

**Note:** A complete development toolchain installation guideline for Keil  $\mu$ Vision or IAR Embedded Workbench is provided within the Application Note **TLD40xx toolchain and evaluation board getting started**.

Connecting the board to a PC via a micro-**USB** cable allows the user to leverage the built-in debugger circuitry. Alternatively, it is possible to connect a SEGGER J-Link BASE debugger (or other compatible debuggers) directly to the 10-pin connector XDEB1, located in the debugger section (see [Figure 7](#)). When using this method, it is crucial to ensure the correct polarity of the mounted connector, as indicated by the dot marking pin 1<sup>6)</sup>.

Additionally, the S1 button provides a convenient reset function. By pressing S1, the power supply to the TLD4020-3ET is temporarily removed, allowing for a device reset.

**Attention:** It needs to be ensured that solder jumper X43 is closed for a proper connection of the on-board debugger.

**Note:** In case of connection issues with the debugger, trimmer R8 shall be rotated all the way in clockwise direction in addition to the jumper X30 being left open.

<sup>3</sup> Keil  $\mu$ Vision download [\[8\]](#)

<sup>4</sup> IAR Embedded Workbench download [\[9\]](#)

<sup>5</sup> SEGGER J-Link drivers download [\[6\]](#); J-Link version 7.96a or newer is required

<sup>6</sup> A suitable connector for Segger J-Link debuggers is the **9-Pin Cortex-M Adapter** [\[7\]](#)

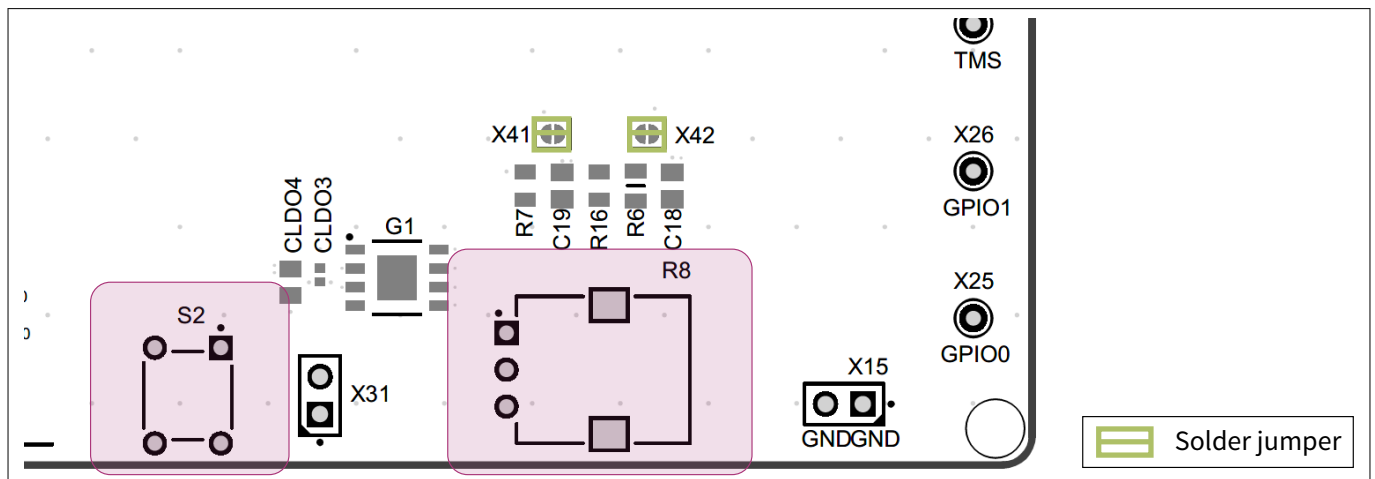
## 2 TLD4020-3STD\_EVAL – main board

### 2.6 Interfaces

#### 2.6.1 GPIOs interfaces

The TLD4020-3ET device features two *general purpose input output (GPIO)* pins that can be configured and tested to evaluate various application use cases.

To facilitate this, a trimmer (R8) and a push button (S2) are conveniently located on the board, with the trimmer connected to GPIO0 and the push button connected to GPIO1. These components can be easily accessed and utilized by connecting the X42 and X41 solder jumpers, respectively.



**Figure 8** TLD4020-3STD\_EVAL - GPIOs interfaces

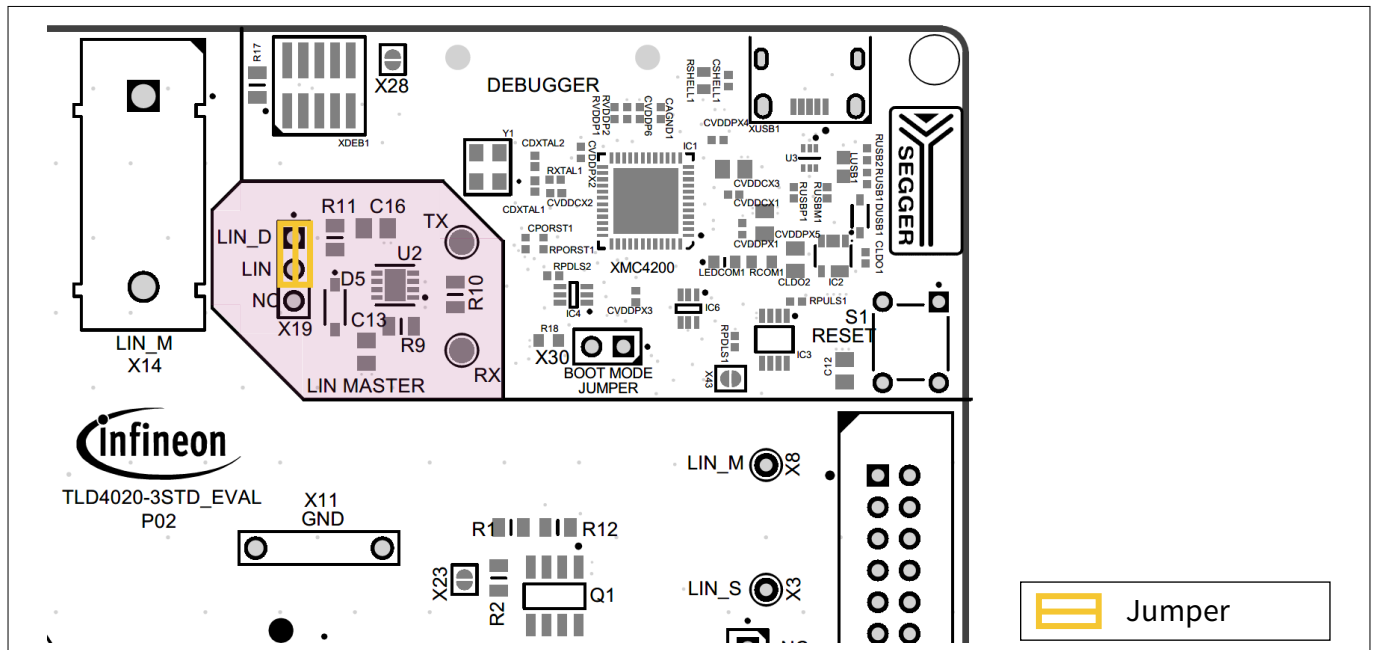


## 2 TLD4020-3STD\_EVAL – main board

### 2.6.2 LIN master transceiver interface

The TLD4020-3STD\_EVAL is equipped with an integrated [LIN](#) master transceiver, providing a convenient interface to the LIN bus. To connect the LIN master to the device's LIN bus, use the X19 connector.

When the micro-[USB](#) cable is connected to a PC, a virtual serial port is established, enabling the user to transmit and receive data over the LIN bus. Furthermore, the LIN master and debugger functions can be utilized simultaneously via the USB connection, allowing for seamless testing and debugging of the device.



**Figure 9** TLD4020-3STD\_EVAL - LIN master section

## 2 TLD4020-3STD\_EVAL – main board

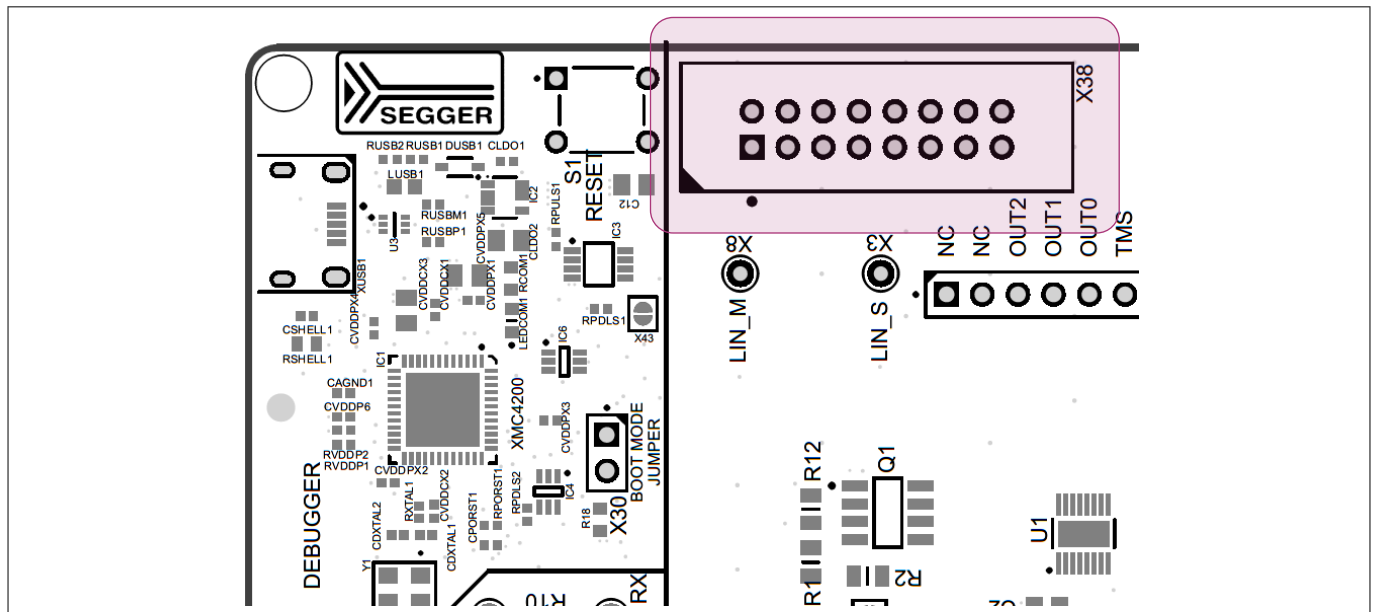
### 2.6.3 Bootstrap loader interface

The TLD4020-3STD\_EVAL makes it possible to control the firmware of the TLD4020-3ET device through the user interface *Infineon BSL programming tool for MCUs*<sup>7)</sup>.

A dedicated connector X38<sup>8)</sup> is present to allow the connection to an external *Infineon uIO Stick v2*<sup>9)</sup>, which acts as hardware support to establish a UART-over-LIN communication to the device and to enable the *BSL* features.

**Attention:** *The external power supply unit must be disconnected when using the bootstrap loader interface. Supply voltages are provided by the Infineon uIO Stick v2 device.*

For a complete description of the BSL protocol functionality refer to the device *User manual* [2] and *Firmware user manual* [3].



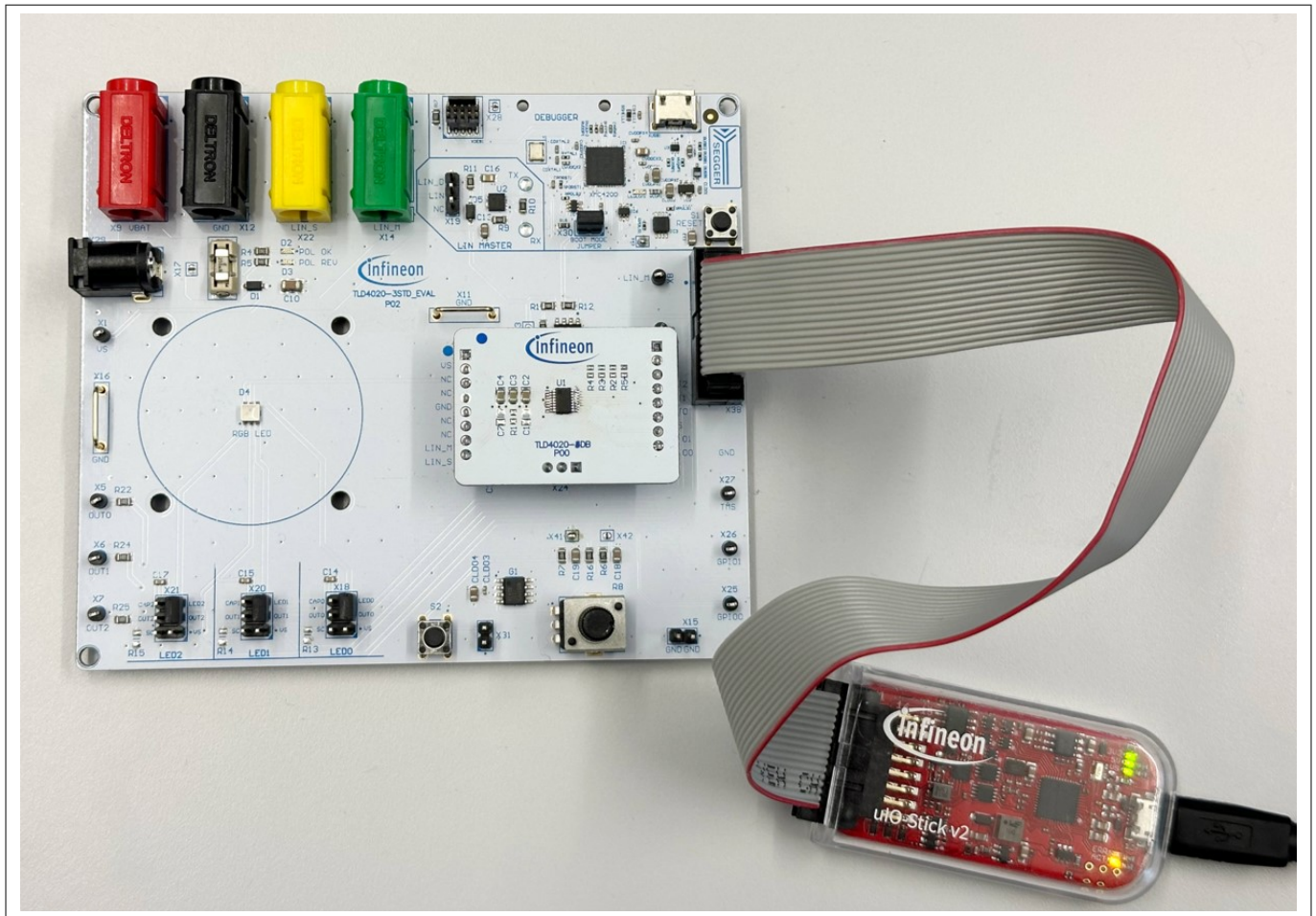
**Figure 10** TLD4020-3STD\_EVAL - BSL connector X38

<sup>7)</sup> *Infineon BSL programming tool for MCUs* can be downloaded from the Infineon Developer Center IDC [5]

<sup>8)</sup> Connector available only from P02 board layout revision onwards

<sup>9)</sup> For information on the Infineon uIO Stick v2 refer to [4]

## 2 TLD4020-3STD\_EVAL – main board



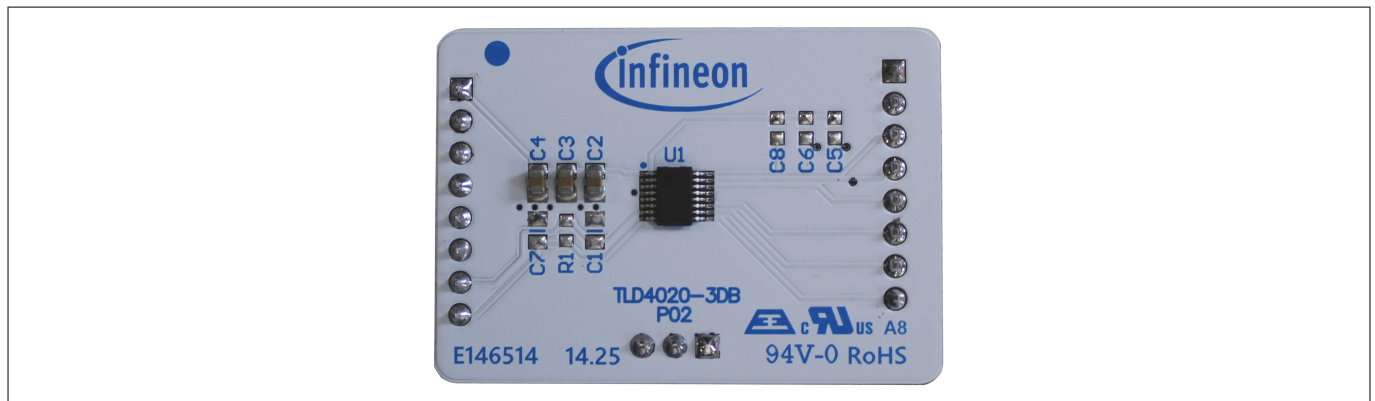
**Figure 11**      **TLD4020-3STD\_KIT - Bootstrap loader interface**

### 3 TLD4020-3DB – daughter board

## 3 TLD4020-3DB – daughter board

### 3.1 The board at a glance

To facilitate the programming of multiple devices or to replace a device, a daughter board TLD4020-3DB can be attached to the main board TLD4020-3STD\_EVAL.

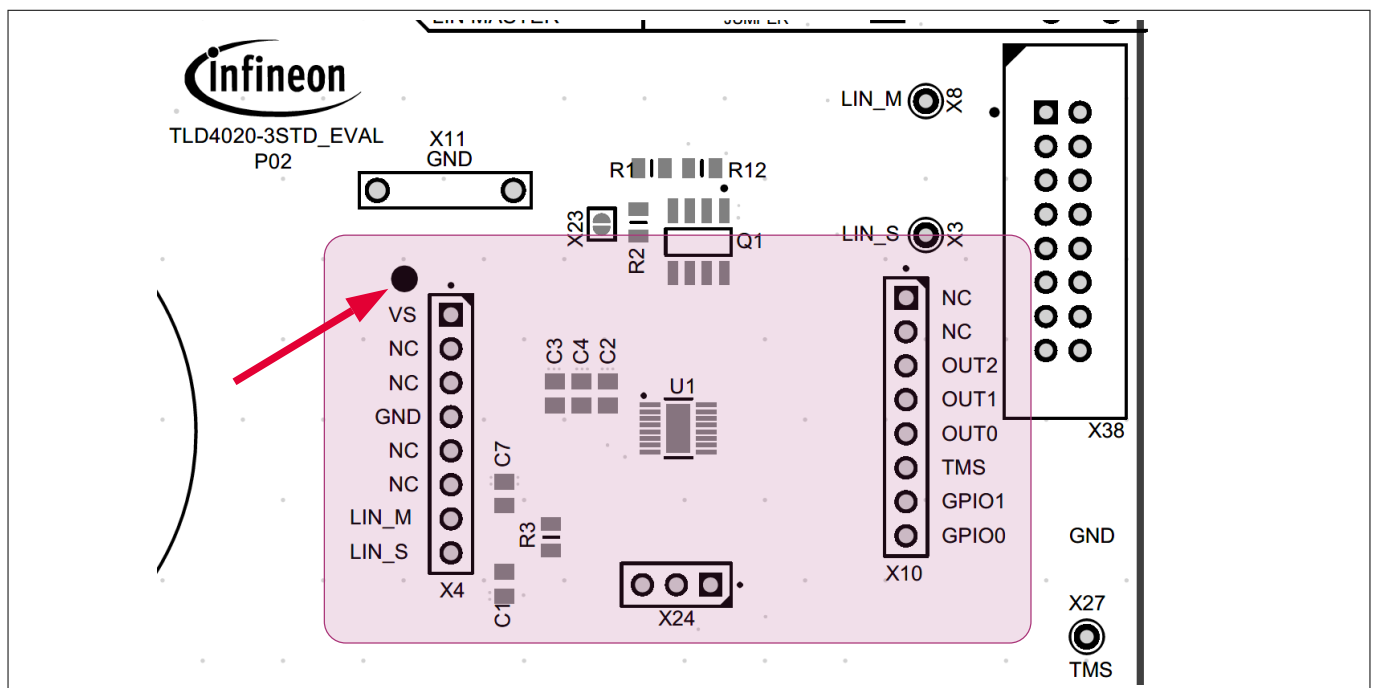


**Figure 12** TLD4020-3DB - Top side view

Before connecting the daughter board, the U1 device needs to be removed from the main board, if it is present. This involves desoldering the U1 chip from its current position.

Once the U1 chip has been removed, the daughter board can be connected to the main board using the pin strips X4, X10, and X24.

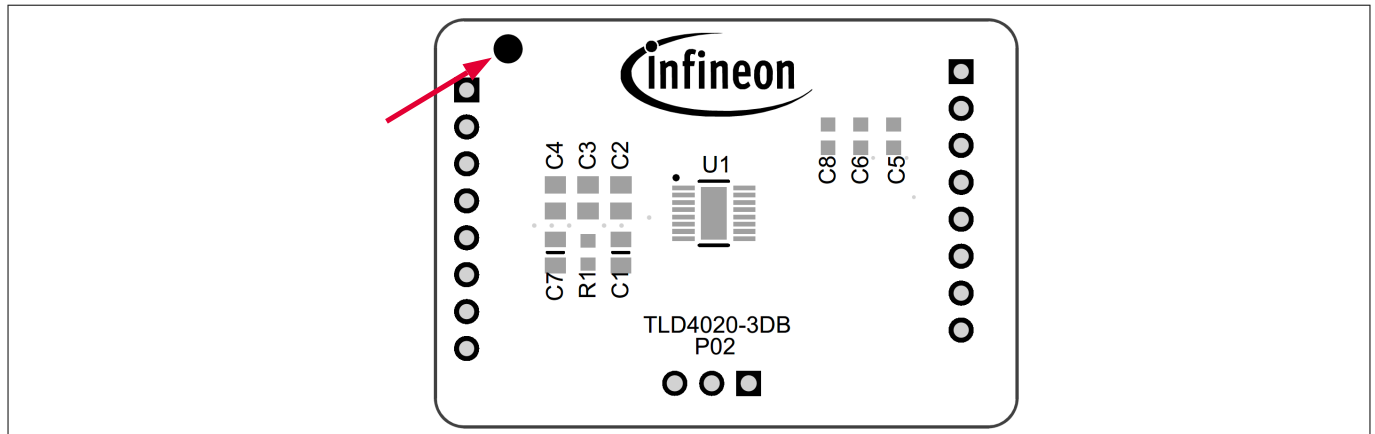
It is essential to ensure proper alignment and polarity between the two boards to prevent malfunctions. To achieve this, the dots present on both boards (indicated by the red arrows in the figures below) must be positioned with the same orientation. This important step ensures a secure and functional connection between the main board and the daughter board.



**Figure 13** TLD4020-3STD\_EVAL - Orientation dot



### 3 TLD4020-3DB – daughter board



**Figure 14** TLD4020-3DB - Orientation dot

## 3.2 Main features

- Pre-assembled LITIX™ TLD4020-3ET device

## 4 System design

# 4 System design

## 4.1 TLD4020-3STD\_EVAL

### 4.1.1 Bill of material

Ref Designator	Value	Manufacturer	Manufacturer P/N	Not Fitted item
C1, C7	100pF	MuRata	GCM2165G2A101JA16	
C2, C3, C4, C12, C13, C18, C19	100nF	AVX	08051C104JAT2A	
C10	10uF	Samsung	CL32B106KBJNNWE	
C14, C15, C17	10nF	Kemet	C0603C103J3GAC	
C16	1nF	TDK Corporation	CGA4F2X7R2A102M085AE	
CAGND1, CLDO1, CLDO3, CSHELL1, CVDDCX1, CVDDCX2, CVDDP6, CVDDPX1, CVDDPX2, CVDDPX3, CVDDPX4	100nF	TDK Corporation	CGA2B3X7R1H104K050BB	
CDXTAL1, CDXTAL2	12pF	MuRata	GCM1555C1H120JA16	
CLDO2, CLDO4, CVDDPX5	10uF	MuRata	GCM21BR71A106KE22	
CPORST1	10nF	TDK Corporation	CGA2B3X7R1H103K050BB	
CVDDCX3	4.7uF	MuRata	GCM21BR71C475KA73	
D1, D5	1N5819HW-7-F	Diodes Incorporated	1N5819HW-7-F	
D2	Green LED	Vishay	TLMP1100-GS08	
D3, LEDCOM1	Red LED	Vishay	TLMS1100-GS08, TLMS1000-GS08	
D4	RGB LED	NICHIA CORPORATION	NSSM313AT	
DUSB1	BAT60A	Infineon Technologies	BAT60A	
G1	TLF80511EJ V50	Infineon Technologies	TLF80511EJ V50	
IC1	IFX_XMC4200Q48K256AB XUMA1	Infineon Technologies	XMC4200Q48K256AB XUMA1	
IC2	TLS202B1MBV33	Infineon Technologies	TLS202B1MBV33	
IC3	SN74LVC2T45DCTT	Texas Instruments	SN74LVC2T45DCTT	

#### 4 System design

Ref Designator	Value	Manufacturer	Manufacturer P/N	Not Fitted item
IC4, IC6	SN74LVC1T45DCKR	Texas Instruments	SN74LVC1T45DCKR	
LUSB1	60R	MuRata	BLM18PG600SN1D	
Q1	AUIRF7343Q	Infineon Technologies	AUIRF7343Q	
R1, R2, R5, R9, R12, R17	10k	Vishay	CRCW080510K0FK	
R3, R13, R14, R15	–	–	–	Not Fitted
R4	20k	Vishay	CRCW080520K0FK	
R6	2.7k	Vishay	CRCW08052K70FK	
R7, R16	10k	Yageo	RC0805FR-0710KL	
R8	10k	Bourns	PTV09A-4020U-B103	
R10	3.9k	Vishay	CRCW08053K90FK	
R11, R22, R24, R25	1k	Panasonic	ERJ-P06J102V	
R18	470R	TE Connectivity	CRGCQ0603F470R	
RCOM1	680R	Yageo	AC0603FR-07680RL	
RPDLS1, RPDLS2, RPORST1, RUSB2	10k	Vishay	CRCW040210K0FK	
RPULS1, RUSB1, RVDDP1, RVDDP2	4.7k	Vishay	CRCW04024K70FK	
RSHELL1	1.1MEG	Vishay	CRCW06031M10FK	
RUSBM1, RUSBP1	22R	Vishay	CRCW040222R0FK	
RX, TX	Test Point 2mm	–	–	
RXTAL1	150R	Vishay	CRCW0402150RFK	
S1, S2	B3F-1020	Omron	B3F-1020	
U1	–	Infineon Technologies	TLD4020-3ET	Not Fitted
U2	TLE7259-3LE	Infineon Technologies	TLE7259-3LE	
U3	TPD2E1B06DRLR	Texas Instruments	TPD2E1B06DRLR	
X1, X3, X5, X6, X7, X8, X25, X26, X27	5001	Keystone Electronics Corp.	5001	
X2	0154.250DR	Littelfuse	0154.250DR	
X4, X10	TSW-108-07-L-S	Samtec	TSW-108-07-L-S	
X9	571-0500	Deltron	571-0500	
X11, X16	D3082-05	Harwin	D3082-05	
X12	571-0100	Deltron	571-0100	
X14	571-0400	Deltron	571-0400	
X15, X30, X31	TSW-102-08-G-S	Samtec	TSW-102-08-G-S	
X17, X23, X28, X41, X42, X43	Solder Jumper 2 Pins	–	–	

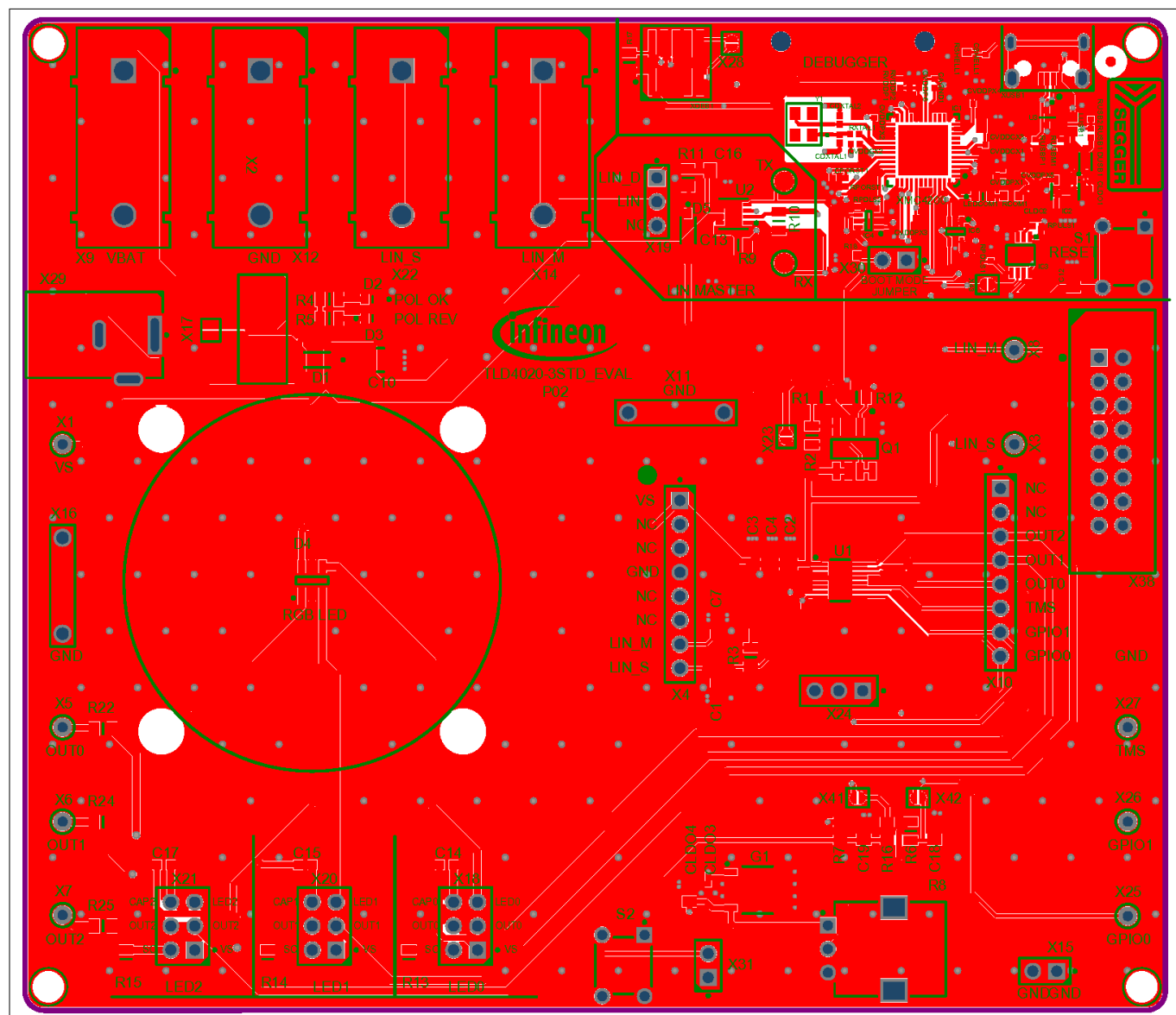
#### 4 System design

Ref Designator	Value	Manufacturer	Manufacturer P/N	Not Fitted item
X18, X20, X21	HTSW-103-07-L-D	Samtec	HTSW-103-07-L-D	
X19	HTSW-103-07-L-S	Samtec	HTSW-103-07-L-S	
X22	571-0700	Deltron	571-0700	
X24	TSW-103-07-L-S	Samtec	TSW-103-07-L-S	
X29	54-00129	Tensility International Corp.	54-00129	
X38	SBH11-PBPC-D08-ST-BK	Sullins	SBH11-PBPC-D08-ST-BK	
XDEB1	FTSH-105-01-L-DV-K	Samtec	FTSH-105-01-L-DV-K	
XUSB1	6,29105E+11	Würth Elektronik	6,29105E+11	
Y1	Crystal 12MHz	Kyocera	CX3225CA12000D0H SSCC	



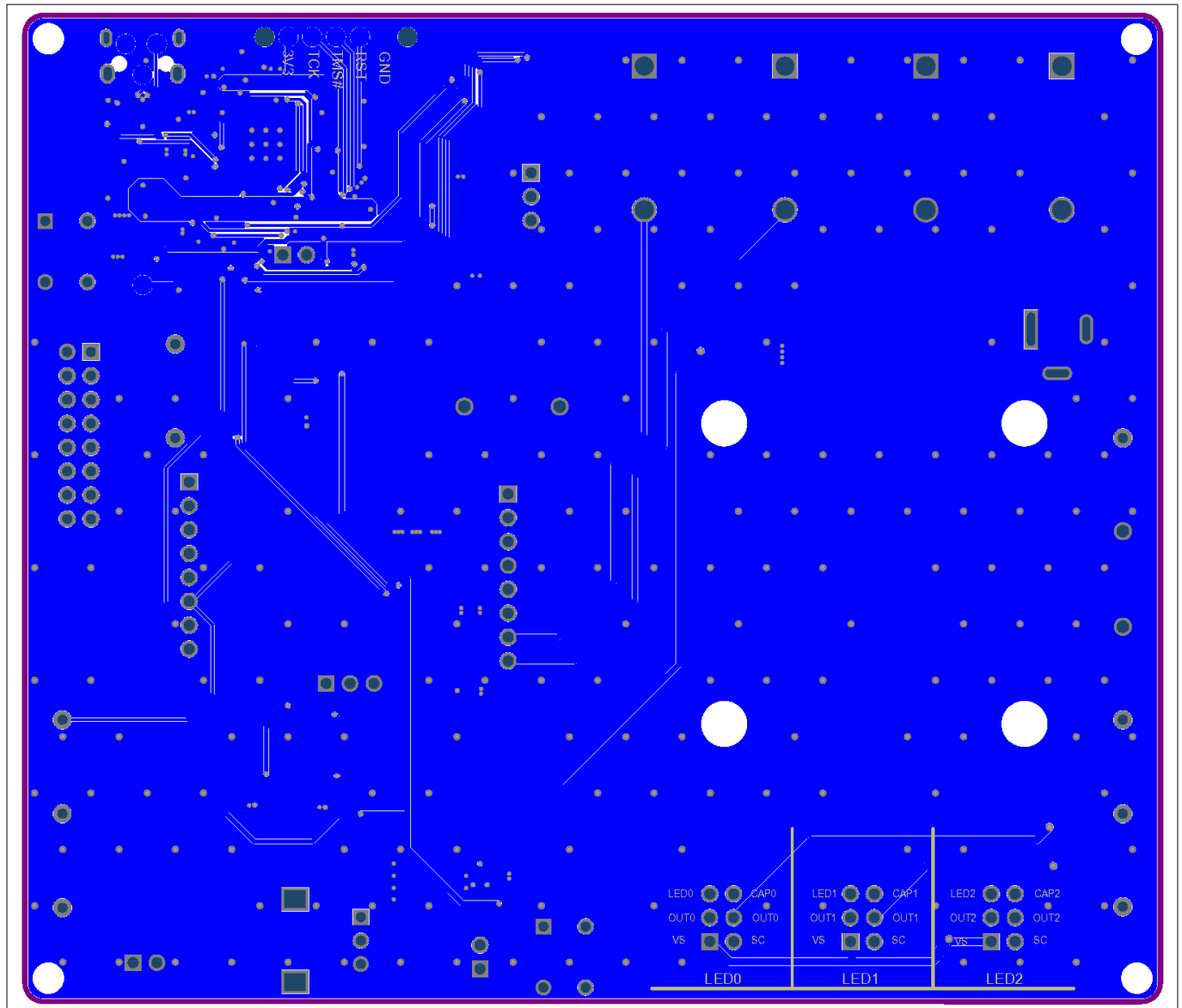
## 4 System design

### 4.1.2 PCB layout



**Figure 15** Top overlay

## 4 System design



**Figure 16** **Bottom overlay**

4 System design

4.1.3 Schematics

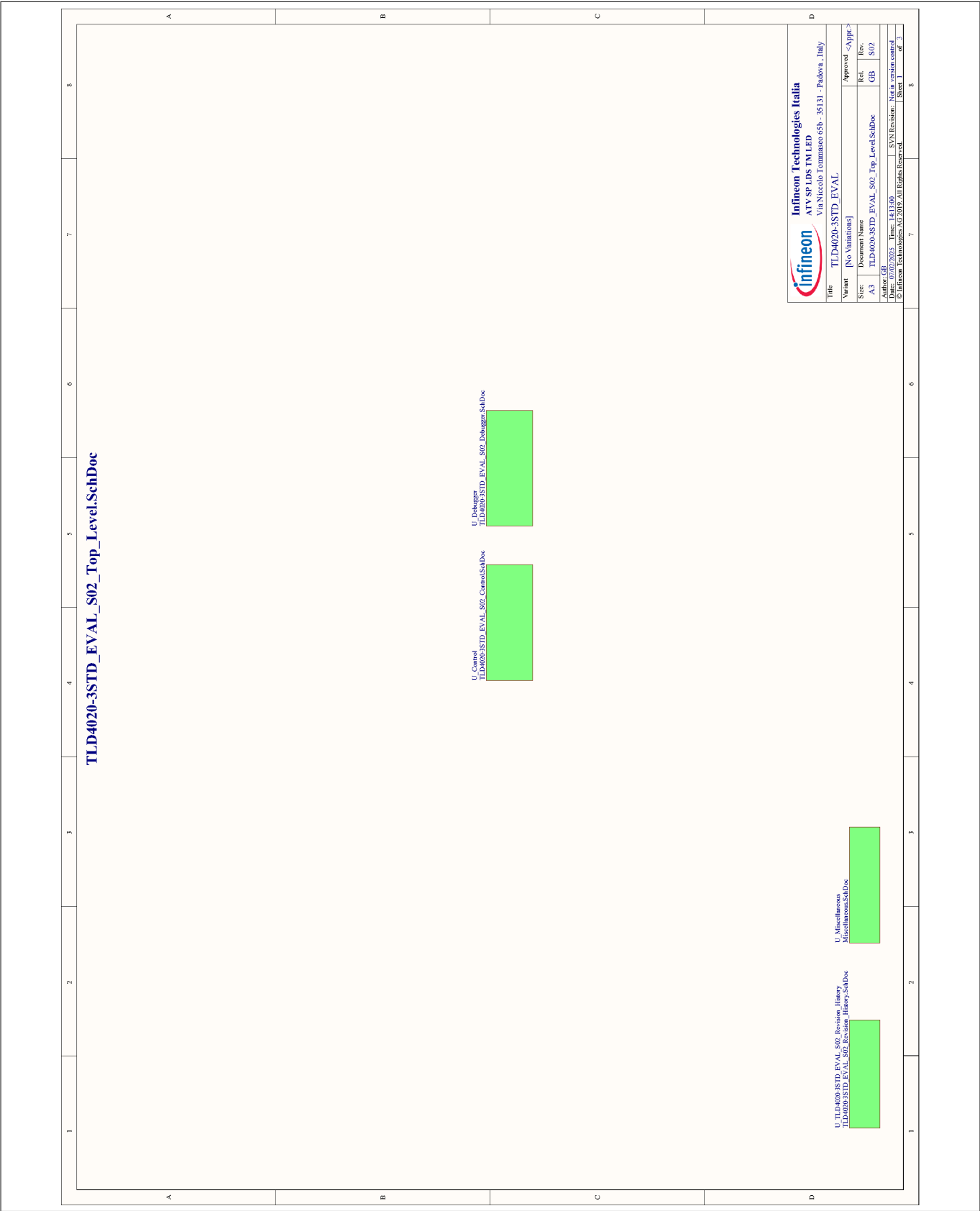


Figure 17 Top level schematic





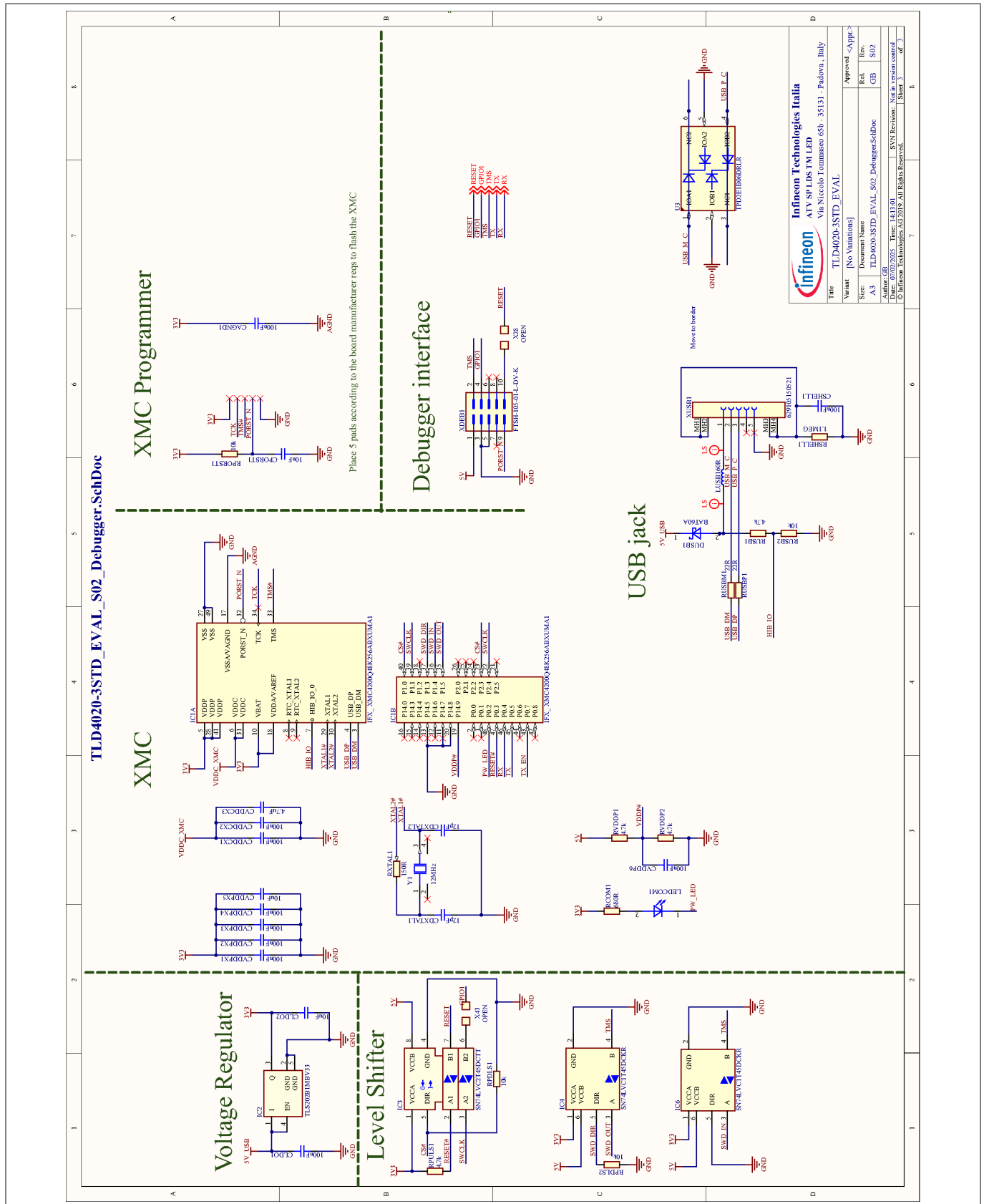


Figure 19

Debugger schematic

## 4 System design

### 4.2 TLD4020-3DB

#### 4.2.1 Bill of material

Ref Designator	Value	Manufacturer	Manufacturer P/N	Not Fitted item
C1, C7	100pF	–	–	Not Fitted
C2, C3, C4	100nF	AVX	08051C104JAT2A	
C5, C6, C8	10nF	–	–	Not Fitted
R1	–	–	–	Not Fitted
<b>U1</b>	<b>TLD4020-3ET</b>	<b>Infineon Technologies</b>	<b>TLD4020-3ET</b>	
X1, X2	SSW-108-01-G-S	Samtec	SSW-108-01-G-S	
X3	SSW-103-01-G-S	Samtec	SSW-103-01-G-S	

#### 4.2.2 PCB layout

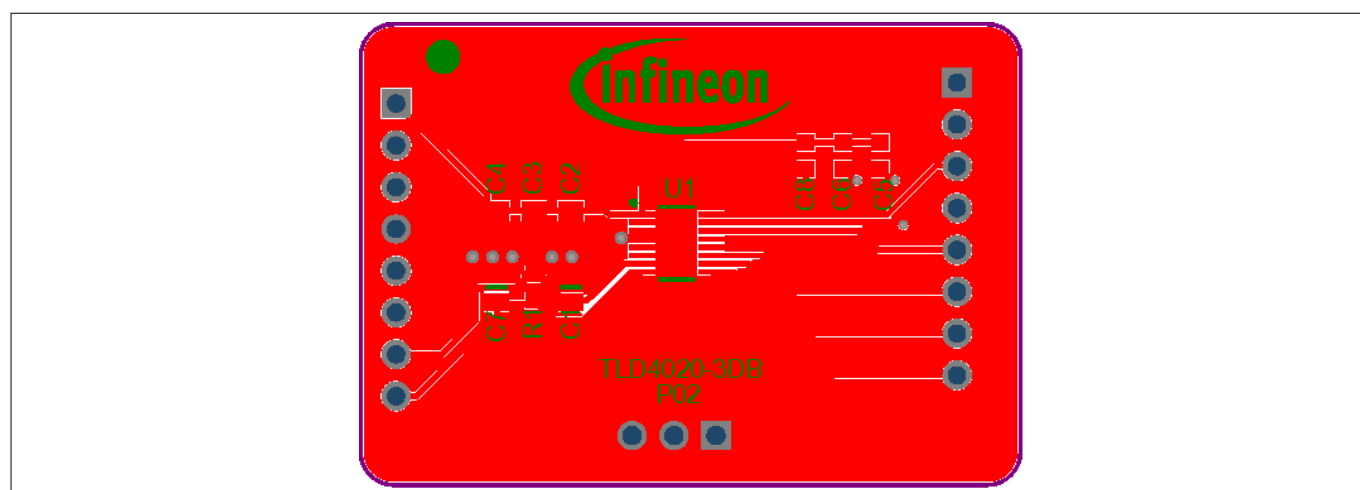


Figure 20 Top overlay

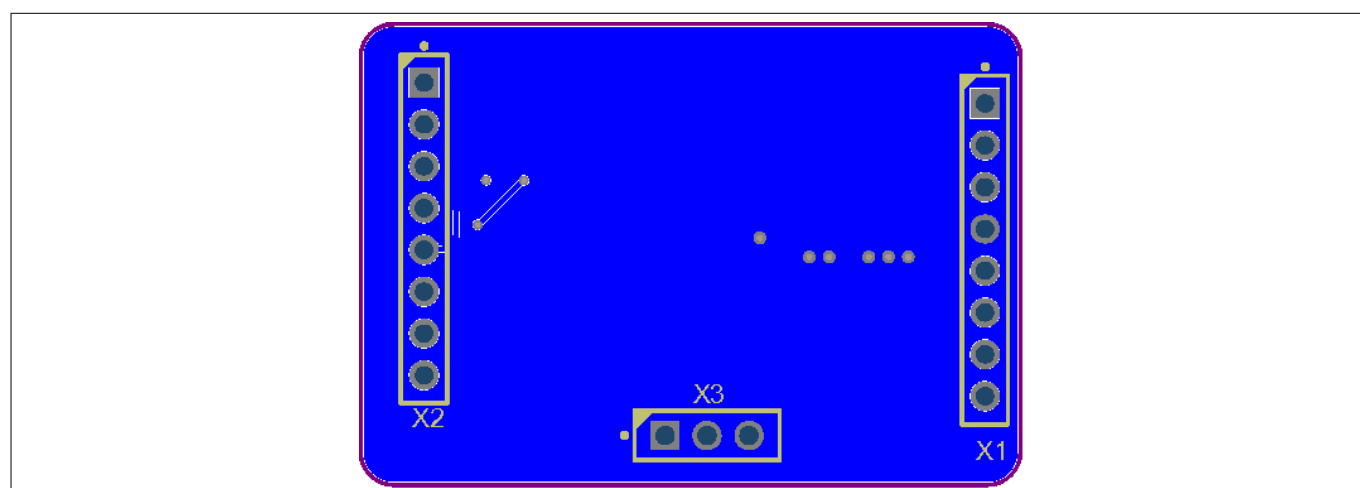


Figure 21 Bottom overlay

4 System design

4.2.3 Schematics

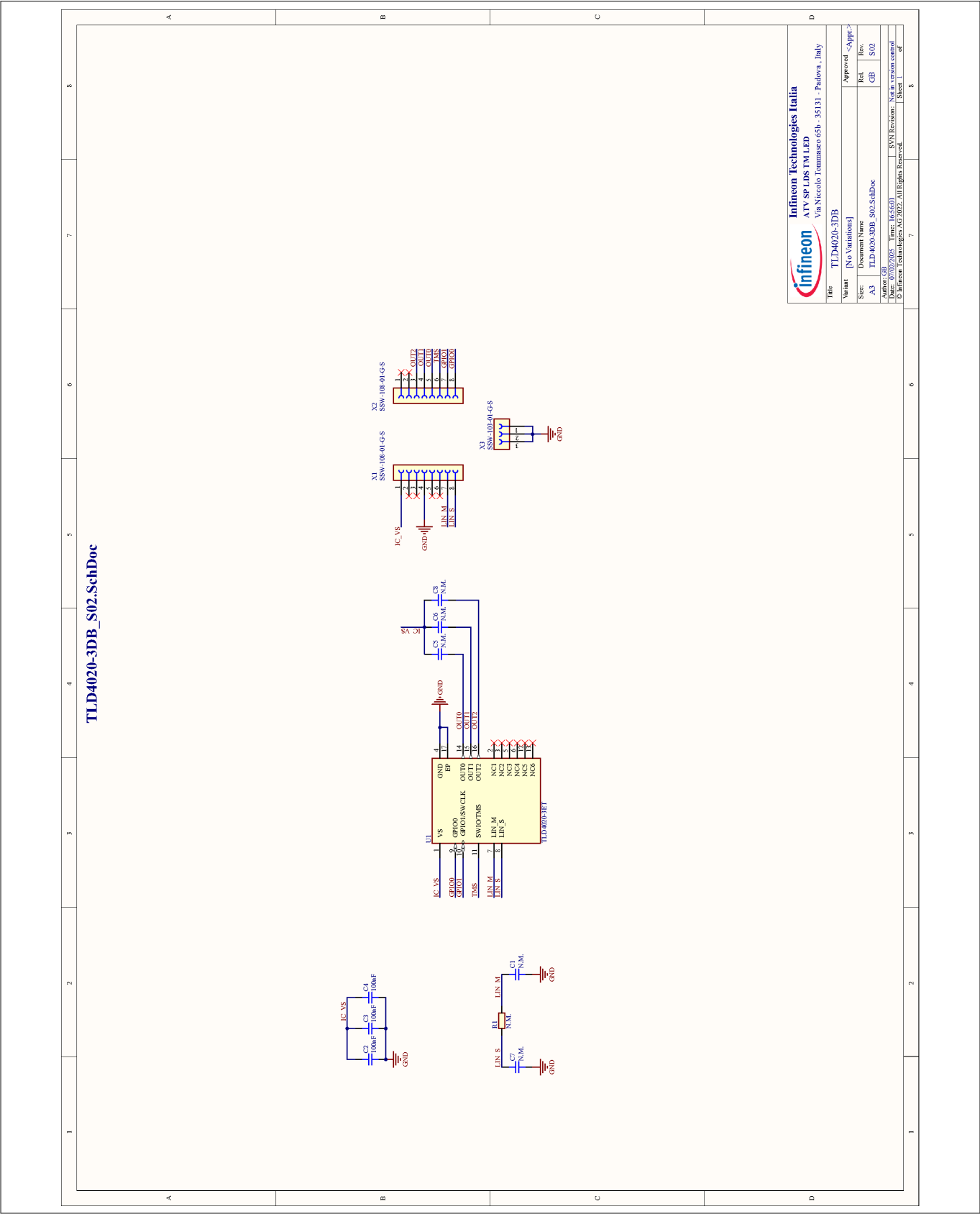


Figure 22 Schematic

## References

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- [2] Infineon: *TLD4020-3ET User manual*
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## Glossary

**bootROM**

*boot code in ROM (bootROM)*

The location of boot code.

**BSL**

*bootstrap loader (BSL)*

A small program or routine that is responsible for initializing the system and loading the main operating system or application into the memory of the target device during the system boot-up process.

**GPIO**

*general purpose input output (GPIO)*

**LED**

*light-emitting diode (LED)*

A semiconductor circuit that emits light when activated.

**LIN**

*local interconnect network (LIN)*

**SWD**

*serial wire debug (SWD)*

A communication interface and protocol used for debugging and programming embedded systems, particularly microcontrollers and other integrated circuits.

**USB**

*universal serial bus (USB)*

An industry standard that defines cables, connectors, and communication protocols used in a bus for connection, communication, and power supply between computers and electronic devices.

## Revision history

Document version	Date of release	Description of changes
Rev. 1.00	2025-07-03	<ul style="list-style-type: none"><li>Initial user guide release</li></ul>



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