Infineon small signal MOSFETs

General information

About this document

Scope and purpose

IC technology in semiconductors is constantly developing, with gate width and total die dimension shrinking each year. Keeping pace with this technological development, the approaches of circuit designers for PCBs have also changed. However, even now, in electrical circuit boards discrete power components remain key components for multiple use cases, and they cannot be integrated into compact ICs because of their different semiconductor processes. This application note is a general introduction to Infineon small signal MOSFETs such as discrete MOSFETs.

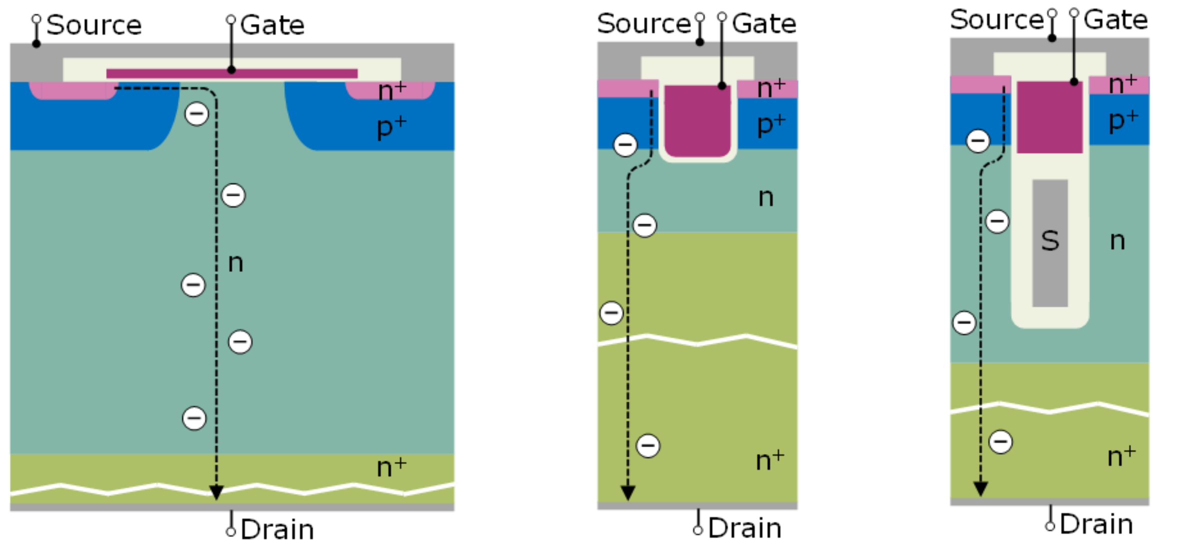
Intended audience

This application note is aimed at mixed signal circuit designers.

Table of contents

1 Different technologies provide a variety of characteristics

Figure 1 shows the structures used for Infineon small signal MOSFETs. In the history of power MOSFETs, “VD-MOS” started with a planar structure, and it is through developing this structure that power MOSFETs have continued to improve their performance. The trench structure brought more compactness to the integration of the cells and enabled more powerful MOSFETs. Field-plate MOSFET technology compensates for the electric field near the PN junction to help reduce $R_{DS(on)}$ while increasing VBDSS. Using different technologies, Infineon small signal MOSFET products cover a wide range of voltage classes. **Figure 2** shows the product performance distribution for VBDSS vs. V_{th}. As shown, N-channel MOSFET products (P-channel MOSFET products) have 0 V ~ 600 V (-300 V ~ 0 V) of VBDSS with 0.5 V ~ 2 V (-0.5 V ~ -2.0 V) of threshold voltage. This product range provides designers with great flexibility for their application designs. In fact, small signal MOSFETs are used in a wide range of applications with different voltage classes – for example, EV battery systems requiring more than 400 V for VDS, and mobile applications supplied by 3.6 V as the nominal voltage of a lithium-ion battery cell.



(a) Planar (b) Trench (c) Field-plate trench

Figure 1 **VD-MOS structure**

Different technologies provide a variety of characteristics

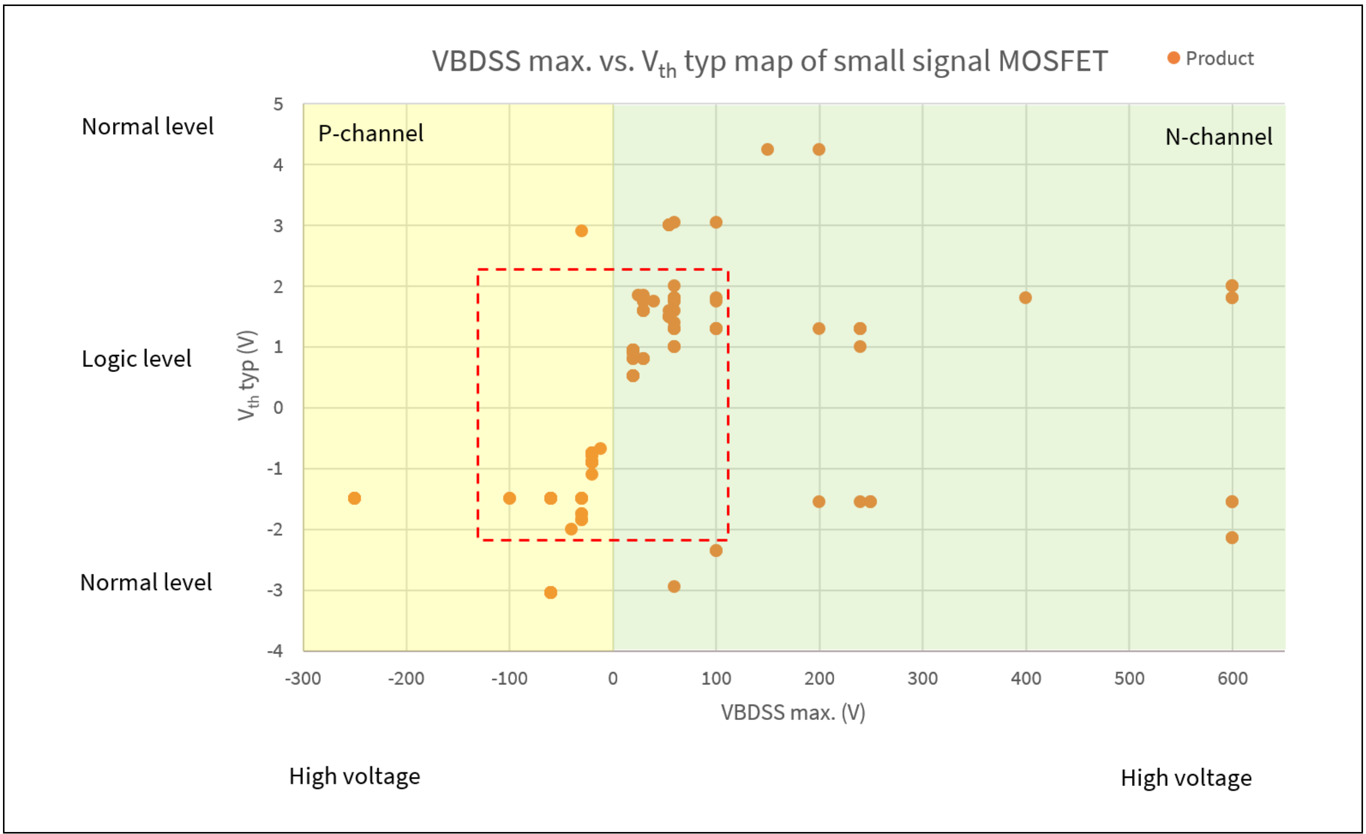
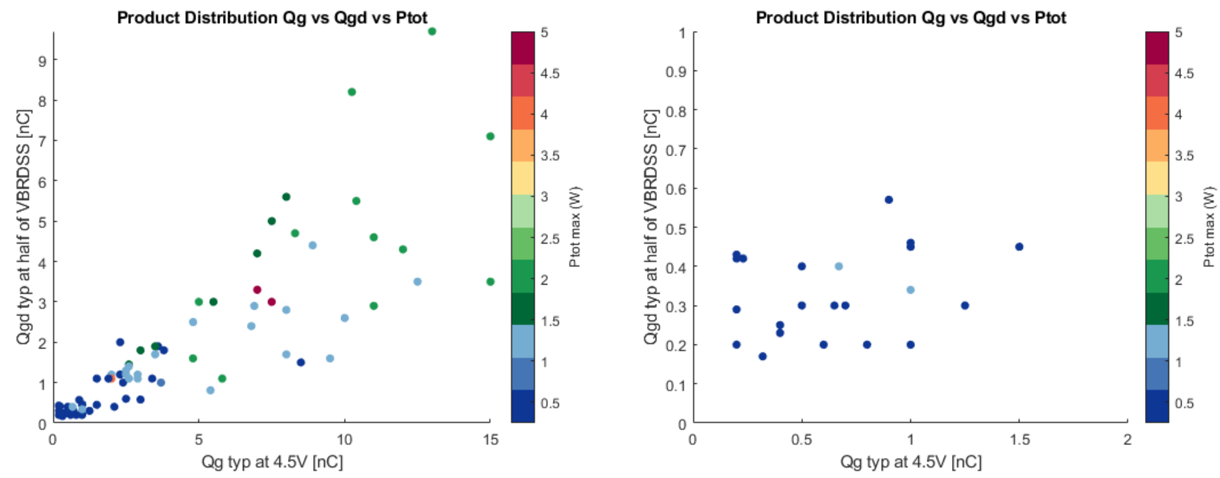


Figure 2 Small signal enhanced mode MOSFETs V_{th} vs. VBDSS map

2 Required performance

Nowadays it is quite rare to find discrete components in electrical applications, because IC technology managed to reduce them through integration into the IC. But there are still several important functions of discrete MOSFETs that cannot yet be integrated into the IC. One of the important roles of discrete MOSFETs is power distribution in applications. Even now there are many cases in which the discrete power components are outside the IC. This means that technologies for miniaturizing and integrating circuits are not always developing in the same direction, and this makes the process more difficult. This is why the discrete power MOSFET still plays an important role in applications. It requires high current-carrying capacity as well as switching capacity because it is often used as a switching device. The area shown by the red dashed line in **Figure 3** indicates common products, and this is the product specification most often required in frequent operating conditions. (If the data distribution is plotted in 3D x, y and z axes are Qg_{typ}, Qgd_{typ} and $P_{totalMax}$, respectively.) Small Qg and Qgd help fast-switching performance and, as shown in **Figure 3**, they can also retain enough power dissipation performance.



(a) In whole range (b) In expanded range

Figure 3 **Product distribution Qg vs. Qgd vs $P_{totalMax.}$**

3 Package features

Infineon small signal MOSFETs present a variety of small packages that can flexibly support different use cases. As shown in **Table 1**, they are equipped with a small outline transistor (SOT) package, which has become one of the most popular small package series. These packages save space in the applications without losing the required thermal dissipation capability, thus providing the designer with many possible options thanks to their footprint compatibility and design friendliness. As it is widely known, the SOT package is highly compatible with other package series.

Table 1 Package dimensions

Package	Terminals	Body length (mm)	Body width (mm)	Min. terminal pitch (mm)	Body length x body width (mm^2)
SC59	3	3	1.3	0.95	3.9
SOT-223	4	6.5	3.5	2.3	22.8
SOT-23	3	2.9	1.3	0.95	3.8
SOT-323	3	2	1.25	0.65	2.5
SOT-363	6	2	1.25	0.65	2.5
SOT-89	4	4.5	2.5	1.5	11.3
TSOP-6	6	2.9	1.6	0.95	4.6

4 Thermal characteristics

Regarding the basic equation for calculating thermal characteristics, it is possible to calculate the allowable maximum current through the product using the following equation. In such calculations, one of the key parameters is the R_{thJC}. However, this is only for steady-state. Should a dynamic thermal behavior be required, Z_{thJC} would be necessary. The Z_{thJC} diagram can be found in the product datasheet, but it is always Z_{thJC} and not Z_{thJA}. Z_{thJA} will change drastically depending on application conditions, and it makes the intrinsic value hard to deliver with the package. The following are equations in steady-state. In order to monitor the dynamic thermal behavior with Zth, it is recommended to use the L3 model in spice simulation, as described in the following chapters.

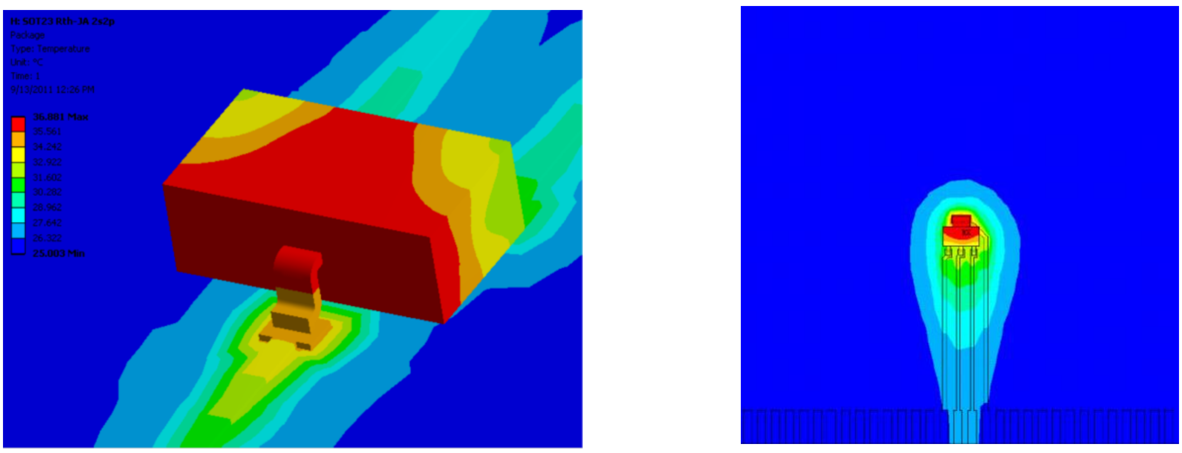
$$I_{\mathrm{DS}} = \frac{\Delta T_{\mathrm{MAX}}}{R_{\mathrm{thJC}}(t_{\mathrm{pulse}}) * VDS} \quad \text{Eq. 1}$$

$$\Delta T_{\mathrm{MAX}} = T_j - T_c = R_{\mathrm{thJC}} * \ P_{\mathrm{dissipated}} \quad \text{Eq. 2}$$

$$P_{\mathrm{dissipated}} = P_{\mathrm{totalMax.}} \quad \text{Eq. 3}$$

4.1 3D thermal simulation

One can see the typical results of thermal dissipation analysis and a clear image of the thermal flow in these packages. Infineon has a wide database of simulation results by ANSYS®. However, the simulation information is not accessible from outside the company. If a customer needs it they should contact their local technical customer support. As shown in the following figures, Infineon small signal packages are designed to allow for thermal dissipation. These packages allow products to have higher current in comparison to ICs, which are also difficult to integrate into the circuit. Below are several examples of simulation results. **Figure 4** shows the thermal flow and **Figure 5** is the graph of thermal resistance between junction to case (R_{thJC}) vs. chip size. The different lines represent different chip thickness in which "top" means R_{thJC} between junction and top side of the case.



(a) SOT-23 thermal simulation (b) SOT-223 thermal simulation

Figure 4 Example thermal simulation by ANSYS®

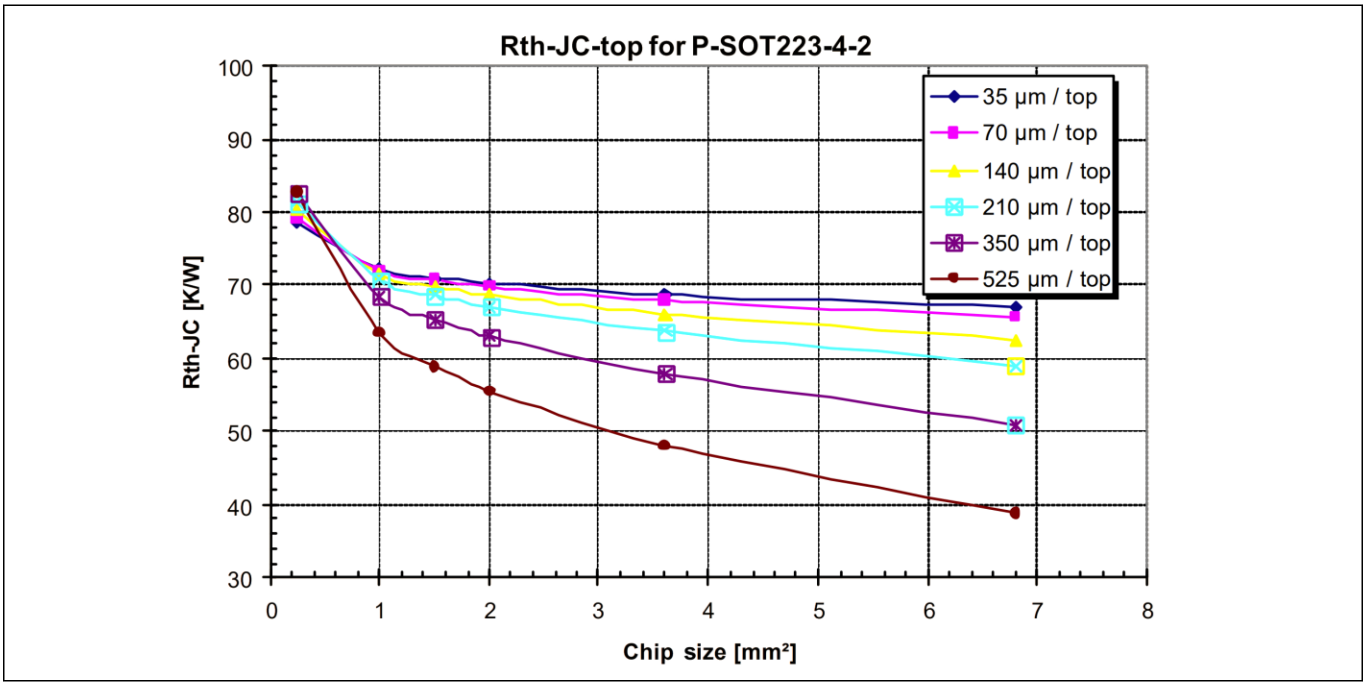
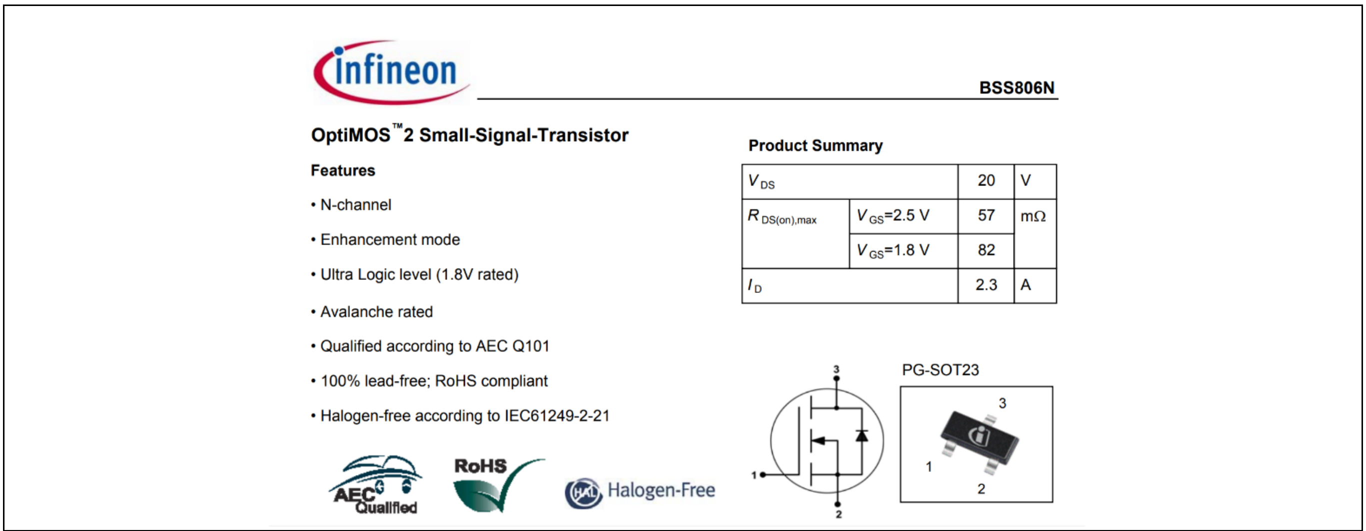


Figure 5 **Example of R_{thJC} vs. chip size according to different chip thickness**

4.2 2D simulation

One of the most useful customer calculation tools is the Spice circuit simulator. The Infineon website offers downloadable Spice models for all of the products. The L3 model includes information on Z_{th}, as shown in **Figure 7**. Using this model, customers can easily make a thermal analysis of the product for their specific use case. For a detailed explanation, see **[2]**. Below is a brief explanation of the calculation method using **BSS806N** to calculate Z_{thJC}. **Figure 7** describes Z_{th}.



BSS806N

OptiMOS™2 Small-Signal-Transistor

Features

- N-channel
- Enhancement mode
- Ultra Logic level (1.8V rated)
- Avalanche rated
- Qualified according to AEC Q101
- 100% lead-free; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product Summary

V_{DS}		20	V
$R_{DS(on),max}$	V_{GS}=2.5 V	57	mΩ
	V_{GS}=1.8 V	82	
I_D		2.3	A

Figure 6 **Datasheet for BSS806N**

Thermal characteristics

```
G_TH  0     Tb   VALUE =  {Pb(abs(I(Ls)),V(Tj,Tcase),Rrbond*(1+(limit((V(Tb)+V(Tj))/2,-200,999)-25)*4m))}
Cthb  Tb       0              1p
Rthb  Tb       Tj             {Rtb}
Rth1  Tj       t1             {72.91m+limit(Zthtype,0,1)*26.98m}
Rth2  t1       t2             {796.9m+limit(Zthtype,0,1)*294.92m}
Rth3  t2       t3             {4.09+limit(Zthtype,0,1)*1.28}
Rth4  t3       t4             {11.88+limit(Zthtype,0,1)*11.21}
Rth5  t4       Tcase          {56.78+limit(Zthtype,0,1)*53.57}
Cth1  Tj       0              2.513u
Cth2  t1       0              6.514u
Cth3  t2       0              50.593u
Cth4  t3       0              389.69u
Cth5  t4       0              600u
Cth6  Tcase    0              6m

.ENDS

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Figure 7 **Spice model for BSS806N**

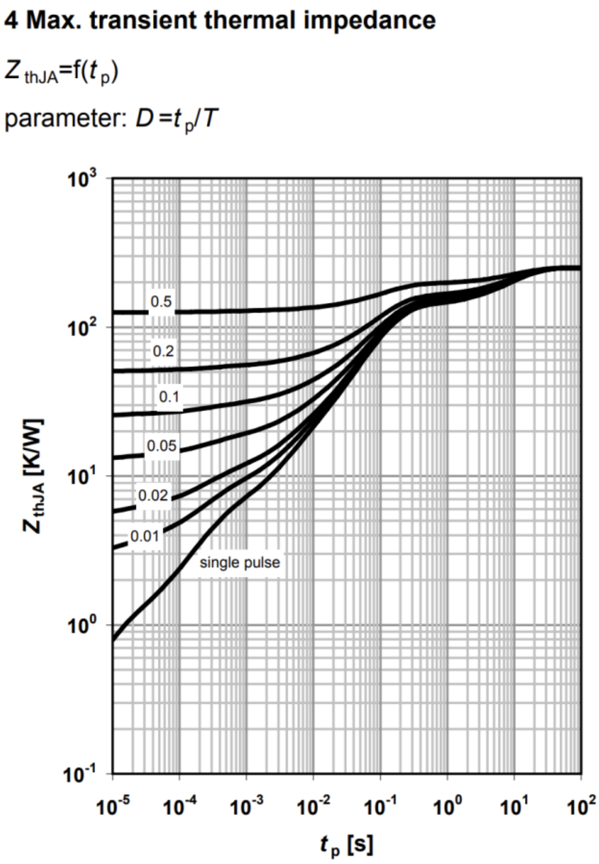

Figure 8 **Z_{thJA} vs. t_p curve in the datasheet for BSS806N**

If Z_{thJC} vs. t_p curve needs to be calculated (similarly to Z_{thJA} vs. t_p in **Figure 8**), a transient simulation with sweeping t_p width is required. Here you can see the time domain transient simulation result with changing the switching duty cycle. This is an example of a simulation giving the estimated Z_{thJC}. The L3 model provides the user with temperature information about the model from the pin-in voltage. By connecting a voltage probe to the T_j and T_{case}, the user can understand the temperature of the p-n junction and case top temperature, respectively. In the schematic (**Figure 9**), the pulse generator is sending switching V_{gs} voltage, which switches the MOSFET on and off. I_d current flows from the drain to the source, and the ARB1 component is measuring

Thermal characteristics

and calculating the I_d current, V_{DS} voltage and $P_{cond} = I_d * V_{DS}$. As the equation shows, $(T_j - T_{case})/P_{generated}$ gives back Z_{thJC}. The graph is the result of the simulation in which the MOSFET was switching at 50 kHz, which is the switching frequency. As shown in **Figure 10**, the Z_{thJC} is changing according to the duty cycle. By using different simulations, a different analysis could be performed, giving the designer not only electrical information but useful thermal information.

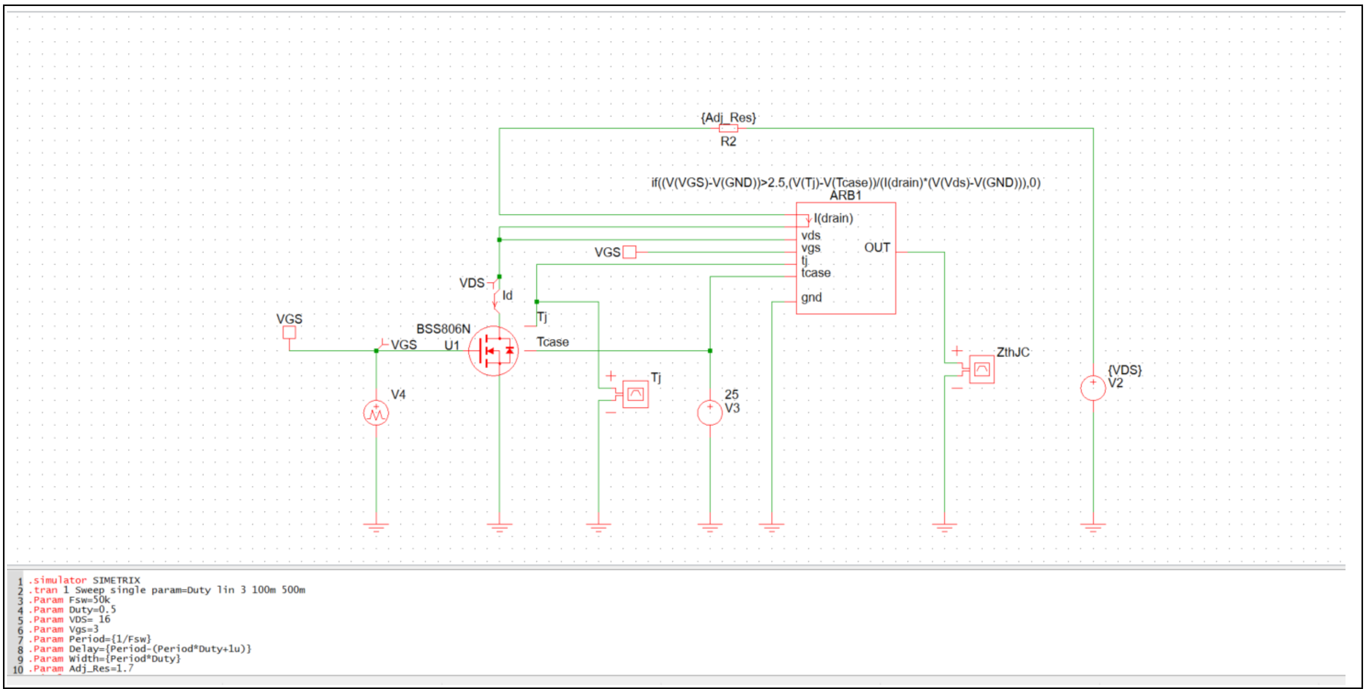

Figure 9 **Schematic of Spice simulation**

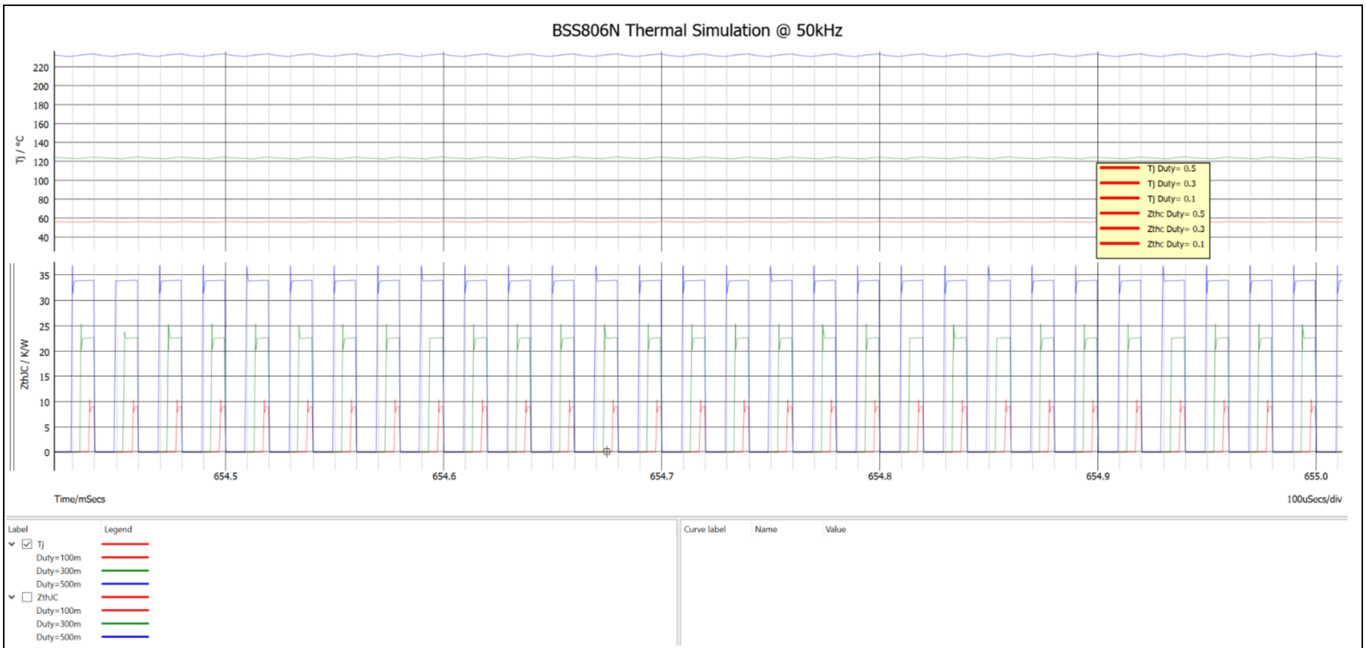

Figure 10 **Result of Spice simulation**

5 Multiple uses covering different characteristics

Figure 11 shows possible applications in which small signal MOSFETs can be used. Load intensity is represented on the vertical axis and switching speed is on the horizontal axis. The color represents the range of V_{DS} voltage. High voltage can be up to 600 V and low voltage can be close to 20 V. The figure provides a better overview to understand how small signal MOSFETs can be employed in a wide range of use cases.

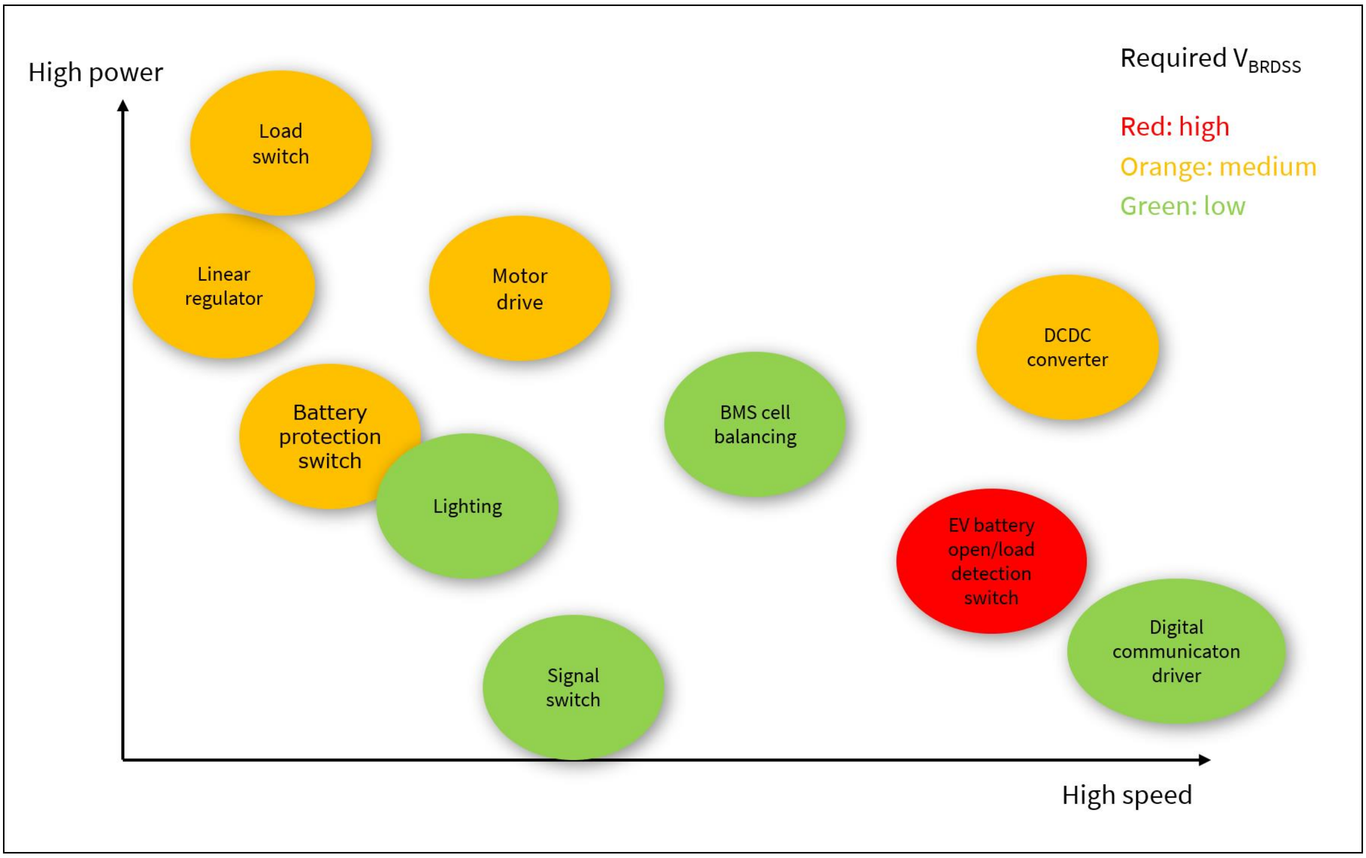

Figure 11 Map of applications for small signal MOSFETs

6 ESD robustness

This final chapter describes the qualification level of the products. In particular, the most concerning defect in electrical product fabrication is ESD. Other small signal MOSFETs do not have specific ESD protection. However, Infineon products have intrinsic ESD robustness depending on die size as shown in **Table 2**. For specific use cases there are products with ESD protection as shown in **Table 3**.

Table 2 Example of intrinsic ESD robustness of small signal MOSFETs

Chip size (mm^2)	ESD class
0.64	ESD HBM 0A (< 125 V) ESD CDM C3 (> 1000 V)
1.38	ESD HBM 0B (125 V to < 250 V) ESD CDM C3 (> 1000 V)
1.96	ESD HBM 1A (250 V to < 500 V) ESD CDM C3 (> 1000 V)
3.41	ESD HBM 1B (500 V to < 1000 V) ESD CDM C3 (> 1000 V)
6.24	ESD HBM 1C (1000 V to < 2000 V) ESD CDM C3 (> 1000 V)

Table 3 Small signal MOSFETs with ESD protection

Product name	Package	HBM ESD class	ESD voltage range (V)	VBRDSS (V)	MOSFET
BSD314SPE	SOT-363	1C	1 k to 2 k	-30 V	Single
BSL305SPE	TSOP-6	1C	1 k to 2 k	-30 V	Single
BSL308PE H	TSOP-6	2	2 k to 4 k	-30 V	Dual
BSL314PE H	TSOP-6	1C	1 k to 2 k	-30 V	Dual
BSS308PE	SOT-23	2	2 k to 4 k	-30 V	Single
BSS314PE	SOT-23	1C	1 k to 2 k	-30 V	Single
BSS806NE H	SOT-23	1C	1 k to 2 k	20 V	Single

References

[1] Infineon Technologies AG. AP99007 (2017): Linear Mode Operation and Safe Operating Diagram of Power-MOSFETs, V 1.1, **available online**

[2] Infineon Technologies AG. AN_201712_PL11_001 (2017): Dynamic thermal behavior of MOSFETs, V 1.0, **available online**

[3] Infineon Technologies AG. AN 2014-02 (2014): Simulation models for Infineon Power MOSFET, V 2.0, **available online**

[4] B. Jayant Baliga, Fundamentals of Power Semiconductor Devices, Springer, ISBN-13: 978-3319939872

Revision history

Document revision	Date	Description of changes
V 1.0	2022-08-08	Initial release
V 1.1	2022-10-17	Error corrections, Table 3 added
V 1.2	2022-11-10	Link to figure 2 corrected, replaced denomination “small signal products” with “small signal MOSFETs”

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