OPTIGA™ Authenticate NBT

Hardware integration guide

About this document

Scope and purpose

The scope of this document is to provide information and guidance on how to connect the OPTIGA™ Authenticate NBT to a host controller. It contains several connectivity examples, comprehensive data on the SMD package and lists the electrical parameters for the OPTIGA™ Authenticate NBT and its interfaces. Additionally, the document outlines the relevant data for the hardware configuration at the time of delivery.

The purpose of this document is to assist customers, such as device integrators and PCB board developers to integrate the OPTIGA™ Authenticate NBT into a PCB.

Intended audience

This document is primarily intended for device integrators and PCB board manufacturers.

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1 Introduction

This chapter provides an explanation of how this guide fits into the OPTIGA™ Authenticate NBT documentation landscape and a short product overview.

Chapter 2 contains different recommendations for connecting the OPTIGA™ Authenticate NBT externally.

Chapter 3 provides information about available delivery forms and how the product's interfaces are assigned to the package pins.

Chapter 4 provides the following technical data:

- Absolute maximum ratings
- Operational characteristics include information on the electrical DC and AC characteristics, I2C interface characteristics, NFC interface characteristics, IRQ interface characteristics, package characteristics, and performance characteristics of the device

***Note**: For a collection of all available support material for the product, refer to its product page [10].*

1.1 Documentation landscape

The documentation landscape for the OPTIGA™ Authenticate NBT is depicted in Figure 1, providing an overview of the essential artifacts needed to integrate the device into the hardware and software. This figure illustrates the various documentation resources that are available to assist you in the integration process, both in terms of hardware and software. By following these guidelines and using the available resources, a successful integration of the OPTIGA™ Authenticate NBT into the product can be achieved.

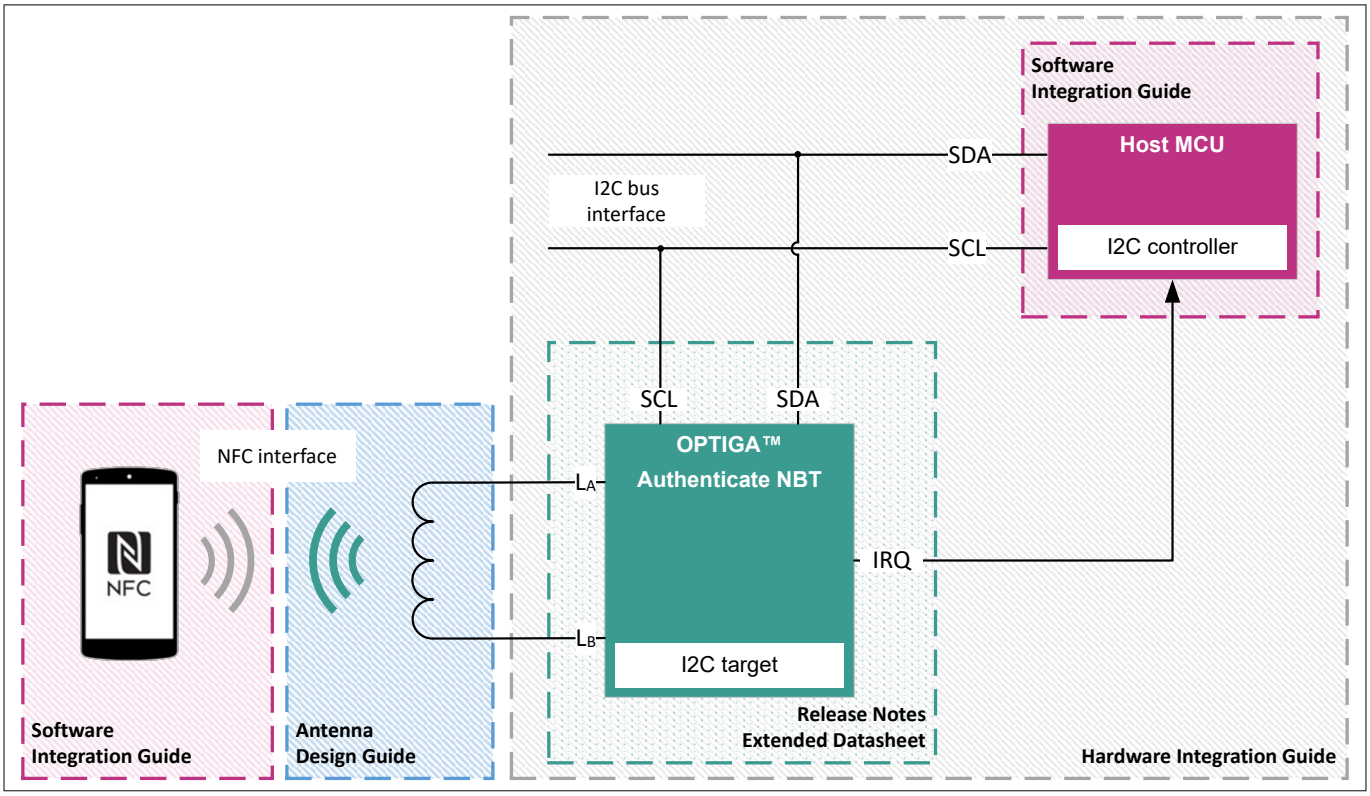

Figure 1 OPTIGA™ Authenticate NBT documentation landscape

The Hardware Integration Guide for the OPTIGA™ Authenticate NBT is designed to aid customers who are integrating the device into their devices or PCB boards. This guide is intended for device integrators and PCB board developers who are seeking comprehensive information about incorporating the device into their designs. When used alongside the OPTIGA™ Authenticate NBT Antenna Design Guide (refer to [13]) and General

recommendations for board assembly of Infineon packages (refer to [15]), customers receive a complete set of instructions and guidelines needed to integrate the OPTIGA™ Authenticate NBT into devices and PCB boards.

1.2 NFC I2C bridge tags

NFC Bridge Tags are dual-interface tags that enable contactless features for IoT devices via an I2C controller interface, allowing for a touch-and-go experience with a mobile phone. On one side, the NFC Bridge Tags include a contactless passive NFC interface and on the other side, a contact-based I2C target interface that connects to the MCU of the IoT device.

The OPTIGA™ Authenticate NBT harnesses the Integrity Guard 32 security architecture to provide an option for the end-user with symmetric and asymmetric cryptographic operations, as well as password-based data protection schemes. As a result, the device is ideal for security demanding applications.

This product includes device authentication, pass-through and asynchronous data transfer modes, which can be used for variety of applications such as:

- Keyless access and activation of shared mobility vehicles
- Controlled access to personal electronic devices such as HDD
- Theft prevention for electronic goods by authenticated activation

This tag can also be used in healthcare and industrial applications. The OPTIGA™ Authenticate NBT, in combination with healthcare sensors, enables access to information through an NFC-enabled mobile phone or reader. Furthermore, the device is an ideal product for industrial applications such as headless configuration and parametrization of devices, assembly line programming and fault diagnostics.

2 Hardware overview

The OPTIGA™ Authenticate NBT is a high-performance dual-interface bridge tag, which includes a contactless passive NFC interface and an I2C target interface for connecting to an I2C controller (host MCU). For example, in IoT applications, it can be operated as an NFC-to-I2C bridge tag. The interfaces can be operated independently, which opens up a wide range of application use cases for the OPTIGA™ Authenticate NBT (refer to [11]).

2.1 Connectivity

This section outlines some key principles for the integration of the OPTIGA™ Authenticate NBT in different application scenarios. Additionally, this section provides recommendations for external connection of the OPTIGA™ Authenticate NBT. Understanding the product and interface configuration at delivery is essential to determine the behavior of the device during the initial startup process.

2.1.1 NFC-only tag

In this particular application scenario, the OPTIGA™ Authenticate NBT is used as an NFC tag, specifically in applications related to brand protection. In this configuration, the OPTIGA™ Authenticate NBT can operate as a standalone device without requiring any connection to a host. The device must at least be connected to an NFC antenna through its L_A and L_B pins. In this setup, the device obtains energy from the electromagnetic RF field generated by an NFC reader in range via the antenna. Once powered up, the device is ready to be used in the target use case.

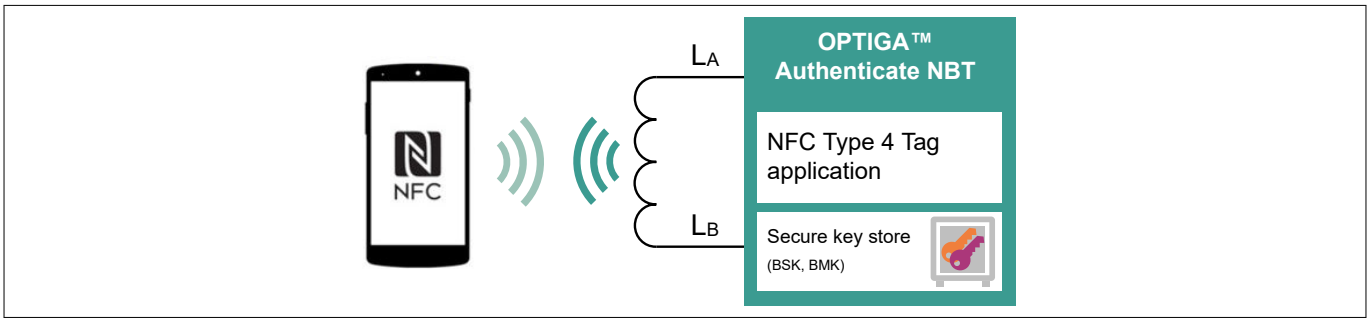

Figure 2 NFC-only tag setup

The OPTIGA™ Authenticate NBT may also be connected to an external supply via its power pins (V_{CC}, GND). In this setup, the device is powered from the external supply and may communicate with the NFC reader in the range of its NFC antenna. This configuration enables longer NFC communication distances.

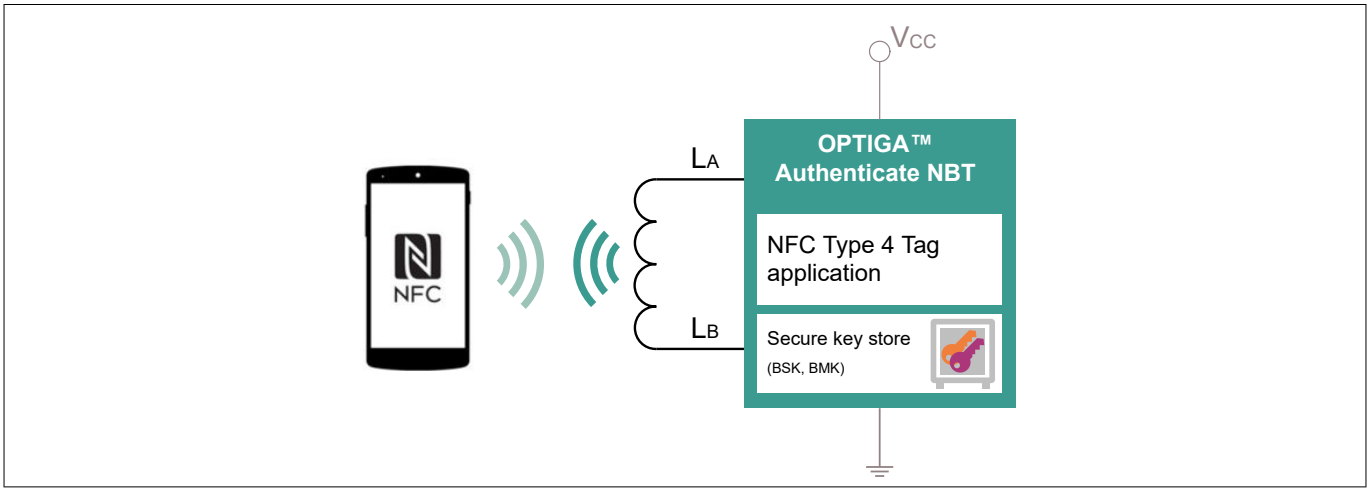

Figure 3 V_{CC}-powered tag setup

2.1.2 Bridge tag

In the bridge tag setup, the OPTIGA™ Authenticate NBT is embedded into a system that includes a host MCU and an NFC antenna. The device is connected to the host MCU via its I2C target interface and externally supplied from the host system through its power pins (V_{CC} and GND) . The contactless, passive NFC interface is operated via the antenna connected to L_A and L_B pins.

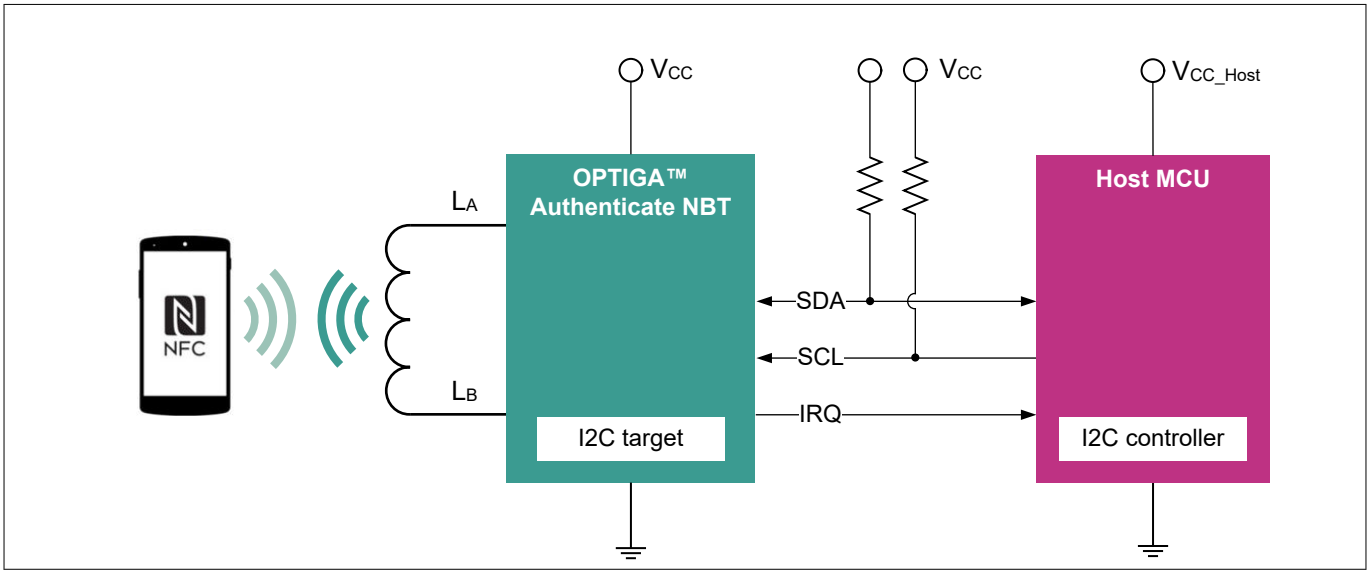

Figure 4 Bridge tag

While the host MCU and the OPTIGA™ Authenticate NBT may be powered with different voltages (V_{CC_Host} and V_{CC}), a single voltage domain is preferred to avoid the usage of level shifters for the digital lines (SCL, SDA and IRQ). V_{CC} must not exceed the allowed input voltage levels of the I2C controller device.

2.1.3 Bridge tag - host controlled hibernation

In the context of bridge tag applications, it may be necessary to power down components to reduce the overall power consumption of the system. Even though the OPTIGA™ Authenticate NBT does not have a hibernation feature, it can still be disconnected from the supply (V_{CC} and GND) by utilizing an external circuitry. To avoid any indirect power supply through the I2C bus interface lines (SCL, SDA), it is recommended to disconnect them along with the external supply if the device is not in use. The sequence can be controlled by an application on the host MCU.

Figure 5 illustrates some options to implement host controlled hibernation, depending on the host system's design. Assuming that the host system only manages the OPTIGA™ Authenticate NBT as the solitary device linked to the I2C interface, the hibernation mechanism will comprise of a simple switch, which is controlled via the EN line.

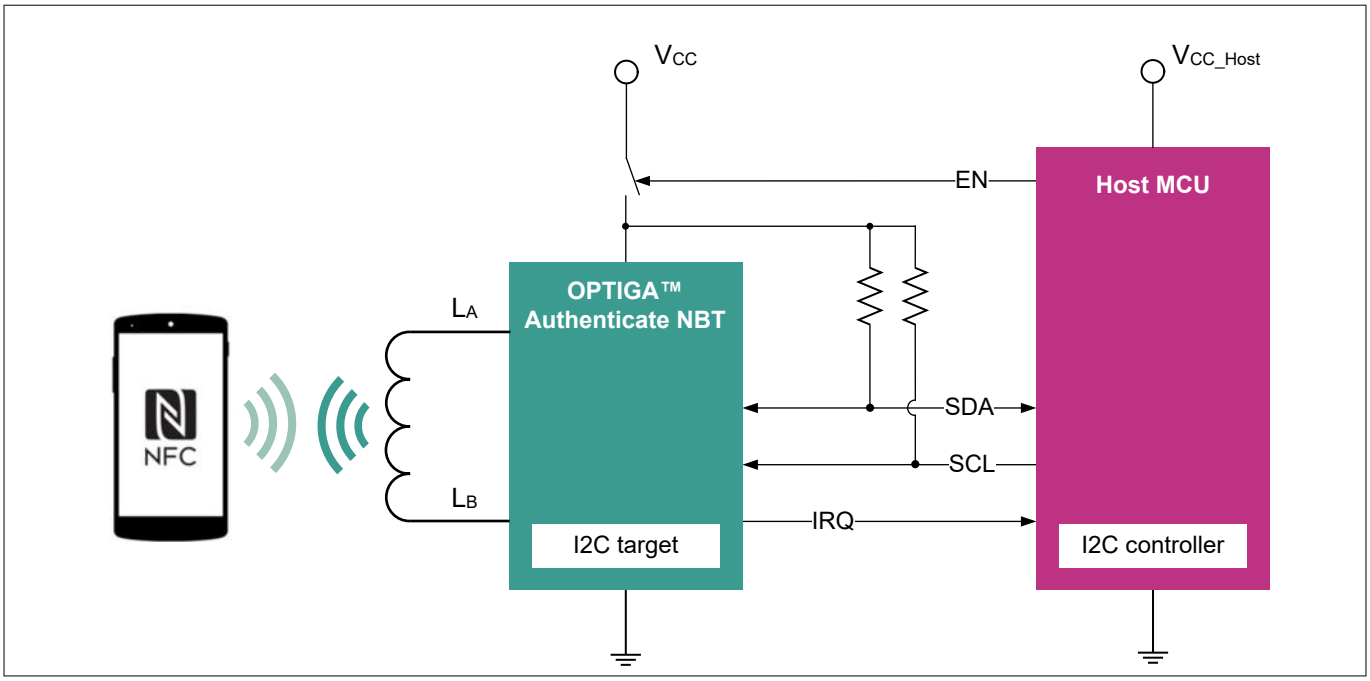

Figure 5 Bridge tag – host controlled hibernation - OPTIGA™ Authenticate NBT only

In order to avoid any unintentional power supply through the SCL and SDA lines, it is important to disable the I2C bus interface. This can be achieved by reconfiguring it to an input. Additionally, it is necessary to deactivate internal pull-up resistors (if available).

If there are multiple devices communicating via the I2C bus, bidirectional switches to open the SCL and SDA lines are controlled by the host MCU.

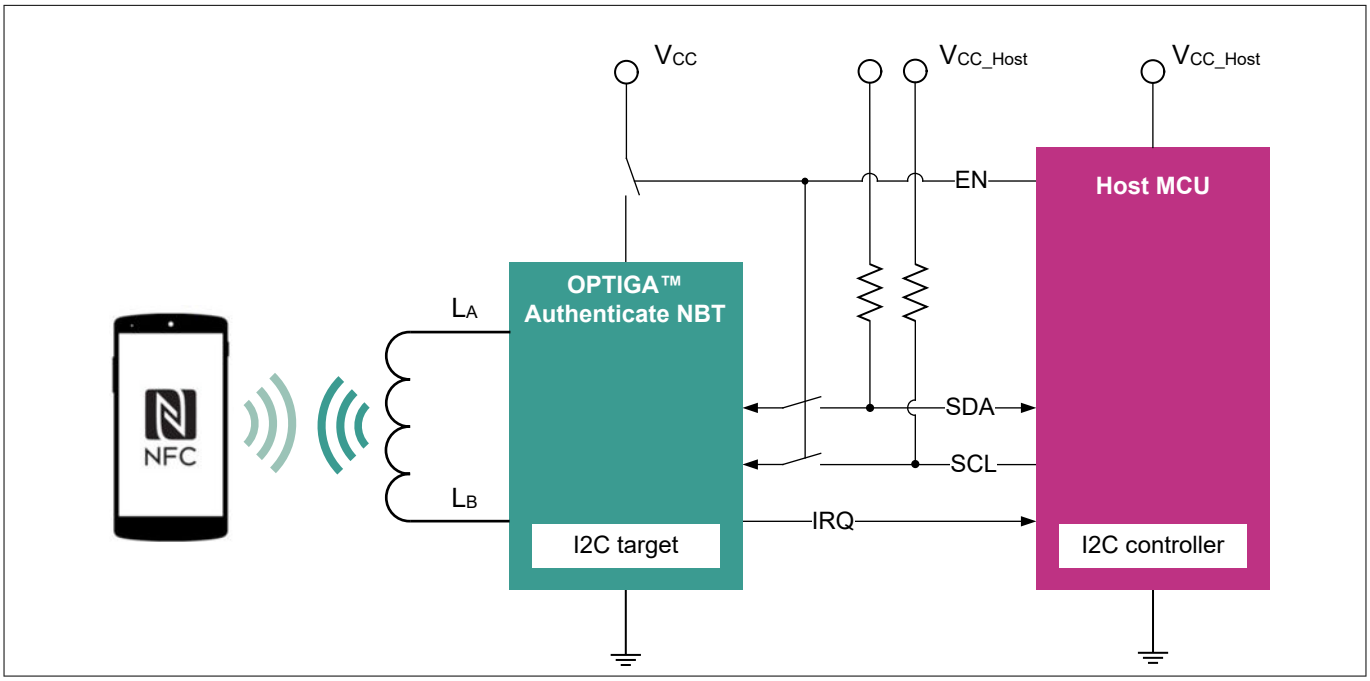

Figure 6 Bridge tag – host controlled hibernation - multiple I2C bus devices

2.1.4 Bridge tag - field detection - wake-up signal generation

Another aspect that can be considered in bridge tag applications, along with the need to reduce system power consumption, pertains to the generation of a wake-up signal upon detection of the RF field of an NFC reader.

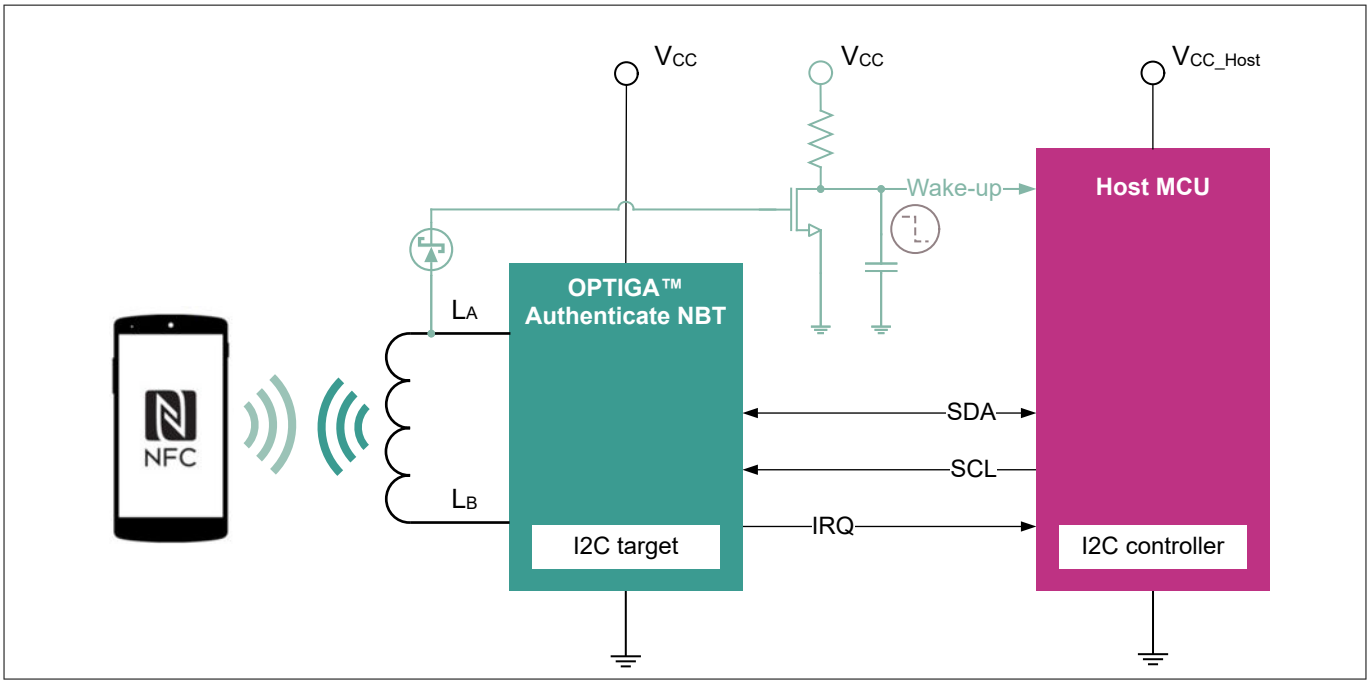

Figure 7 Bridge tag - field detection - wake-up signal generation

A field detection circuitry is directly connected to the NFC antenna of the OPTIGA™ Authenticate NBT to achieve this objective. The circuit is capable of sensing the presence of an RF field and generating a wake-up signal for the host MCU.

2.2 Initial interface and product configuration

The OPTIGA™ Authenticate NBT is delivered with initial configurations for the NFC interface, the I2C interface and the IRQ line. Additionally, the current limitation functionality is disabled by default. These default settings, as shown in Table 1, determine the initial product behavior.

Table 1 Product configuration at delivery

Interface	Parameter	Default setting
NFC	Interface	Enabled
	UID	7-byte UID
	WTXM (M= multiplier)	'1'
I2C	Interface	Enabled
	I2C device address	18_H
	I2C speed	Fast mode plus (1000 kHz)
	Idle timeout	500 ms
	I2C driver strength	Strong
IRQ	Function	Disabled

(table continues...)

Table 1 (continued) Product configuration at delivery

Interface	Parameter	Default setting
	Pull-up/pull-down setting	none (no pull)
	Output type	Push-pull
	Assertion level	Active-high
	IRQ event	RF field on
Power consumption	Current limitation	No current limitation

By integrating the OPTIGA™ Authenticate NBT into a system that includes a host MCU and an antenna enables control of the device via NFC and/or I2C interface. The interface settings, as well as other product configurations, can be customized to meet the needs of a target application. For more information, refer to [11].

2.3 Functional compliance

The OPTIGA™ Authenticate NBT, including its integrated Type 4 Tag application, complies with the following:

- NFC Forum Type 4 Tag Technical Specification [3]
- NFC Forum Analog Technical Specification [4]
- NFC Forum Digital Protocol Technical Specification [5]
- NFC Forum Activity Technical Specification [6]
- NFC Forum NDEF Technical Specification [7]

3 Delivery forms

This chapter provides information about available delivery forms and how the product's interfaces are assigned to the package pins. For further information on compliance of the packages with European Parliament Directives, see Chapter 3.2.

For details and recommendations on the assembly of packages on PCBs, please refer to [14].

3.1 SMD package

The following package is available:

- PG-USON-8-8

The figures in the sections below show the following aspects of the package:

- **Package outline:** It shows the package dimensions of the device in the individual packages
- **Package footprint:** It shows footprint recommendations
- Tape and reel packing
- **Sample marking pattern:** It describes the productive sample marking pattern on the package
- **Package layout:** It shows a simple layout with the pin numbers described in the pin-to-signal reference section

***Notes**:*

1. *The drawings are for information only and not drawn to scale. More detailed information about package characteristics and assembly instructions is available on request.*

2. *Unless specified otherwise, all figure dimensions are given in mm.*

3.1.1 PG-USON-8-8

Package outline

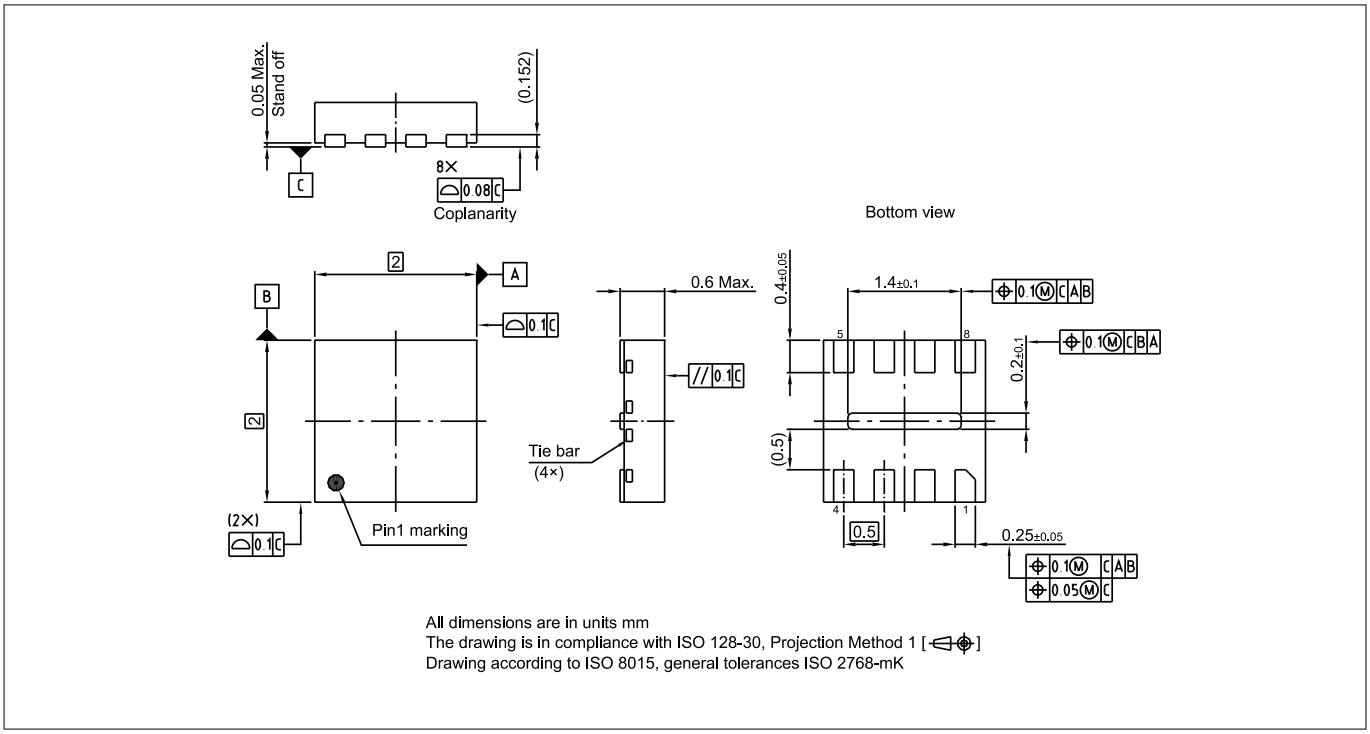

Figure 8 PG-USON-8-8 package outline

Package footprint

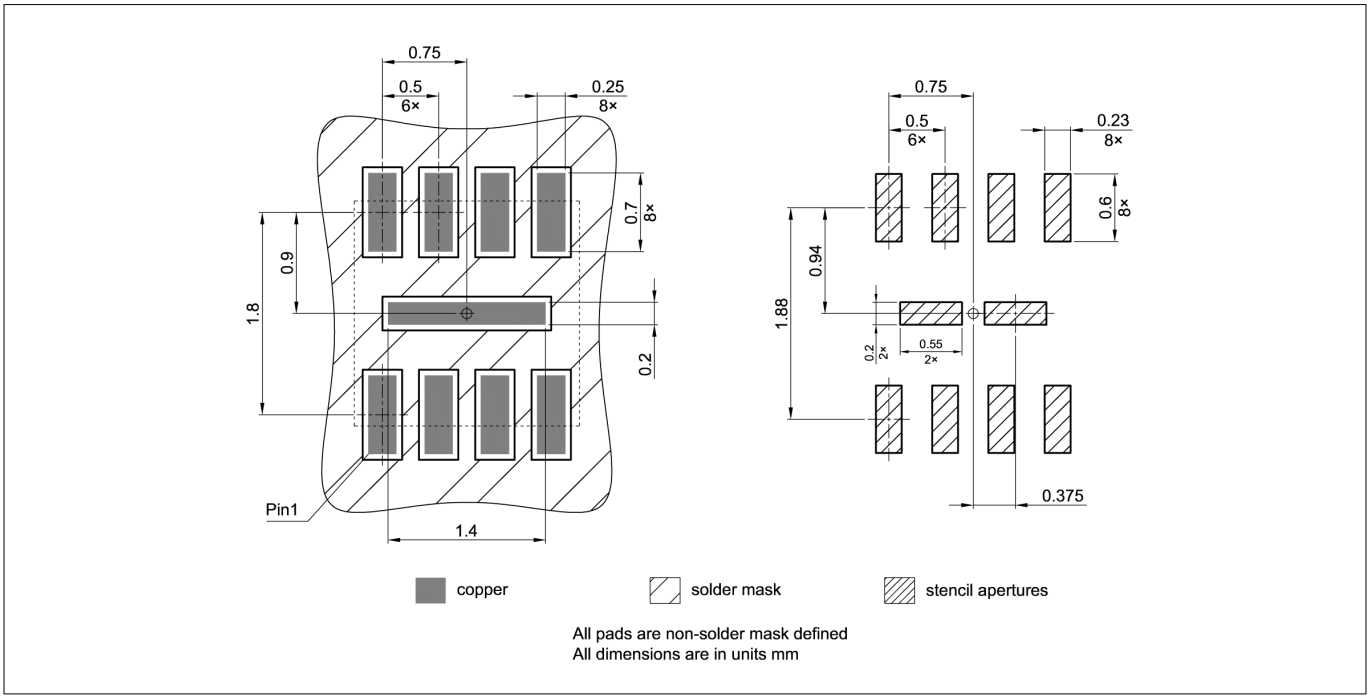

Figure 9 PG-USON-8-8 package footprint

Tape & reel packing

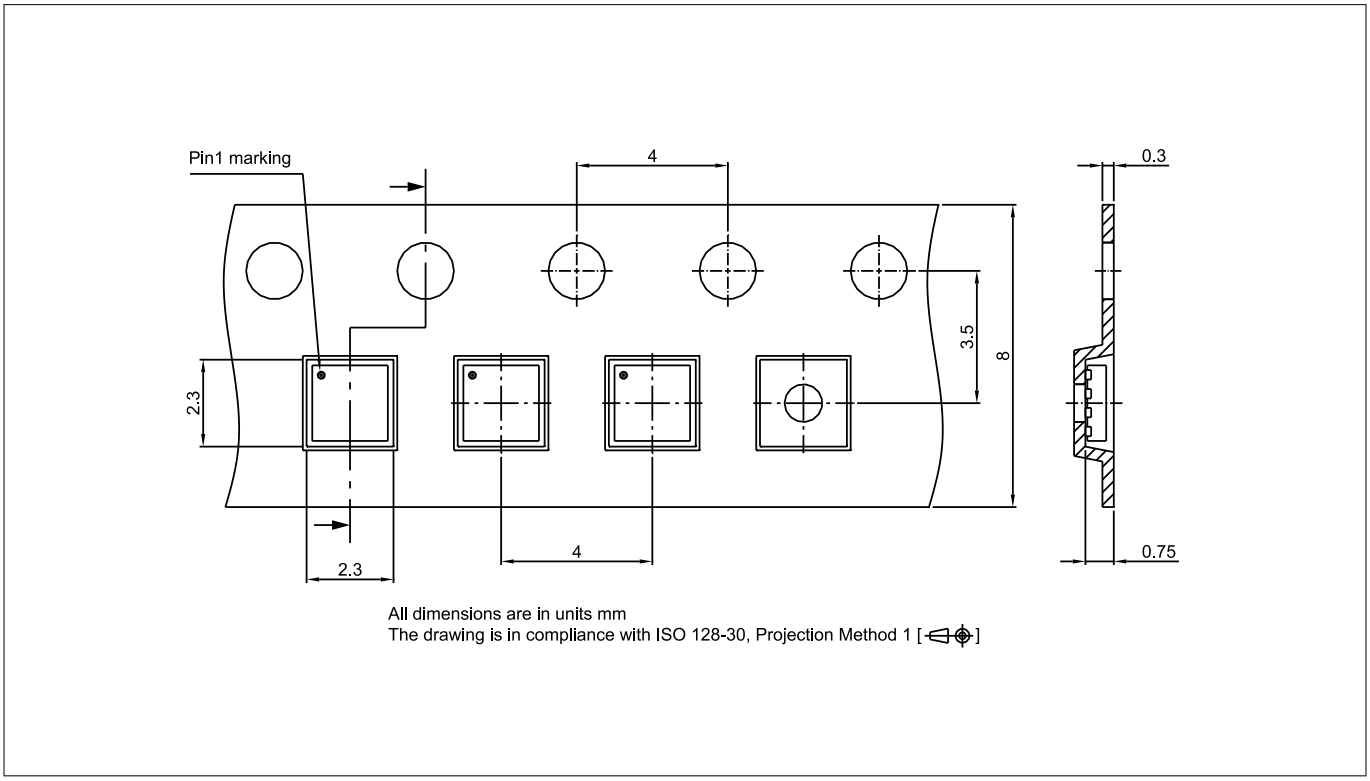

Figure 10 PG-USON-8-8 tape & reel packing

Production sample marking pattern

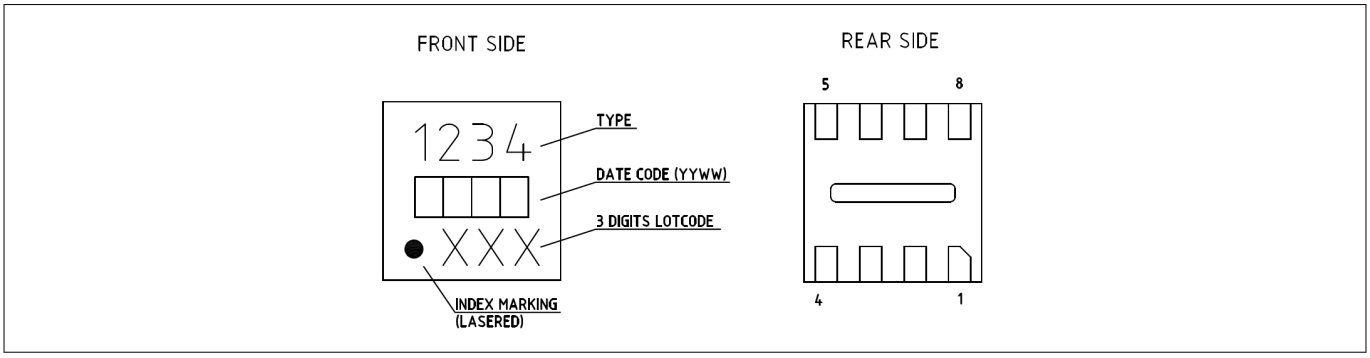

Figure 11 PG-USON-8-8 sample marking pattern

The dot indicates pin 1 for the chip. The following table describes the sample marking pattern:

Table 2 Marking table for PG-USON-8-8 packages

Indicator	Description
1234[1)]	**Type code** • OPTIGA™ Authenticate NBT: NBT2
□□□□	**Production date:** “<YYWW>”, two bytes, BCD coded • <YY>: Production year • <WW>: Production week It is inserted during fabrication
XXX	**Lot code** It is defined and inserted during fabrication, issued by the packaging site

1) "1234" in Figure 11 represents a wildcard.

Package layout

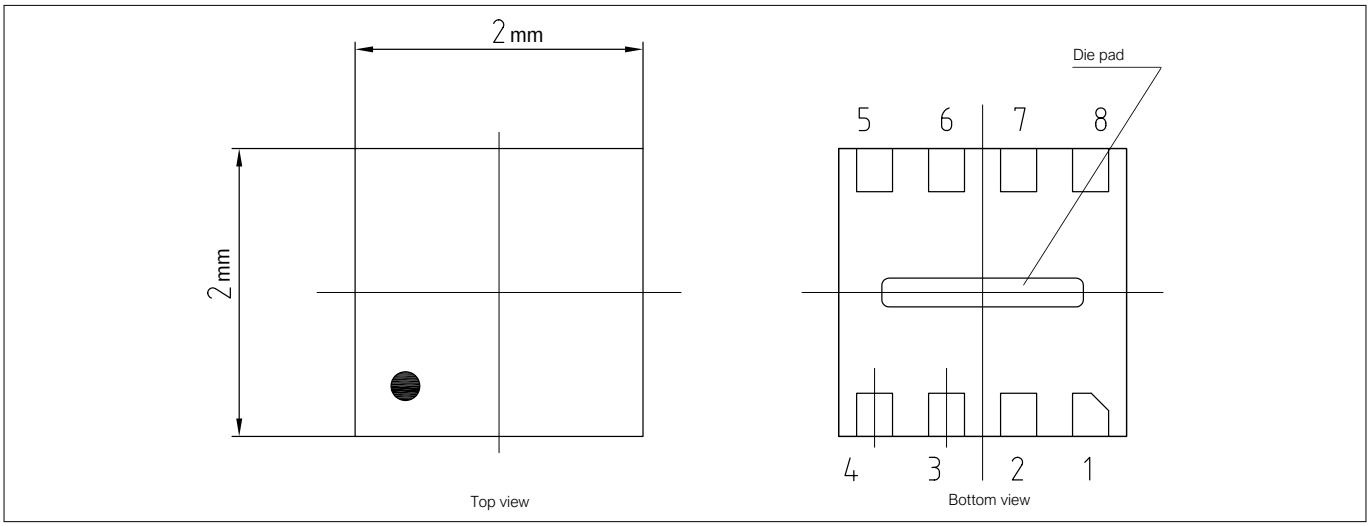

Figure 12 PG-USON-8-8 package layout

***Note**: It is recommended to connect the exposed die pad to the common ground reference (GND) for heat distribution.*

Pin-to-signal reference

Table 3 Pin-to-signal reference for PG-USON-8-8

Pin	Symbol	Pin configuration	Signal function/remarks
1	GND	GND	Power supply: Common ground reference
2	L_A	Contactless	Antenna connection: Contactless usage
3	SDA	I/O	I2C interface: Data line
4	NC	-	No internal connection
5	IRQ	Output	Interrupt: The respective output function can be configured
6	SCL	Input	I2C interface: Clock line
7	L_B	Contactless	Antenna connection: Contactless usage
8	V_{CC}	PWR	Power supply: Power and pad supply (V_{CC})

3.2 RoHS compliance

On January 27, 2003 the European Parliament and the council adopted the directives:

- 2002/95/EC on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment ("RoHS")
- 2002/96/EC on Waste Electrical and Electronic Equipment ("WEEE")

Some of these restricted (lead) or recycling-relevant (brominated flame retardants) substances are currently found in the terminations (e.g. lead finish, bumps, balls) and substrate materials or mold compounds.

The European Union has finalized the Directives. It is the member states' task to convert these Directives into national laws. Most national laws are available, some member states have extended timelines for implementation. The laws arising from these Directives have come into force in 2006 or 2007.

The electro and electronic industry has to eliminate lead and other hazardous materials from their products. In addition, discussions are on-going with regard to the separate recycling of certain materials, for example plastic containing brominated flame retardants.

Infineon is fully committed to giving its customers maximum support in their efforts to convert to lead-free and halogen-free[1)] products. For this reason, Infineon's "Green Products" are ROHS-compliant.

Since all hazardous substances have been removed, Infineon calls its lead-free and halogen-free semiconductor packages "green." Details on Infineon's definition and upper limits for the restricted materials can be found here.

The assembly process of our high-technology semiconductor chips is an integral part of our quality strategy. Accordingly, we will accurately evaluate and test alternative materials in order to replace lead and halogen so that we end up with the same or higher quality standards for our products.

The use of lead-free solders for board assembly results in higher process temperatures and increased requirements for the heat resistivity of semiconductor packages. This issue is addressed by Infineon by a new classification of the Moisture Sensitivity Level (MSL). In a first step the existing products have been classified according to the new requirements.

1 Any material used by Infineon is PBB and PBDE-free. Plastic containing brominated flame retardants, as mentioned in the WEEE directive, will be replaced if technically/economically beneficial.

3 Delivery forms

4 Hardware details

The OPTIGA™ Authenticate NBT includes a contactless passive NFC interface and an I2C target interface for connecting to an I2C controller (host MCU). The interfaces are configurable and support following features.

I2C interface:

- Target interface, 7-bit address, initial value: 18_H
- Supported clock frequencies:
  - Standard mode (SM) 100 kHz
  - Fast mode (FM) 400 kHz
  - Fast mode plus (FM+) 1000 kHz
- Protocol: GlobalPlatform T=1' I2C [8] and [9]

NFC interface:

- 7-byte UID (fixed, programmed during manufacturing at Infineon)
- ISO/IEC 14443-4 Type A [2]
- Data rate: Up to 848 kbit/s
- Frame size: 255 bytes
- WTX handling enabled
- Chaining supported
- NFC Forum Type 4 Tag compliant (see Chapter 2.3)

IRQ line:

- Configurable behavior depending on the mode of operation
  - Wake-up signal for host system
  - Indicating NFC state machine state transitions
  - Signaling I2C Data transfer
  - Initiating pass-through mode

4.1 Technical data

This section provides a brief overview of the absolute maximum ratings and operational characteristics of the OPTIGA™ Authenticate NBT. These include electrical AC and DC characteristics, interface characteristics and package characteristics.

***Notes**:*

1. *T_A as given for the operating temperature range of the device unless otherwise stated*

2. *All currents flowing into the device are considered positive*

4.1.1 Absolute maximum ratings

This section defines the absolute maximum ratings. Stresses exceeding the values listed in Table 4 may permanently damage the device. This is only a stress rating; functional operation of the device under these or any other conditions with values greater than those specified in the operational characteristics sections of this specification is not implied. Long-term exposure to absolute maximum rating conditions may have an impact on device reliability, including NVM data retention and programming endurance.

Table 4 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Operating temperature, ambient	T_A	-25	-	+85	°C	T_J (max) must not be exceeded
Operating temperature, ambient, extended range, no NFC field available	$T_{A\_EXT\_NONFC}$	-40	-	+105	°C	T_J (max) must not be exceeded; maximum depends on PCB design and operating conditions
Operating temperature, ambient, extended range, NFC field available	$T_{A\_EXT\_NFC}$	-40	-	+85	°C	T_J (max) must not be exceeded
Junction temperature	T_J	-	-	+110	°C	T_J (max) must not be exceeded
Supply voltage	V_{CC}	-0.3	-	4.6	V	
Input voltage SDA, SCL, IRQ	$V_{IN\_I2C\_IRQ}$	-0.3	-	V_{CC} + 0.3 or 4.6	V	
Input voltage (L_A - L_B)	V_{IN_LALB}	-6.0	-	+6.0	V	Maximum peak-to-peak amplitude of the AC input voltage at conditions of the "Alternating magnetic field" as per ISO/IEC14443-1 [1]
Input current (L_A - L_B)	I_{IN_LALB}	-	-	+/-150	mA	Maximum peak-to-peak amplitude of the AC input voltage at conditions of the "Alternating magnetic field" as per ISO/IEC14443-1 [1]
ESD robustness SDA, SCL, IRQ	$V_{ESD\_I2C\_IRQ,HBM}$	4000	-	-	V	Human body model
ESD robustness SDA, SCL, IRQ	$V_{ESD\_I2C\_IRQ,CDM}$	750	-	-	V	Charge device model
ESD robustness L_A, L_B	$V_{ESD\_LALB,HBM}$	3000	-	-	V	Human body model
ESD robustness L_A, L_B	$V_{ESD\_LALB,CDM}$	750	-	-	V	Charge device model
ESD robustness L_A, L_B against SDA, SCL, IRQ	$V_{ESD\_LALB\_I2C\_IRQ,HBM}$	2000	-	-	V	Human body model
ESD robustness L_A, L_B against SDA, SCL, IRQ	$V_{ESD\_LALB\_I2C\_IRQ,CDM}$	750	-	-	V	Charge device model
NVM data retention		10	-	-	Years	T_A = 25°C
NVM cycle endurance		200.000	-	-	Cycles	per NVM block[1)]

(table continues...)

Table 4 (continued) Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Storage temperature	T_S	+5	-	+40	°C	Infineon-originally packed, 10..75% humidity, up to 36 months. Condensation and bedewing shall be avoided

1) NVM blocks are not individually addressable with APDUs

4.1.2 Operational characteristics

This section specifies the AC and DC characteristics of the OPTIGA™ Authenticate NBT, as well as details about the specific interfaces provided by the device.

4.1.2.1 AC electrical characteristics

This section describes the AC electrical characteristics of the device.

Table 5 AC electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
V_{CC} ramp-up time	t_{VCCR}	2 *1)*	-	-	µs	0 to 100% of V_{CC} target voltage ramp
Device start-up time V_{CC} powered	$t_{STARTUP\_VCC}$	-	1	-	ms	T_A = +25°C Defines the time from power-on (V_{CC} ≥ 1.62 V) to STANDBY mode
Device start-up time NFC field powered	$t_{STARTUP\_NFC}$	-	420	-	µs	T_A = +25°C Class-5 reference antenna, resonance frequency: 13.8 MHz
Contactless interface initialization time	t_{INIT_NFC}	-	150	-	µs	T_A = +25°C Device is V_{CC} powered, NFC interface initialization time until it is ready for communication

1) At a faster supply ramp-up time the device internal ESD elements cause temporarily a cross current between V_{CC} and GND

Power-up considerations

The ramp-up times in Table 5 are based on the assumption of a linear voltage rise from 0% to 100% of the target voltage level. However, due to the possibility of current spike effects, it is recommended to follow the voltage characteristics shown in the figure below.

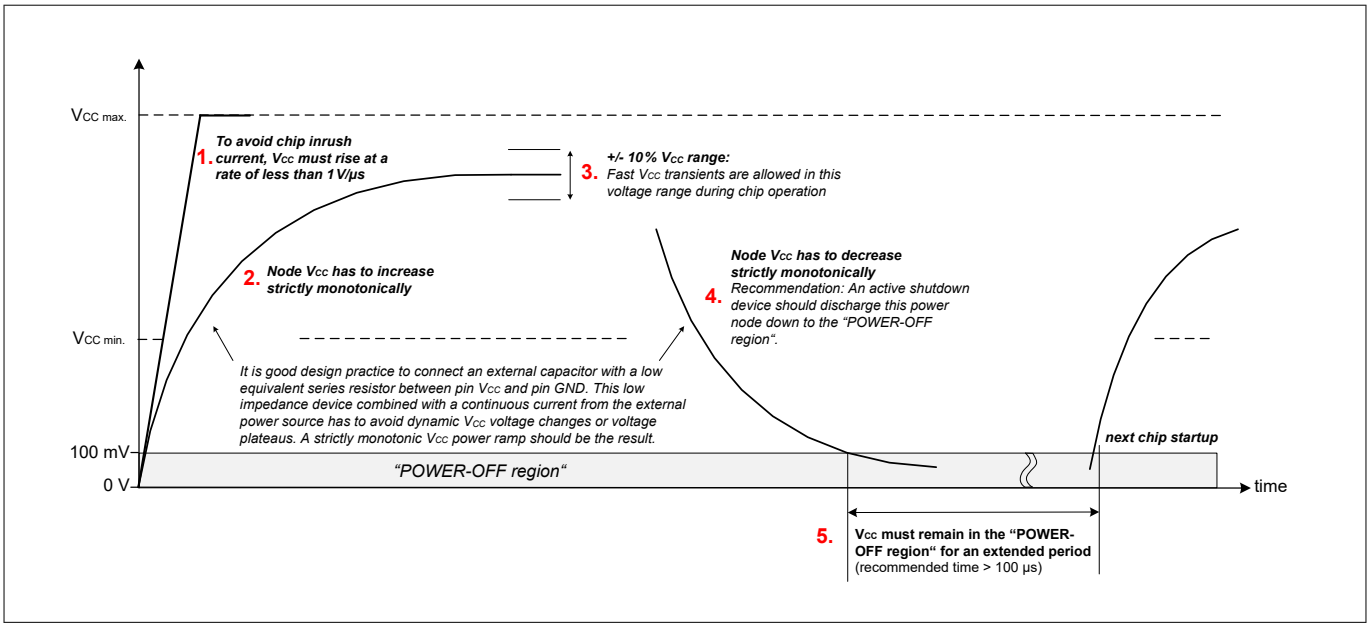

Figure 13 Recommended power-up behavior

Device start-up

After a power-on reset, the device starts by executing a boot initialization sequence before entering STANDBY mode. At the end of the start-up, the pins are re-configured for the use as I2C interface and IRQ.

Prior to re-configuration, the pins are in the hardware reset state:

- SCL and SDA: Input is enabled, output is disabled (SDA), and internal weak pull-up is enabled
- IRQ: Input is enabled, output is disabled[2)]

After the device start-up:

- SCL and SDA pins are reconfigured for I2C operation to open drain and the internal pull-up is disabled
- The IRQ pin is reconfigured to act as output (push-pull)

Figure 14 depicts the device start-up behavior and the corresponding basic timings and average currents.

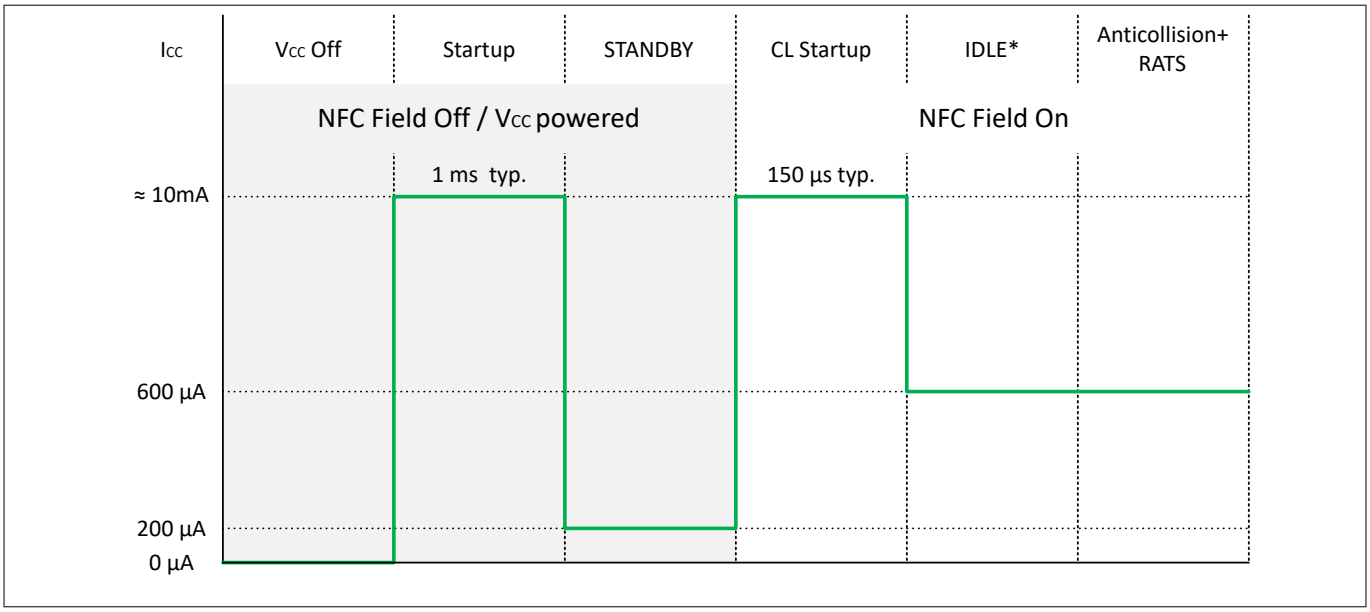

Figure 14 Device start-up behavior

2 The host system and/or external circuitry must keep the IRQ static (0 or 1) during $t_{STARTUP\_VCC}$

4.1.2.2 DC electrical characteristics

This section describes the DC electrical characteristics of the device.

Table 6 DC electrical characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.62	-	3.63	V	Overall functional range
Supply voltage operational	V_{CC_OP}	V_{CC_NOM} *0.9	-	V_{CC_NOM} *1.1	V	During device operation (all states, including STANDBY) the supply voltage must stay within this range around the nominal supply voltage V_{CC_NOM} Maximum operating voltage must stay below V_{CC_max}
Supply current, ACTIVE mode	I_{CC_ACTIVE}	-	10.1	-	mA	V_{CC} = 3.3 V, T_A= 25°C
Supply current, no NFC field available	I_{CC1}	-	9.9	-	mA	V_{CC} = 1.98 V, T_A= 25°C
Supply current, no NFC field available	I_{CC2}	-	10.3	-	mA	V_{CC} = 1.98 V, T_A= 105°C
Supply current, no NFC field available	I_{CC3}	-	10.0	-	mA	V_{CC} = 3.63 V, T_A= 25°C
Supply current, no NFC field available	I_{CC4}	-	10.4	-	mA	V_{CC} = 3.3 V, T_A= 105°C
Supply current, no NFC field available, current limitation enabled	I_{CC1_CURLIM}	-	4.2	-	mA	V_{CC} = 1.98 V, T_A= 25°C Current limitation = ON (default value: 06_H)
Supply current, no NFC field available	I_{CC2_CURLIM}	-	4.4	-	mA	V_{CC} = 1.98 V, T_A= 105°C Current limitation = ON (default value: 06_H)
Supply current, no NFC field available	I_{CC3_CURLIM}	-	4.3	-	mA	V_{CC} = 3.63 V, T_A= 25°C Current limitation = ON (default value: 06_H)
Supply current, no NFC field available	I_{CC4_CURLIM}	-	4.6	-	mA	V_{CC} = 3.63 V, T_A= 105°C Current limitation = ON (default value: 06_H)
Supply current IDLE mode, NFC	$I_{CC\_IDLE\_NFC}$	-	600	-	µA	V_{CC} = 3.3 V, T_A= 25°C
Supply current IDLE mode, I2C	$I_{CC\_IDLE\_I2C}$	-	600	-	µA	V_{CC} = 3.3 V, T_A= 25°C
Supply current STANDBY mode	$I_{CC\_STANDBY}$	-	-	200	µA	V_{CC} = 3.3 V, T_A= 25°C

4.1.2.3 NFC interface characteristics

The interface pads to an antenna coil are L_A and L_B. The resonance frequency of the serial resonance circuit depends on the input capacitance between L_A and L_B and with the coil inductance.

The voltage obtained at the device contacts is primarily defined by the following factors:

- The RF field strength and, together with the coil geometry, the resulting induced voltage
- The resonance frequency and
- The quality factor (mainly defined by the current consumption of the OPTIGA™ Authenticate NBT)

Table 7 NFC interface characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Maximum input current at (L_A - L_B), L_B	$I_{IN\_LALB\_OP}$	-	-	+/-90	mA	Maximum peak input current
L_A/L_B input capacitance	C_P	-	75.6	-	pF	Tolerance +/- 10% see Note

***Notes**:*

1. *Measurement conditions for L_A/L_B input capacitance:*
Threshold point: 2.8 V_{PEAK}, 13.56 MHz, RFI in reception mode (system in STANDBY mode), device operating on contactless power; bare die only (package details available on request, please contact Infineon Technologies).

2. *The parameter L_A/L_B input capacitance is not tested during production. Value ranges are based on measurements during qualification of the product at different technology corners.*

3. *Hints and guidelines for antenna design are available in the Antenna Design Guide document [13].*

4.1.2.4 I2C interface characteristics

The electrical characteristics of the I2C interface are given below.

4.1.2.4.1 General I2C characteristics

Table 8 I2C operational supply and input voltages

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Supply voltage	V_{CC}	1.62	-	3.63	V	V_{CC} to 3.3 V +10%
SDA, SCL input voltage	V_{IN_I2C}	-0.3	-	V_{CC} + 0.5	V	V_{IN_I2C} is the internal voltage domain for the I2C interface, which is internally connected to the V_{CC} pad
	$V_{IN\_I2C\_SWITCHED\ OFF}$	-0.3	-	0.5	V	V_{CC} is switched off. See Note

***Note**: The power supply of the OPTIGA™ Authenticate NBT must not be switched off as the device may drain significant pad input current.*

4.1.2.4.2 I2C standard/fast mode interface characteristics

The electrical characteristics of the I2C interface are in accordance with the I2C bus specification [16] for "standard-mode" (f_{SCL} up to 100 kHz), "fast-mode" (f_{SCL} up to 400 kHz), and "fast-mode plus" (f_{SCL} up to 1 MHz), with the exceptions listed in the tables below.

Table 9 I2C standard mode interface characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
SCL clock frequency	f_{SCL}	0	-	100	kHz	
Input low-level voltage	V_{IL}	-0.3	-	0.3*V_{CC}	V	
Input high-level voltage	V_{IH}	0.7*V_{CC}	-	V_{CC}+0.5	V	
Low-level output voltage	V_{OL1}	0	-	0.4	V	Sink current 3 mA; $V_{CC} \geq 2.7$ V Sink current 2 mA; $V_{CC} < 2.7$ V
Low-level output current	I_{OL}	3 2	-	-	mA	$V_{OL} = 0.4$ V; $V_{CC} \geq 2.7$ V $V_{OL} = 0.4$ V; $V_{CC} < 2.7$ V
Output fall time from V_{IHmin} to V_{ILmax} (at device pin)	t_{OF}	-	-	250	ns	$C_b \leq 400$ pF; $V_{CC} \geq 2.7$ V $C_b \leq 200$ pF; $V_{CC} < 2.7$ V
Hold time for START (S, Sr) condition	$t_{HD;STA}$	4	-	-	µs	
SCL low period	t_{LOW}	4.7	-	-	µs	
SCL high period	t_{HIGH}	4.0	-	-	µs	
Setup time for repeated START (Sr) condition	$t_{SU;STA}$	4.7	-	-	µs	
SDA hold time	$t_{HD;DAT}$	0	-	-	ns	
SDA input setup time	$t_{SU;DAT}$	250	-	-	ns	
SDA/SCL rise time (bus line)	t_r	-	-	1000	ns	
SDA fall time (bus line, input)	t_{fSDA}	-	-	300	ns	
SCL fall time (bus line, input)	t_{fSCL}	-	-	300	ns	
Setup time for STOP (P) condition	$t_{SU;STO}$	4.0	-	-	µs	

(table continues...)

Table 9 (continued) I2C standard mode interface characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Bus free time between STOP (P) and START (S) condition	t_{BUF}	4.7	-	-	µs	
SDA output valid time	$t_{VD;DAT}$	-	-	3.45	µs	
Input capacitance (package pin)	C_I	-	9	15	pF	
Capacitance load for each bus line	C_b	-	-	400 200	pF	$V_{CC} \geq 2.7$ V $V_{CC} < 2.7$ V

Table 10 I2C fast mode interface characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
SCL clock frequency	f_{SCL}	0	-	400	kHz	
Input low-level voltage	V_{IL}	-0.3	-	$0.3*V_{CC}$	V	
Input high-level voltage	V_{IH}	$0.7*V_{CC}$	-	$V_{CC}+0.5$	V	
Low-level output voltage	V_{OL1}	0	-	0.4	V	Sink current 3 mA; $V_{CC} \geq 2.7$ V Sink current 2 mA; $V_{CC} < 2.7$ V
Low-level output voltage	V_{OL2}	0	-	$0.2*V_{CC}$	V	Sink current 2 mA; $V_{CC} \leq 2$ V
Low-level output current	$I_{OL(0.4)}$	3 2	-	-	mA	$V_{OL} = 0.4$ V; $V_{CC} \geq 2.7$ V $V_{OL} = 0.4$ V; $V_{CC} < 2.7$ V
Output fall time from V_{IHmin} to V_{ILmax} (at device pin)	t_{OF}	-	-	250	ns	$C_b \leq 400$ pF; $V_{CC} \geq 2.7$ V $C_b \leq 200$ pF; $V_{CC} < 2.7$ V
Output fall time from V_{IHmin} to V_{ILmax} (at device pin)	t_{OF}	$20*V_{CC}/5.5$ V	-	250	ns	$C_b = 400$ pF
Spikes suppressed by input filters	t_{SP}	-	-	50	ns	
Hold time for START (S, Sr) condition	$t_{HD;STA}$	0.6	-	-	µs	
SCL low period	t_{LOW}	1.3	-	-	µs	

(table continues...)

Table 10 (continued) I2C fast mode interface characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
SCL high period	t_{HIGH}	0.6	-	-	µs	
Setup time for repeated START (Sr) condition	$t_{SU;STA}$	0.6	-	-	µs	
SDA hold time	$t_{HD;DAT}$	0	-	-	ns	
SDA input setup time	$t_{SU;DAT}$	100	-	-	ns	
SDA/SCL rise time (bus line)	t_r	20	-	300	ns	
SDA fall time (bus line, input)	t_{fSDA}	-	-	300	ns	
SCL fall time (bus line, input)	t_{fSCL}	-	-	300	ns	
Setup time for STOP (P) condition	$t_{SU;STO}$	0.6	-	-	µs	
Bus free time between STOP (P) and START (S) condition	t_{BUF}	1.3	-	-	µs	
SDA output valid time	$t_{VD;DAT}$	-	-	0.9	µs	
Input capacitance (package pin)	C_I	-	9	15	pF	
Capacitance load for each bus line	C_b	-	-	400 200	pF	$V_{CC} \geq 2.7$ V $V_{CC} < 2.7$ V

4.1.2.4.3 I2C fast mode plus interface characteristics

The electrical characteristics of the I2C interface are in accordance with the I2C bus specification [16] for "fast mode plus" (f_{SCL} up to 1 MHz), with a few exceptions listed in the table below.

Table 11 I2C fast mode interface characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
SCL clock frequency	f_{SCL}	0	-	1	MHz	
Input low-level voltage	V_{IL}	-0.3	-	$0.3*V_{CC}$	V	
Input high-level voltage	V_{IH}	$0.7*V_{CC}$	-	$V_{CC}+0.5$	V	

(table continues...)

Table 11 (continued) I2C fast mode interface characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Low-level output voltage	V_{OL1}	0	-	0.4	V	Sink current 3 mA; $V_{CC} \geq 2.7$ V Sink current 2 mA; $V_{CC} < 2.7$ V
Low-level output current	I_{OL}	3 2	-	-	mA	$V_{OL} = 0.4$ V; $V_{CC} \geq 2.7$ V $V_{OL} = 0.4$ V; $V_{CC} < 2.7$ V
Output fall time from V_{IHmin} to V_{ILmax} (at device pin)	t_{OF}	-	-	120	ns	$C_b \leq 150$ pF
Spikes suppressed by input filters	t_{SP}	-	-	50	ns	
Hold time for START (S, Sr) condition	$t_{HD;STA}$	260	-	-	ns	
SCL low period	t_{LOW}	500	-	-	ns	
SCL high period	t_{HIGH}	260	-	-	ns	
Setup time for repeated START (Sr) condition	$t_{SU;STA}$	260	-	-	ns	
SDA hold time	$t_{HD;DAT}$	0	-	-	ns	
SDA input setup time	$t_{SU;DAT}$	50	-	-	ns	
SDA/SCL rise time (bus line)	t_r	-	-	120	ns	
SDA fall time (bus line, input)	t_{fSDA}	-	-	120	ns	
SCL fall time (bus line, input)	t_{fSCL}	-	-	120	ns	
Setup time for STOP (P) condition	$t_{SU;STO}$	260	-	-	ns	
Bus free time between STOP (P) and START (S) condition	t_{BUF}	500	-	-	ns	
SDA output valid time	$t_{VD;DAT}$	-	-	450	ns	
Input capacitance (package pin)	C_I	-	9	15	pF	
Capacitance load for each bus line	C_b	-	-	150	pF	

4.1.2.5 IRQ interface characteristics

The electrical characteristics of the OPTIGA™ Authenticate NBT's IRQ pin, including restrictions on maximum sink / source currents, are listed below.

Table 12 DC electrical characteristics of the IRQ

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Output low voltage	V_{OL}	-	-	0.3	V	I_{OL} = 1 mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 4 mA $V_{CC} \geq 2.7$ V
Output low current	I_{OL}	1	-	-	mA	V_{OL} = 0.3 V
Output low current	I_{OL}	4	-	-	mA	V_{OL} = 0.4 V $V_{CC} \geq 2.7$ V
Output high voltage	V_{OH}	V_{CC} – 0.3	-	-	V	I_{OL} = -1 mA
Output high voltage	V_{OH}	V_{CC} – 0.4	-	-	V	I_{OL} = -4 mA $V_{CC} \geq 2.7$ V
Output high current	I_{OH}	-1	-	-	mA	$V_{OH} = V_{CC}$ – 0.3 V
Output high current	I_{OH}	-4	-	-	mA	$V_{OH} = V_{CC}$ – 0.4 V $V_{CC} \geq 2.7$ V
Input capacitance	C_{IN_IRQ}	-	9	15	pF	Pad capacitance is subject to process variation and depending on supply voltage (increasing capacitance at lower supply)

***Note**: The power supply of the OPTIGA™ Authenticate NBT must not be switched off as the device may drain significant pad input current.*

Table 13 AC electrical characteristics of the IRQ

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Output signal rise time	t_r	-	4.5	15	ns	10% V_{CC} to 90% V_{CC} C_{LOAD} = 15 pF pull-up/pull-down: off no DC load
Output signal fall time	t_f	-	4.5	15	ns	90% V_{CC} to 10% V_{CC} C_{LOAD} = 15 pF pull-up/pull-down: off no DC load

4.1.2.6 Package characteristics

The overall thermal performance of a package in a system is generally characterized by junction-to-ambient thermal resistance chains. Typically, the application of the device defines the thermal requirements of the

system while the package type and outline defines the boundary conditions for implementing the thermal management on the PCB assembly.

Table 14 PG-USON-8-8 package characteristics

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Thermal resistance	$R_{th\text{-}ja}$	-	58.1	-	K/W	JEDEC 2s2p board and PG-USON-8-8 package; exposed die pad of package connected to common ground (GND) for heat distribution with two vias
Thermal resistance case to top of package	$R_{th\text{-}jCtop}$	-	96.4	-	K/W	Exposed die pad of PG-USON-8-8 package connected to common ground (GND) for heat distribution with two vias. See Figure 15
Thermal resistance pins and case to bottom of package	$R_{th\text{-}jpins\_Cbot}$	-	6.44	-	K/W	Exposed die pad of PG-USON-8-8 package connected to common ground (GND) for heat distribution with two vias. See Figure 15

Figure 15 shows the thermal equivalent circuit of the packaged device.

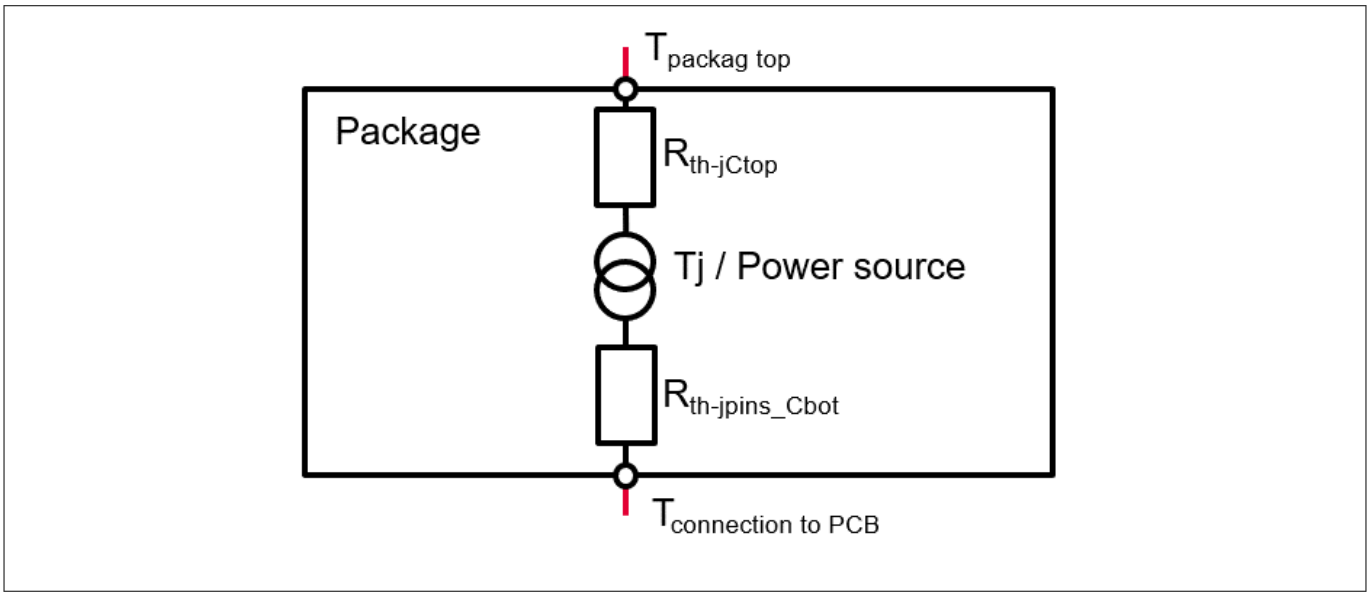

Figure 15 Package characteristics

References

ISO/IEC

[1] ISO/IEC 14443-1:2018: *Cards and security devices for personal identification - Contactless proximity objects - Part 1: Physical characteristics (Fourth edition)*; 2018-04
[2] ISO/IEC 14443-4:2018: *Cards and security devices for personal identification – Contactless proximity objects – Part 4: Transmission protocols (Fourth edition)*; 2018-06

NFC Forum

[3] NFC Forum: *Type 4 Tag Technical Specification (Version 1.2)*; 2022-08-16
[4] NFC Forum: *Analog Technical Specification (Version 2.3)*; 2023-02-03
[5] NFC Forum: *Digital Protocol Technical Specification (Version 2.3)*; 2021-08-03
[6] NFC Forum: *Activity Technical Specification (Version 2.3)*; 2023-02-03
[7] NFC Forum: *NFC Data Exchange Format (NDEF) Technical Specification (Version 1.0);* 2006-07-24

GlobalPlatform

[8] GlobalPlatform: *Card Specification (Version 2.3.1);* 2018-03
[9] GlobalPlatform: *APDU Transport over SPI/I2C (Version 1.0);*2020-01

Infineon

[10] Infineon Technologies AG: *OPTIGA™ Authenticate NBT, product website* - https://www.infineon.com/OPTIGA-Authenticate-NBT
[11] Infineon Technologies AG: *OPTIGA™ Authenticate NBT, Extended Datasheet (latest revision)*
[12] Infineon Technologies AG: *OPTIGA™ Authenticate NBT, Release Notes (latest revision)*
[13] Infineon Technologies AG: *OPTIGA™ Authenticate NBT, Antenna Design Guide (latest revision)*
[14] Infineon Technologies: *Package details PG-USON-8-8* - https://www.infineon.com/cms/en/product/packages/PG-USON/PG-USON-8-8/
[15] Infineon Technologies: *General recommendations for board assembly of Infineon packages* - https://www.infineon.com/dgdl/Infineon-Board_Assembly_Recommendations-General-Package-v05_00-EN.pdf?fileId=5546d4625cc9456a015ccaf4a1fe3a32

Inter-Integrated Circuit

[16] NXP Semiconductors: *I2C-bus specification and user manual (Revision 7.0);* 2021-10-01

Glossary

AC
alternating current (AC)

APDU
application protocol data unit (APDU)
The communication unit between a smart card reader and a smart card.

DC
direct current (DC)
A synonym for static parameters of an electronic circuit, for example defining supply voltages or currents. Its antonym would be dynamic parameters see also AC.

GND
ground (GND)

GP
GlobalPlatform (GP)

I2C
inter-integrated circuit (I2C)

IEC
International Electrotechnical Commission (IEC)
The international committee responsible for drawing up electrotechnical standards.

IRQ
interrupt request (IRQ)
A type of exception that breaks the linear flow of a program. The requesting module needs a software service routine to evaluate its current state and take the necessary actions.

ISO
International Organization for Standardization (ISO)

MCU
microcontroller unit (MCU)
One or more processor cores along with memory and programmable input/output peripherals.

NFC
near field communication (NFC)

PCB
printed circuit board (PCB)

SCL
serial clock line (SCL)

SDA
serial data line (SDA)

Glossary

UID

unique identifier (UID)

WTX

waiting time extension (WTX)
A waiting time extension request, available in the T=0 protocol. The smart card controller sends a 0x60 byte to the IFD, which in turn resets its timeout counter on this event.

Revision history

Reference	Description
Revision 2.1, 2024-04-26	
All	Editorial changes
Revision 2.0, 2024-03-28	
All	Major customer release
Revision 1.1, 2023-07-07	
All	Editorial changes
Revision 1.0, 2023-05-12	
All	Initial release

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CSSCustomerService@infineon.com

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