CoolSiC™ 400 V and 440 V G2 MOSFETs

Infineon's latest generation of SiC MOSFETs

About this document

Scope and purpose

This document introduces Infineon's newly released CoolSiC™ 400 V/440 V G2 silicon carbide (SiC) MOSFETs.

It introduces the new 400 V/440 V voltage class of SiC MOSFETs and their target applications. It also discusses the key technology parameters of these MOSFETs and how they provide system-level benefits for designers. Finally, the document provides application benchmarking in the major targeted topologies – addressing a wide range of applications.

Intended audience

This document is intended for design engineers, technicians, and developers of electronic systems.

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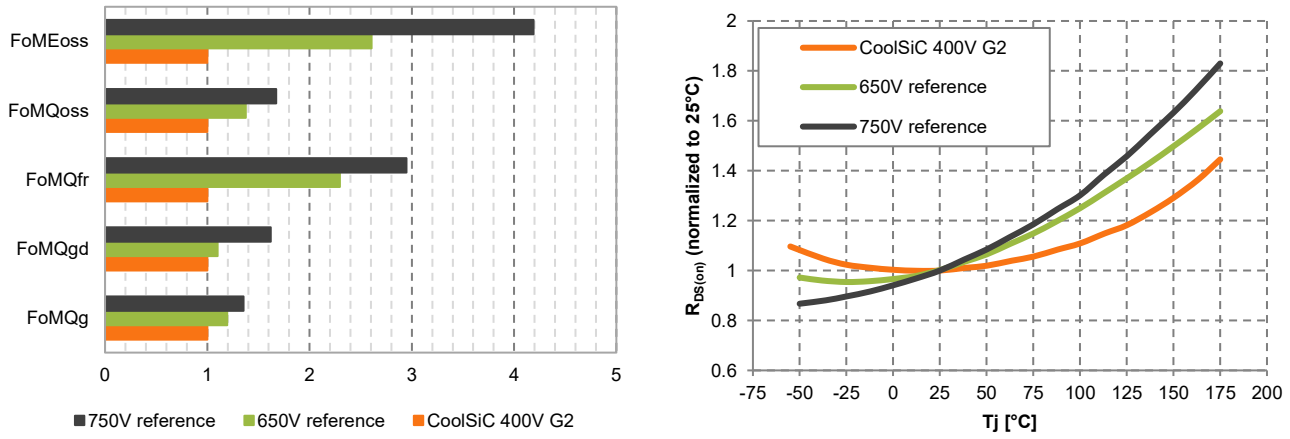
1 Introduction

Infineon's CoolSiC™ G2 400 V MOSFETs have been designed to bridge the gap between the newest generations of switching optimized 200 V Si trench MOSFETs and 600 V Si superjunction (SJ) MOSFETs – to address two-level topologies for bus voltages of up to 300 V_{dc} and enable the adoption of innovative three-level topologies for bus voltages of up to 600 V_{dc}.

Scaling up the 200 V Si trench MOSFETs or scaling down the 600 V Si SJ MOSFETs have resulted in compromises in the switching performance due to large and non-linear input-, output-, and reverse-capacitances, and higher reverse recovery charges. The optimization of CoolSiC™ G2 for a breakdown voltage of 400 V enables significant gains in switching figures of merit (FoM), as shown in Figure 1. These make them a perfect fit for hard-switching applications such as continuous conduction mode (CCM) totem-pole (TP) PFC, and soft-switching applications such as synchronous rectifiers. These devices help achieve the optimal system efficiency and power density, while maximizing the performance-to-cost ratio.



Note: Switching FoMs are defined at the typical operating voltages of each voltage class, namely V_{DS} = 200 V for 400 V SiC and V_{DS} = 400 V for 650 V SiC and V_{DS} = 500 V for 750 V SiC MOSFETs.

Figure 1 Switching and conduction FoM of CoolSiC™ G2 400 V MOSFETs

In hard-switching applications like CCM totem-pole, inverters, and buck/boost converters, the switching-related losses depend on:

- The output charge Q_{oss} of the hard-switching MOSFET and the complementary MOSFET
- Forward recovery charge Q_{fr} of the complementary MOSFET where the hard commutation of the body diode occurs
- Miller capacitance charge Q_{gd}
- Output energy E_{oss} of the hard-switching MOSFET

The substantial improvements in these switching FoM indicate the significant reduction in switching losses, achievable with multi-level topologies where the blocking voltages are reduced, compared to their 2-level counterparts.

In synchronous rectification applications like in the secondary side of a phase-shift full-bridge (PSFB) or dual-active bridge (DAB) DC-DC converters, where hard-commutation of the body diode under non-zero current switching (non-ZCS) condition occurs, the lower bipolar Q_{bip} (formerly denoted by reverse recovery charge, Q_{rr}) contribution to the forward recovery charge Q_{fr} helps mitigate the overshoots and ringing (EMI). In soft-switching applications like the primary side of an LLC or DAB DC-DC converter where zero-voltage switching occurs, the lower output charge Q_{oss} facilitates easier zero voltage switching conditions.

The temperature dependence of the on-state resistance $R_{DS(on)}$ is quite flat, with roughly an ~11% increase at junction temperature T_j = 100°C, which results in a consistent conduction loss profile throughout various load conditions. It also enables the use of higher $R_{DS(on)}$ parts with smaller parasitic capacitances and charges that improve the switching behavior and reduce switching losses. This is particularly important to consider when redesigning systems where legacy Si technologies are used, as the $R_{DS(on)}$ rise vs. junction temperature T_j for Si technologies is significantly steeper, and therefore, a CoolSiC™ 400 V MOSFET with a higher $R_{DS(on)}$ may be the right fit.

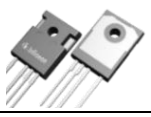
1.1 Portfolio

Table 1 and Table 2 show the released product portfolio in SMD and THD packages. The next sections of this document provide a short introduction to the key technology parameters and value propositions in various power electronics topologies for target applications such as AI, server, telecom, industrial SMPS, solar, energy storage system (ESS), and motor control, among many others. For more information on Infineon products, visit the webpage.

Table 1 CoolSiC™ G2 400 V/ 440 V MOSFETs portfolio in SMD packages

$R_{DS(on),typ}$ [mΩ]	TOLL w. Kelvin source	TOLL w. Kelvin source	D²PAK-7 w. Kelvin source	TOLT w. Kelvin source
				
45	IMT40R045M2H	–	IMBG40R045M2H	IMLT40R045M2H
36	IMT40R036M2H	–	IMBG40R036M2H	IMLT40R036M2H
25	IMT40R025M2H	IMT44R025M2H	IMBG40R025M2H	IMLT40R025M2H
15	IMT40R015M2H	IMT44R015M2H	IMBG40R015M2H	IMLT40R015M2H
11	IMT40R011M2H	IMT44R011M2H	IMBG40R011M2H	IMLT40R011M2H

Table 2 CoolSiC™ G2 400 V MOSFETs portfolio in THD packages

$R_{DS(on),typ}$ [mΩ]	TO247-3	TO247-4 w. Kelvin source
		
45	IMW40R045M2H	IMZA40R045M2H
36	IMW40R036M2H	IMZA40R036M2H
25	IMW40R025M2H	IMZA40R025M2H
15	IMW40R015M2H	IMZA40R015M2H
11	IMW40R011M2H	IMZA40R011M2H

2 Technology parameters

The new 400 V SiC MOSFET trench cell structure is based on the design of the higher voltage classes and is shown in Figure 2. It is an evolutionary next step to the higher voltage classes of Infineon's CoolSiC™ G2 family, with a reduced cell-pitch(1) and refined channel(2) properties, which help achieve significant improvement in device performance over the reference HV SiC MOSFET technologies. An enhanced control over the drift region(3) properties enables a more precise design of the device. Through meticulous optimization of the chip design, e.g., the junction termination, the active area loss has been minimized. This results in a 400 V SiC MOSFET technology that sets new standards for performance, reliability, and efficiency, enabling the development of innovative power electronic topologies and sustainable energy systems.

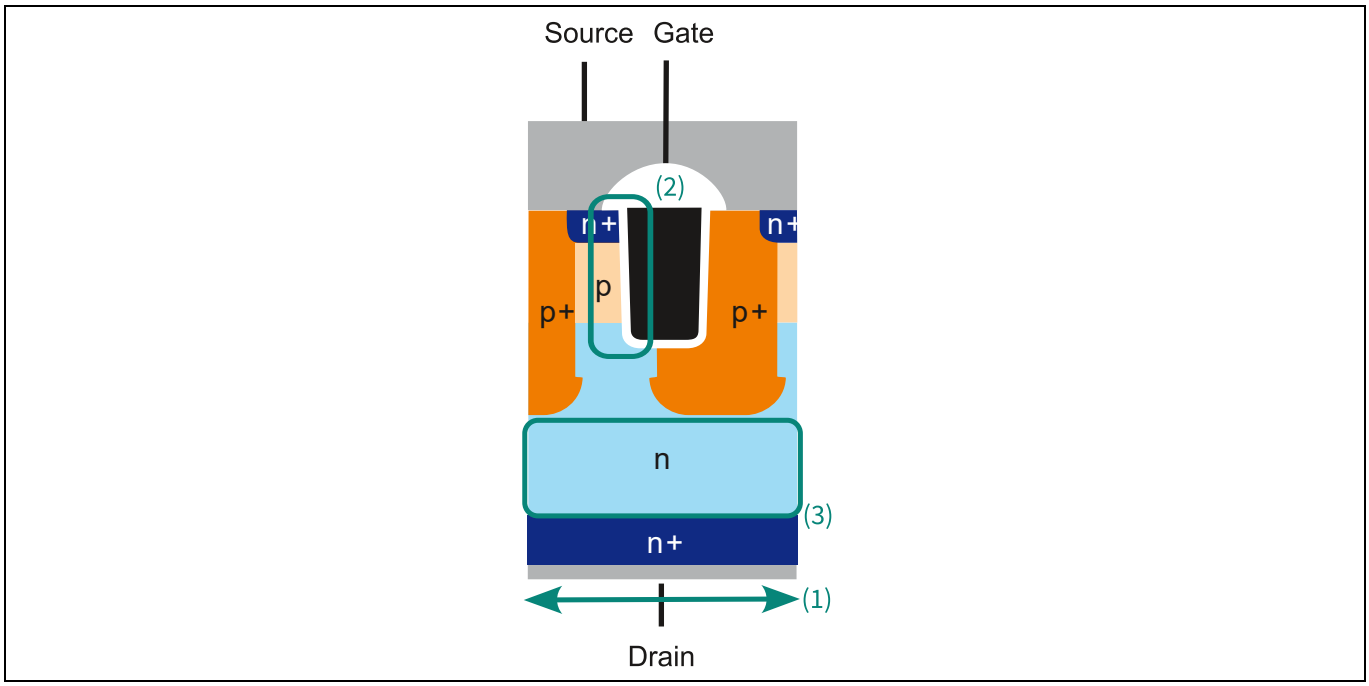


Figure 2 400 V SiC MOSFET cell structure showing (1) cell pitch, (2) channel, and (3) drift region

The important switching and conduction figures of merit (FoMs) are discussed earlier in Section 1. This section further describes the most important technology parameters and provides general recommendations for using CoolSiC™ G2 400 V MOSFETs.

2.1 Commutation robust body diode with low Q_{fr}

Note: CoolSiC™ G2 MOSFETs use a different nomenclature for the body diode recovery parameters compared to CoolSiC™ G1 MOSFETs. The old nomenclature of Q_{rr} alone does not fully explain the values from a standards perspective. Q_{rr} represents only the reverse recovery charge. During the reverse recovery charge measurement, Q_{oss} is also measured. It means that the value in the datasheet of Q_{fr} is the sum of Q_{oss} and Q_{rr}.

Figure 3 shows the hard commutation of the body diode at various temperature and load current conditions. The switching waveforms show negligible dependence on the operating temperature and load current. This shows the commutation robustness of the body diode due to the very low bipolar recovery charges during the forward recovery process.

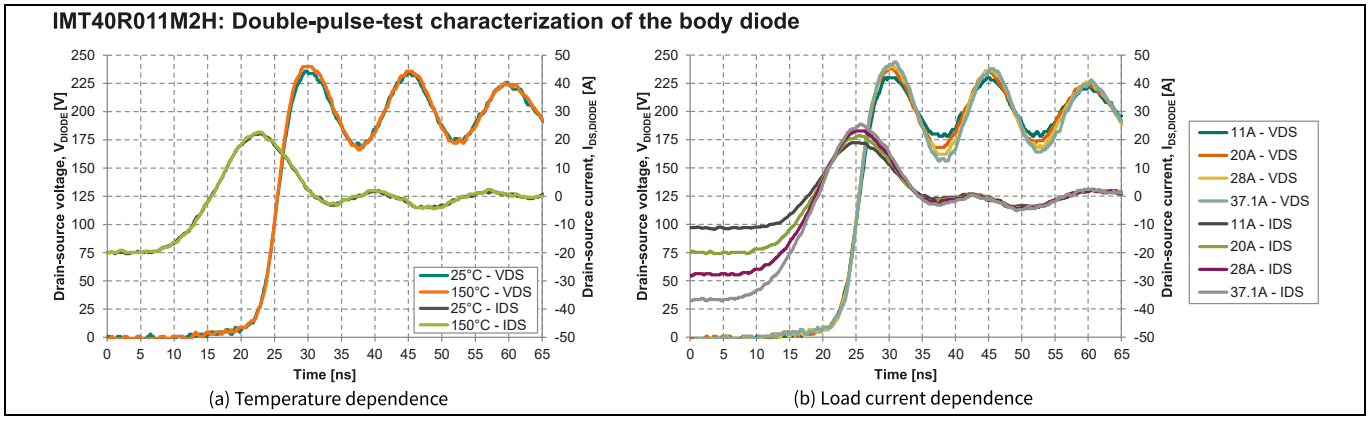


Figure 3 **Double pulse test showing hard commutation of the body diode at various (a) temperature and (b) load current conditions**

Compared to older Si technologies in the similar voltage class, between 250 V–300 V, significant improvements in the body diode's reverse recovery charge have been achieved, as shown in Figure 4.

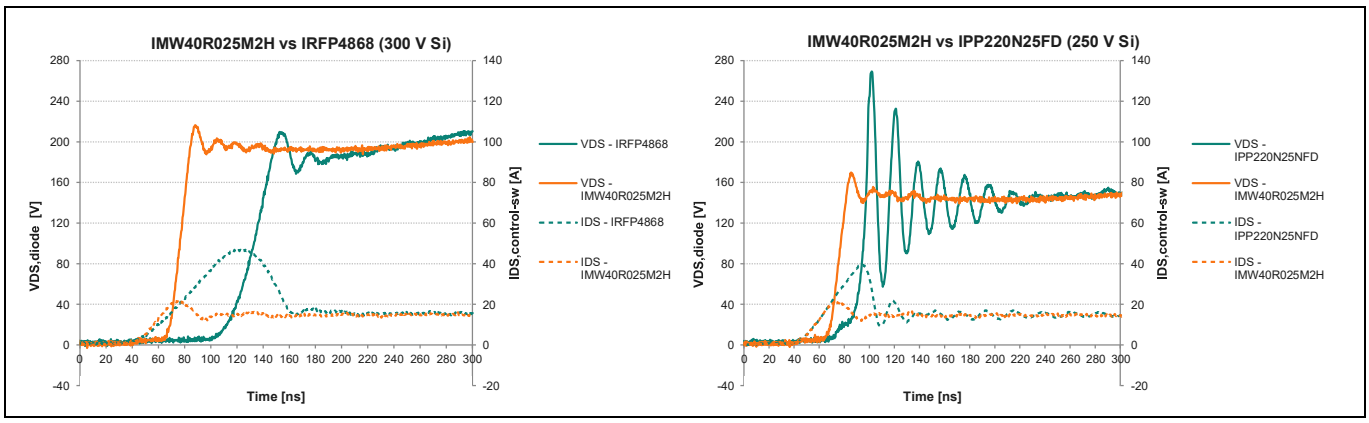


Figure 4 **Comparison of hard commutation of body diode between CoolSiC™ G2 400 V and older Si technologies in 250 V–300 V voltage class**

2.2 Transfer characteristics

The transfer characteristics provide information relevant to determine the driving capability of the CoolSiC™ G2 MOSFETs, as well as the ruggedness in the linear mode of operation, where the MOSFET is susceptible to thermal runaway. The crossing point between the 25°C (straight line) and 175°C (dashed line) lines is named the "thermal instability point". Below the thermal instability point, the MOSFET allows a higher current transfer at a higher temperature that can lead to thermal runaway in the application, depending on the applied gate source voltage. The lower the thermal instability point is located in the transfer characteristics, the more rugged it is in the linear mode of operation to avoid thermal runaway – resulting in an enhanced SOA.

For CoolSiC™ G2 400 V MOSFETs, the thermal instability point is at V_{GS} = ~12.2 V, which makes it fully compatible with 15 V gate driving. However, it is recommended to operate the device with a driving voltage of 18 V, as it provides an additional $R_{DS(on)}$ benefit of approximately 21%.

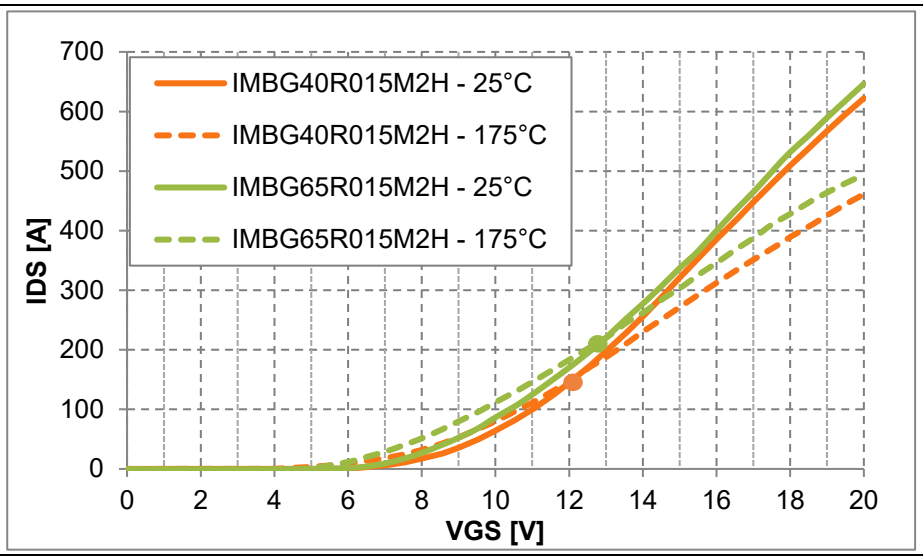


Figure 5 Transfer characteristics comparison: CoolSiC™ G2 400 V vs. 650 V reference MOSFETs

2.3 C_{oss}, C_{rss}, C_{iss} capacitances

The output capacitance C_{oss} has a major impact on the MOSFET's switching losses.

- It influences the required charge Q_{oss} to affect any change in the MOSFET drain-source voltage dV_{DS}/dt, thereby impacting the switching times and V_{DS}/I_{DS} overlap losses. The linearity of C_{oss} is also important not to only ensure clean and controllable switching waveforms with minimal overshoots, but also minimize the switching times and V_{DS}/I_{DS} overlap losses
- In a synchronously switching half-bridge cell, the $Q_{oss,SR}$ of the complementary synchronous rectifier MOSFET needs to be provided during the hard commutation of the body diode to raise the blocking voltage of the diode/SR. This additional $Q_{oss,SR}$-related current flows through the hard-switching control switch and therefore has a major impact on the hard-switching turn-on energy $E_{sw,on}$ of the MOSFET
- The energy stored in the output capacitance E_{oss} is dissipated in the channel during the hard switching turn-on

The reverse capacitance C_{rss} also has important effects on the switching behavior:

- It influences the so called "Miller plateau" region during hard-switching events and therefore the V_{DS}/I_{DS} overlap losses
- The charging/discharging of C_{rss} during any dV_{DS}/dt event injects a certain amount of current to the gate-source capacitance of the complementary SR MOSFET in a synchronous half-bridge, leading to potential Miller (C_{gd} x dV_{DS}/dt) induced parasitic turn-on

The input capacitance C_{iss} impacts the gate drive losses in the system. Figure 6, Figure 7, and Figure 8 show the capacitance characteristics of CoolSiC™ G2 400 V compared to the reference 650 V SiC MOSFET technology. The general behavior is similar, with the 400 V SiC MOSFETs showcasing slightly more linear characteristics.

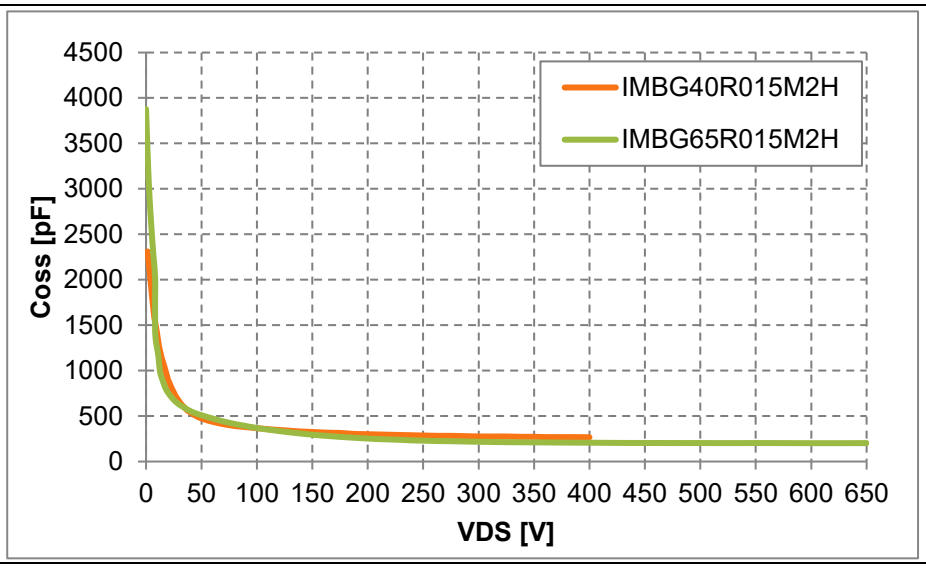


Figure 6 **Output capacitance comparison: CoolSiC™ G2 400 V vs. 650 V reference MOSFETs**

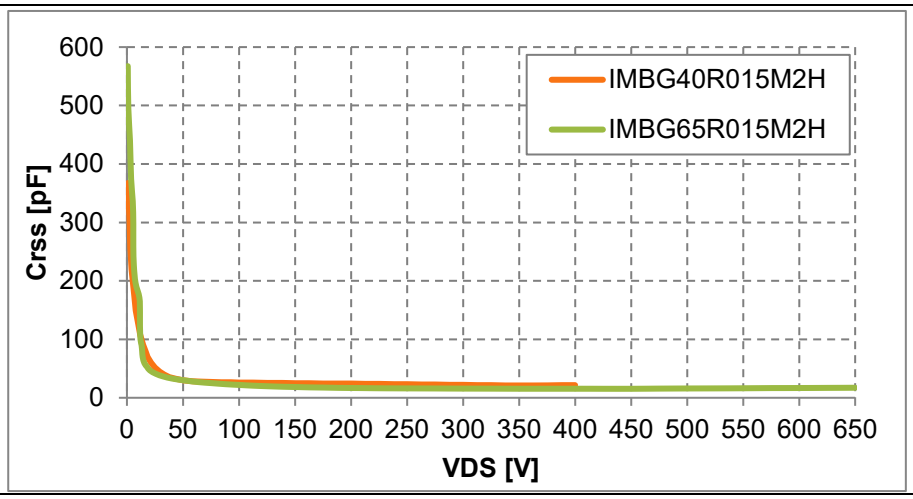


Figure 7 **Reverse capacitance comparison: CoolSiC™ G2 400 V vs. 650 V reference MOSFETs**

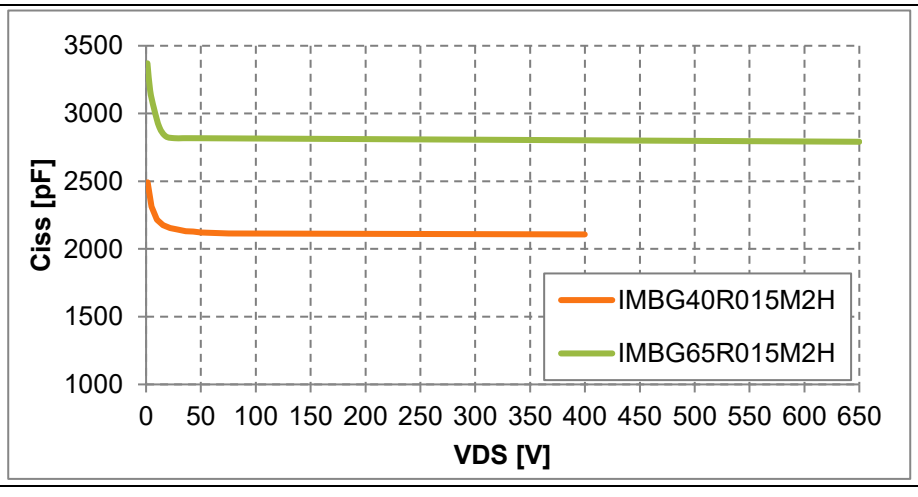


Figure 8 **Input capacitance comparison: CoolSiC™ G2 400 V vs. 650 V reference MOSFETs**

The E_{oss} and the Q_{oss} are derived by the C_{oss} using the following two equations:

$$E_{oss} = \int_0^{400\,V} C_{oss} \cdot V \; dV$$

$$Q_{oss} = \int_0^{400\,V} C_{oss} \cdot \frac{\mathrm{dV}}{\mathrm{dt}} \; \mathrm{d}t$$

Equation 1 **E_{oss} and Q_{oss} calculation**

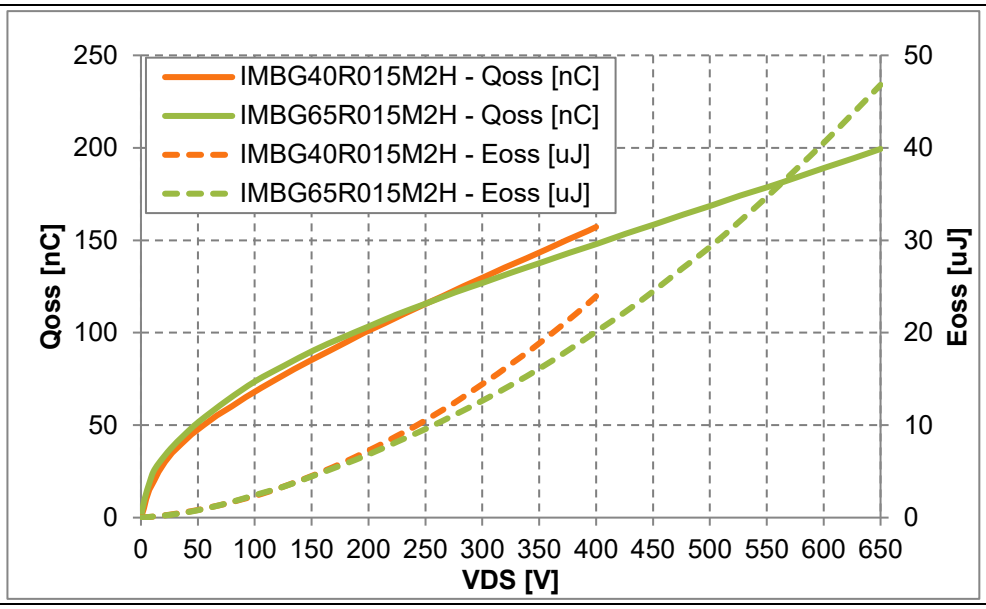


Figure 9 **E_{oss} and Q_{oss} comparison: CoolSiC™ G2 400 V vs. 650 V reference MOSFETs**

2.4 Q_G – gate charge

The gate charge is an indicator of how fast a device can be turned on and off. It also describes the charge needed to fully activate the device and provides an indicator for switching losses.

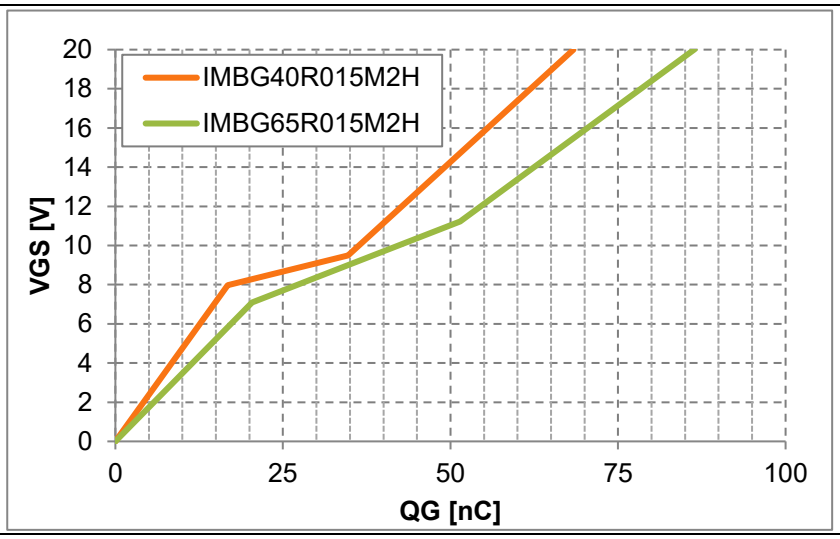
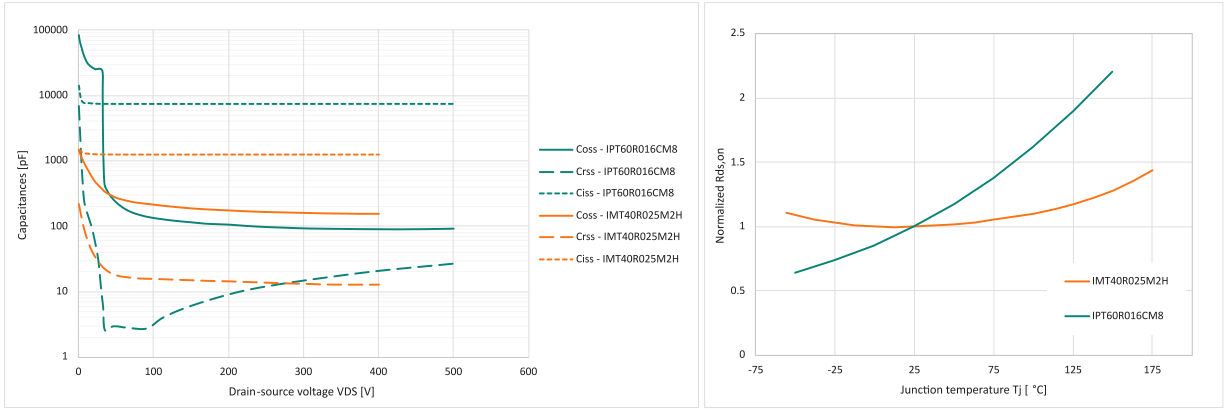


Figure 10 **Q_G comparison: CoolSiC™ G2 400 V vs. 650 V reference MOSFETs**

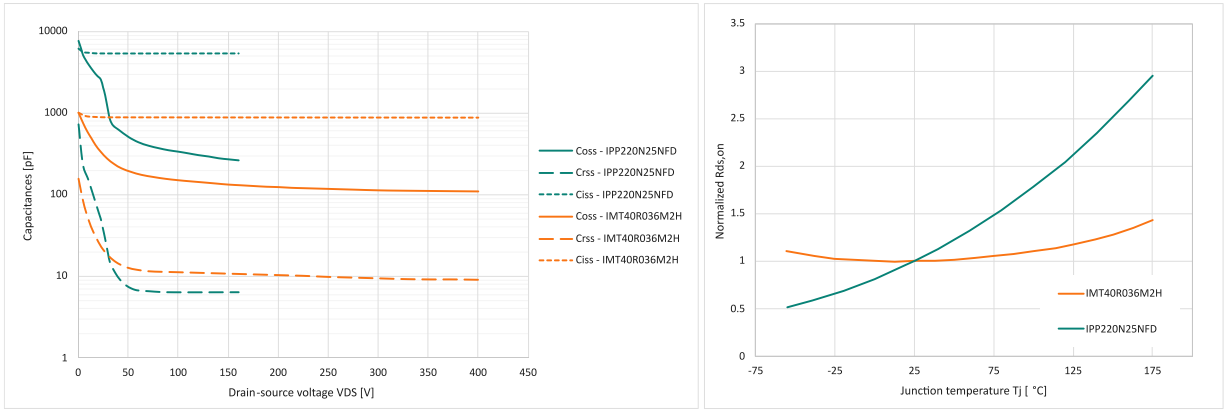
2.5 Positioning of CoolSiC™ G2 400 V between 200 V–600 V Si technologies

Figure 11 shows the benchmarking of key switching and conduction parameters of CoolSiC™ G2 400 V with CoolMOS™ 8 600 V and OptiMOS™ 3 250 V fast-diode (FD) technologies. The parts are chosen to have similar $R_{DS(on)}$ at T_j = 100°C.

The key conclusion is that CoolSiC™ G2 400 V MOSFETs exhibit linear and lower parasitic capacitances, which should provide better and faster switching characteristics with lower switching losses. The $R_{DS(on)}$ dependence on the temperature is also significantly lower for CoolSiC™ G2 400 V MOSFETs, leading to a stable loss profile as a function of load and enabling the choice of higher $R_{DS(on)}$ parts with lower parasitic capacitance to further reduce switching losses and improve efficiency.



(a) Benchmarking to CoolMOS™ 8 600 V



(b) Benchmarking to OptiMOS™ 3 FD 250 V

Figure 11 Benchmarking and positioning of CoolSiC™ G2 400 V vs. 250 V and 600 V Si MOSFETs

In summary, CoolSiC™ G2 400 V MOSFETs can be positioned in systems where a blocking voltage 150 V < $V_{DS,block}$ < 300 V is needed. Compared to 250 V–300 V Si technologies, it provides a performance benefit leading to a good cost-performance ratio. Compared to 500 V–650 V Si technologies, it provides cost and performance benefits and gives you the option to use a “right-fit” voltage class where a higher $V_{(BR)DSS}$ = 500 V–600 V rating is not required.

3 Gate driving

3.1 Flexibility in using Kelvin source and power source as reference

CoolSiC™ 400 V MOSFETs are offered in a 4-terminal configuration with a Kelvin source (KS) pin – also known as source Sense (SS) – which you can use as a reference for driving the gate. This helps decouple the power path and gate drive path by effectively excluding the common source inductance (CSI) from the gate drive path, as shown in Figure 12 (a).

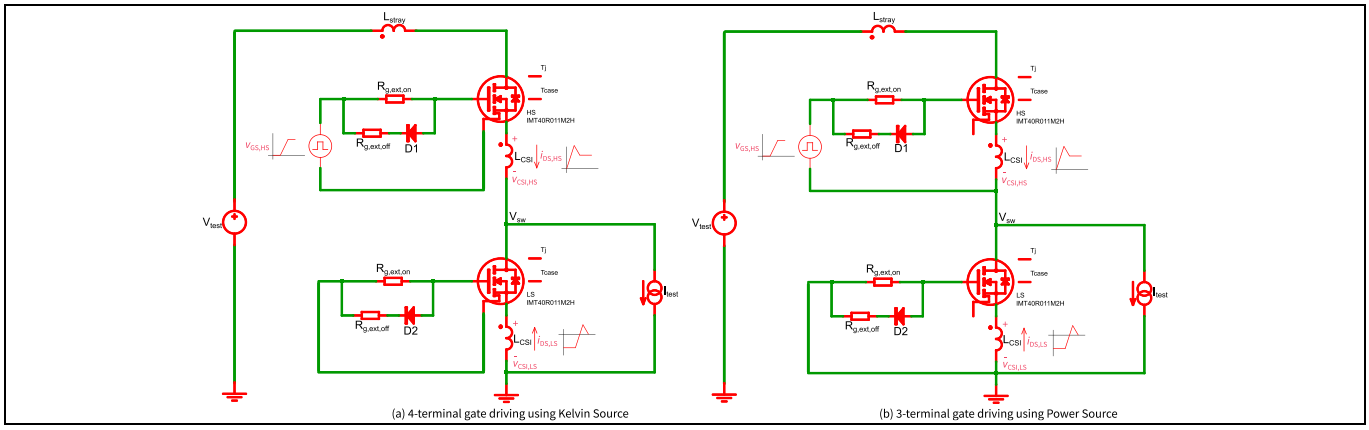


Figure 12 Gate driving using (a) Kelvin source (4-terminal) vs. (b) power source (3-terminal)

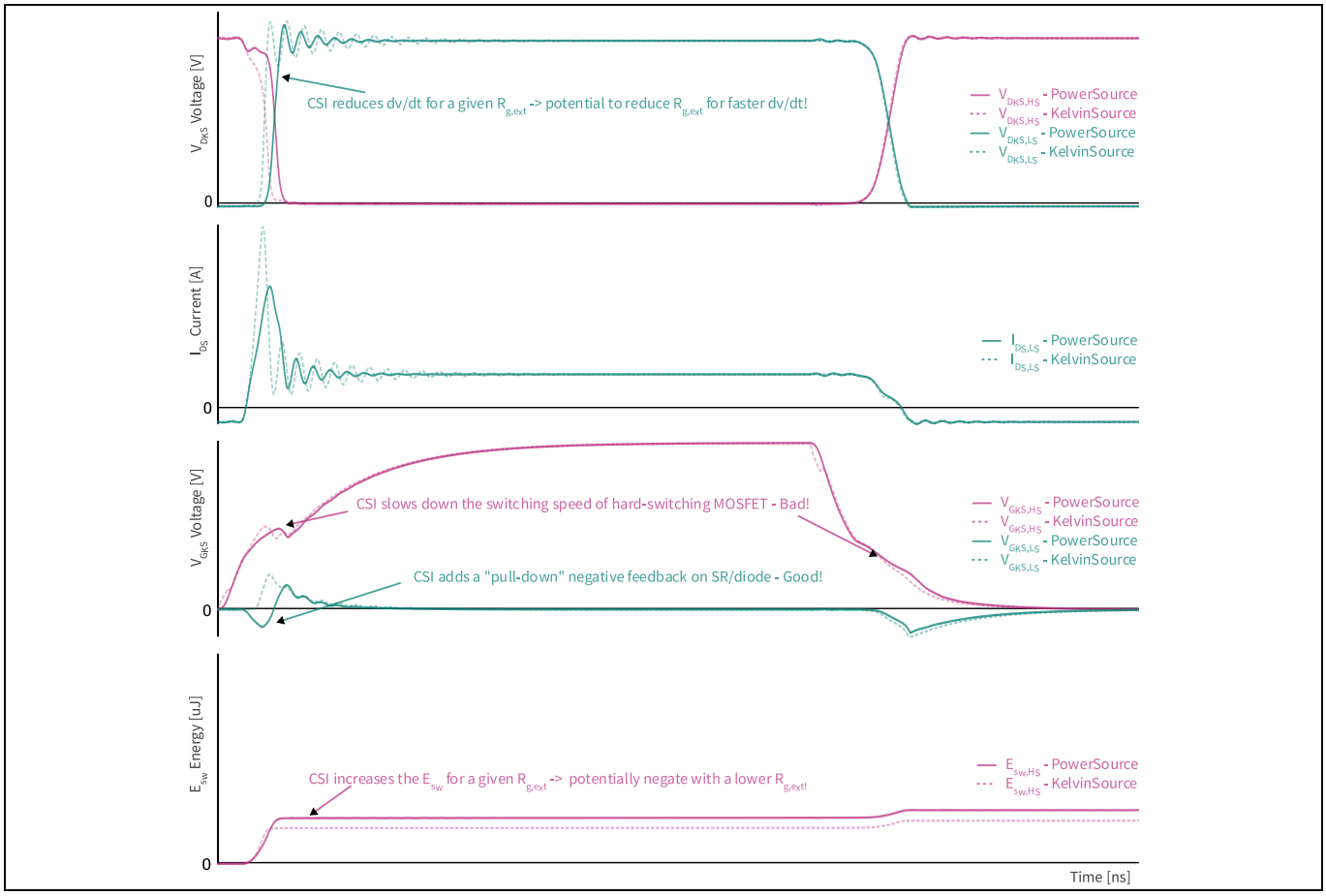


Figure 13 Illustrative switching waveforms showing the effect of CSI on hard-switching control switch and synchronous rectifier

The effect of CSI on the hard-switching control MOSFET and the complementary synchronous rectifier is shown in Figure 13 and discussed in [14]. For a given gate drive network ($R_{g,ext,on,off}$), the CSI slows down the switching speeds of the hard-switching control MOSFET during turn on and off, which increases the switching losses in the control FET. On the other hand, during the turn on of the control MOSFET and hard commutation of the body diode, the CSI adds useful "negative" feedback to the gate, which can help mitigate C_{GD} x dV_{DS}/dt Miller-induced parasitic turn-on, especially in cases where the pull down strength of the gate driver is insufficient.

Infineon's CoolSiC™ MOSFETs are offered in low-inductance packages like TOLL, where it may be beneficial to leverage the CSI and use power source reference for 3-terminal driving to tune the gate drive network impedance and control the switching behavior. This is shown in Figure 14 with half-bridge buck-mode measurements using a combination of Kelvin source and power source referenced driving and various $R_{g,ext}$.

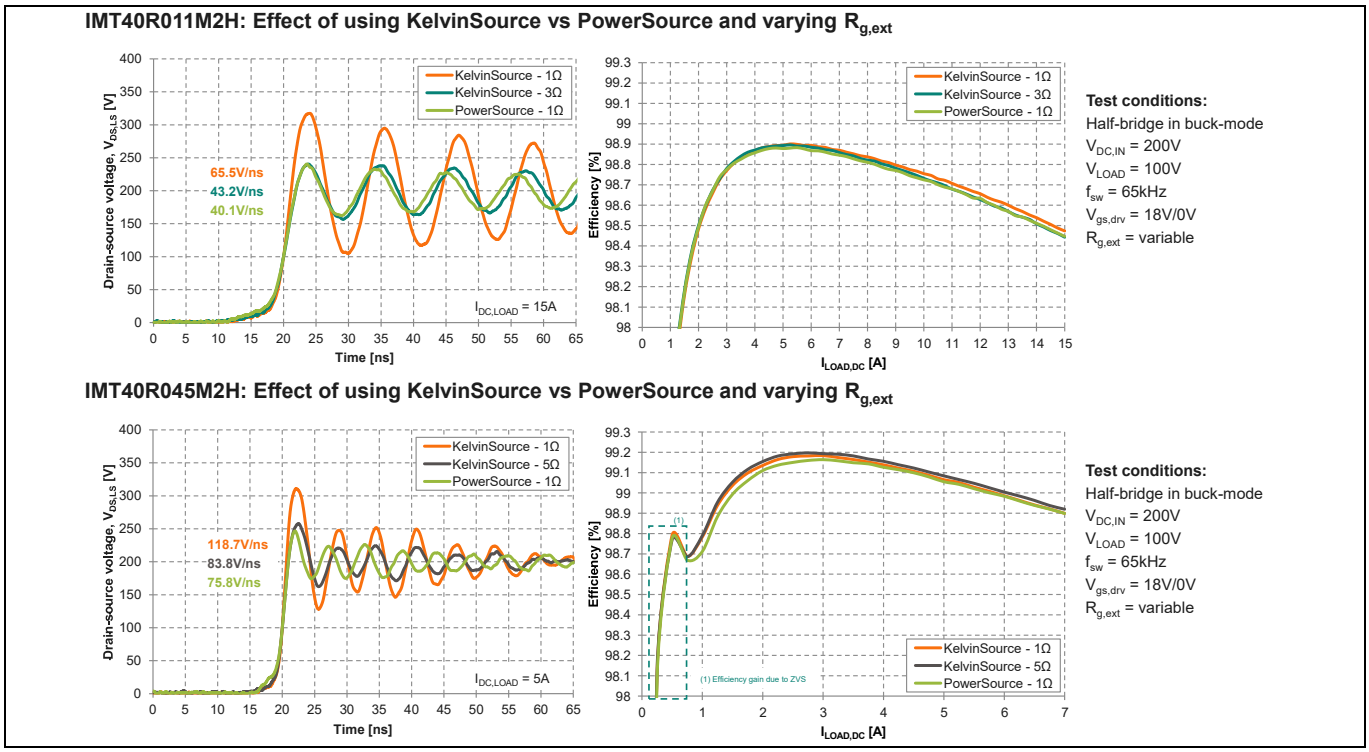


Figure 14 Flexible controllability of switching speeds using 4-terminal and 3-terminal gate driving

In summary, the choice of Kelvin source vs. Power source reference for the gate driving of CoolSiC™ G2 400 V MOSFETs should consider the following aspects:

- **With unipolar driving:**
  - For low-inductance packages like TOLL, it may be beneficial to evaluate 3-terminal gate driving with power source to use the CSI and tune the gate impedance network (e.g., by lowering $R_{g,ext}$) for the required switching speeds to utilize the "negative" feedback of CSI on synchronous rectifier MOSFETs. This is also demonstrated in reference designs [14], [17], and [1]
  - For high-inductance packages like TO247, 4-terminal gate driving with Kelvin source would likely provide optimal switching performance
- **With bipolar driving:**
  - For all packages, it is recommended to evaluate 4-terminal gate driving with Kelvin source to get the best switching performance

3.2 Gate driving voltage

As shown in Table 3, CoolSiC™ G2 400 V MOSFETs have an extended static and transient maximum rating for gate source voltage to allow a robust design with 80% derating, as recommended by the IPC9592-B standard even while using bipolar gate driving with 18 V/- 5 V.

Table 3 Maximum gate drive voltage ratings of CoolSiC™ G2 400 V enabling IPC 9592-B derating

Parameter	Symbol	Values			Unit	Note/test condition
		Min.	Typ.	Max.		
Gate source voltage (static)	$V_{GS,DC}$	-7	–	23	V	–
Gate source voltage (dynamic)	$V_{GS,AC}$	-10	–	25	V	$t_{pulse} \leq 500$ ns, duty cycle ≤ 1 %

The recommended gate driving voltage window during operation is shown in Table 4. Although it is possible to use +15 V turn-on gate voltage, it comes with a penalty of approximately a ~21% higher $R_{DS(on)}$ at datasheet-specified conditions. Therefore, to get the lowest $R_{DS(on)}$, it is recommended to use +18 V turn-on gate voltage. CoolSiC™ G2 MOSFETs fully support bipolar gate driving with negative gate turn-off voltages of -5 V–0 V, as covered in Section 3.2.1. This is especially beneficial to design circuits compatible with 2nd source SiC MOSFETs in the market that require bipolar driving.

In summary, unipolar driving with 18 V / 0 V for CoolSiC™ G2 400 V MOSFETs is recommended due to the simplicity of the gate driving and auxiliary supply circuits.

Table 4 Recommended gate drive voltages for CoolSiC™ G2 400 V MOSFETs

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Recommended turn-on voltages	$V_{GS(on)}$	15 (higher $R_{ds(on)}$; supported)	18 (lowest $R_{ds(on)}$; recommended)	–	V	–
Recommended turn-off voltages	$V_{GS(off)}$	-5 (higher complexity; supported)	0 (simpler; recommended)	–	V	–

3.2.1 Negative gate turn-off voltages with bipolar driving

Infineon's CoolSiC™ MOSFETs have a very low Miller ratio ($Q_{gd}/Q_{gs,th}$) and an industry-leading gate-threshold voltage ($V_{GS,th}$) which make them robust against $C_{gd} \times dV_{DS}/dt$ induced parasitic re-turn-on (PTO). Therefore, they do not need negative gate drive voltage for turn-off and show the best behavior regarding PTO in the market with unipolar gate driving (e.g., $V_{GS,on,off}$ = 18 V/0 V).

However, a lot of SiC MOSFETs in the market still require a negative turn-off voltage with bipolar gate driving (e.g., $V_{GS,on,off}$ = 18 V/-5 V). Therefore, to facilitate second sourcing, CoolSiC™ G2 MOSFETs have an improved gate oxide, enabling negative gate source voltage during turn-off and are fully compatible with bipolar gate driving. This results in an even easier-to-use and easier-to-drive CoolSiC™ G2 MOSFETs, which support both unipolar and bipolar gate driving.

Figure 15 shows the expected $R_{DS(on)}$ drift as a function of the number of switching stress cycles over the lifetime. It must be highlighted that there is still a positive $V_{GS,th}$ drift and a corresponding $R_{DS(on)}$ drift over the lifetime, as with all SiC MOSFETs available in the market. However, this $R_{DS(on)}$ impact is negligible, as shown in Figure 15 and in the following example for a typical hard-switched CCM TP PFC application profile [16].

- Operation lifetime (s): 1.577E+8 (5 years)
- Switching frequency (kHz): 65
- Cycle duration (s): 1/switching frequency = 0.0000154
- Number of cycles at the end of life: operational lifetime/cycle duration = ~1.025 E+13

For a gate drive voltage of +18 V/-5 V at 100°C, the expected $\Delta R_{DS(on)}$ is < 3%. This drift is within datasheet specifications, and has minimal impact on efficiency and performance at the system level.

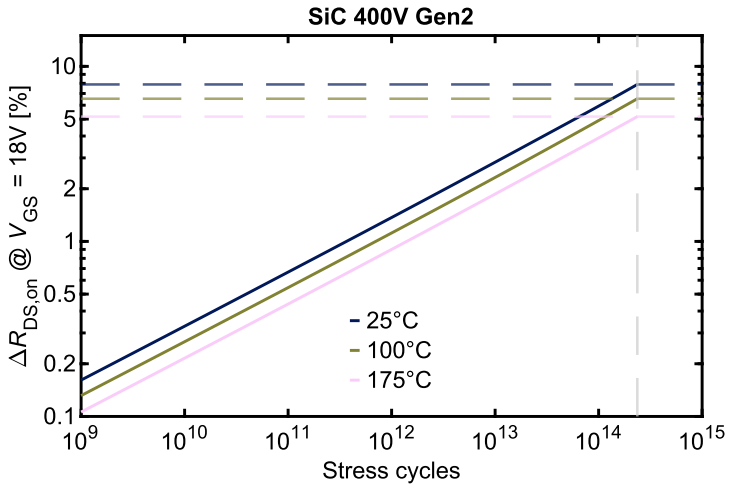


Figure 15 $R_{DS(on)}$ drift over lifetime

Furthermore, CoolSiC™ G2 400 V/440 V MOSFETs allow transient gate-source voltage peaks down to -10 V, leaving headroom for voltage peaks coming from high dV/dt or gate loop parasitic inductances from the PCB design.

3.3 Selection of gate driver ICs for CoolSiC™ 400 V–650 V MOSFETs

Infineon's family of EiceDRIVER™ gate driver ICs suitable to drive CoolSiC™ MOSFETs is shown in Figure 16.

	Product	N. channel	Package	Input-to-output isolation: Type	Input-to-output isolation: Rating	UVLO typ ON / OFF	VDD range	Output peak source / sink current[1]	CMTI (min.)	Propagation delay (typ.)	Propagation delay accuracy
	1EDN9550B 1EDN6550B	1-ch	SOT-23 6-pin	Non-isolated (1EDN-TDI)	CMR: ≤ ± 200 V_{DC} ≤ ± 400 V_{AC}	14.9 V / 14.4 V 12.2 V / 11.5 V	20V (22V max abs)	5 A / -9 A	n.a.	45 ns	-7 ns / +10 ns
	1EDB9275F 1EDB6275F	1-ch	DSO-8 150mil	Isolated (Functional / single protection)	V_{ISO} = 3 kV_{rms} (UL 1577)	14.9 V / 14.4 V 12.2 V / 11.5 V	20V (22V max abs)	5 A / -9A	300 V/ns	45 ns	-4 ns / +4 ns
	2EDB9259Y	2-ch	DSO-16 150mil	Isolated (Functional)	V_{ISO} = 3 kV_{DC} (UL 1577)	14.9 V/ 14.4 V	20V (22V max abs)	5 A / -9 A	150 V/ns	38 ns	-5 ns / +9 ns
	2EDR9259X 2EDR6259X 2EDR9258X 2EDR6258X	2-ch	DSO-16 300mil	Isolated (Reinforced)	V_{IOTM} = 8 kV_{pk} (VDE 0884-10) V_{ISO} = 5.7 kV_{rms} (UL 1577)	14.9 V/ 14.4 V 12.2 V/ 11.5 V 14.9 V/ 14.4 V 12.2 V/ 11.5 V	20V (22V max abs)	5 A / -9 A	150 V/ns	38 ns	-9 ns / +9 ns
	1ED3124MU12F 1ED3125MU12F	1-ch 1-ch, Miller Clamp	DSO-8 150mil	Isolated (Functional / single protection)	V_{ISO} = 3 kV_{rms} (UL 1577)	12.5 V / 10.5 V 12.5 V / 10.5 V	35V (40V max abs)	13.5 A / -14 A 10 A / -9 A	200 V/ns	90 ns	± 10 ns

For more information, visit Gate driver ICs

Figure 16 Infineon's EiceDRIVER™ gate driver ICs for CoolSiC™ MOSFETs

4 Target applications and topologies

CoolSiC™ G2 400 V MOSFETs are suitable for any application and topology that needs a typical drain-source blocking voltage of $V_{DS,typ}$ = 150 V–300 V. This new-generation technology is specifically ideal for various applications with continuous hard commutation on a conducting body diode. The following sections introduce some target applications that provide usage scenarios without limits for designers.

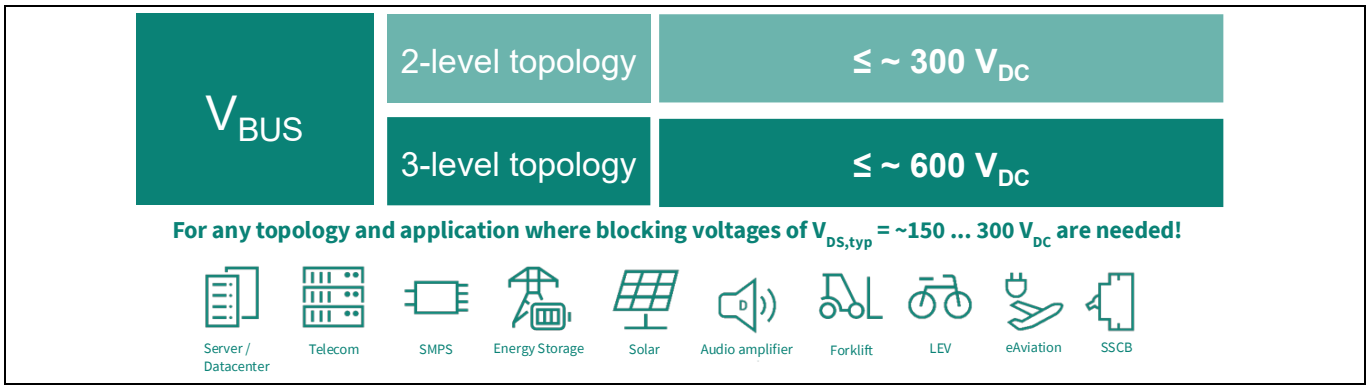


Figure 17 Positioning of CoolSiC™ G2 400 V MOSFETs for various applications and topologies

4.1 2-level and 3-level flying capacitor totem pole AC-DC PFC

For industrial applications with a nominal single-phase AC line voltage of 120 V_{ac} (e.g., in US and Japan) and rectified DC-link voltages up to 300 V_{dc}, CoolSiC™ G2 400 V can be used in two-level (2L) CCM TP PFCs. In such applications, which does not require 650 V voltage blocking capability, the CoolSiC™ G2 400 V MOSFETs offer all the advantages of using SiC wide bandgap (WBG) technology at a reduced price.

For AI servers, traditional datacenters and telecom applications with nominal single-phase AC line voltages ranging from 180 V–347 V_{ac} (e.g., in Canada) and rectified DC-link voltages ranging from 400 V–600 V_{dc}, CoolSiC™ G2 400 V MOSFETs enable the adoption of a novel three-level (3L) flying capacitor (FC) CCM TP topology for the highest performance in efficiency and power density.

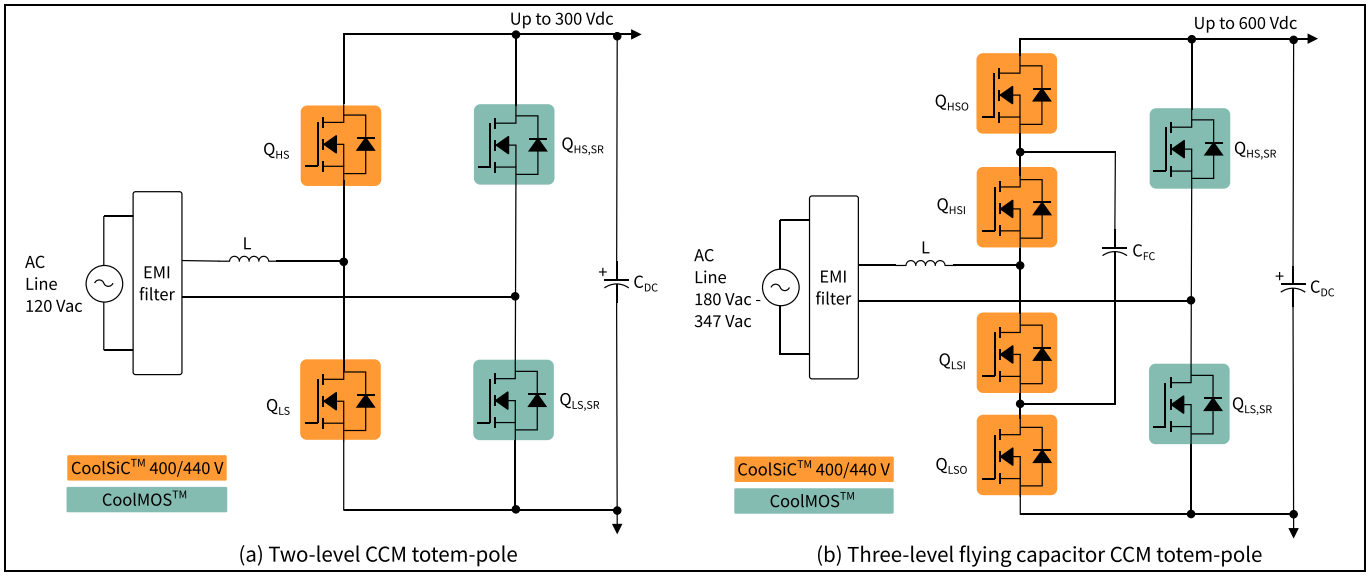


Figure 18 Application examples for CoolSiC™ G2 400 V/440 V: (a) two-level and (b) three-level bidirectional totem pole topology – depending on the AC voltage

Advantages of using CoolSiC™ G2 400 V in 3L flying capacitor CCM totem pole PFCs

- High-frequency leg MOSFETs block ~V_{DC}/2, enabling the usage of 400 V rated switches with better FoMs, effectively lowering the switching losses significantly
- Commutation robust body diode with a low Q_{fr} helps minimize body diode reverse recovery losses
- Lower voltage swing across the inductor (0.5 x factor) combined with the benefits of “series interleaving”, where the inductor ripple frequency is twice that of the HF leg MOSFET switching frequency, enables a significant reduction (0.25 x factor) in the required inductance value
- CCM mode results in a lower PFC inductor ripple current, leading to lower RMS currents and THD compared to CrCM or TCM modes. Additionally, the fixed-frequency operation simplifies the control and EMI filter designs

4.1.1 Fundamentals of 3L flying capacitor CCM TP PFCs

The 3L flying capacitor high-frequency switching cell can be simplified into two half-bridges – inner and outer – as shown in Figure 19. Each of them has a high-side (HS) and low-side (LS) MOSFET, which are switched with complementary PWM signals. The inner and outer leg PWM signals have a phase shift of 180° – leading to a “series interleaving” operation. At any given time, two MOSFETs conduct and two MOSFETs are in the blocking state, with the flying capacitor (charged to ~V_{DC}/2) ensuring the voltage stress of MOSFETs in blocking state is ~V_{DC}/2. This enables using lower voltage rated switches in the 3L FC switching cell with better FoMs and lower cost.

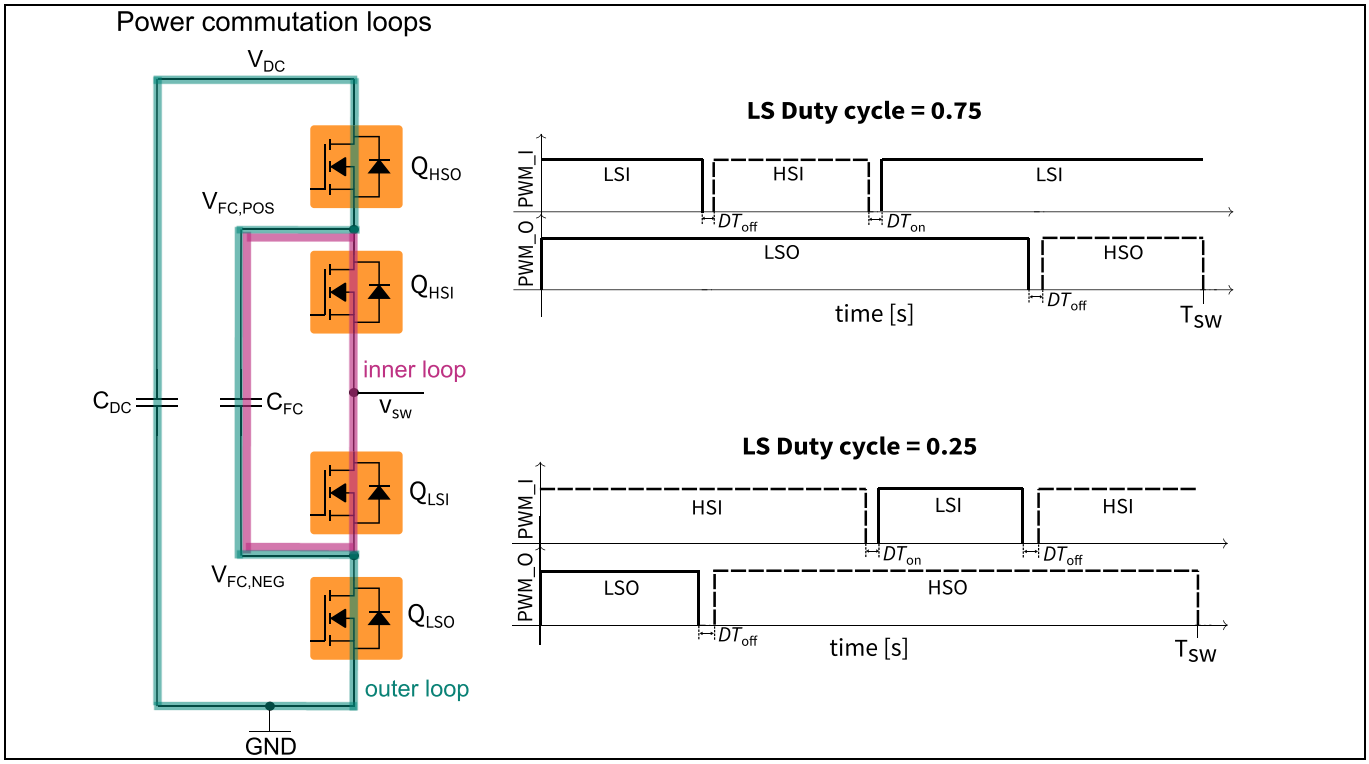


Figure 19 Simplified structure of the three-level flying capacitor high-frequency switching cell

A detailed representation of the PWM signals and operation modes in a 3L FC CCM TP PFC for boost PFC operation in positive AC-line cycle is shown in Figure 20. Some key details to highlight are:

- The switching node voltage V_{sw} can have three levels – (1) V_{DC}, (2) V_{FC} or $V_{DC} – V_{FC}$, and (3) 0 V (GND) – leading to the nomenclature “three-level” topology. Under all conditions, the flying capacitor voltage should be maintained around $V_{DC}/2$ with a voltage ripple of ΔV_{FC}
- The time period of the inductor current ripple is half that of the MOSFET switching period T_{sw}. This indicates the “frequency doubling” effect due to series interleaving operation. Effectively, the current ripple frequency of the inductor is twice the switching frequency of the MOSFETs
- In every switching cycle, the flying capacitor has a charging and discharging state of operation. By controlling the duration of these periods and ensuring a steady state balance of $Q_{charge} = Q_{discharge}$, the voltage of the flying capacitor can be regulated as discussed in [1], [2], and Section 5.1

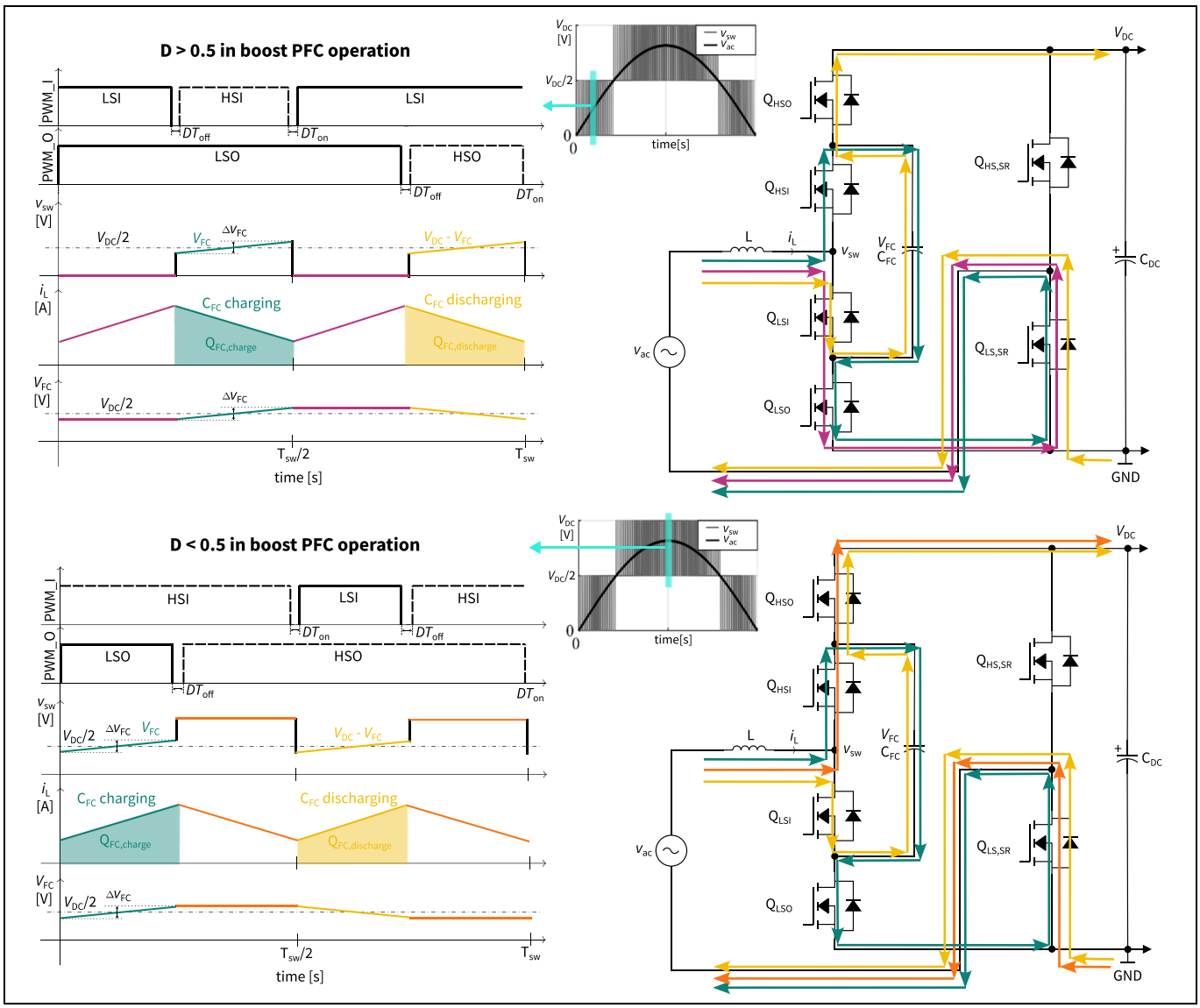


Figure 20 Idealized operational waveforms at D < 0.5 and D > 0.5 modes of operation in a 3L FC CCM TP PFC showing the conduction states and current paths for positive AC line cycle

4.1.2 Comparison of 3-level flying capacitor vs. 2-level CCM TP PFCs

Figure 21 shows the volt-seconds applied to the inductor by a 3-level flying capacitor switching cell compared to its conventional 2-level half-bridge counterpart.

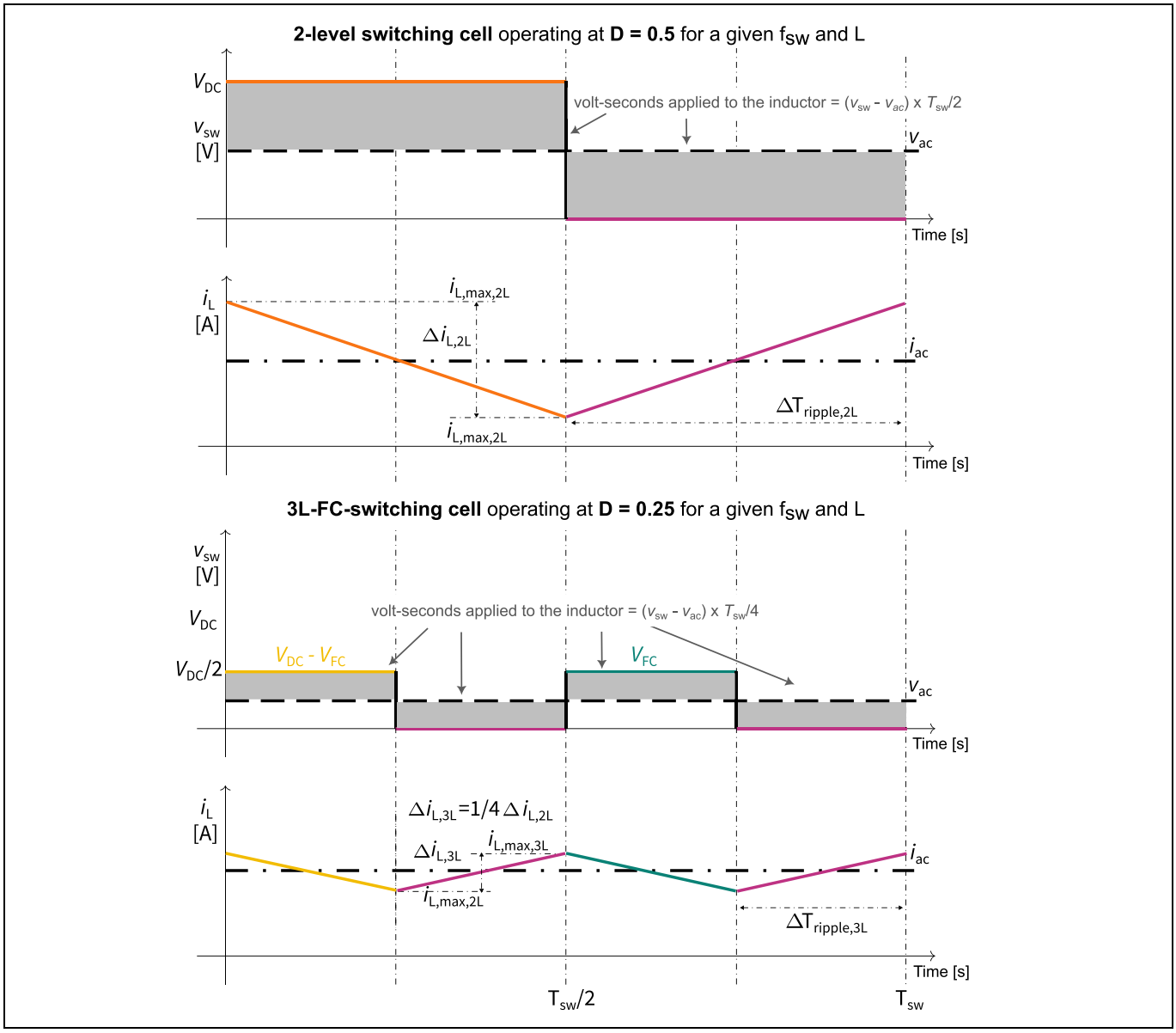


Figure 21 Comparison of volt-seconds applied to the inductor in 2L and 3L flying capacitor switching cells

For a given value of inductance and device switching frequency, the worst-case inductor ripple current with a 3-level flying capacitor switching is 1/4th that of a 2-level switching cell. The dependence of ripple current as a function of the duty cycle of operation is represented in Figure 22. It is evident that to get the same ripple current as a 2-level switching cell, an inductance value of ¼ that of its 2-level counterpart is sufficient. This is due to two factors:

1. Frequency doubling at the switching node due to series interleaving, which reduces the ripple time
2. 3-level voltage waveform, which reduces the voltage applied across the inductor

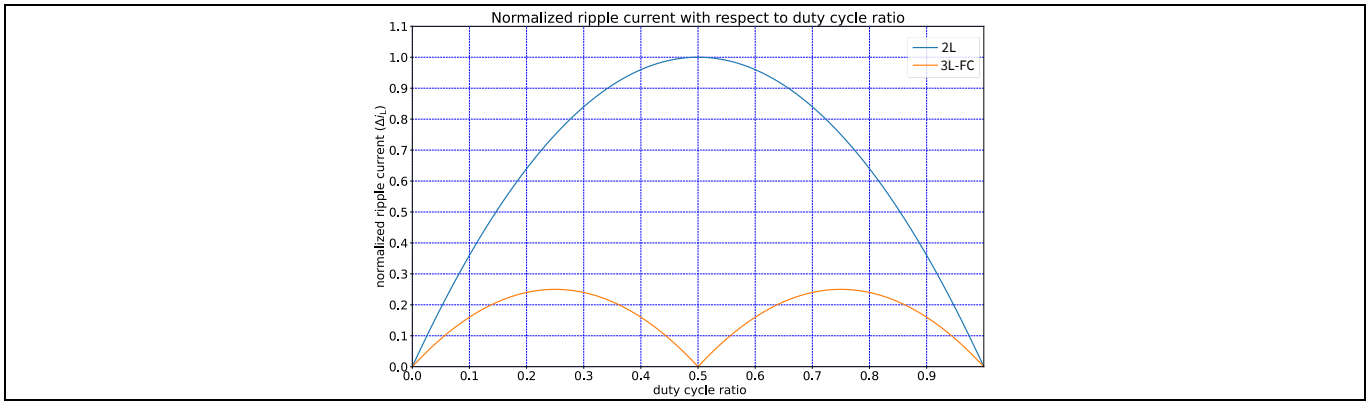


Figure 22 Normalized ripple current as a function of duty cycle of operation for a given switching frequency and inductance value with a 2L and 3L flying capacitor switching cell

There are two degrees of freedom in designing a 3-level flying capacitor topology:

1. Potential to reduce the inductance
2. Choice of switching frequency as a lever to balance the reduction of inductance and converter efficiency, as summarized in Table 5

Table 5 Degrees of freedom in designing a 3-level flying capacitor topology

	Topology	Case 1: f_{sw} (3L) = f_{sw} (2L)	Case 2: f_{sw} (3L) = f_{sw} (2L)/2
Conduction losses	2-level	$P_{cond} = I_{rms}^2 R_{on}$	$P_{cond} = I_{rms}^2 R_{on}$
	3-level	$P_{cond} = 2\ I_{rms}^2 R_{on}$	$P_{cond} = 2\ I_{rms}^2 R_{on}$
Switching losses[1)]	2-level	$P_{sw} = f_{sw} E_{sw}$	$P_{sw} = f_{sw} E_{sw}$
	3-level	$P_{sw} = 2\ f_{sw} (E_{sw}/2)$	$P_{sw} = 2\ (f_{sw}/2)\ (E_{sw}/2)$
Inductance and ESR for same Δi_L	2-level	L and ESR	L and ESR
	3-level	L/4, much lower ESR and smallest inductor	L/2, lower ESR and smaller inductor
Design outcome		Optimized for highest power density	Optimized for highest efficiency

1) A simplified representation to show that the overlap idealized switching losses reduce by at least half in the 3-level topology, but the reduction in reality is higher

A detailed comparison between the 3-level flying capacitor and 2-level CCM TP TPCs using measurements from their Infineon reference designs is given in Section 5.1.

4.1.3 Design considerations in 3-level flying capacitor CCM TP PFCs

4.1.3.1 Dimensioning of the flying capacitor

The following parameters impact the dimensioning of the flying capacitor:

- **Switching frequency (f_{sw}):** Higher f_{sw} → Lower C_{FC}
- **Maximum allowed voltage ripple (ΔV_{FC}):** Higher ΔV_{FC} → Lower C_{FC}. Typically, ΔV_{FC} = 10-20% of $V_{FC,typ}$
- **Maximum load dependent inductor current (i_L):** Higher i_L → Higher C_{FC}

The following equations describe the impact of these parameters on the dimensioning of the flying capacitor.

$$\Delta Q_{FC} = i_L * \Delta t$$
$$\Delta t = (0.5 - |D - 0.5|) * T_{sw}$$
$$\Delta Q_{FC} = C_{FC} * \Delta V_{FC}$$
$$C_{FC} \geq \frac{i_L}{\Delta V_{FC} * 2 * f_{sw}} \; at \; D = 0.5$$

Equation 2 Equations for dimensioning of the flying capacitor

For high power density designs (e.g., AI server PSUs and BBUs) that also require high reliability, MLCC capacitors with soft-edge termination or metal-cap termination, along with a good PCB design to minimize solder stress can be a good solution [3]. Typically, MLCCs with X7T or similar material also have capacitance drop under DC and temperature bias. Therefore, 450 V rated single or stacked metal cap MLCC capacitors can be considered to mitigate the capacitance drop under DC bias.

4.1.3.2 Startup and pre-charging of the flying capacitor

During a cold startup of the PSU with the flying capacitor uncharged (V_{FC} = 0 V), two possible scenarios can occur depending on the location of the DC-link pre-charging NTC + relay, as shown in Figure 23, leading to a potential overvoltage stress on outer-leg MOSFETs Q_{HSO} and Q_{LSO} (NOT on inner leg MOSFETs Q_{HSI} and Q_{LSI}), if CoolSiC™ 400 V MOSFETs are used. As an example, with $V_{ac,rms,max}$ = 305 V, $V_{DS,pk}$ = ~431 V.

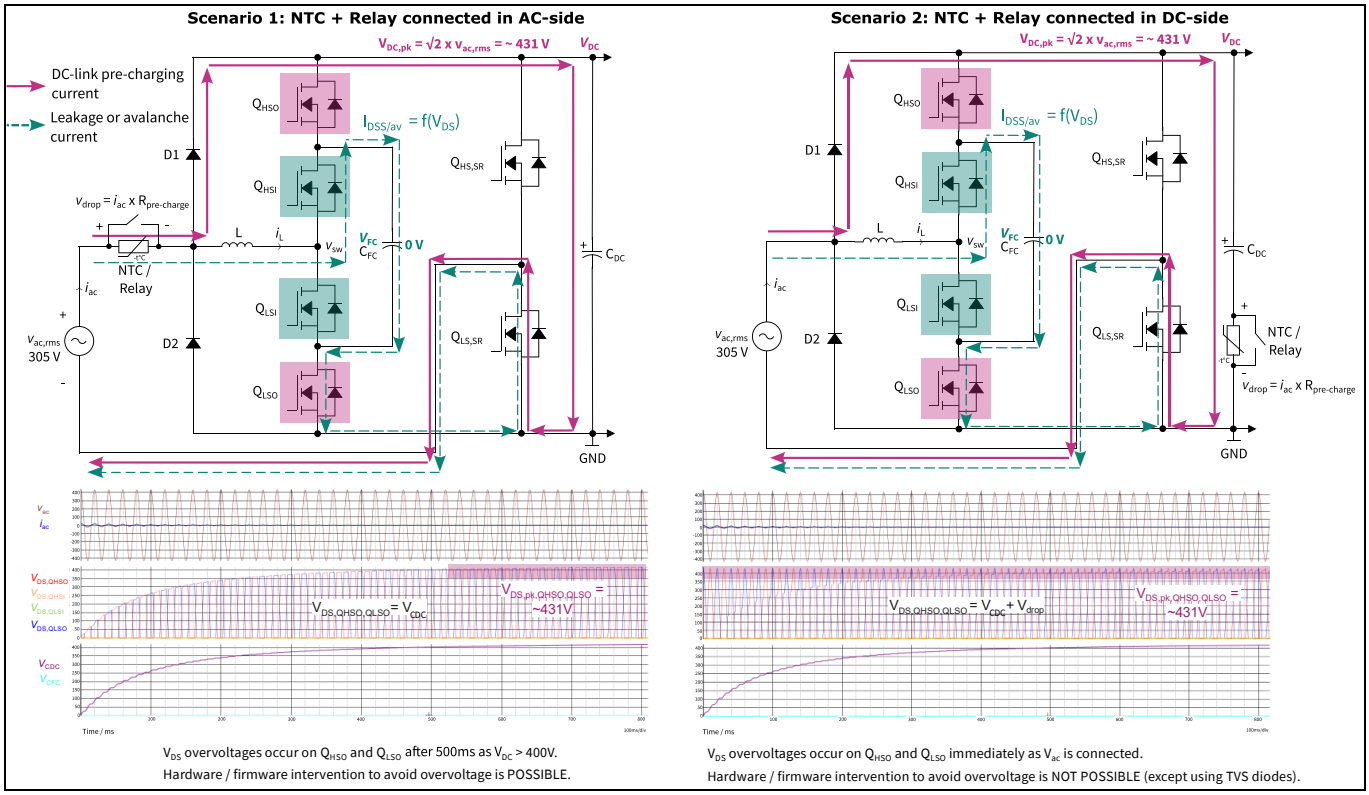


Figure 23 Cold startup scenarios under two DC-link pre-charging NTC + relay configurations without flying capacitor charged

- **Scenario 1 – NTC + relay connected in AC-side**
  - The voltage stress of the outer leg MOSFETs ($V_{DS,QHSO}$ and $V_{DS,QLSO}$) follows the DC link voltage (V_{DC})
  - It is therefore possible to have hardware- or firmware-based solutions to pre-charge the flying capacitor before the DC-link is fully charged and avoid the overvoltage stress on the outer leg MOSFETs, assuming 400 V SiC MOSFETs are used
  - **Startup methods:**
    1. Passive clamping and FC pre-charging using TVS diodes
    2. Firmware-based flying capacitor (FC) pre-charging
    3. Active FC pre-charging [1]
    4. Using extended 440 V_{dc}/455 V_{tr} rated SiC MOSFETs without FC pre-charging
- **Scenario 2 – NTC + relay connected in DC-side**
  - The voltage stress of the outer leg MOSFETs ($V_{DS,QHSO}$ and $V_{DS,QLSO}$) follows the AC voltage (V_{ac}), with $V_{DS,QHSO,QLSO,pk}$ = ~431 V immediately upon AC connection at 90° grid voltage phase angle
  - **Start-up methods:**
    1. Passive clamping and FC pre-charging using TVS diodes
    2. Using extended 440 V_{dc}/455 V_{tr} rated SiC MOSFETs without FC pre-charging

Figure 24 shows the behavior of the CoolSiC™ 400 V MOSFETs – using IMT40R045M2H, chosen from a lot showing the worst-case breakdown voltage ($V_{(BR)DSS}$) – during cold-startup without pre-charging the flying capacitor. It is important to highlight that even with V_{DS} > 400 V, the MOSFETs do not go into avalanche or full breakdown until the tested voltage of $V_{ac,rms}$ = 325 V, indicating the robustness of CoolSiC™ 400 V MOSFETs to overvoltage stresses.

- **Case 1 – with $V_{ac,rms}$ = 295 V (equipment limited):** The peak drain-source voltages on the outer leg MOSFETs are around ~416 V. With multiple repetitive AC line cycles, the charging and discharging of C_{oss} results in some charges injected into the flying capacitor, which results in a linear rise in the V_{FC} voltage

- **Case 2 with $V_{ac,rms}$ = 325 V (applied using an auto-transformer):** Much higher peak drain-source voltages of around ~461.3 V on the outer leg MOSFETs are observed. As expected, this results in much higher drain-source leakage currents of ~20 mA, but this leakage current charges up the flying capacitor and in the subsequent AC-line cycles, the drain-source voltage stress is reduced in a self-limiting manner.

  Consequently, two regions are observed:
  1. A non-linear higher I_{DSS} related V_{FC} charging, as indicated in Figure 24 (b)
  2. The linear C_{oss} charging/discharging related V_{FC} charging, as indicated in Figure 24 (b)

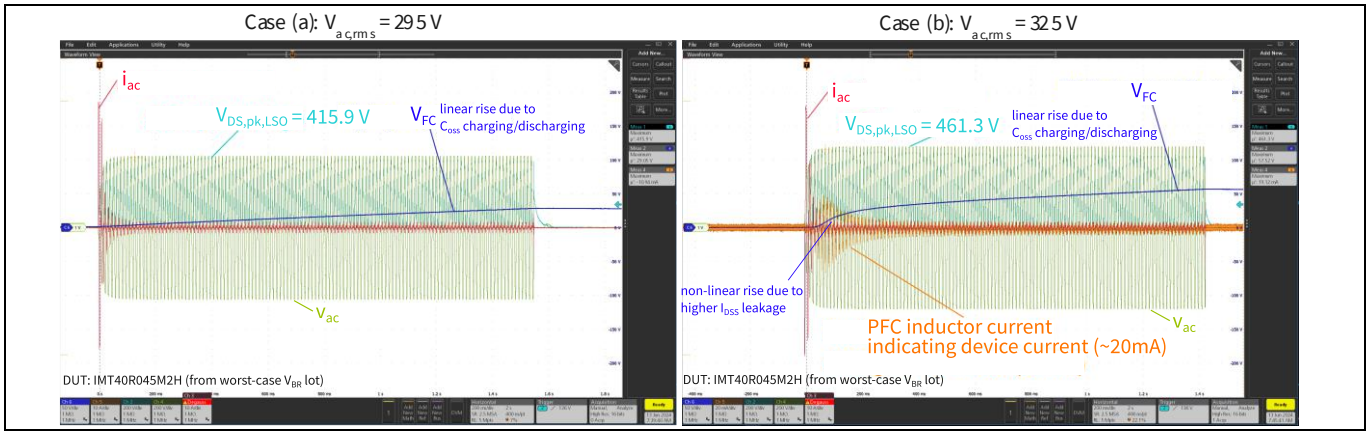


Figure 24 Startup of 3L FC PFC without pre-charging the flying capacitor

To understand and distinguish between the higher I_{DSS} leakage and avalanche breakdown of CoolSiC™ 400 V MOSFETs, additional DC and pulsed overvoltage stress tests were done on the IMT40R045M2H samples from the same lot showing the worst-case breakdown voltage. As shown in Figure 25 (a), in the region of V_{DS} = ~431 V at $V_{ac,rms,max}$ = 305 V, the MOSFETs exhibit merely higher I_{DSS} leakage currents and do not go into avalanche.

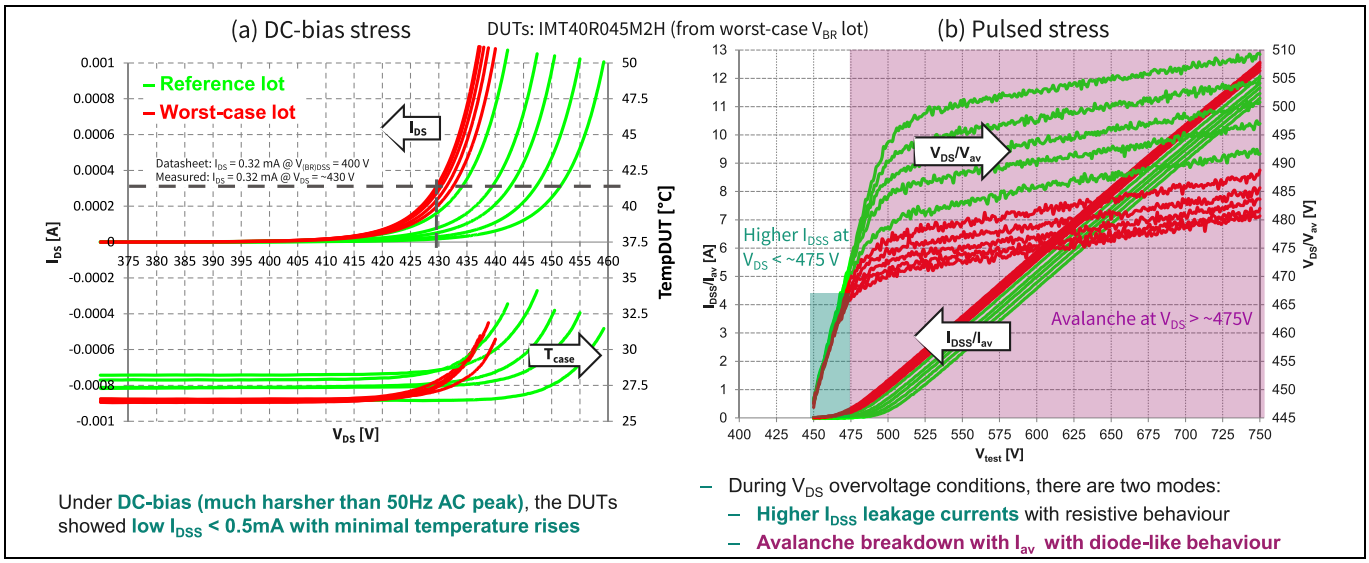


Figure 25 DC and pulsed overvoltage stress tests to distinguish between higher leakage and avalanche breakdown regions

Extended voltage rated CoolSiC™ 440 V MOSFETs with 440 V_{dc}/455 V_{tr} ratings for 3L FC CCM TP PFC *without* flying capacitor pre-charging

Although the regular CoolSiC™ 400 V SiC MOSFETs can safely withstand the startup overvoltages without flying capacitor pre-charging, in order to comply with the derating guidelines recommended by standards like the IPC-9592-B (see summarized in Table 6), a technology variant of the CoolSiC™ 400 V MOSFETs with higher epi thickness is offered, with $V_{(BR)DSS}$ = 440 V and $V_{(BR)DSS,tr}$ = 455 V to enable 95% derating at $V_{ac,rms,max}$ = 305 V.

Note: During the operational lifetime in the 3L FC CCM TP PFC, the HF-leg MOSFETs block $V_{DS,nom} = V_{DC}/2$ = ~200 V, and hence, offer a derating of >50% for the drain-source voltage.

Table 6 Derating guidelines for drain-source voltage provided by IPC 9592-B

Device type	Parameter	Derating factor
Power MOSFET and IGBT	Drain–source	≤ 80 % including repetitive spikes for devices rated > 200 V
	Collector–emitter voltage	Single event spike at 95% of the maximum rating

Cold startup *without* FC pre-charging using CoolSiC™ 440 V MOSFETs to comply with IPC 9592-B

- Q_{HSI} and Q_{LSI} have no overvoltage stress at cold startup. Q_{HSO} and Q_{LSO} experience the overvoltage stress for a few milliseconds at the AC line frequency (50 Hz/ 60 Hz)
- MOSFETs do not switch immediately during cold startup. Cumulative stress time for an estimated 10k PSU startup cycles over lifetime would be << 1h. After the controller is initialized, it is assumed that the flying capacitor voltage is regulated at $V_{FC} = V_{DC}/2$ = ~200 V, such that all HF-leg MOSFETs block ~$V_{DC}/2$ during normal and idle operation

Therefore, the startup AC line frequency stress voltages can be considered as a cumulative single event stress and 95% V_{DS} derating can be applied for $V_{ac,rms,max}$ = 305 V ($V_{DS,pk}$ = ~431 V), considering $V_{(BR)DSS,tr}$ = 455 V, as shown in Table 7.

Table 7 Key electrical static parameters of IMT44R011M2H enabling IPC 9592-B derating *without* flying capacitor pre-charging

Parameter	Symbol	Values			Unit	Note/Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	440	–	–	V	V_{GS} = 0 V, I_D = 1.33 mA
Transient drain-source breakdown voltage (6)	$V_{(BR)DSS,tr}$	455	–	–	V	V_{GS} = 0 V, I_D = 13.3 mA, t_{pulse} ≤ 10 ms, duty cycle ≤ 50%

In summary, the key considerations in selection of voltage class to apply the derating guidelines are:

- **DC-link pre-charging NTC + relay connection**
  - Connected to AC side: FC pre-charging is possible → Evaluate 400 V/440 V MOSFETs
  - Connected to DC link: FC pre-charging is possible only if TVS diodes are used → Evaluate 440 V/650 V MOSFETs
- **Input AC voltage range**
  - 180-305 V_{ac}
    - FC pre-charging done → Evaluate 400 V/440 V MOSFETs
    - FC pre-charging **not** done → Evaluate 440 V MOSFETs for 95% derating and 650 V MOSFETs for >80% derating at startup
  - 100-265 V_{ac}
    - FC pre-charging done → Evaluate 400 V/440 V MOSFETs
    - FC pre-charging **not** done → Evaluate 440 V MOSFETs with close to 85% derating and 650 V MOSFETs for >80% derating at startup
- **Dimensioning of the flying capacitor (C_{FC})**
  - Sufficient C_{FC} → Even AC self-balancing could be sufficient
  - Limited C_{FC} → FC ripple voltage can be hard to limit without a dedicated control loop
  - With good V_{FC} balancing → 400 V/440 V MOSFETs for >80% derating during operational lifetime
  - Without good V_{FC} balancing → 650 V MOSFETs for >80% derating during operational lifetime

If measures to pre-charge the flying capacitor during the startup are implemented, it is possible to avoid any overvoltage concerns during startup altogether. Some of the possible methods to pre-charge the flying capacitor during startup can be summarized as follows:

- **Passive clamping and flying capacitor pre-charging using TVS diodes**

Using TVS diodes in parallel to outer leg MOSFETs Q_{HSO} and Q_{LSO} ensures the TVS diodes clamp the voltage across outer leg MOSFETs when $V_{DS} > V_{TVS,clamp}$. The clamping current through the TVS diode passes through the flying capacitor, thus pre-charging it and self-limiting the severity of the TVS diode clamping in subsequent AC line cycles, as shown in Figure 26

It must be mentioned that the TVS diodes add additional parasitic junction capacitance (C_j), which effectively gets added in parallel to the C_{oss} of the outer MOSFETs causing additional losses (slower slew rates and additional Q_{oss}/E_{oss} losses). However, the magnitude of C_j of TVS diodes are typically a fraction of the C_{oss} of the MOSFETs. Therefore, the impact of the additional C_j on power dissipation is expected to be low, thanks also to

the low inherent switching losses in the 3L FC PFC due to multilevel operation. This method can be used for both scenarios of DC link pre-charging NTC + relay configurations discussed earlier. Hardware measurements and validations of this method have been demonstrated in [4] and [5].

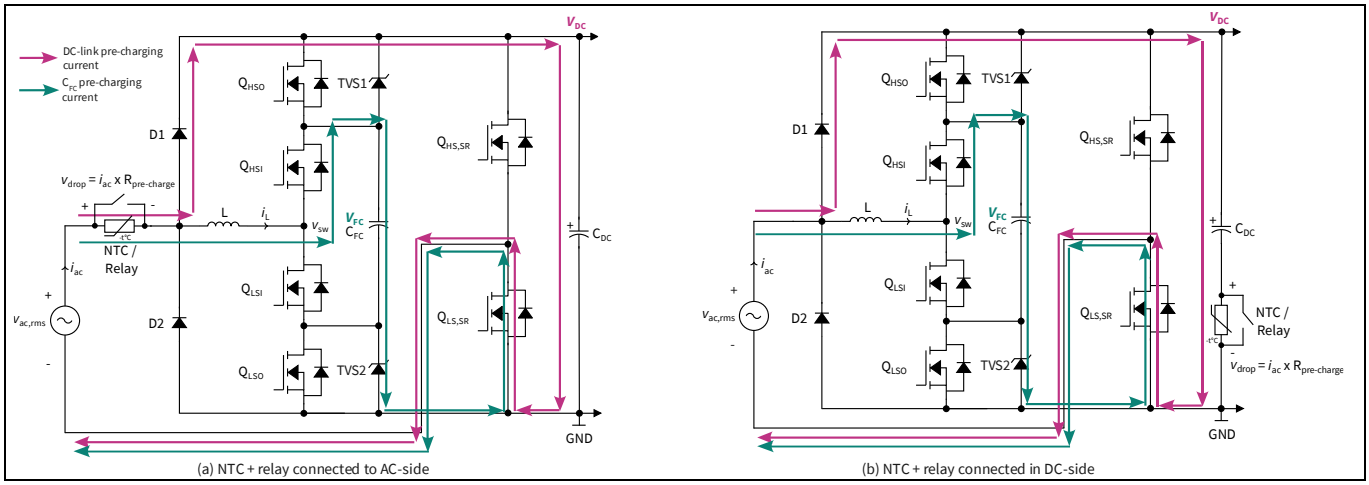


Figure 26 Passive clamping and flying capacitor pre-charging using TVS diodes

- **Firmware-based methods to pre-charge the flying capacitor**

Firmware-based methods require the DC link pre-charging NTC + relay to be connected to the AC-side and a fast auxiliary supply enabling controlling the gates of MOSFETs from the controller (MCU) before the DC link is fully charged. This is feasible due to the large voltage headroom of 400 V SiC MOSFETs ($V_{DS,nom}$ = 200 V).

a) **Charging the flying capacitor in parallel with the DC-link capacitor**

This method pre-charges both the DC link capacitor and flying capacitor in parallel. This is shown in Figure 27, where the outer low-side MOSFET Q_{LSO} is turned on to provide a charging path for the flying capacitor.

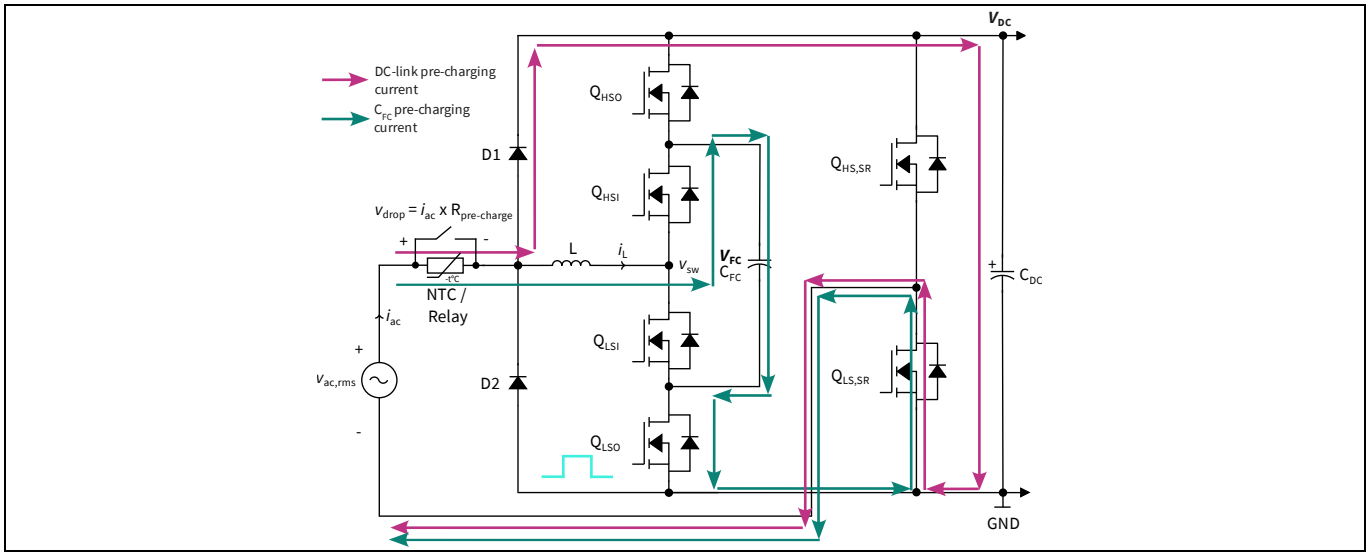


Figure 27 Charging the flying capacitor in parallel with DC-link capacitor

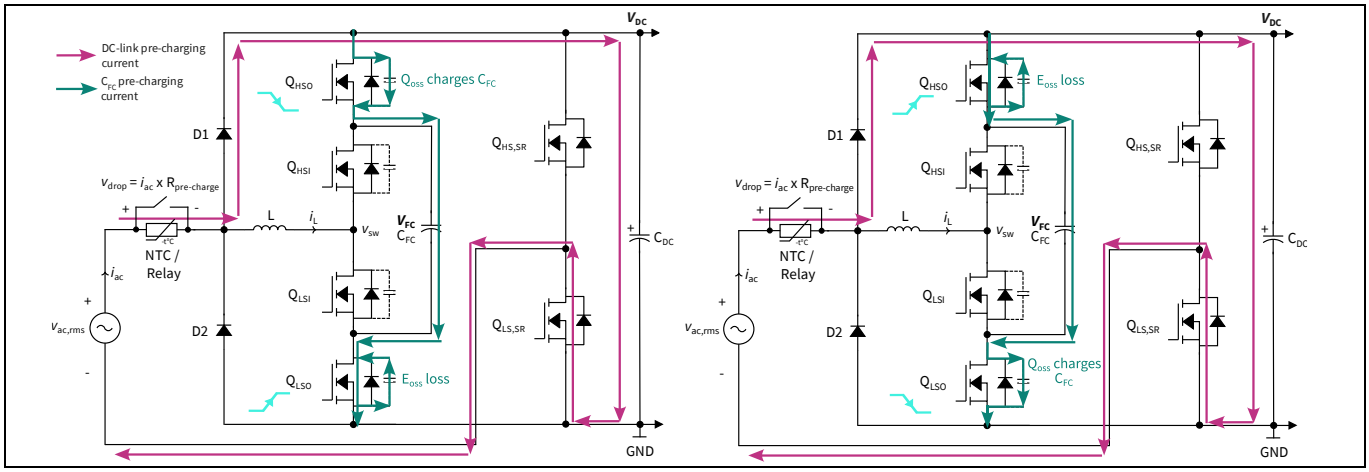


Figure 28 Complementary HF switching of outer MOSFETs to pre-charge the C_{FC} using Q_{oss} injection

b) **Active high-frequency switching and Q_{oss} injection to charge the flying capacitor**

The complementary high-frequency switching of the outer leg MOSFETs injects charge (Q_{oss}) into the flying capacitor during each switching event, as shown in Figure 28. During the switching events, the E_{oss} energy stored in C_{oss} is dissipated in the channel of the MOSFET that is hard-switching on. The speed of pre-charging is dependent on:

1. Capacitance of flying capacitor C_{FC}
2. Switching frequency during pre-charging ($f_{sw,pre-charge}$)
3. Q_{oss} of MOSFET

As an example, with IMT40R015M2H, C_{FC} = 8 uF and $f_{sw,pre-charge}$ = 200 kHz, around 50 ms are needed to pre-charge the C_{FC} from 0 V to 200 V. Similarly, in the case of complementary switching of the inner leg MOSFETs, the charge (Q_{oss}) is extracted from the flying capacitor. Therefore, this method is suitable for charging and discharging the C_{FC}. It can also be used to balance the flying capacitor during the PSU turn off.

A detailed review of the firmware-based flying capacitor pre-charging and balancing methods is provided in [6].

- **Active pre-charging of the flying capacitor**

Similar to the passive diode clamped solution, an actively controlled current source introduced in [1] can be used to pre-charge the flying capacitor, as shown in Figure 29. This method works independent of control intervention without the need for a fast-aux. supply and MCU initialization but requires the DC-link pre-charging NTC and relay to be placed on the AC-side. It is turned-on and -off based on a hysteresis value to ensure that the flying capacitor is always charged to ~V_{DC}/2. The biggest advantage of this solution is that it is cost effective, occupies a small space, and is completely disabled during the normal operation of the PSU.

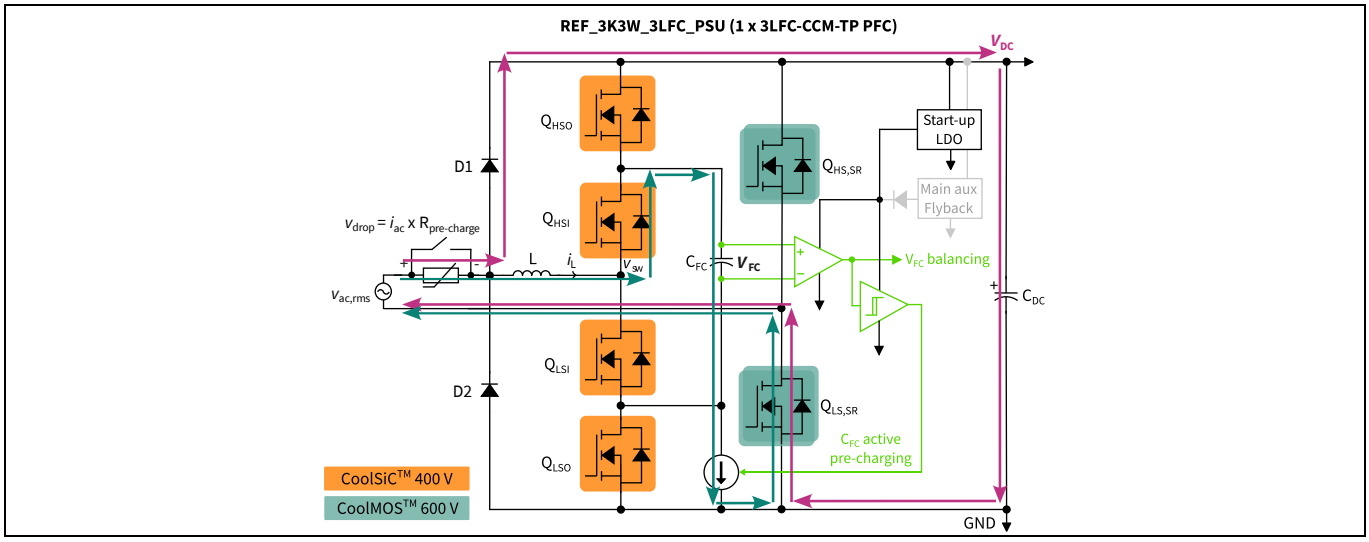


Figure 29 Active pre-charging of the flying capacitor using a controlled current source [1]

4.1.3.3 Auxiliary power supply and isolated gate driving

In conventional 2-level topologies, it is common to use a bootstrapping scheme to derive the power supply of high-side switches. Although it is a low-cost and low-complexity solution, it poses some challenges in the 3-level flying capacitor topology if cascaded bootstrapping is used to supply all the three floating high-side switches.

Namely, overcharging could occur due to the higher forward voltage drop of the SiC MOSFET body diode (V_{SD} ~ 3.5 V) while undervoltage could occur for higher levels of bootstrapping due to the forward voltage drop of the bootstrap diodes (V_{SD} ~ 0.5 V).

One solution is to use bootstrapping to higher gate drive bus voltages and then using an LDO for post-regulation to 18 V. However, a more proven and robust solution is proposed in [1], which uses a cost-effective low-space planar PCB-based isolated auxiliary power supply to generate four isolated 18 V outputs to drive the four HF-leg MOSFETs, as shown in Figure 30 and Figure 31.

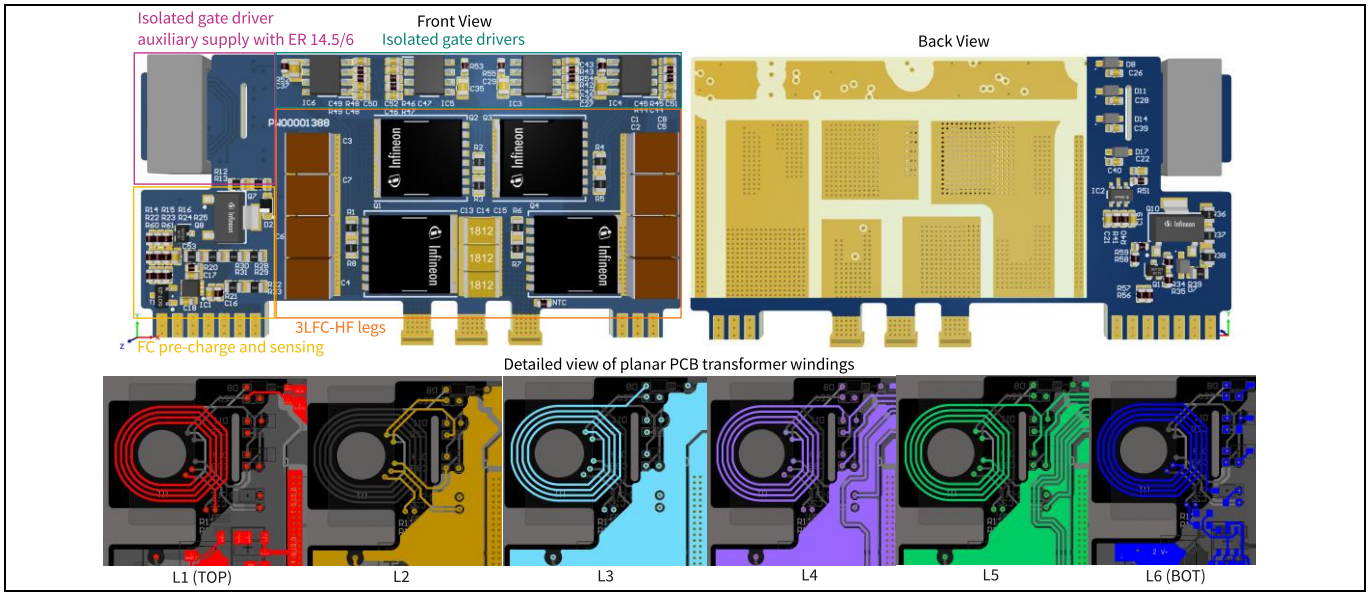


Figure 30 Low-cost and low-space isolated auxiliary power supply integrated in the 3L flying capacitor HF switching cell daughterboard (70 mm x 36 mm) [1]

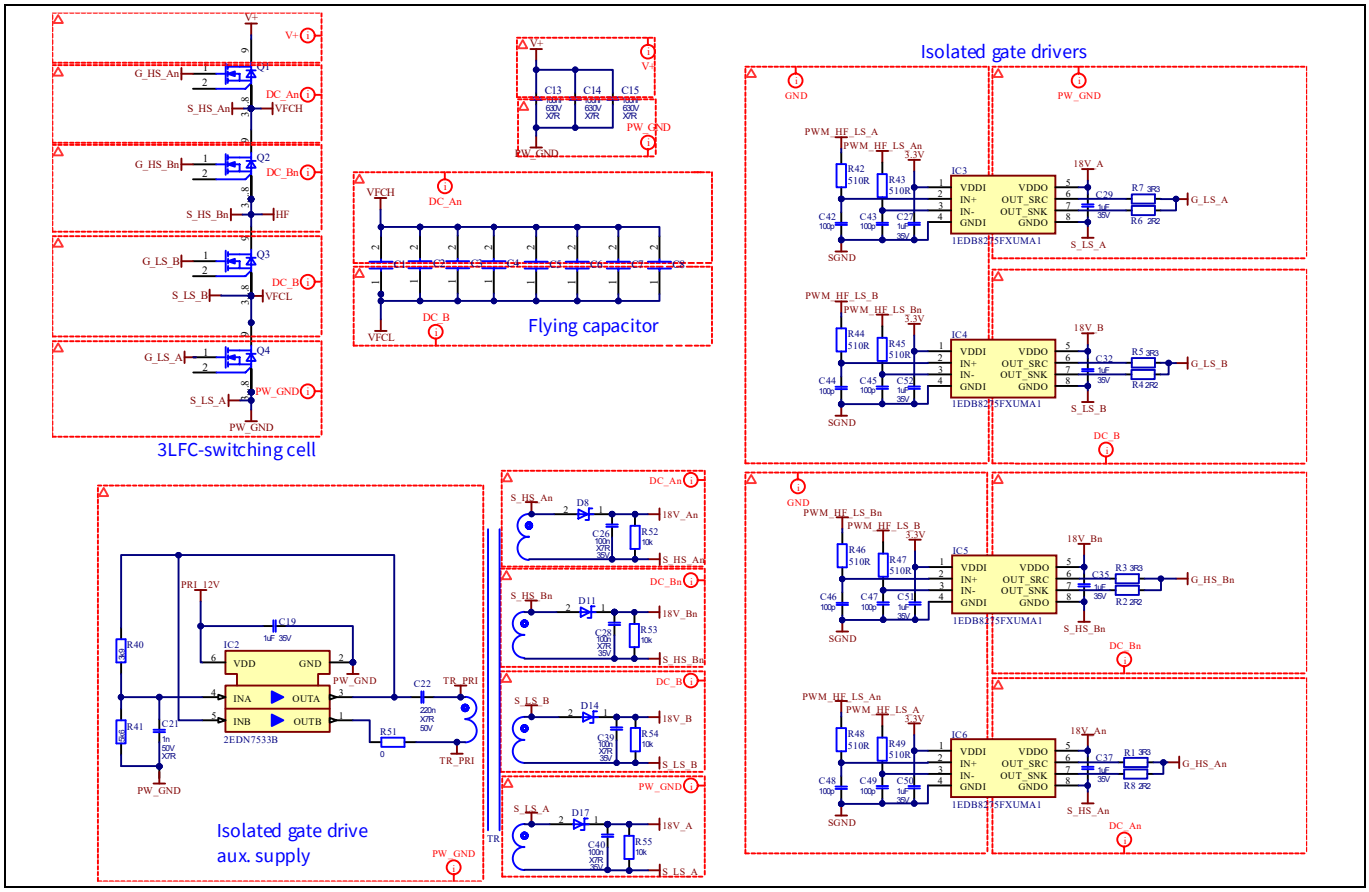


Figure 31 Isolated auxiliary supply for gate driving of the 3L FC HF switching cell [1]

The isolated supply uses a self-resonating oscillator switching at ~600 kHz to drive a planar PCB transformer with a turns ratio N = 4 : 4 and uses a low-cost ER 14.5/6 ferrite core with no air gap for an effective magnetizing inductance of ~17.6 µH. The auxiliary supply and gate driver stages are integrated in the 70 mm x 36 mm x 7 mm HF-leg daughterboard due to its low space, with the ferrite cores assembled using metal clamps, as shown in Figure 30. Because all the drivers are always supplied, this is a reliable and proven solution across all situations – steady state, dynamics, and abnormal operating conditions.

4.1.3.4 AC line surge protection

Fundamentally, the impact of input voltage surge (e.g., due to lightning strikes) on both the 2-level and 3-level flying capacitor CCM totem pole PFC topologies and their mitigation measures are similar. The key difference in the 3-level flying capacitor CCM TP PFC is how the voltage of the flying capacitor is impacted during surge events, as it impacts the voltage sharing between the inner and outer HF leg MOSFETs. This is highlighted in Figure 32, showing a surge current path through the flying capacitor when the HF leg MOSFETs are switching during a differential surge event.

- **Differential mode surge:**

  A differential mode surge occurs across line to neutral. Common protection measures include:

  - Using varistors (MOVs) across the line to neutral
  - Using the DC link pre-charging diodes to route a part of the surge current to the DC link capacitors and use the bulk electrolytic capacitors to absorb the surge energy partially, as shown in Figure 32

The key measure to protect the HF leg MOSFETs in 3L FC CCM TP PFC is to implement a fast detection of surge events and stopping PWM. This can be done through the input line V_{ac} overvoltage protection (OVP) or PFC inductor overcurrent protection (OCP). Effectively, as the PWM operation is stopped, the surge currents through the flying capacitor will cease to over-charge or discharge the flying capacitor. For further reference, hardware measurements of surge tolerance in the 3-level flying capacitor CCM TP PFC have been demonstrated in [7].

- **Common mode surge:**

  A common mode surge occurs across line and neutral to PE. Common measures to mitigate this are using a combination of MOVs and gas discharge tubes (GDTs), as shown in Figure 32.

  A detailed review of surge protection for SMPS applications is covered in [8] and [9].

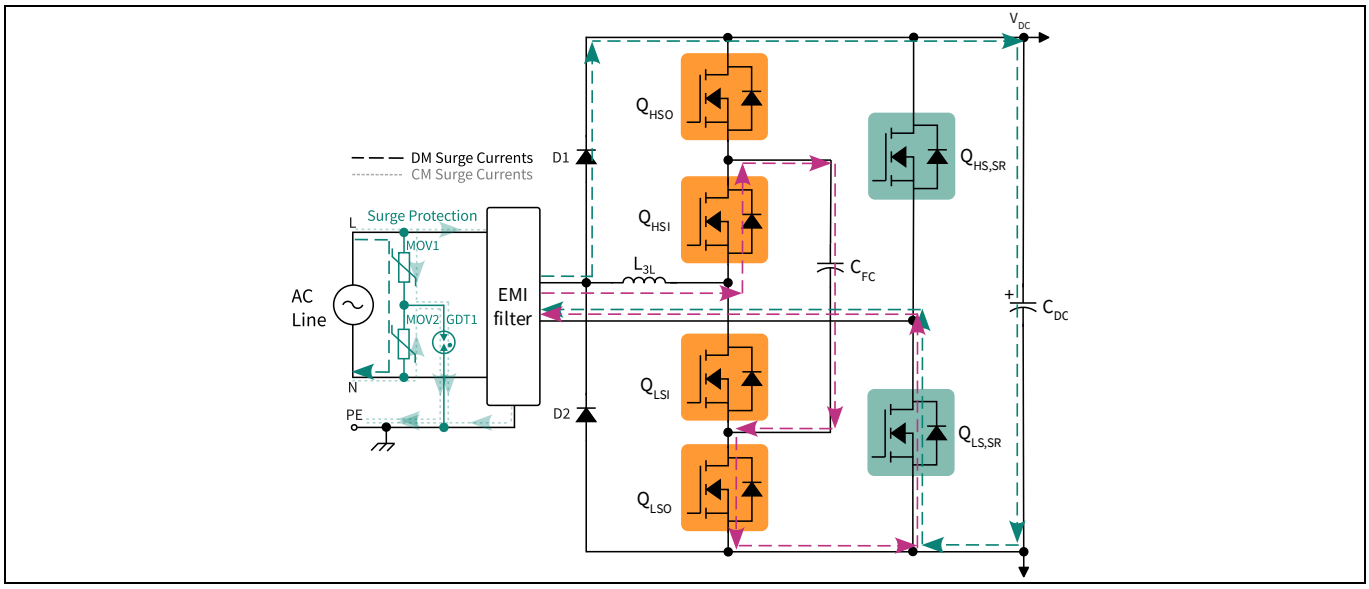


Figure 32 AC line surge protection in 3-level flying capacitor CCM TP PFCs

4.2 3-level converters for DC-AC inverter operation

4.2.1 3-level active neutral point clamped converter

As shown in Figure 33, the 3-level active neutral point clamped converter (3L-ANPC) inverter can be used for DC-AC inverter operations in numerous applications, from solar grid-tied inverters to motor drives, with the following advantages:

- 3-level output voltage (± V_{DC}/2, 0) at the switching node improves AC voltage waveform quality, reduces THD, and minimizes the filter size due to the volt-second reduction
- All switches block and switch only V_{DC}/2, leading to reduced switching losses and lower EMI
- Improved power stage efficiency and power density due to multilevel operation, as explained in Section 4.1, with inherently lower current ripple and consequent filter size reduction
- Compared to lower voltage motor control systems (e.g., with V_{BAT} = 48 V), moving to a higher battery voltage (e.g., with V_{BAT} = 400 V) could eliminate the need to parallel MOSFETs and reduce the necessary copper, leading to system level performance improvements and cost savings
- Better thermal management due to heat spreading over 18 MOSFETs in a 3-phase application. However, this comes with additional complexity due to more components compared to other multilevel topologies

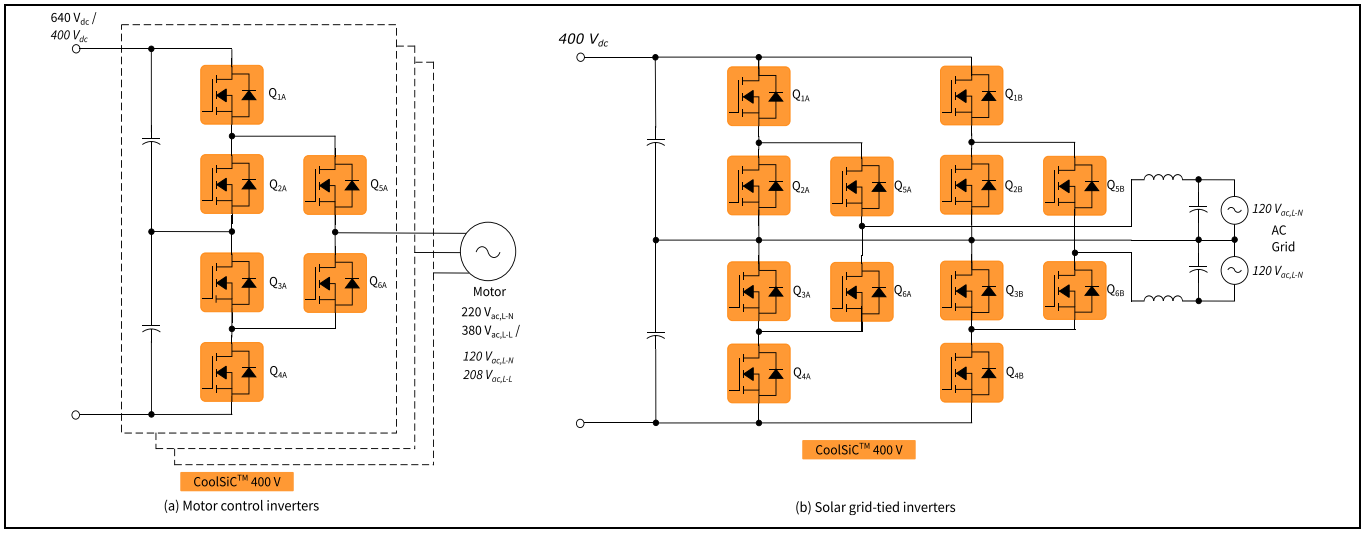


Figure 33 3L-ANPC converter for (a) motor control inverters and (b) solar grid-tied inverters

Some commonly used modulation methods for the 3L-ANPC converter are shown in Figure 34. In contrast to the conventional modulation methods (a) 2H4L, (b) 4H2L, and (c) 6H0L discussed in [10] and [11], the (d) 6H0L-2F modulation method discussed in [12] and [13] results in effective switching node frequency doubling as shown in Figure 34 (d), where the V_{swA} voltage has twice the frequency of pulses compared to others.

Note: Si CoolMOS MOSFETs or IGBTs can be an alternative option for switches operating at grid frequency, with the 400 V SiC MOSFETs offering a higher performance due to a flat $R_{DS(on)}$ vs. T_j.

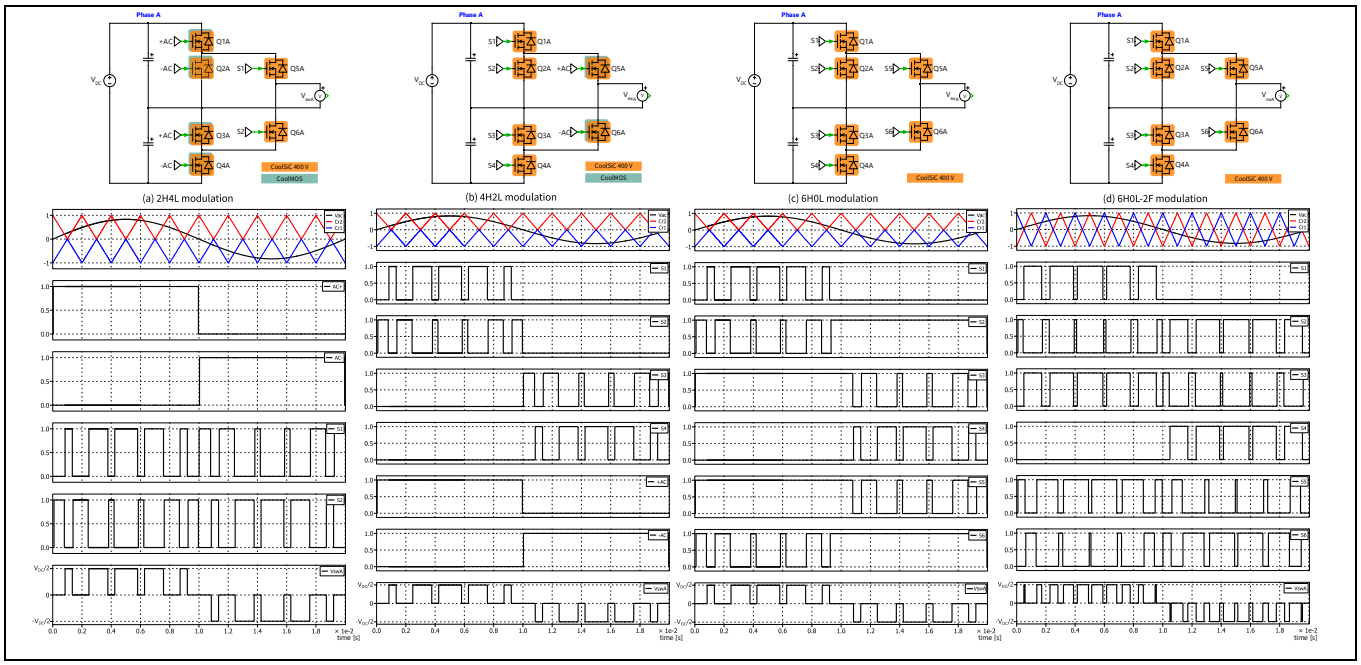


Figure 34 Some modulation schemes for 3L-ANPC converters

Figure 35 shows idealized steady-state switching waveforms seen in the 3L-ANPC converter with 4H2L modulation method for a 2 x 120 V_{ac} split-phase AC output inverter with per phase load of 3 kW. Section 5.3 provides hardware measurements from a 10 kW 3-phase 3L-ANPC inverter evaluation board.

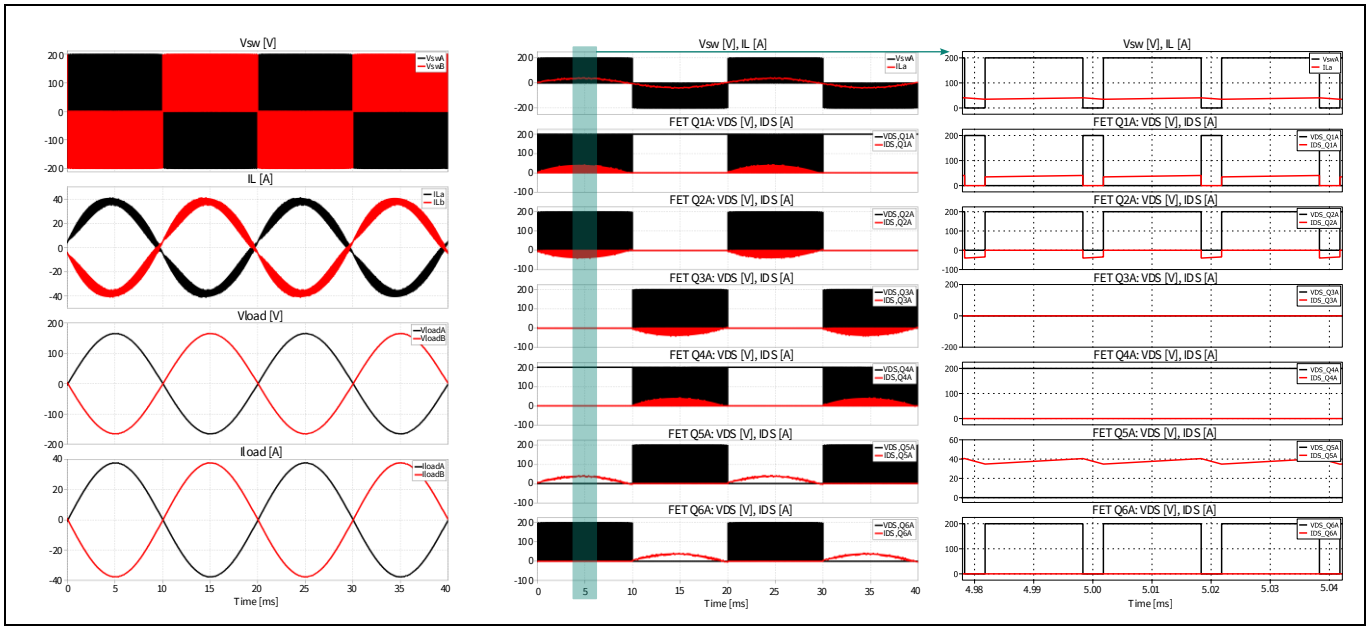


Figure 35 Idealized operational and switching waveforms in a 2 x 120V_{ac} split-phase AC output 3L-ANPC inverter, with V_{DC} = 400 V, f_{sw} = 50 kHz, and per-phase load $P_{loadA,B}$ = 3 kW

4.2.2 3-level T-type neutral point clamped converter

The 3-level T-type neutral point clamped converter (3L-TNPC) converter uses a combination of 650 V and 400 V rated SiC MOSFETs, as shown in Figure 36. The key benefits of this topology are:

- 3-level output voltage (± V_{DC}/2, 0) at switching node improves AC voltage waveform quality, reduces THD, and minimizes the filter size due to the volt-second reduction
- Q_{1x} and Q_{4x} block V_{DC}, but switch only V_{DC}/2, leading to reduced switching losses and lower EMI. The back-to-back connected switches Q_{2x} and Q_{3A} block V_{DC}/2 and can be rated to use lower voltage MOSFETs
- Fewer components compared to other multilevel topologies, leading to balanced performance and simplicity
- Natural split-phase AC output with two phases for 120 V_{ac} grid AC systems, without subsequent conversion

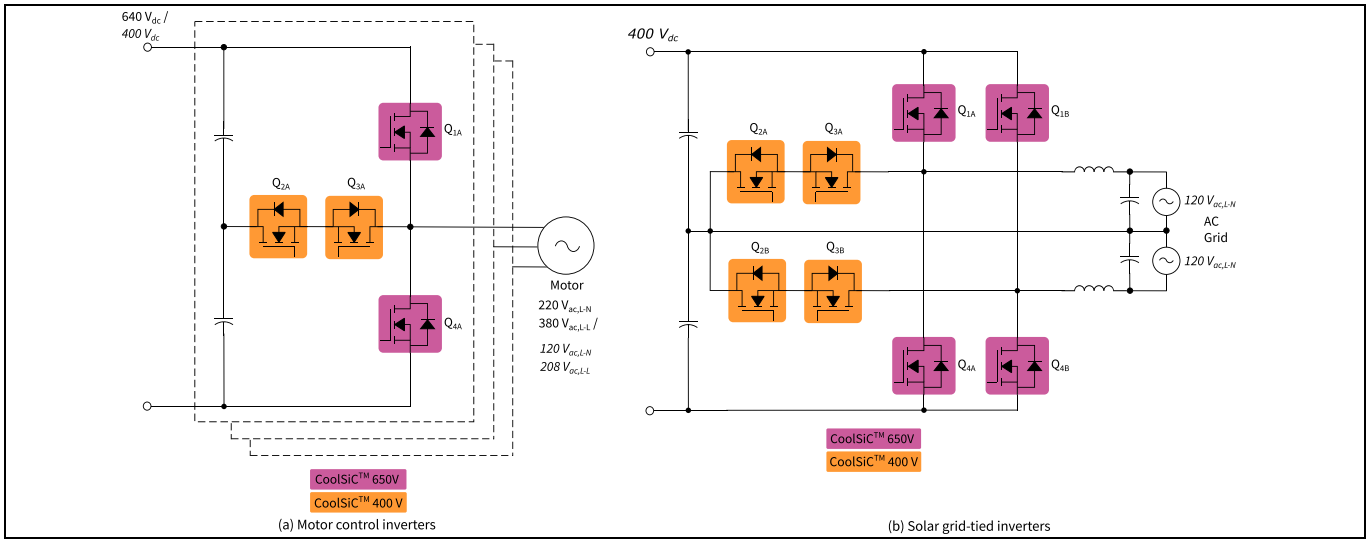


Figure 36 3L-TNPC converter for solar grid-tied and motor control inverters

A typical modulation method for 3L-TNPC is shown in Figure 37, along with idealized steady-state switching waveforms seen in this converter for a 2 x 120 V_{ac} split-phase AC output inverter with per phase load of 3 kW shown in Figure 38.

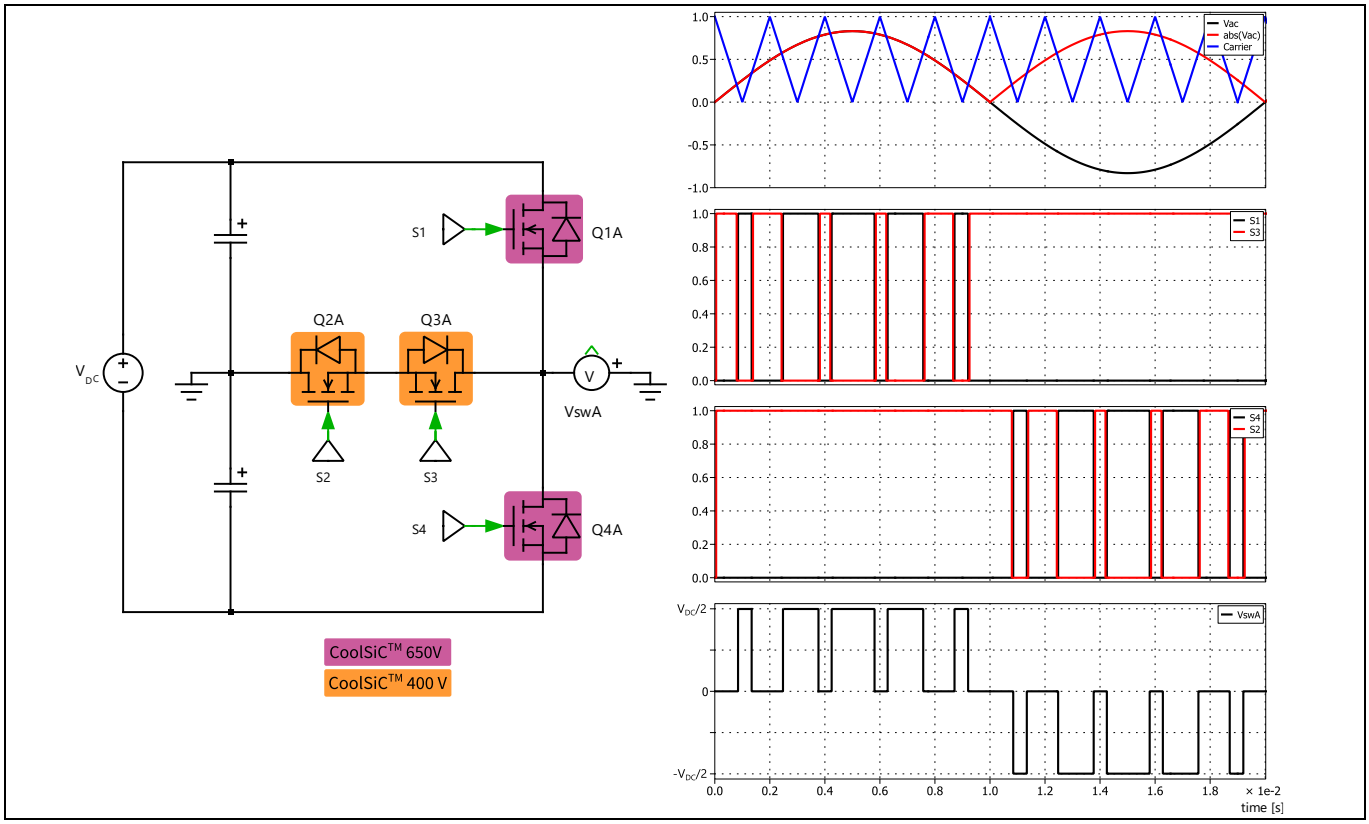


Figure 37 Modulation scheme in 3L-TNPC converter

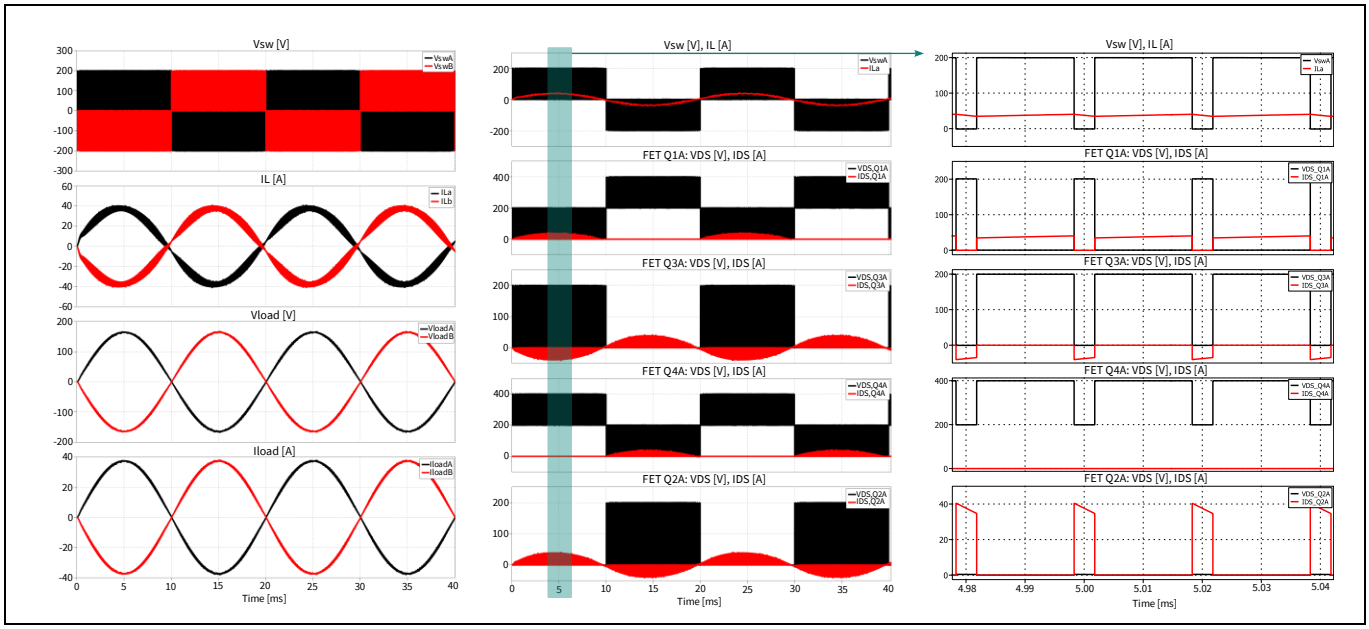


Figure 38 Idealized operational and switching waveforms in a 2 x 120V_{ac} split-phase AC output 3L-TNPC inverter, with V_{DC} = 400 V, f_{sw} = 50 kHz, and per phase load $P_{loadA,B}$ = 3 kW

4.3 2-level B6 converter for DC-AC inverter operation for motor control

Compared to the conventional 36 V, 48 V, 72 V, or 96 V battery-based motor drives in LEVs (e.g., high-power forklifts), using higher voltage battery packs like 180 V or 288 V enables an improvement in system efficiency and power density, leading to a higher power capability.

Section 5.4.1 provides the hardware benchmarking of a 288 V drive system using 400 V SiC MOSFETs compared to a 48 V drive system using 80 V Si MOSFETs. Due to the much lower currents in high-voltage systems, lower copper (e.g., busbars) requirement and reduced – and even eliminated – need to parallel MOSFETs result in system-level cost savings.

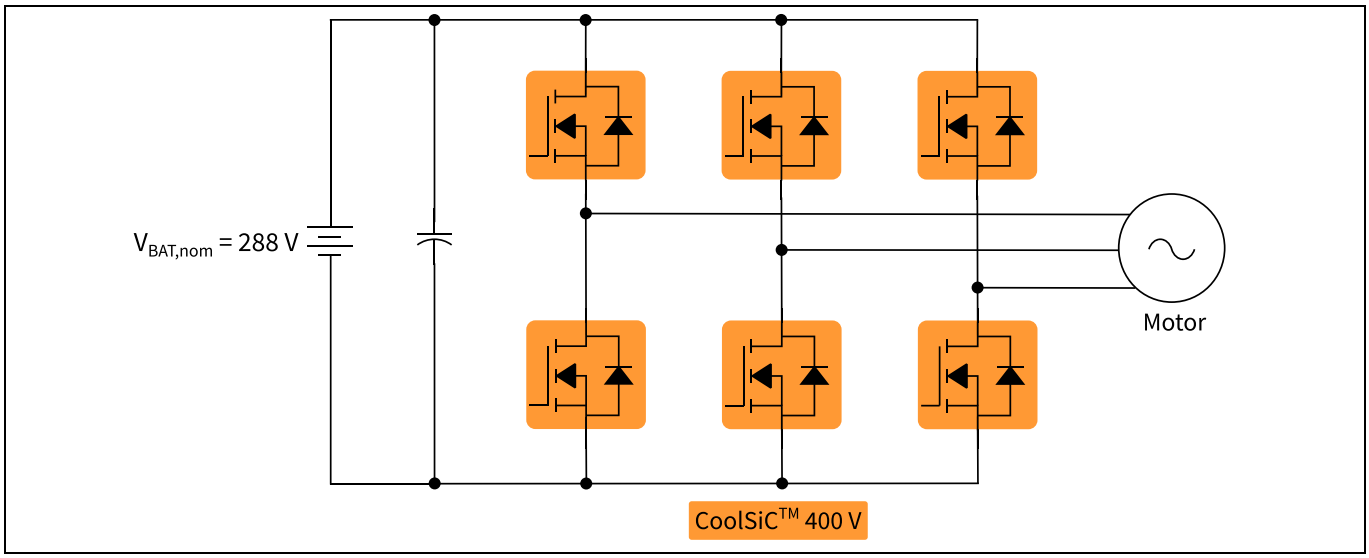


Figure 39 2-level B6 converter for motor control applications with higher battery voltages

4.4 2-level and 3-level DC-DC converters

4.4.1 3-level flying capacitor buck/boost for HV power backup units in AI datacenters

In AI datacenters, power backup units (PBUs) consisting of battery backup units (BBUs) using Li-ion batteries are used to provide long-term backup during power shortages and capacitor bank-storage units (CBUs) using supercapacitors and electrolytic capacitors to supply short-term power surge due to GPU workloads, as shown in Figure 40.

With the bus voltages going to ±400 V or 0/800 V architectures, the 3-level flying capacitor buck/boost DC-DC converter is a promising non-isolated topology for this application as an alternative to the conventional 2-level buck/boost topology, enabling the use of lower voltage-rated switches and smaller passive components. It offers a higher current handing capability due to high full-load power stage efficiency and the potential to reduce the number of interleaved stages in a high-power design to improve power and energy density. The operation principle is the same as that of the 3-level flying capacitor PFC described in Section 4.1. Benchmarking of the 3-level flying capacitor buck/boost versus its 2-level counterpart using a 10 kW hardware demonstrator is provided in Section 5.2.

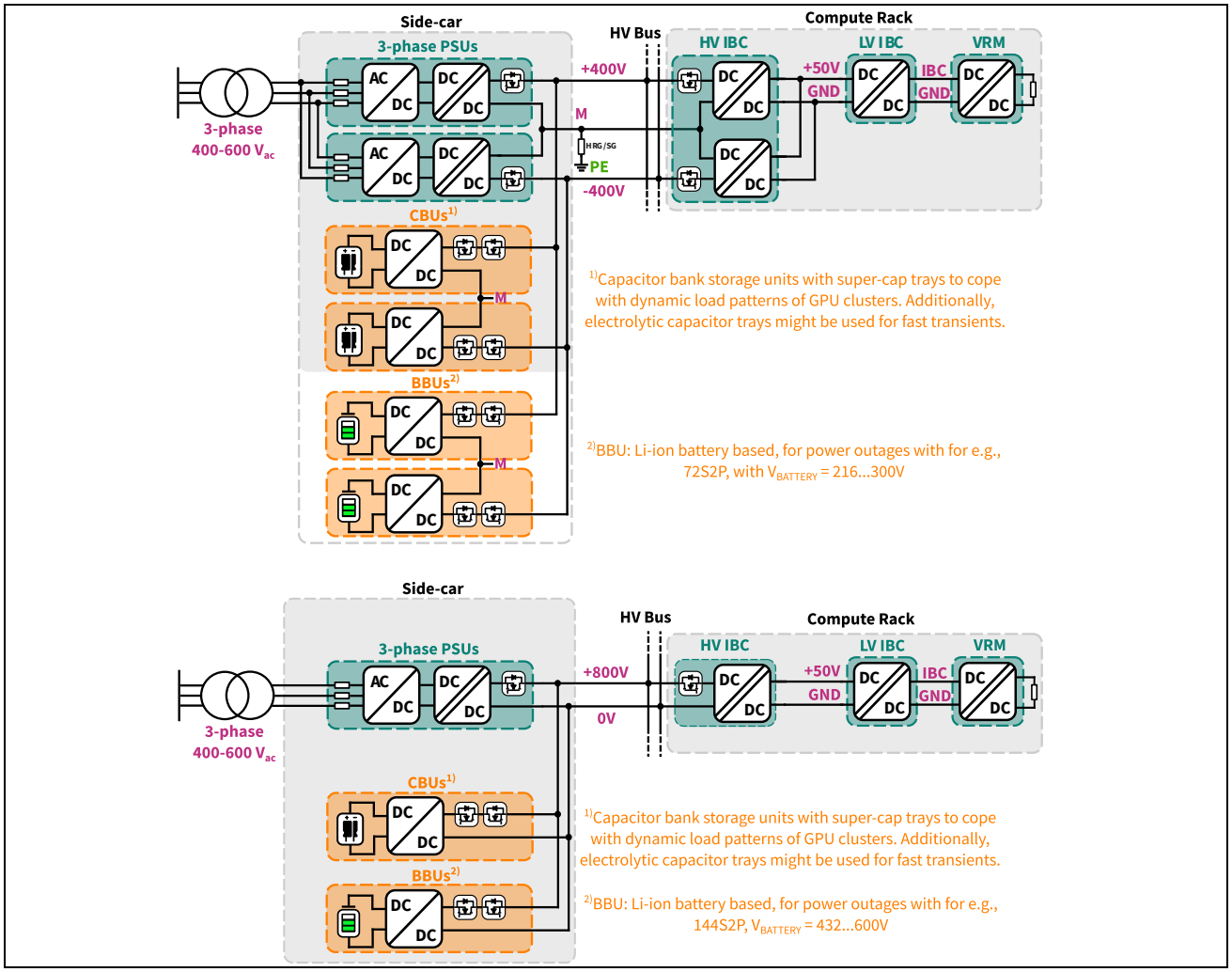


Figure 40 Next-generation HVDC architectures for AI datacenters

As shown in Figure 41, for 400 V PBUs, the 2-level topology would need 650 V rated switches and the 3-level topology enables the use of 400 V rated switches. For 800 V PBUs, the 2-level topology would need 1200 V rated switches and the 3-level topology enables the use of 650 V rated switches.

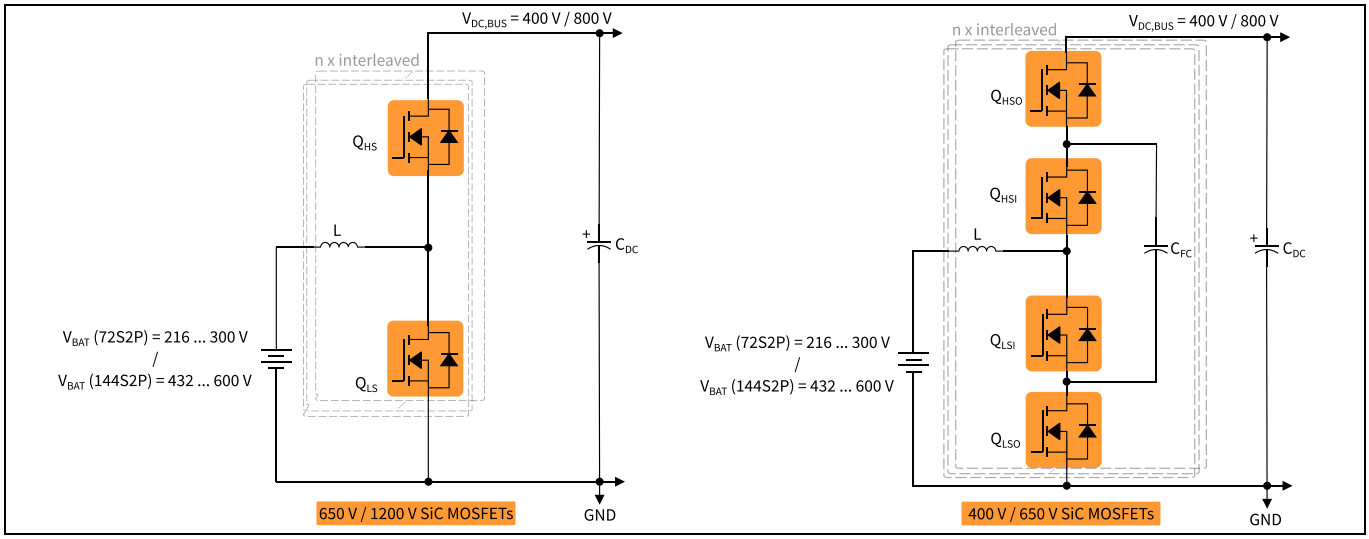


Figure 41 3-level flying capacitor buck/boost for non-isolated high-voltage power back-up units

4.4.2 2-level DC-DC converters for series-connected solar panels

In residential and commercial solar photovoltaic (PV) energy storage systems (ESS), series-connected PV modules need DC-DC converter modules to interface to the energy storage element and subsequent DC-AC inverter stages. Compared to traditional 650 V Si switches (MOSFETs and IGBTs), the 400 V SiC MOSFETs offer a cost and performance optimized wide-bandgap technology with superior switching and conduction losses. Figure 42 shows an example for a 48 V battery system with a buck DC-DC converter. Depending on the PV system and the number of series/parallel connected PV modules along with the subsequent power conversion stages, other topologies like boost, buck-boost, or even flyback converter can be a viable alternative.

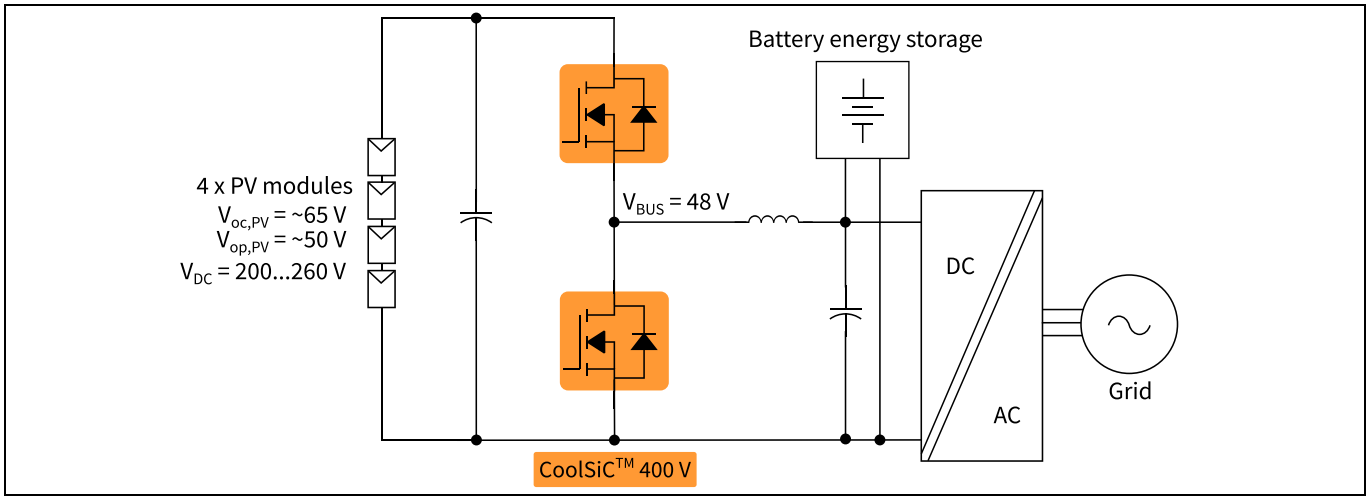


Figure 42 2-level buck DC-DC converter for series-connected solar panel systems

4.4.3 Isolated DC-DC converters for industrial applications: DAB, LLC, and PSFB

As shown in Figure 43, depending on the input/output voltages, the CoolSiC™ 400 V MOSFETs can be used in various topologies where a blocking voltage of ~150 to ~300 V_{DC} are needed, with the following benefits:

- **Dual-active bridge (DAB):** In this inherently bidirectional topology, the soft-switching figure of merit, FoM_{oss} = Q_{oss} x $R_{DS(on)}$ and flat $R_{DS(on)}$ vs. T_j are of importance
- **LLC:** In the classic resonant LLC converter with full-bridge rectification, the flat $R_{DS(on)}$ vs. T_j is beneficial. Linear C_{oss} and low Q_{oss} of the CoolSiC™ 400 V MOSFETs results in an ideal operation of the synchronous rectifier MOSFETs with linear switching behavior
- **Phase-shifted full bridge (PSFB):** Depending on full-bridge or center-tap rectification, the 400 V SiC MOSFETs can be used as synchronous rectification (SR) MOSFETs for various output voltages. The key value proposition of CoolSiC™ 400 V MOSFETs in this topology is the hard commutation robust body diode with low forward recovery charges Q_{fr}, which is reflected to the primary side and affects the circulating currents, as well as impacts the overshoots on the SR MOSFETs

For applications like high power battery chargers for light electric vehicles (LEVs) with nominal battery voltages of 48-180 V_{DC} or telecom rectifiers and industrial power supplies with 45-56 V_{DC} isolated output, the CoolSiC™ 400 V MOSFETs in the secondary side of these isolated topologies could be a good fit.

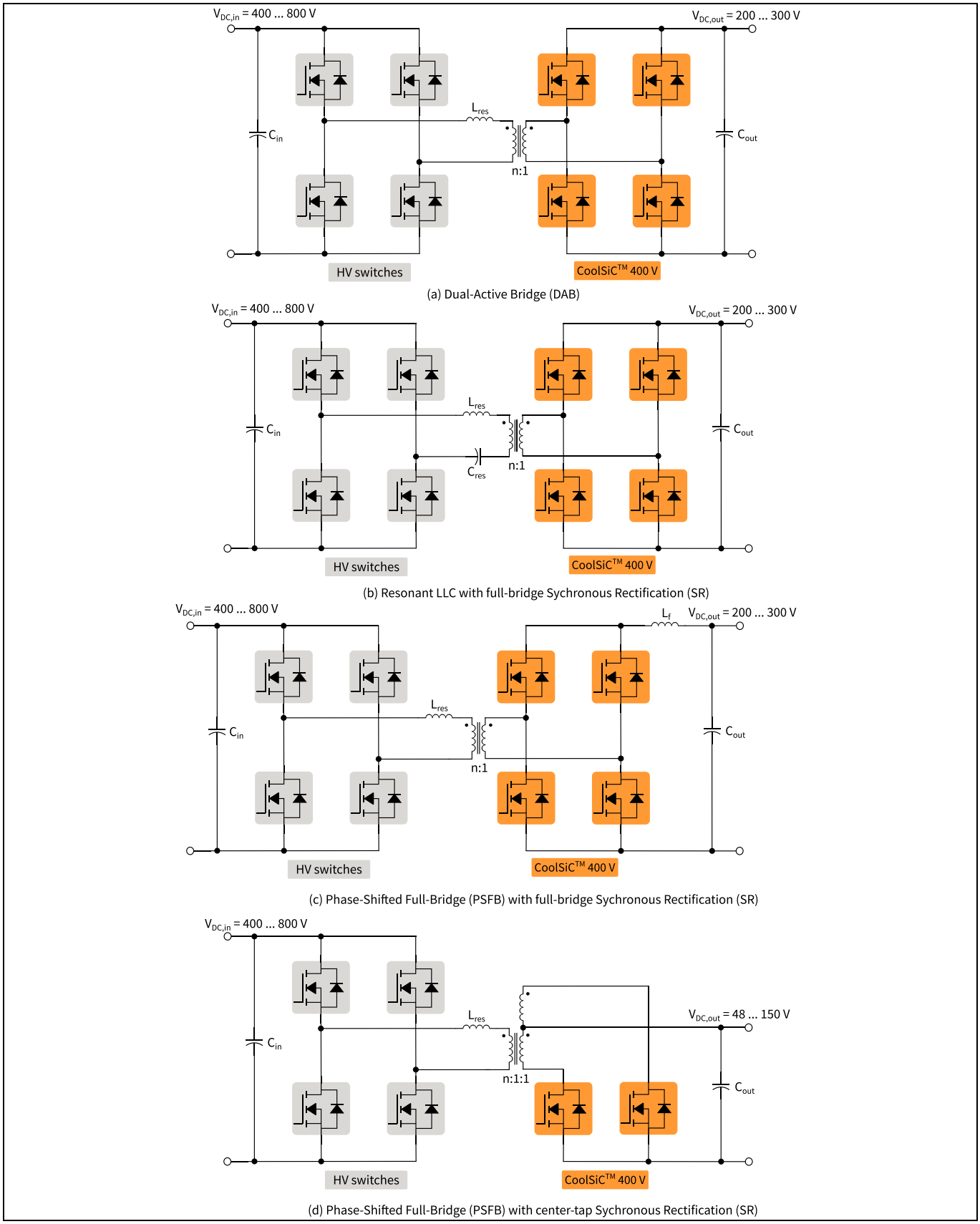


Figure 43 Isolated DC-DC converters for industrial applications: (a) DAB, (b) resonant LLC, and PSFB with (c) full-bridge and (d)center-tap SR

4.5 Class-D audio amplifiers for high voltage low-Z and high-Z loads

CoolSiC™ 400 V MOSFETs enable Class-D audio amplifier designs capable of driving both high-impedance (high-Z) and low-impedance (low-Z) amplifiers due to their linear capacitances that support operation across various bus voltages. This results in reduced stock keeping units (SKUs) with simplified inventory management and provides system flexibility, enabling using the same amplifier for various applications without being constrained by low-Z or high-Z load handling capability.

The excellent switching and conduction FoMs ($R_{DS(on)}$, Q_{fr}, C_{oss}) result in reduced losses and better thermal performance compared to traditional Si MOSFETs. Figure 44 shows a system-level application diagram in a Class-D audio amplifier reference design. Table 8 summarizes the key benefits of CoolSiC™ 400 V MOSFETs in it.

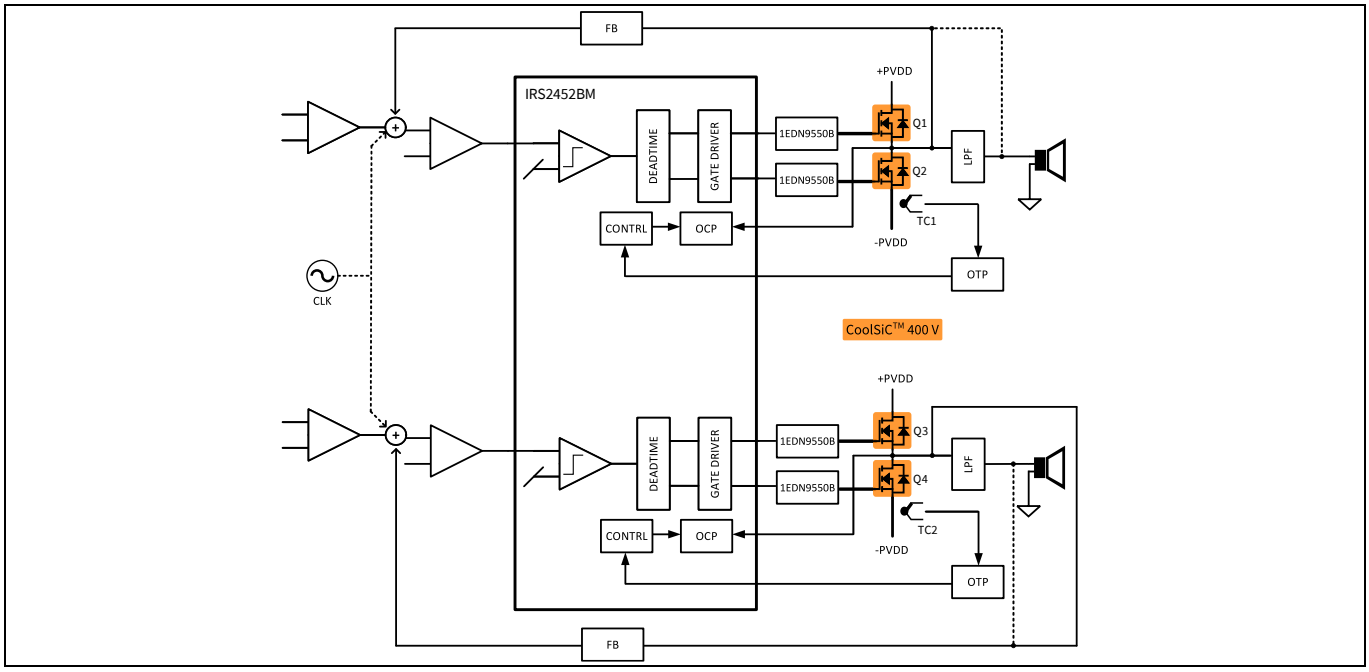


Figure 44 CoolSiC™ 400 V MOSFETs for power stage of Class-D amplifiers

Table 8 Key parameters and benefits of CoolSiC™ 400 V MOSFETs in Class-D audio amplifiers

Benefit	Low Q_{fr}	Low and linear C_{oss}	Low $R_{DS(on)}$	Flat $R_{DS(on)}$ vs. T_j
Efficiency	Reduced reverse recovery losses, supports faster switching (dv/dt)	Lower switching losses and extended ZVS range due to low Q_{oss}, minimizes heat generation, enables low Z and high Z driving capability	Lower conduction losses, minimizes heat generation, enables low Z drive capability	Maintains efficiency across operating temperature and load range
EMI	Reduces high-frequency ringing from Q_{fr}	Linear dv/dt with clean switching waveforms under hard-switching and extended ZVS range	–	–
Audio quality	Lowers THD+N by reducing switching noise and shorter dead times	Lowers THD+N by reducing switching noise; reduces distortion through faster dv/dt and reduced dead time	–	–

5 Application tests

5.1 3-level flying capacitor CCM-totem pole PFC for datacenter and edge AI

In order to fairly evaluate the 2-level and 3-level flying capacitor CCM totem pole PFCs, it is vital to also consider parallel interleaved 2-level CCM totem pole PFC. An example comparison of two 3.3 kW PFCs from [1] and [17] is shown in Figure 45.

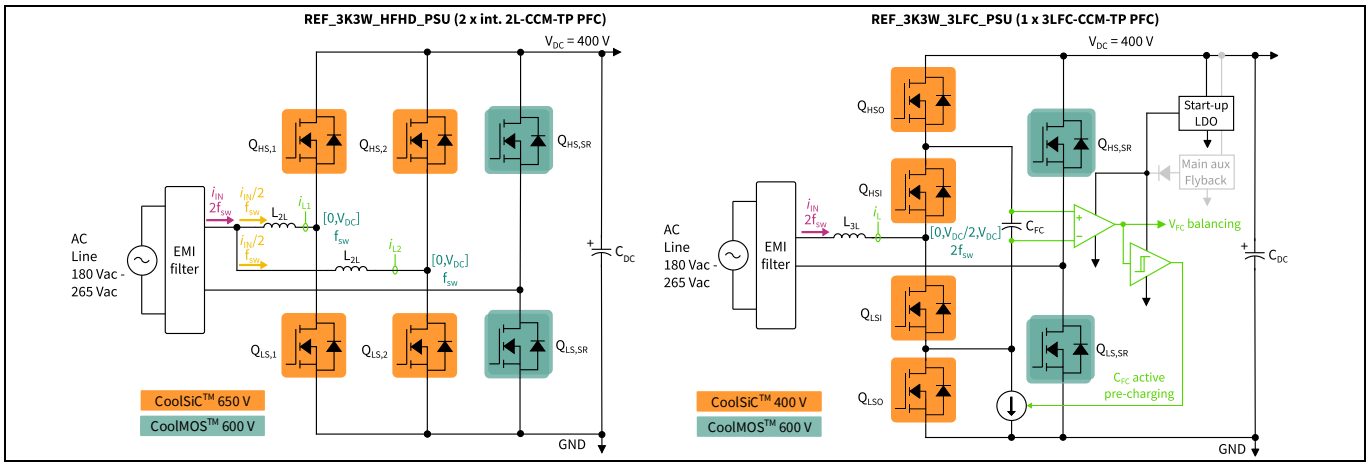


Figure 45 Equivalent comparison of a 3.3 kW interleaved 2-level CCM totem pole PFC with 3-level flying capacitor CCM totem pole PFC

Table 9 Comparison of interleaved 2-level vs. single 3-level flying capacitor CCM totem pole PFCs

	2 x int. 2L CCM TP PFC [17]	**1 x 3L-FC CCM TP PFC [1]**
High-frequency (HF) leg MOSFETs	• 4 x CoolSiC™ 650 V parallel interleaved • $R_{ds(on),2L}$ = 57 mΩ ↑ due to interleaved parallel connection	• 4 x CoolSiC™ 400 V series interleaved • $R_{ds(on),3L}$ = 25 mΩ ↓due to interleaved series connection
Gate drivers for HF leg MOSFETs	• 4 x 1-channel or 2 x 2-channel • 2 x 2EDB9259Y	• 4 x 1-channel • 4 x 1EDB8275F, similar cost as 2 x 2-ch
Aux.-supply for HF leg gate drivers	3 x non-isolated aux. supplies using bootstrapping and LDO post regulation	4 x isolated aux. supplies using a planar PCB transformer driven by a self-resonating oscillator
PWMs	2 x PWMs – 180° phase-shifted – f_{sw}	2 x PWMs – 180° phase-shifted – f_{sw}
Ancillary and sensing (only showing differences)	2 x hall-effect current sensors for $i_{L1,2}$	1 x hall-effect current sensor for i_L and 1 x differential voltage sensor for V_{FC}, flying capacitor pre-charging circuit
Passive components (only showing differences)	• 2 x PFC chokes with CH270060GT14 / 64 T / 1.12 mm φ / 358 µH / 53 mΩ ESR • $i_{AC}/2$ – [0,V_{DC}] – f_{sw} → L_{2L} • Total volume similar to single choke in non-interleaved 2L-CCM-TP-PFC	• 1 x PFC choke with CH270060GT/42 T/1.53 mm φ/132 µH/16 mΩ ESR • i_{AC} – [0,V_{DC}/2,V_{DC}] – 2f_{sw} → L_{2L}/4 • Lower ESR and lower core losses • Magnetic volume / cost reduction ~60% • Flying capacitors 6 x C5750X7T2W105K250KA
Thermal design	• Heat spreading due to interleaving • Inductors and switches share current	• Heat spreading due to interleaving • Lower ESR and lower core losses in choke • Higher efficiency >0.3 % with better FoM switches reduce power dissipation
EMI	• 2 x f_{sw} effective i_{IN} current + Δi_{IN} reduction • DM EMI reduction compared to non-interleaved 2L CCM TP PFC	• 2 x f_{sw} effective i_{IN} current + Δi_{IN} reduction • DM EMI reduction same as in int. 2L CCM TP • Expected improvement in CM EMI due to multilevel v_{sw} with lower dv/dt

The control block diagrams of both the interleaved 2-level and 3-level flying capacitor CCM totem-pole PFCs are shown in Figure 46, with the following details of importance:

- Fundamentally, the PFC control architectures are quite similar with two key differences – in the case of the 3L FC CCM TP PFC, there is only one current loop and an additional flying capacitor balancing loop
- The additional V_{FC} balancing P-controller with control variable ΔD complements the natural/inherent AC cycle V_{FC} balancing. The ΔD (<< 1 % in normal operation) varies the duty cycle of one of the PWM legs to vary the charge injected to or extracted from the flying capacitor proportional to the sensed error. The P-controller runs at a relatively low frequency of 5 kHz in the REF_3K3W_3LFC_PSU [1]
- In both architectures, the average PFC inductor current is sensed through an ADC trigger. In the case of int. 2L CCM TP PFC, the ADC is triggered at half the duty cycle set point (CR2 = ½ CR1). In the case of 3L FC PFC CCM TP PFC, the ADC is triggered at the peak of the triangular timer (CCU80.CC81), with the current control loop (Result ISR (iLoop)) updating the duty cycle for both inner and outer legs at the rate of the switching period of the triangular timer (CCU80.CC81). For D > 0.5, the mid-point of the falling current slope is sampled, and for D < 0.5 the mid-point of the rising current slope is sampled

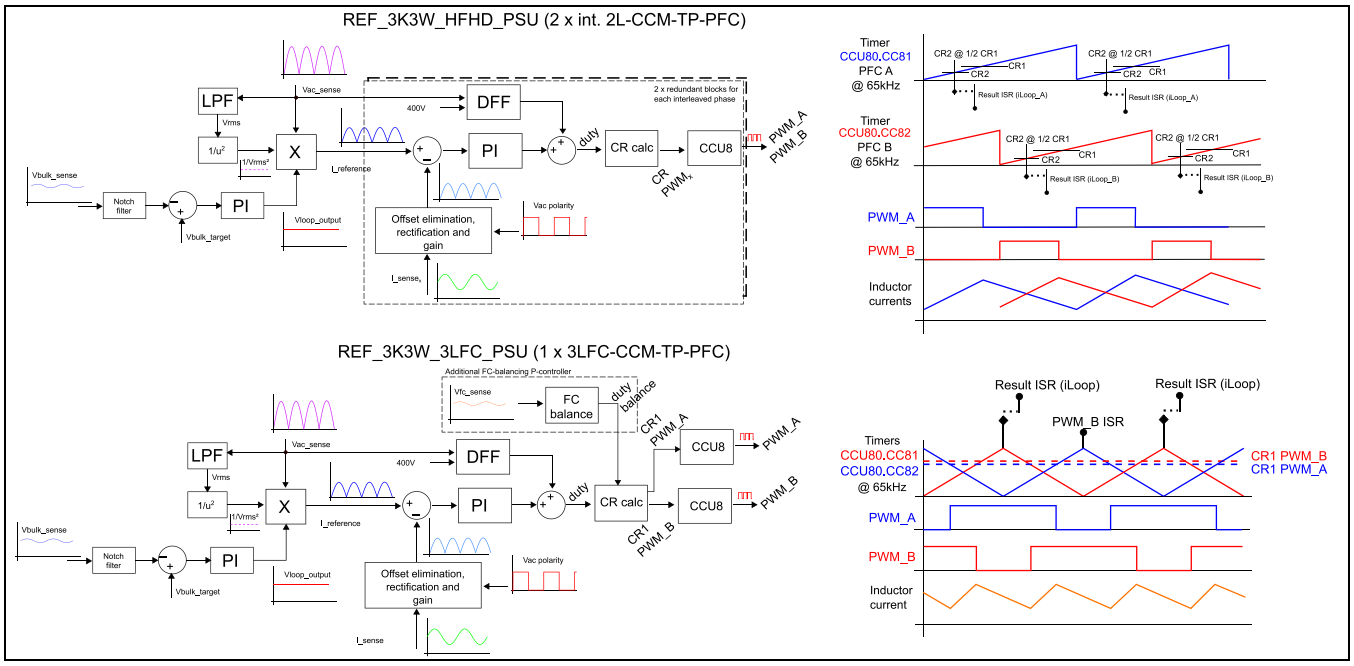


Figure 46 Control block diagrams of 3L flying capacitor and interleaved 2L CCM totem pole PFCs

The developed hardware reference design REF_3K3W_3LFC_PSU is shown in Figure 47. The comparison of efficiencies between the two topologies is shown in Figure 48 for standalone PFC operation, with detailed system level measurements (e.g., startup, LCDO, dynamic load jumps, etc.) covered in [1] and [17]. The peak efficiency with 3L FC PFC is improved by >0.3% and light load efficiency is improved by >0.8 %. In summary, the 3L FC CCM TP PFC provides a higher-efficiency and power density compared to the conventional interleaved 2L CCM TP PFC.

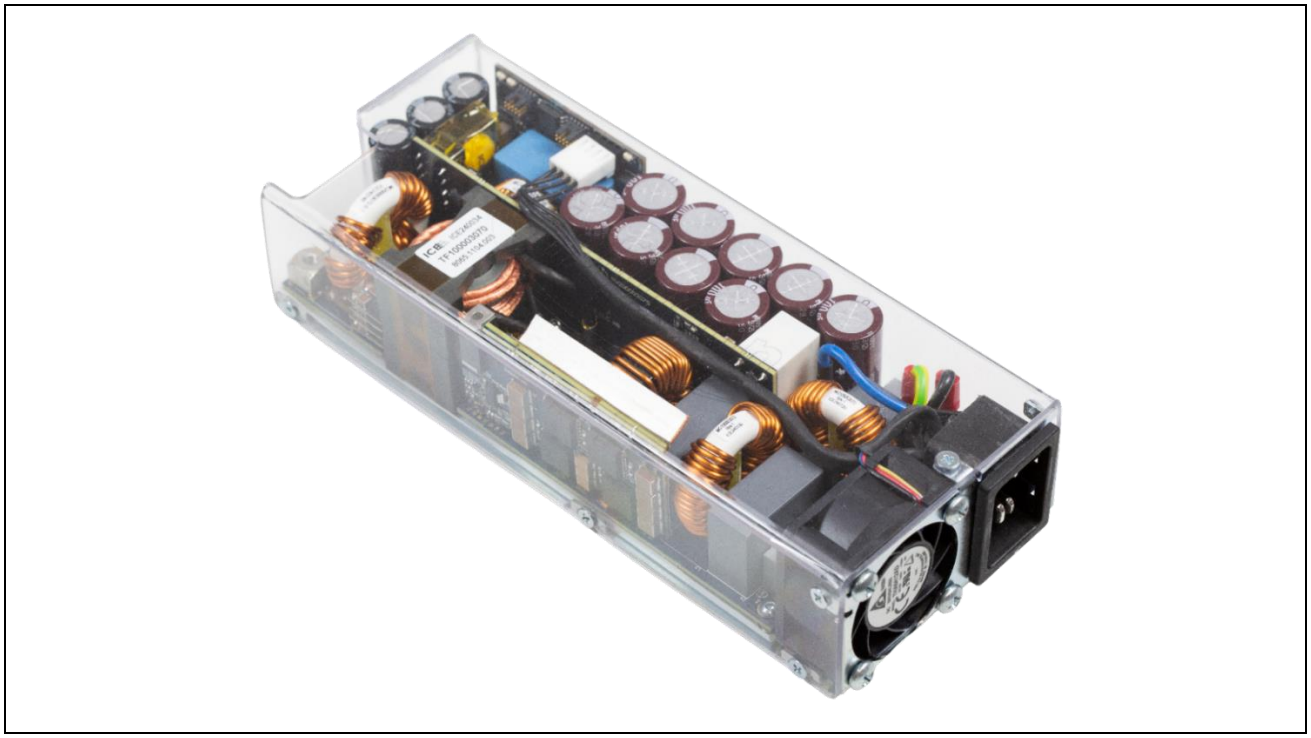


Figure 47 **3.3 kW PSU reference design REF_3K3W_3LFC_PSU [1] using 3-level flying capacitor CCM totem pole PFC with IMT40R025M2H**

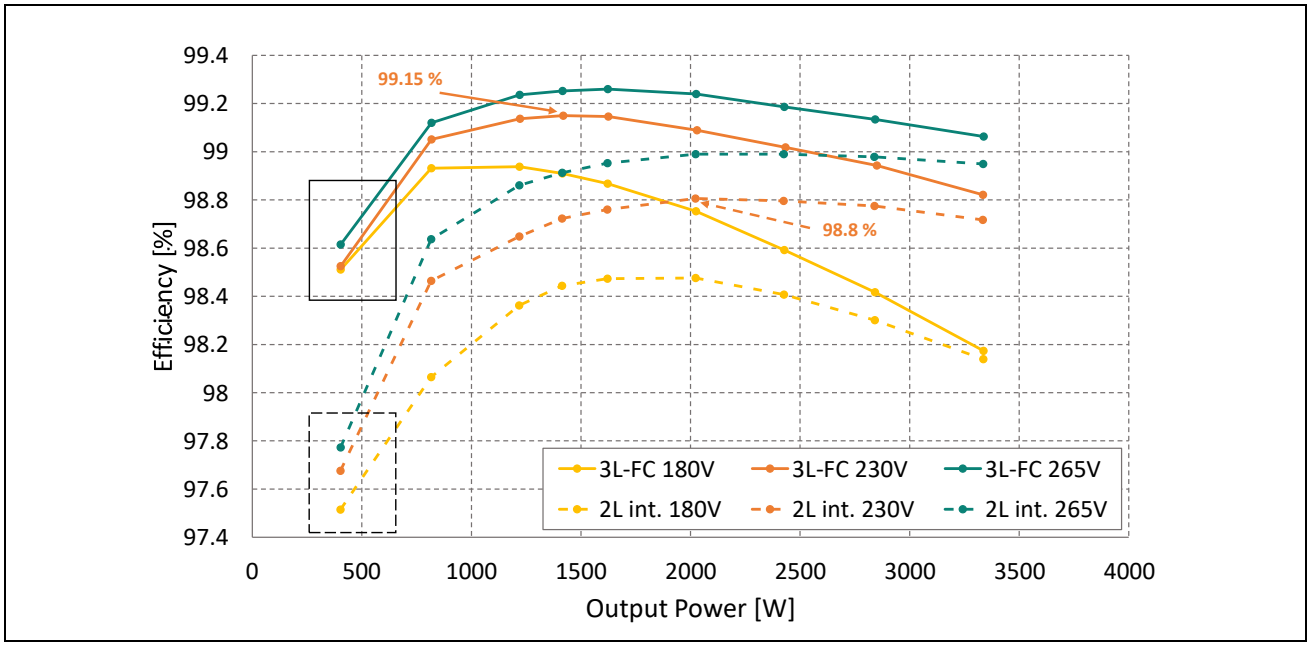


Figure 48 **Measured standalone PFC efficiencies of a 3.3 kW 3L FC CCM TP PFC [1] vs. interleaved 2L CCM TP PFC [17] as a function of output power for various input line voltages**

5.2 3-level flying capacitor DC-DC converters for high-voltage power backup units

A 10 kW hardware demonstrator REF_10KW_3LBUCK_SIC400 [2] with CoolSiC™ 400 V MOSFETs in a 3-level flying capacitor buck DC-DC converter is shown in Figure 49. It can also be configured as a 2-level buck DC-DC converter by shorting the two outer MOSFETs (Q_{HSO} and Q_{LSO}) and replacing the inner two MOSFETs (Q_{HSI} and Q_{LSI}) with 650 V SiC MOSFETs.

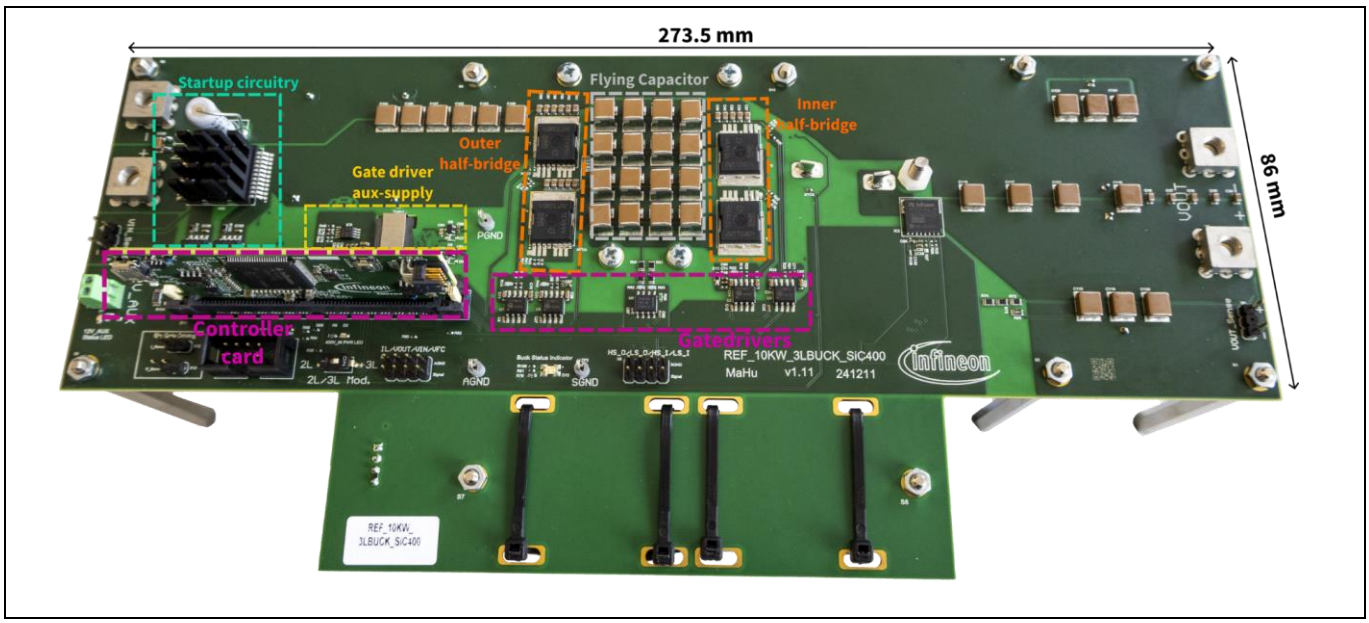


Figure 49 Hardware demonstrator of a 10 kW 3-level flying capacitor DC-DC converter using 400 V SiC MOSFETs for 3-level and 650 V SiC MOSFETs for 2-level operation

The benchmarking between a 2-level and 3-level flying capacitor topology in buck mode and the resulting efficiency comparison is shown in Figure 50 and the thermal comparison shown in Figure 51.

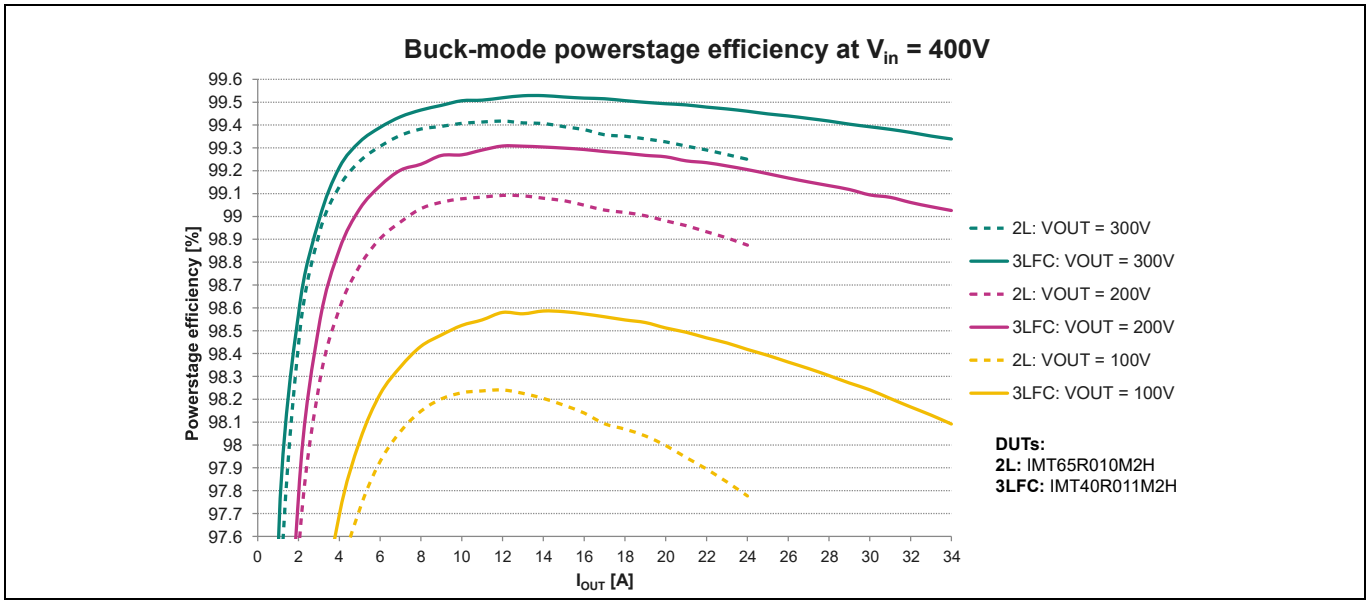


Figure 50 Efficiency measurements as a function of load current in 2-level vs. 3-level converter in buck mode of operation at V_{in} = 400 V various duty cycles and 65 kHz switching frequency

The 3-level flying capacitor topology provides a highly efficient solution, enabling using lower-voltage MOSFETs with enhanced FoMs. With an efficiency of over 99.3% at 300 V output and 10 kW output power, the reduced energy losses and thermal distribution across four MOSFETs enable increased current capacity per phase in high-power, interleaved multi-phase designs.

Due to the reduced voltage-time product applied to the inductor, a potential 4x decrease in inductance requirements is possible. For a given inductor size, the lower equivalent series resistance (ESR) and core losses lead to a 41.7% increase in current handling capacity per phase in a multi-phase, high-power design with interleaved phases. This, in turn, reduces the number of interleaved stages, increasing power density and freeing up space for additional Li-ion batteries or capacitors, further boosting energy density.

However, implementing the 3-level flying capacitor topology poses challenges, including increased control complexity due to the need for pre-charging and balancing the flying capacitors, as well as the requirement for a higher number of pulse-width modulation (PWM) channels. These challenges were already addressed in the Section 4.1 on 3-level flying capacitor CCM TP PFCs.

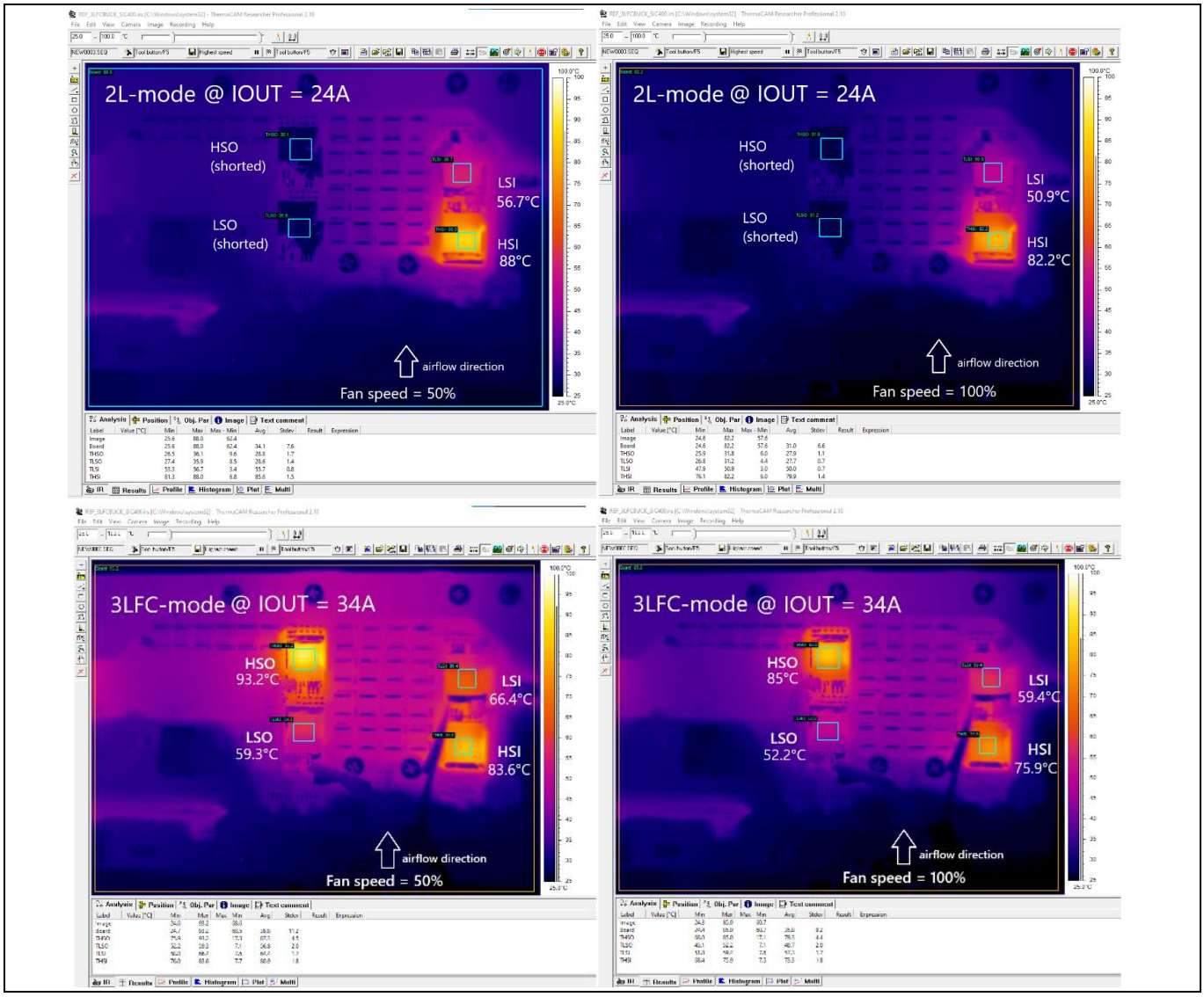


Figure 51 Thermal steady-state measurements at max load current in 2-level vs. 3-level flying capacitor DC-DC converter in buck mode of operation with V_{in} = 400 V at D = 0.75 [2]

5.3 3-level active neutral point clamped inverter for inverter applications

The hardware demonstrator for the 3L-ANPC inverter introduced in EVAL_10KW_3LANPC_SIC [18] is shown in Figure 52. The board is designed as a topology evaluation platform to address DC-AC inverter applications like motor control drives and grid-tied inverters for solar or energy storage systems. The inverter has 18 x 11 mΩ CoolSiC™ G2 400 V MOSFETs in TOLL package, which offers high reliability due to the absence of MOSFET paralleling, while also offering high efficiency due to the high-voltage DC bus operation up to V_{DC} = 600V.

To provide the highest flexibility covering a wide range of application requirements, an output filter is not populated on board. The power stage efficiency was measured using an inductive resistive load (1mH + variable resistance) excluding the gate driver and controller stage losses. The auxiliary supply card for gate driving provides 18 isolated gate drive voltages and uses a reliable and cost-effective solution based on a planar PCB transformer in a forward converter. The 4H2L modulation scheme introduced in Section 4.2.1 is used with an “open loop” Sine-PWM modulator.

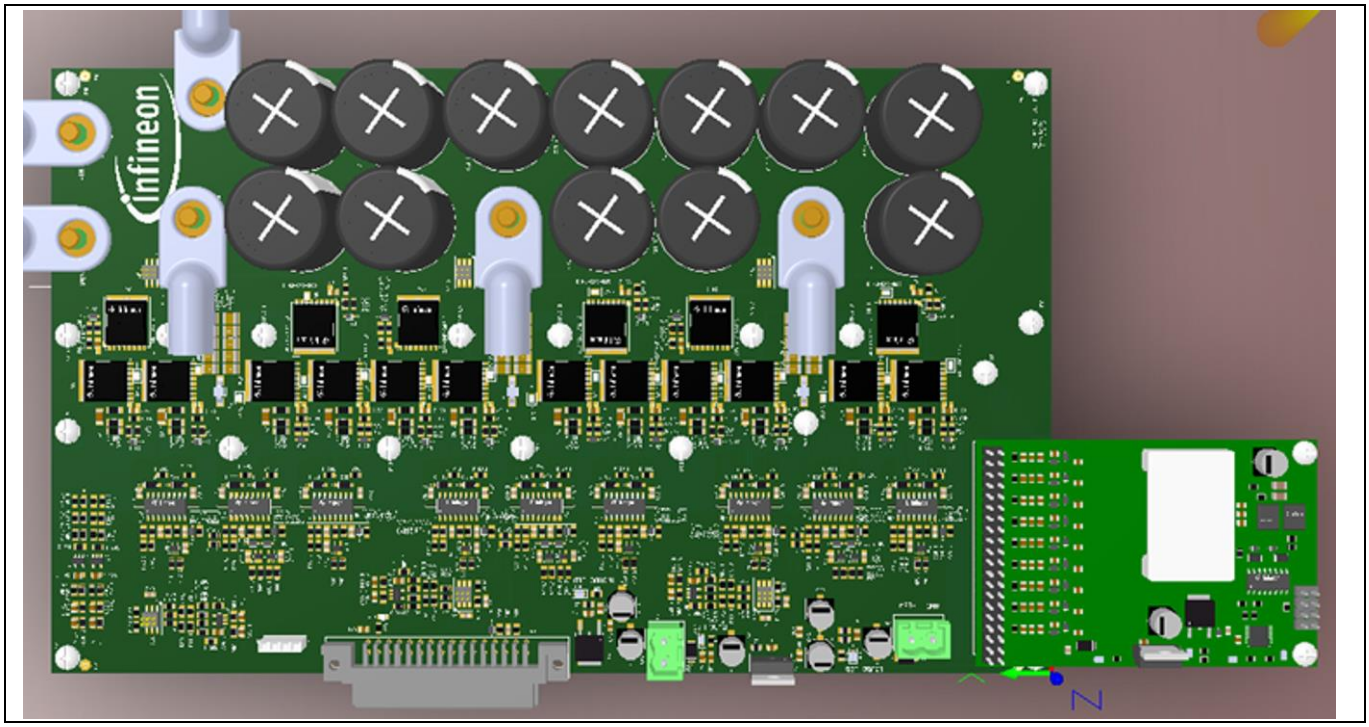


Figure 52 Hardware demonstrator of a 10 kW 3L-ANPC inverter using CoolSiC™ 400 V MOSFETs [18]

5.3.1 Application tests to emulate motor control drives

To emulate the application conditions encountered in a motor control drive inverter application, the inverter was configured to run at a switching frequency of 10 kHz with a dv/dt per switch limited to < 5 V/ns for a DC-bus voltage of V_{DC} = 600 V, as discussed in [10]. The efficiency measurements are shown in Figure 53, while the switching waveforms are shown in Figure 54.

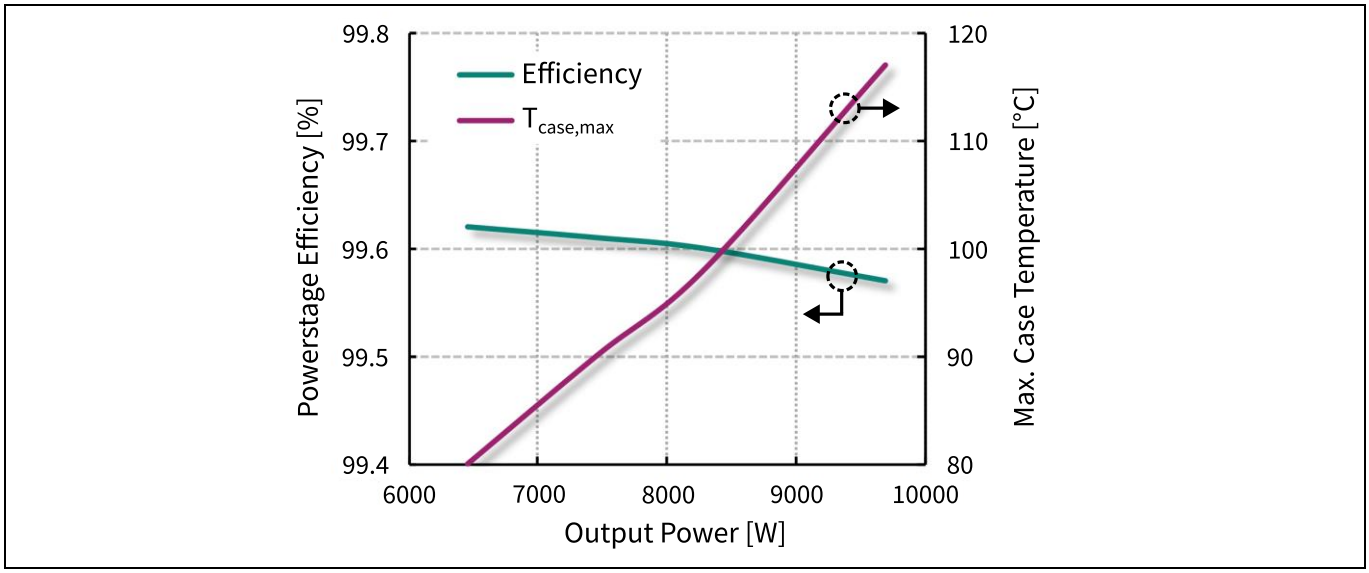


Figure 53 **Measurement of power stage efficiency and max. case temperature without heat sink, with V_{DC} = 600 V, f_{sw} = 10 kHz, t_{dead} = 500 ns, dv/dt = 5 V/ns, $R_{g,ext,on,off}$ = 30 Ω [10]**

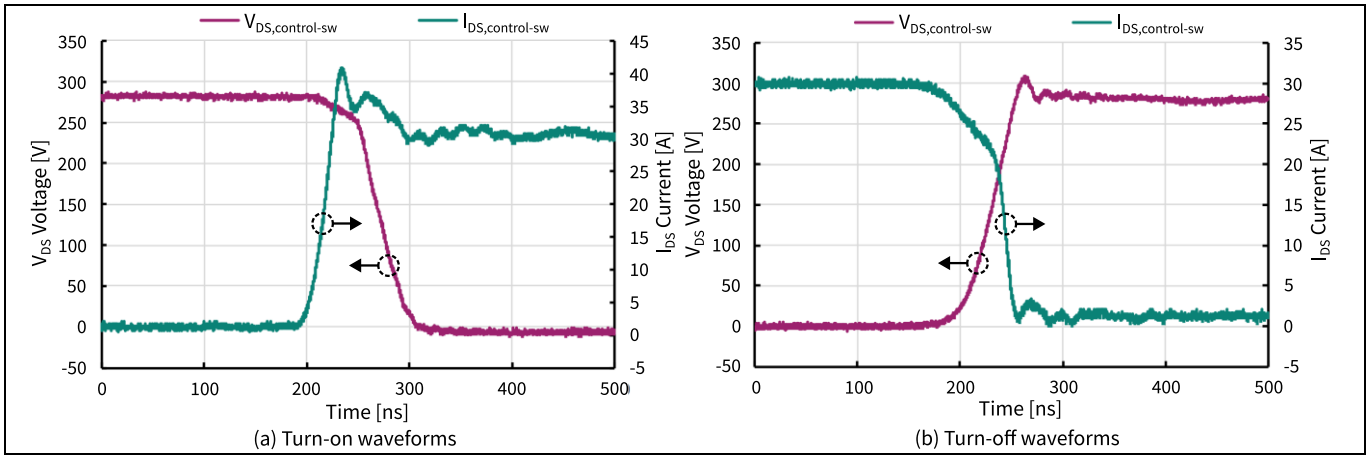


Figure 54 **Turn-on and turn-off waveforms of the hard-switching control switch using a double-pulse test with V_{test} = 300 V, I_{test} = 30 A, di/dt = ~750 A/µs, dv/dt = 5 V/ns, $R_{g,ext,on,off}$ = 30 Ω [10]**

5.3.2 Application tests to emulate grid-tied inverters for solar and energy storage systems

To emulate the application conditions encountered in a grid-tied inverter application, the inverter is configured to run at a switching frequencies of 10 kHz and 30 kHz with a dv/dt per switch limited to < 10 V/ns for a DC-bus voltage of V_{DC} = 400 V, as discussed in [19]. The efficiency measurements are shown in Figure 55, while the switching waveforms are shown in Figure 56.

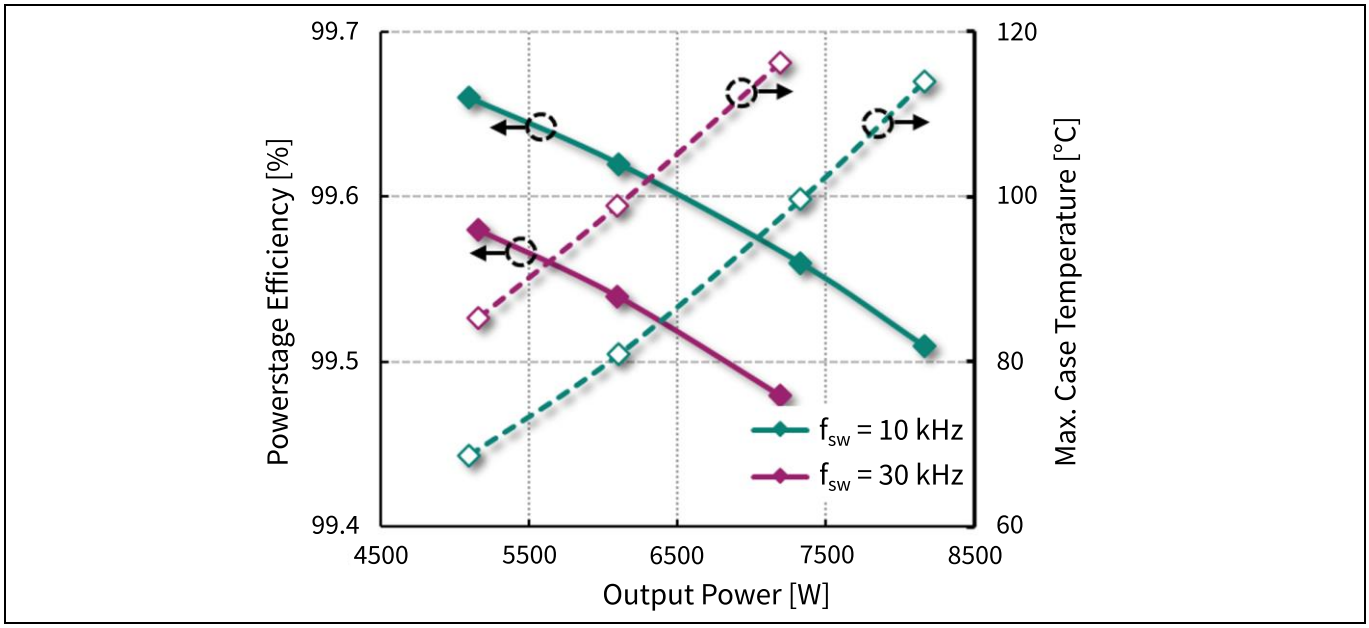


Figure 55 **Measurement of power-stage efficiency and max. case temperature without heatsink, with V_{DC} = 400 V, f_{sw} = 10 & 30 kHz, t_{dead} = 500 ns, dv/dt = ~10 V/ns, $R_{g,ext,on,off}$ = 15 Ω/0 Ω [19]**

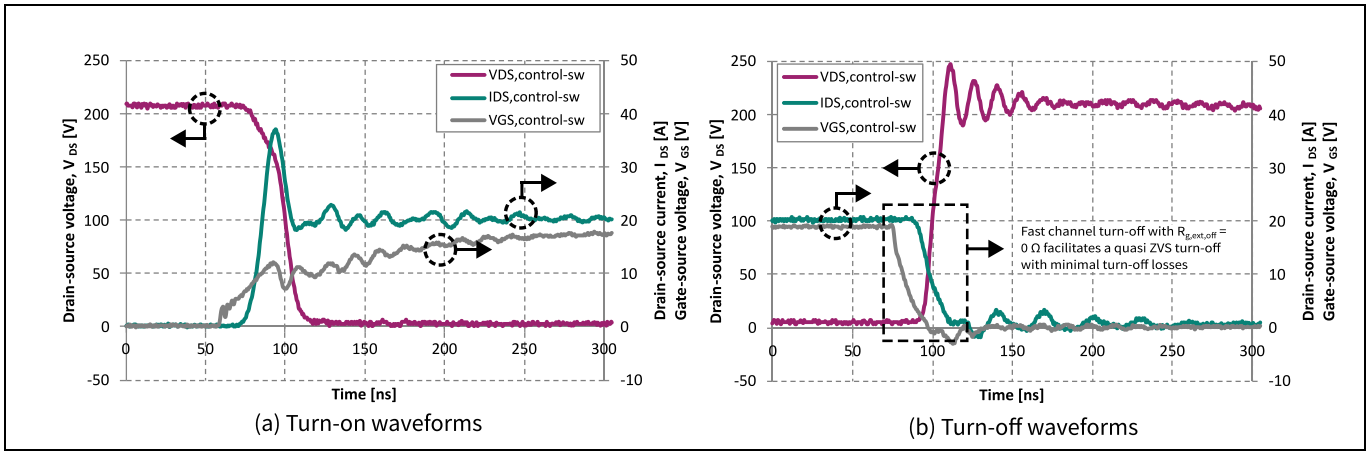


Figure 56 **Turn-on and -off waveforms of the hard-switching control switch using a double-pulse test with V_{test} = 200 V, I_{test} = 20 A, di/dt = ~2500 A/µs, dv/dt = ~10 V/ns, $R_{g,ext,on,off}$ = 15 Ω /0 Ω [19]**

5.4 2-level B6 inverter for motor control application

The hardware demonstrator for 2-level B6 inverter introduced in EVAL_10KW_B6_SIC400V [20] is shown in Figure 57. The board is designed as a topology evaluation platform to address DC-AC inverter applications for motor control drives. The inverter has 6 x 11 mΩ CoolSiC™ G2 400 V MOSFETs in TOLL package which offers high reliability due to the absence of MOSFET paralleling, while also offering high efficiency due to the high-voltage DC bus operation up to V_{DC} = 300 V. To provide the highest flexibility covering a range of application requirements, an output filter is not populated on board. The power stage efficiency was measured using a motor load, excluding the gate driver and controller stage losses.

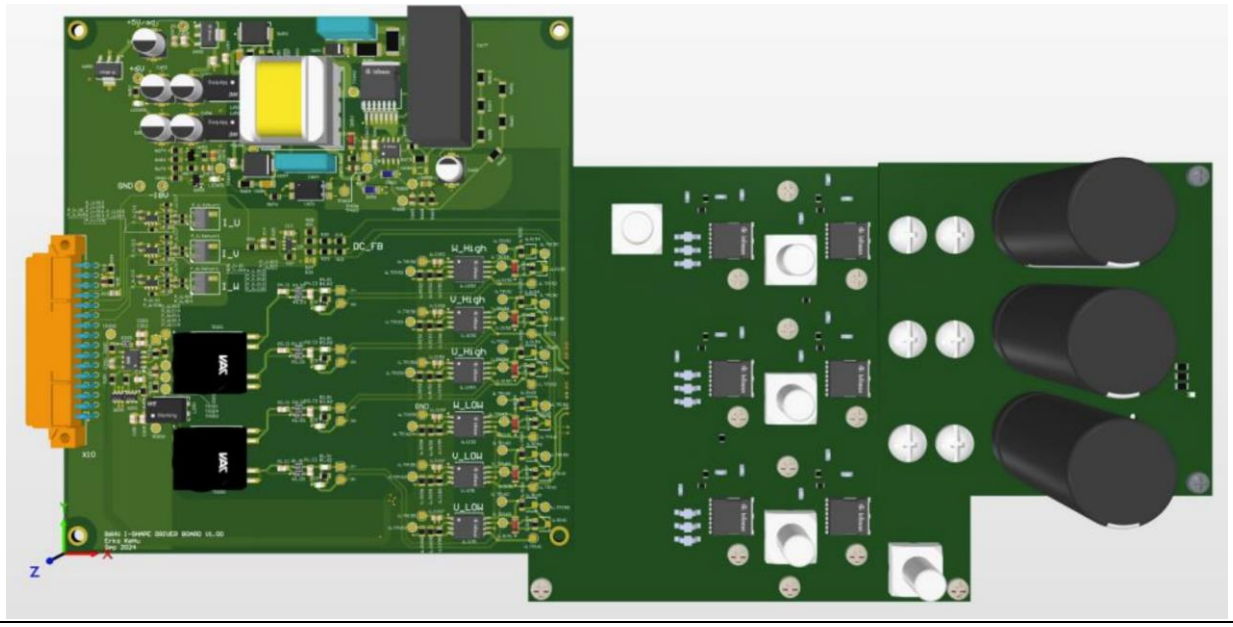


Figure 57 Hardware demonstrator of a 10 kW 2L B6 inverter using CoolSiC™ 400 V MOSFETs [20]

To emulate the application conditions encountered in a motor control drive inverter application, the inverter is configured to run at a switching frequency of 10 kHz with a dv/dt per switch limited to < 5 V/ns for a DC bus voltage of V_{DC} = 300 V. The efficiency measurements are shown in Figure 58, while the switching waveforms are shown in Figure 59.

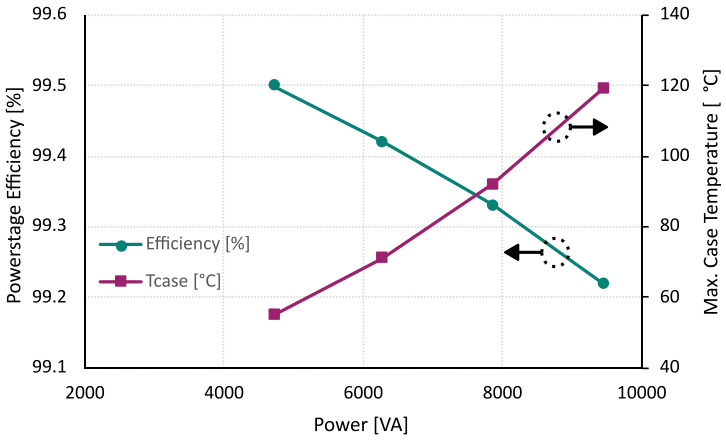


Figure 58 Measurement of power stage efficiency and max. case temperature without heatsink, with V_{DC} = 300 V, f_{sw} = 10 kHz, t_{dead} = 150 ns, dv/dt = 5 V/ns, $R_{g,ext,on,off}$ = 15 Ω/20 Ω [20]

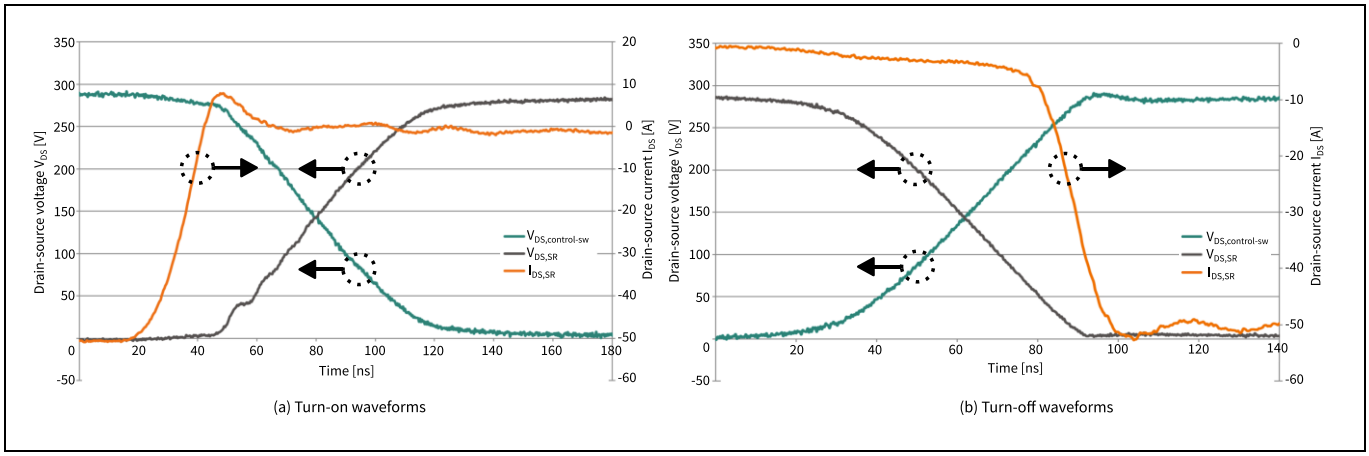


Figure 59 **Turn-on and -off waveforms using a double-pulse test with V_{test} = 300 V, I_{test} = 50 A, dv/dt = ~5 V/ns, $R_{g,ext,on,off}$ = 15 Ω/20 Ω [20]**

5.4.1 Application benchmarking a high-voltage (288 V) vs. a low-voltage (48 V) motor control drive

CoolSiC™ G2 400 V MOSFETs enable the design of 2-level B6 inverter motor control drive systems with higher battery voltages up to 288 V. Compared to conventional 48 V drives, increasing system voltage yields higher efficiency and power density. Due to the reduced currents, it has a much lower copper requirement, translating into lower system costs. There is also a potential to reduce and even eliminate paralleling of MOSFETs, which improves system reliability. Figure 60 shows an improvement of up to 38% in power output for a given maximum case temperature limit of 120°C, along with switching waveforms.

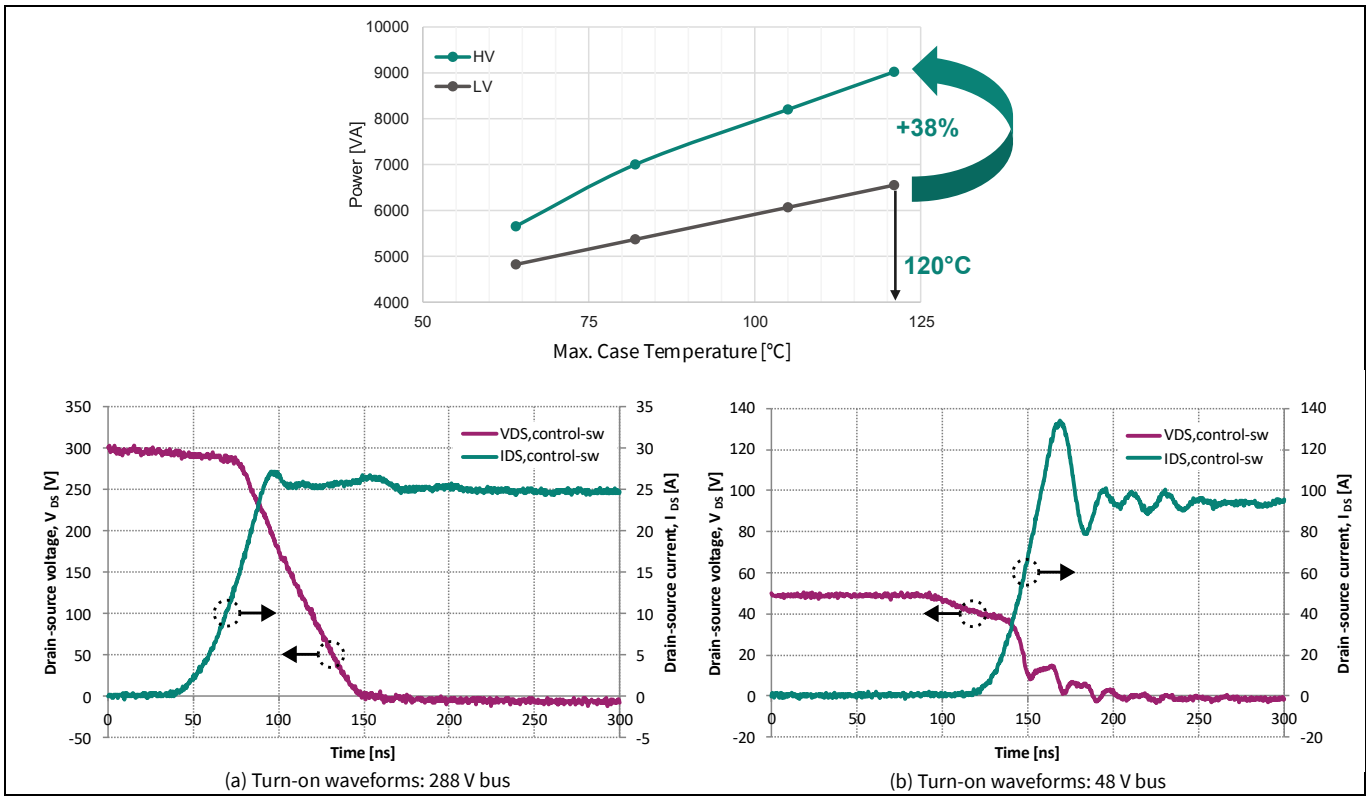


Figure 60 **Thermal benchmarking of a 288 V vs. 48 V drive system and turn-on waveforms using a double pulse test with dv/dt = ~5 V/ns**

5.5 Class-D audio amplifier

The hardware reference design for Class-D audio using CoolSiC™ G2 400 V MOSFETs is shown in Figure 61. The reconfigurable and flexible platform supports three packages – TOLT, TO247-4, and TOLL, with each package configuration of the board having a unique power rating dictated by the thermal stack.

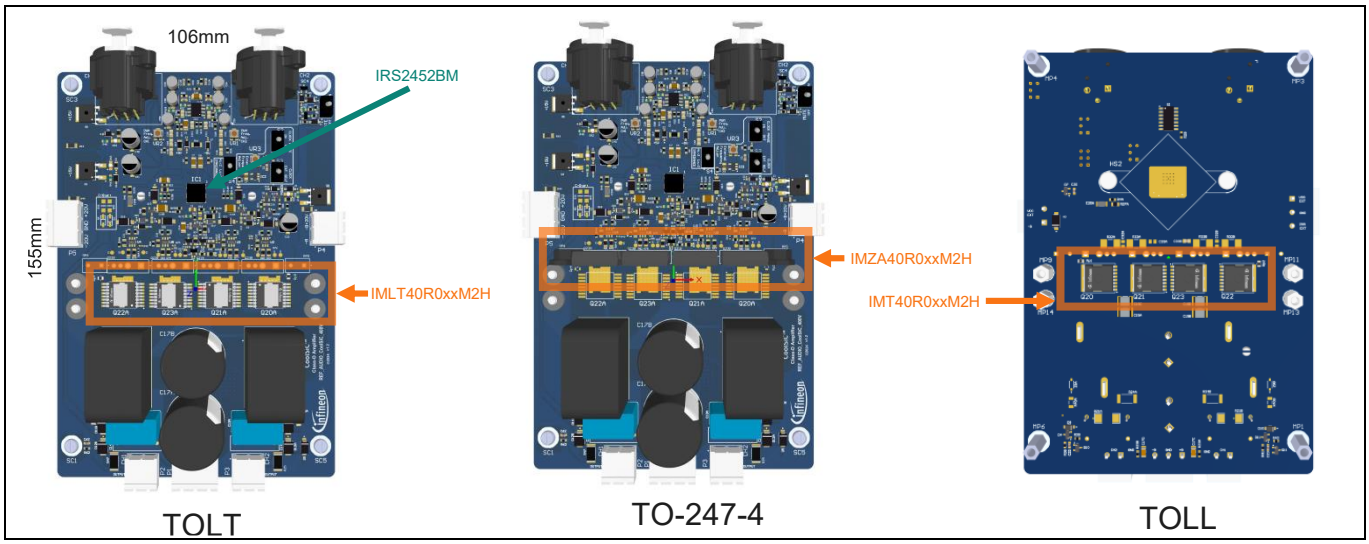


Figure 61 Hardware reference design for Class-D audio amplifiers using CoolSiC™ G2 400 V MOSFETs

The THD+N values measured in high-Z 10 Ω and low-Z 4 Ω loads are shown in Figure 62 and the worst-case thermal measurements at low-Z

4 Ω condition is shown in Figure 63. The measurements were taken with IMZA40R045M2H, bus voltage V_{BUS} = +/- 148 V, switching frequency f_{sw} = 300 kHz, and audio frequency f = 1 kHz.

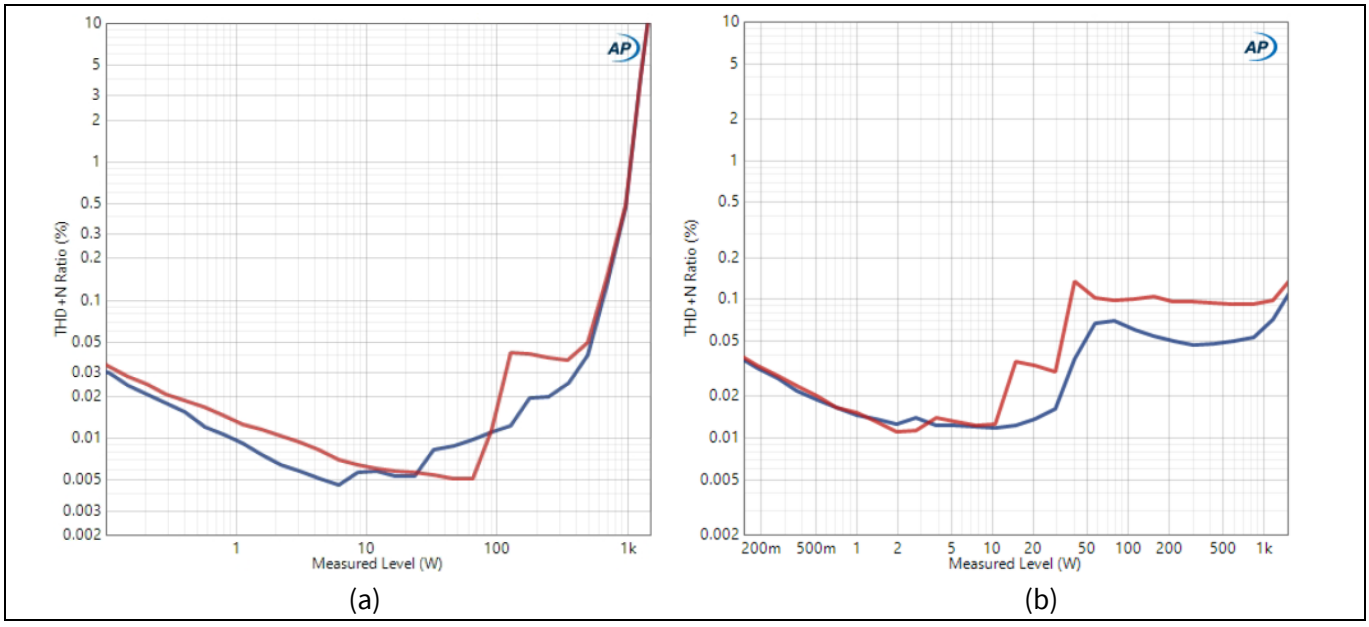


Figure 62 THD+N measurements at (a) high-Z 10 Ω and (b) low-Z 4 Ω loads using IMZA40R045M2H

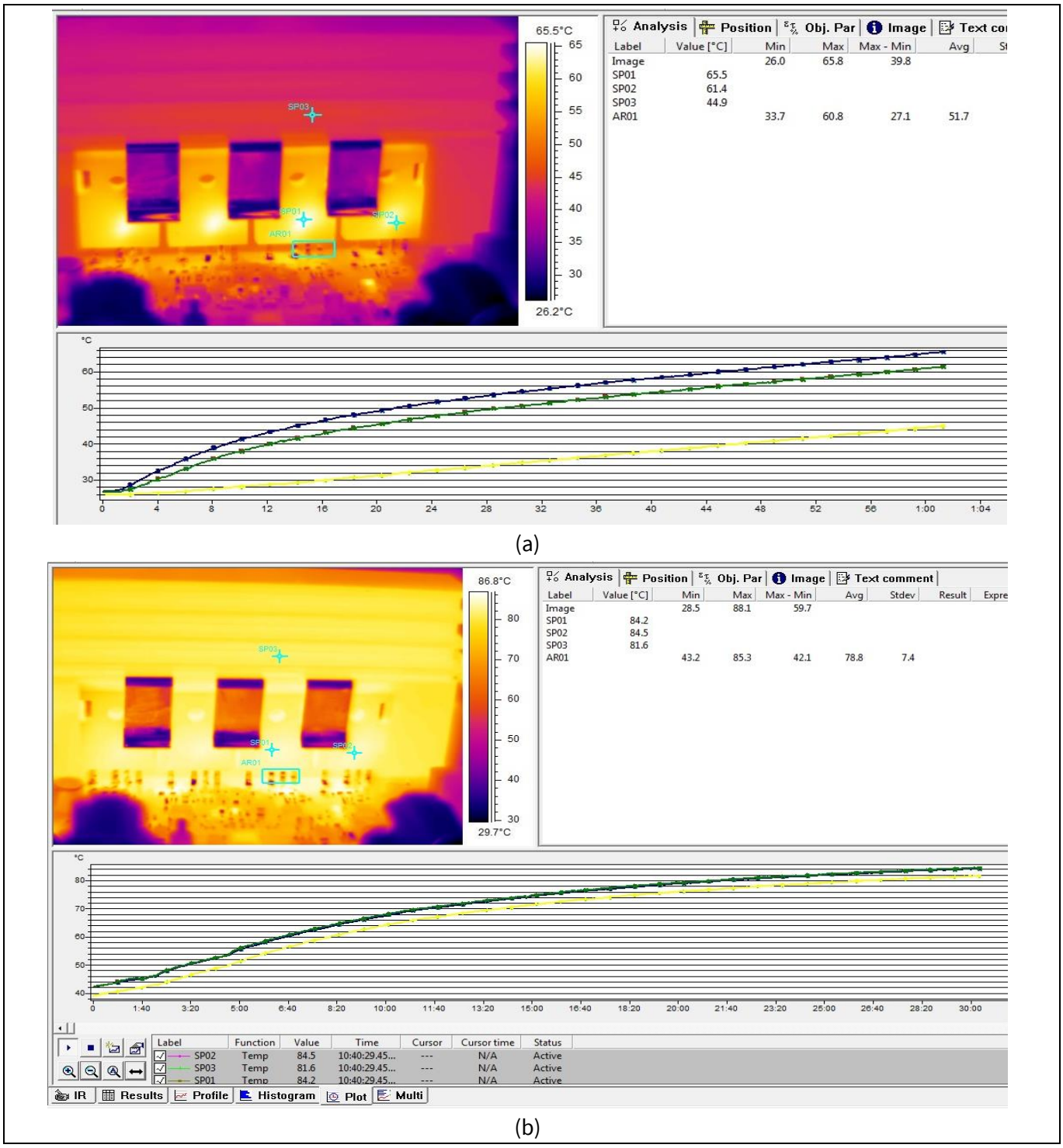


Figure 63 Thermal measurements at (a) 1000 W x 2 / 4 Ω after 1 minute and (b) 125 W x 2 / 4 Ω after 30 minutes using IMZA40R045M2H

Short circuit protection was tested to verify the ruggedness of CoolSiC™ 400 V IMZA40R045M2H MOSFETs under abnormal conditions of operation. OCP was set to 67 A, which is thrice the nominal load at 1000 W /4 Ω load. The measurements were performed for bus voltage V_{BUS} = +/- 150 V, switching frequency f_{sw} = 300 kHz, and audio frequency of 1 kHz. Figure 64 shows the waveforms under continuous output short condition and Figure 65 shows the waveforms with dead output short under operation at 1000 W /100% load.

Figure 64 **Continuous output short waveforms using IMZA40R045M2H, (a) Overview and (b) Zoomed; CH1 = CSD, CH2 = V_{DD} of gate drive, CH3 = V_S, CH4 = Output current from a Rogowski coil**

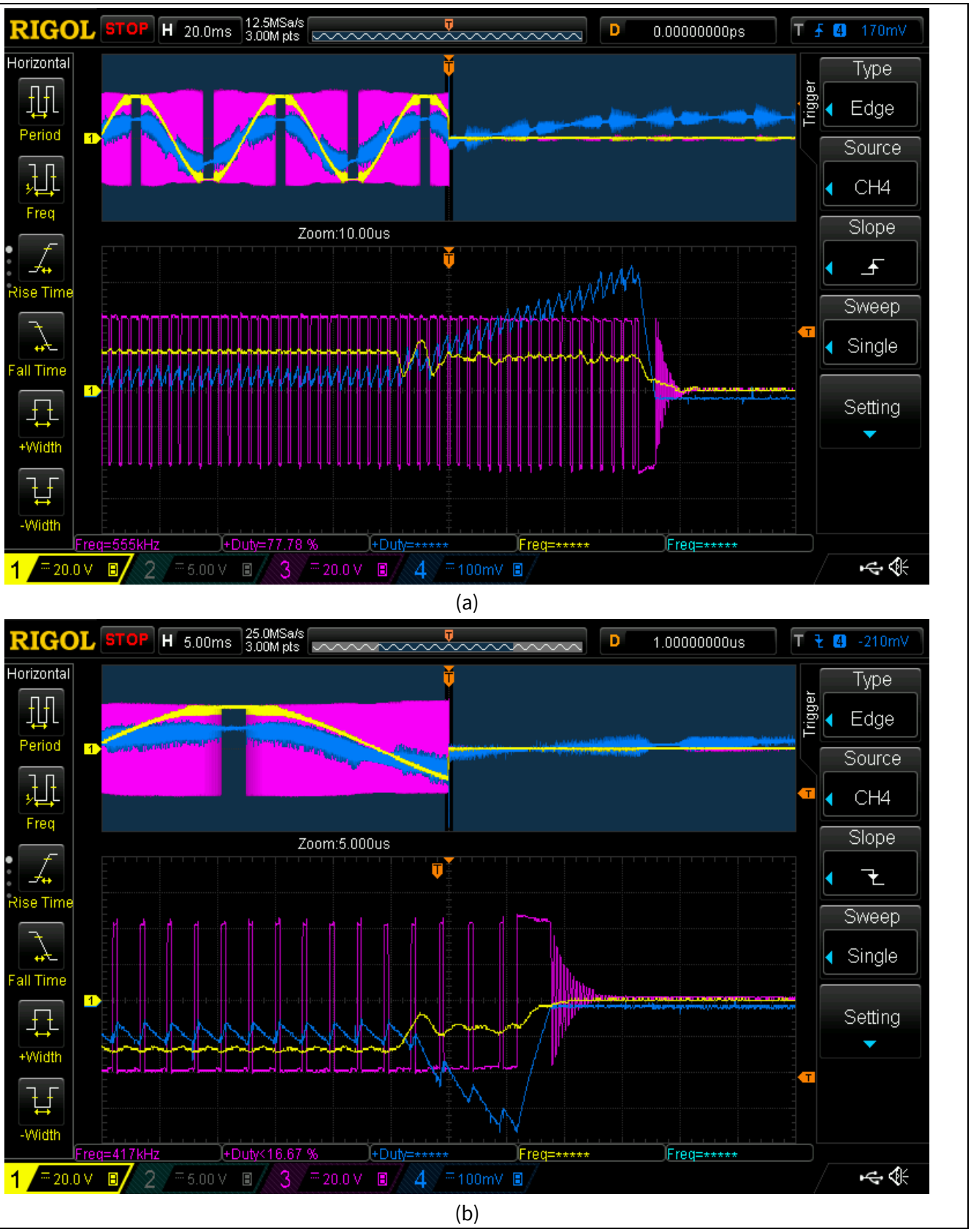


Figure 65 **Output short under 100% load using IMZA40R045M2H, (a) high-side and (b) low-side short; CH1 = Output, CH2 = V_{DD} of gate drive, CH3 = V_S, CH4 = Output current from a Rogowski coil**

6 Summary

This document describes the newest second generation of CoolSiC™ MOSFETs in a new voltage class of 400 V/440 V. The improvements in switching and conduction FOMs achieved with Infineon’s industry leading trench SiC MOSFET technology – optimized for 400 V/ 440 V blocking voltage – indicate the benefits of adopting multilevel topologies.

It also provides further details about the technology and product features. The superior gate oxide allows using negative gate driving while the thermal coefficient point lies below 15 V, resulting in a full 15 V capable driving scheme. The key target applications and topologies for this new voltage class are discussed in detail, with the benefits of the technological parameters demonstrated through application results showcasing the highest efficiency and ease of use in end applications.

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