CoolSiC™ JFET

Cascode Evaluation Board for Solid-State Circuit Breaker Applications

Featuring the latest generation of silicon carbide (SiC) JFETs

About this document

Scope and purpose

This application note introduces the design principles, features, and functionality of the evaluation board utilizing Infineon's 750V and 1200V CoolSiC™ JFET technology. It covers the unique capabilities of the cascode configuration and the evaluation board in back-to-back (B2B) configurations.

Key use cases such as single pulse inductive clamping, repetitive inductive clamping, and dV/dt ruggedness are discussed.

Intended audience

The intended audience for this document are design engineers, technicians, and developers of electronic systems.

Table of contents

About this document **1**
Table of contents **2**
1 Introduction **3**
1.1 CoolSiC™ JFET technology 3
1.2 Avalanche capability 4
2 CoolSiC™ JFET in cascode configuration **8**
2.1 Why cascode configuration 8
2.2 Gate drive concept 10
3 CoolSiC™ JFET cascode evaluation board **12**
3.1 Detailed gate drive circuit 16
3.2 Circuit design and layout considerations 16
4 Test set-up **18**
4.1 Single pulse inductive clamping 18
4.2 dV/dt ruggedness test 19
5 Summary **22**
Revision history **23**
Disclaimer **23**

1 Introduction

Solid-state circuit breakers (SSCBs) are increasingly preferred over traditional mechanical circuit breakers due to significant potential benefits. The SSCB has advantages when handling high-current switching and commutations, offering superior performance under demanding conditions. The absence of mechanical contacts ensures arc-free switching and significantly reduced wear and tear. As a matter of fact, this leads to higher reliability, extended operational lifetime, and improved overall system performance.

In SSCBs the CoolSiC™ JFETs switches are commonly selected due to their low on-resistance characteristics. These switches provide huge benefits, as they are fast, reliable, and precise in operation. Furthermore, CoolSiC™ JFETs, being normally-on devices, are particularly well-suited for applications requiring efficient and robust current flow management. Their unique features and capabilities make them an ideal choice for enhancing the performance of modern SSCBs.

While the JFETs normally-on characteristics being a benefit in many application conditions, some applications call for a normally-off device which can be achieved by the JFET cascode configuration. The application note will focus on cascode technology implemented by using CoolSiC™ JFET and LV-MOSFET as separate devices to achieve best-in-class R_{DSon} capability.

1.1 CoolSiC™ JFET technology

CoolSiC™ JFET technology has been developed by Infineon to serve the special requirements of solid-state switching applications. It is optimized for:

- lowest R_{DSon} values to reduce losses in conduction mode
- highest level of switching ruggedness required by this kind of applications in AC or DC systems
- improved control capability to enable effortless integration of solid-state technology into AC or DC power distribution applications.

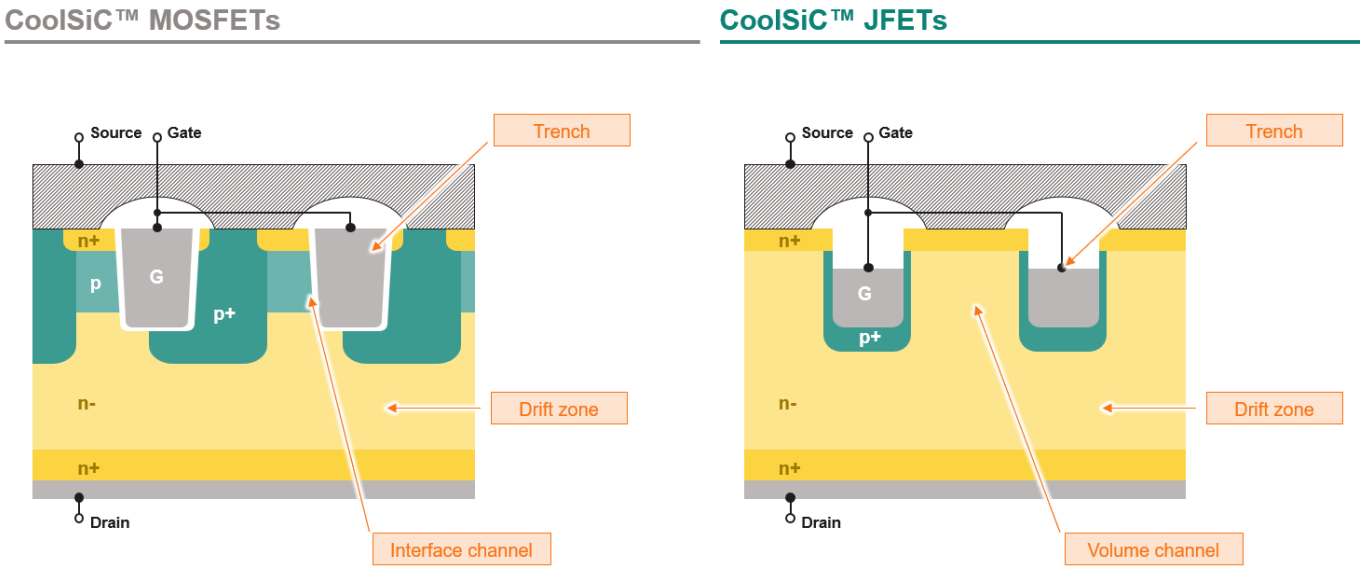

Figure 1 **Overview: CoolSiC™ MOSFET vs. CoolSiC™ JFET technology**

The comparison of the MOSFET cell structure and the JFET cell structure reveals several differences. The most prominent difference is the volume channel of the JFET cell structure being used to conduct the load current. As the volume channel is much wider compared the interface channel of the MOSFET cell structure, the achievable RDSon is much lower per unit area.

Second point to mention is the p-doped gate structure. As it is not shielded towards the drift zone, the gate-drain capacitance of the JFET cell structure is much higher per unit area compared to the MOSFET cell structure. The higher gate-drain capacitance needs to be considered when designing the gate drive circuit.

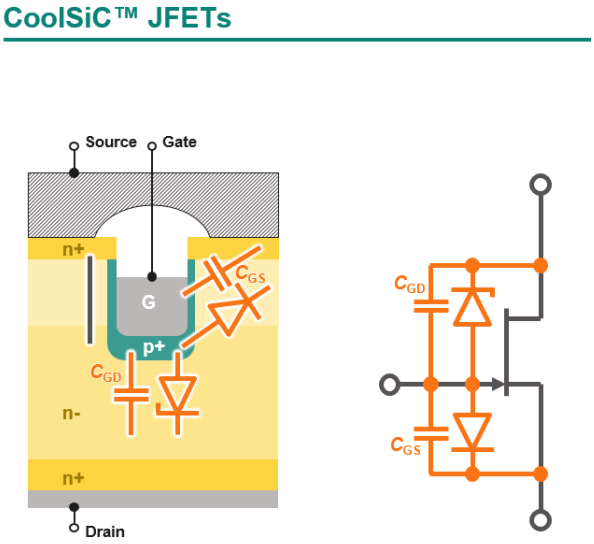

Figure 2 **Overview: CoolSiC™ JFET – equivalent circuit diagram**

The schematic above shows an equivalent circuit representation of the JFET cell structure. While the capacitors are very much similar to the well-known MOSFET structure, the gate-drain and the gate-source diodes are unique to the JFET cell structure. For solid-state switching applications, the gate-drain diode plays a major roll, as it enables very rugged switching characteristics.

For more detailed information on the CoolSiC™ JFET technology and how it compares to CoolSiC™ MOSFET technology, please see separate application note.

1.2 Avalanche capability

CoolSiC™ JFET technology is very well suited to solid-state switching applications due to its inherent rugged switching capability. The following section provides more details on how the JFET avalanche capability is used for this type of application conditions.

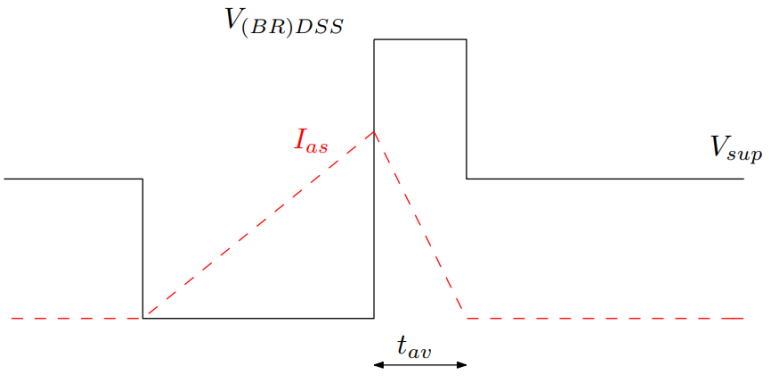

Figure 3 **JFET - avalanche**

The avalanche capability of the CoolSiC™ JFET is specified in the datasheets accordingly. The datasheet provides the characteristic values to specify this feature enabling very rugged switching characteristics need for solid-state switching applications.

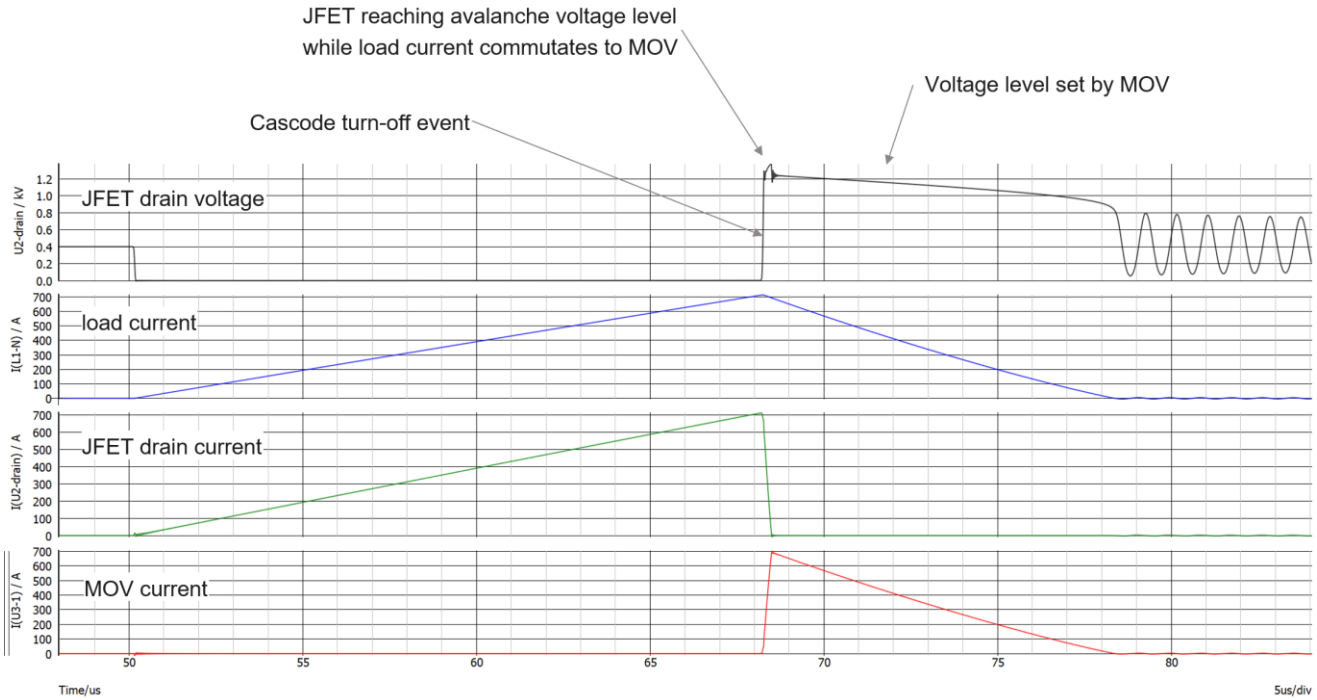

Figure 4 **Turn-off transient waveforms, JFET reaching avalanche voltage level while commutating the load current to MOV.**

As pointed out before, CoolSiC™ JFET technology offers unparalleled switching ruggedness. Even in high inductive operating condition where the stored energy would exceed the avalanche energy limits given in the datasheet, it enables very much simplified circuit design. The JFET can operate with a standard MOV only, as it can be driven into avalanche conditions to support the current commutation to the MOV as the main energy absorbing element. The JFET drain voltage would exceed V_{DSS} and operate in avalanche mode. This operation mode is permitted as long as the max. current level is limited to I_{AS} (see below).

IJCQ120RM23J1
CoolSiC™ 1200 V SiC JFET

1 Package

1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}	reflow soldering (MSL1 according to JEDEC J-STD-020)			260	°C
Thermal resistance, junction-ambient	$R_{th(j-a)}$				62	K/W
JFET thermal resistance, junction – case	$R_{th(j-c)}$			0.045	0.06	K/W

2 JFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		1200	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	$V_{GS} = 2$ V	$T_c = 25$ °C	592	A
			$T_c = 105$ °C	414	
Peak drain current, t_p limited by $T_{vj(max)}$ [1]	I_{DM}	$V_{GS} = 2$ V		TBD	A
I^2t value	$\int I^2t$		$t_p = 30$ µs [2]	TBD	A^2s
			$t_p = 10$ ms [3]	TBD	
Avalanche energy, single pulse	E_{AS}	I_D = TBD, $V_{DD} = 100$ V, $L = 1$ µH		256	mJ
Avalanche energy, repetitive	E_{AR}	I_D = TBD, $V_{DD} = 100$ V		TBD	mJ
Avalanche current, single pulse	I_{AS}	$L = 1$ µH		716	A
Gate-source voltage, max. transient voltage	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.001$		TBD	V
Gate-source voltage, max. static voltage [4]	V_{GS}			-20/2	V
Gate current, static	I_G			TBD	mA
Gate current, pulse	$I_{G,pulse}$			TBD	A
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		$T_c = 25$ °C	2564	W
			$T_c = 100$ °C	1282	

Figure 5 **CoolSiC™ JFET datasheet - Example**

For solid state circuit breaker and power distribution application, the “Avalanche energy, single pulse” and “Avalanche current, single pulse” are most relevant. The first value gives the energy the device can absorb under given conditions, and the second value provides the maximum current in this particular operating mode. Please note, when turning off a high current (> 500A) in highly inductive environment, the device blocking voltage will exceed the nominal blocking voltage V_{DSS} (1200V for the example above) significantly.

Introduction

The JFET device is designed to handle the overvoltage peak (> 1400V for V_{DSS} = 1200V type devices) under given avalanche conditions without failure.

2 CoolSiC™ JFET in cascode configuration

2.1 Why cascode configuration

The CoolSiC™ JFET can be used with two different basic circuits:

- direct JFET circuit, featuring a normally-on characteristics
- JFET in cascode configuration, enabling a normally-off behavior.

The JFET cascode configuration adds an additional low-voltage MOSFET in series connection to the JFET source. By turning off the low-voltage MOSFET the JFET source will be positively biased and, in this way, a negative gate to source voltage at the JFET is created. For the low-voltage MOSFET a normally-off devices is selected, and therefore the JFET will be pushed into blocking mode even no gate signal is present at the low-voltage MOSFET.

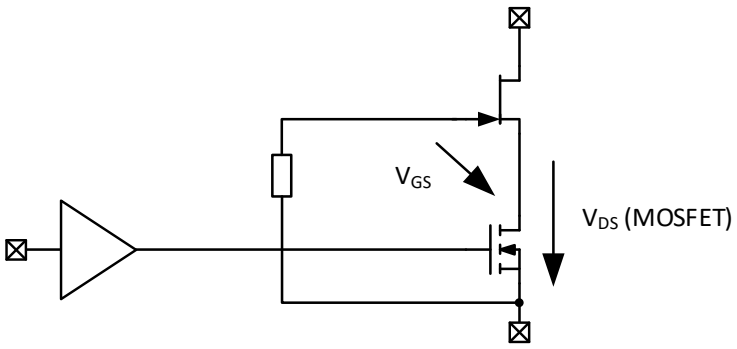

Figure 6 **Cascode basic circuit**

The blocking voltage of the low-voltage MOSFET V_{DS} (Optimos™ 5) is used to provide a negative V_{GS} to the JFET ($-V_{GS} = V_{DS}$). The JFET will block the high voltage according to the selected device, the low-voltage MOSFET blocks only a voltage in the range of the JFET pinch-off voltage level of about 10-20V.

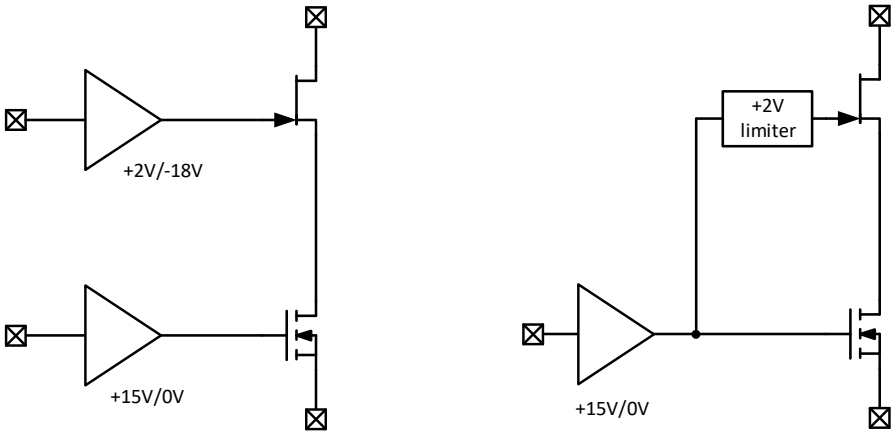

Figure 7 **Driving schematics**

In general, the two power semiconductors can be driven separately or with only a single gate driver. Using separate drivers would enable more control flexibility e.g. JFET for load switching and low-voltage MSOFET for safe turn-off only. The single driver cascode configuration will switch both devices at the same time but requires significantly less components and board space.

While the dual driver configuration allows separate control of both switches, it requires quite high effort to be implemented. As separate control capability is not required for SSCB type application, the single drive scheme is preferred. This application note focusses on the single driver scheme.

For more information on the direct JFET circuit and characteristics, please see separate application note.

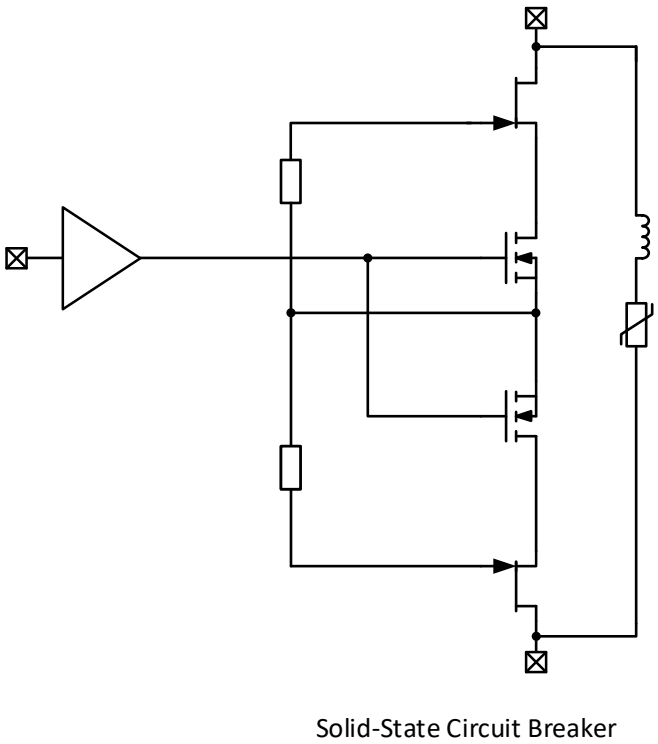

Figure 8 **Typical JFET-Cascode configuration for SSCB application**

Figure 8 shows a typical configuration for solid state circuit breaker (SSCB) applications. Bidirectional blocking and conduction capability is required for AC applications. To handle inductive energy of line and/or load a metal oxide varistor (MOV) is added in parallel to the bidirectional cascode assembly. In case of fast commutation of load current to the MOV, the leakage inductance of the MOV parallel path becomes a critical parameter. The JFET cascode will be driven into avalanche conditions for the time needed to complete the commutation.

Later it will be shown that the JFET can handle this special switching condition and provides very rugged switching performance.

2.2 Gate drive concept

The CoolSiC™ JFET requires a gate voltage of +2V for optimal turn-on and a negative value of -18V for turn-off. Even the JFET device would be able to conduct load current at +0V at the gate, overdriving the gate to +2V reduces the effective R_{DSon} by ~8-10%.

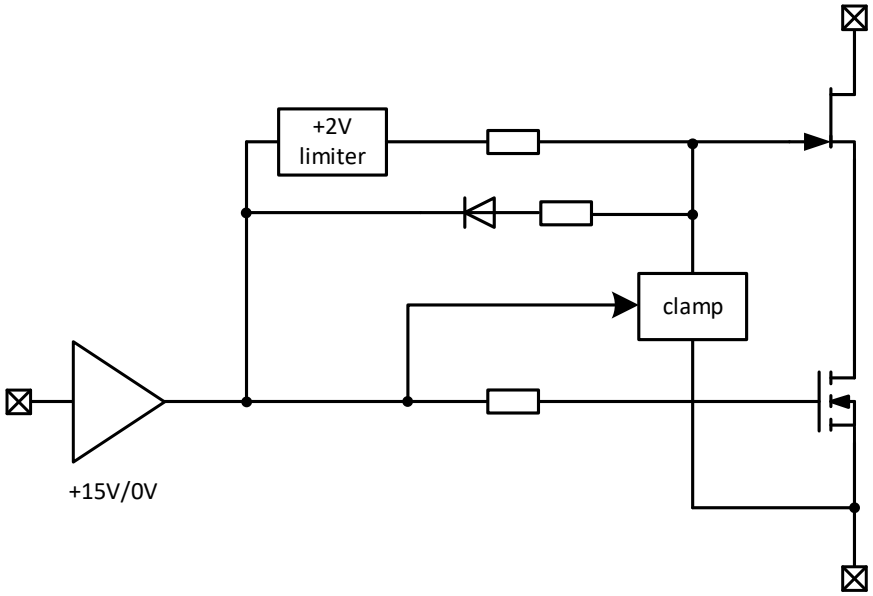

Figure 9 **JFET Cascode gate driver block diagram**

The above block diagram (Figure 9) shows the essential parts of the single drive JFET cascode. For the main driver a standard MOSFET gate drive IC providing +15V/0V driving capability is selected (e.g. 1ED3124MU12H). The output of the device drives the low-voltage MOSFET directly via a resistor, separate resistors for turn-on and turn-off can be used.

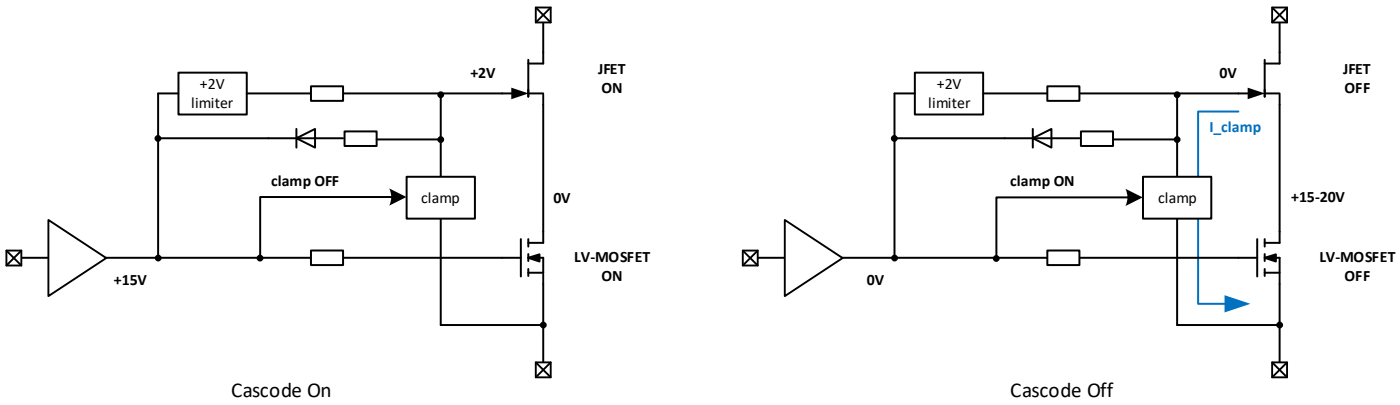

Figure 10 **Switching states**

When switched on, the gate drive IC provides positive gate bias to the LV-MOSFET and to the JFET gate pin. Positive gate bias at the JFET gate is limited to +2V, not to drive the gate-source diode of the JFET into conduction mode. Even though the JFET is a normally-on semiconductor device, a light positive gate bias of +2V reduces the effective R_{DSon}. Positive gate bias of the LV-MOSFET connects the JFET source potential to the reference. The clamp circuit is disabled as it is not used in on-mode.

When switching off the JFET cascode circuit, the gate drive IC will switch to 0V output and turn-off the LV-MOSFET as well as it will provide 0V reference to the JFET gate. When the LV-MOSFET turns off, its drain potential will rise to roughly 15-20V, which in provide a more positive source potential to the JFET with respect to the 0V potential at the JFET gate generating a negative gate-to-source voltage for the JFET and will turn-off the device. To prevent the JFET gate from being positively biased in case of dV/dt induced gate current the clamp circuit is enabled. The clamp circuit will short any gate current to the reference potential (I_{CLAMP}).

3 CoolSiC™ JFET cascode evaluation board

The evaluation board is used to demonstrate the performance of the JFET cascode circuit in solid-state circuit breaker application. The board is connected to the load circuit via P5 and P7. On the control or primary side of the board, +24V auxiliary power supply is connected as well as digital pulse signal for switching.

The board uses isolated DC/DC converter with low coupling capacitance and appropriate isolation rating to power the gate drive circuit. Isolated gate drivers are used to control the JFET and the LV-MOSFETs.

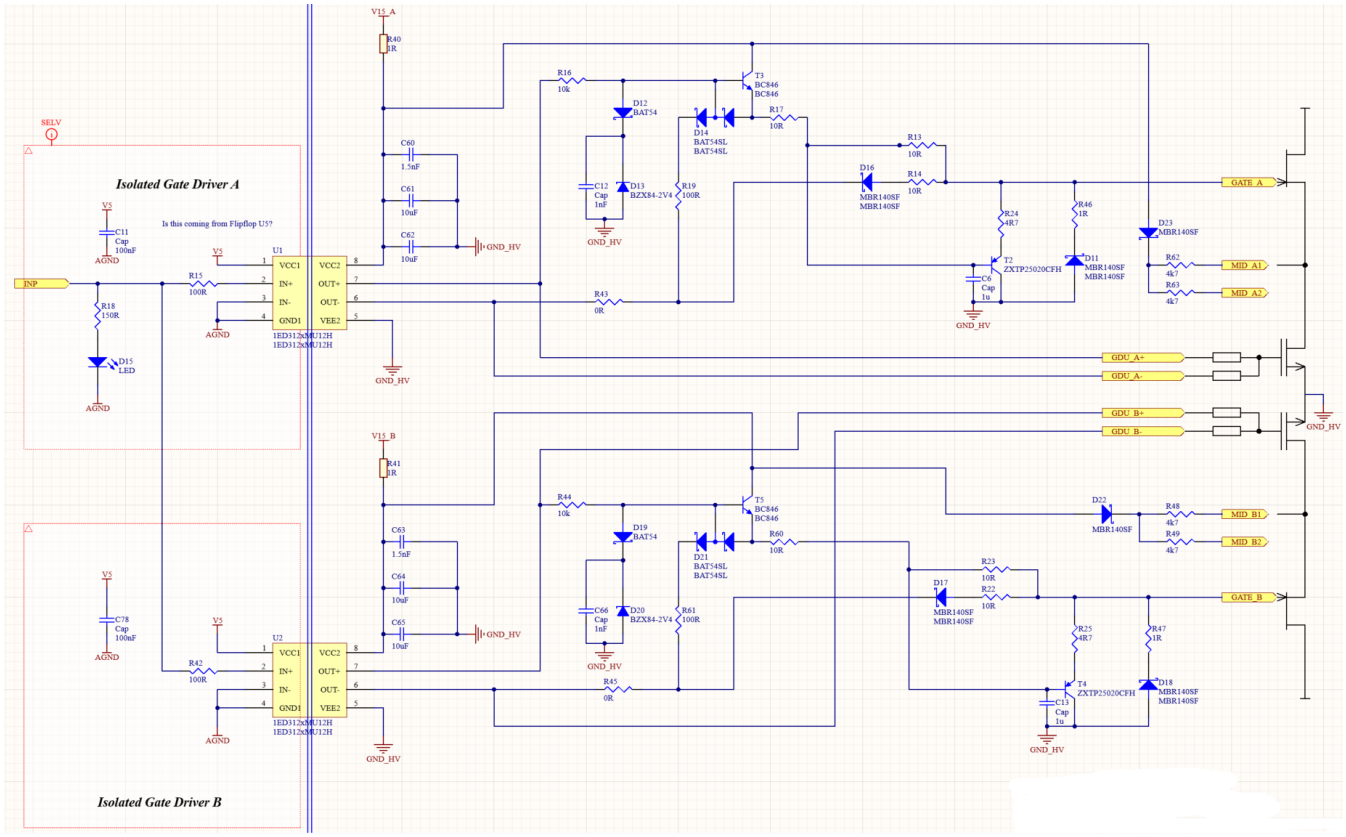

Figure 11 **Gate drive schematics**

Each of the JFET cascode circuits connected back-to-back are controlled via separate gate drive circuit to prevent coupling and provide higher gate drive current capability.

The gate drive circuit shown in Figure 11 features a +2V positive overdrive of the JFET gate. The gate drive circuit is designed to enable positive overdrive of the JFET power device from a single +15V power supply only.

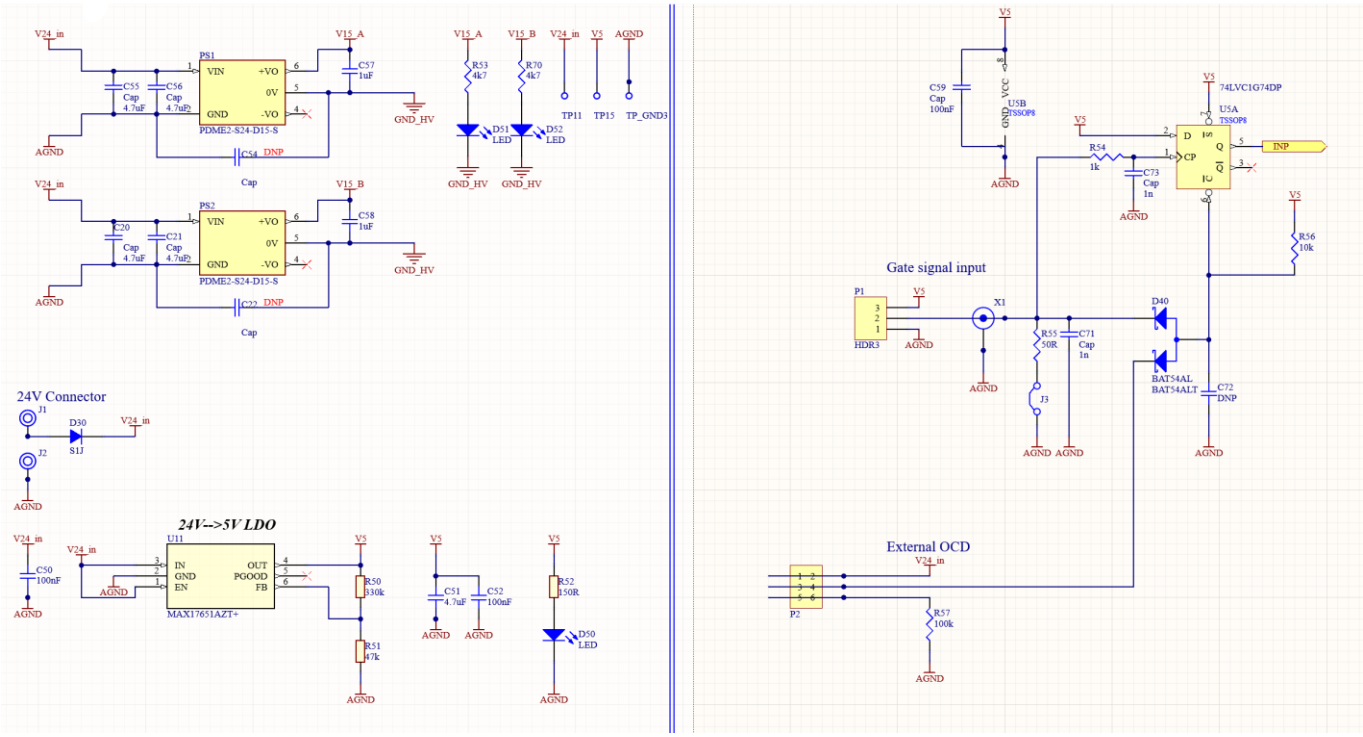

Figure 12 **Gate drive power supply**

The two gate drivers are supplied by separate DC/DC converters to provide stable power supply to each of them. To secure proper switching, the control signal is routed via a pulse shaping circuit.

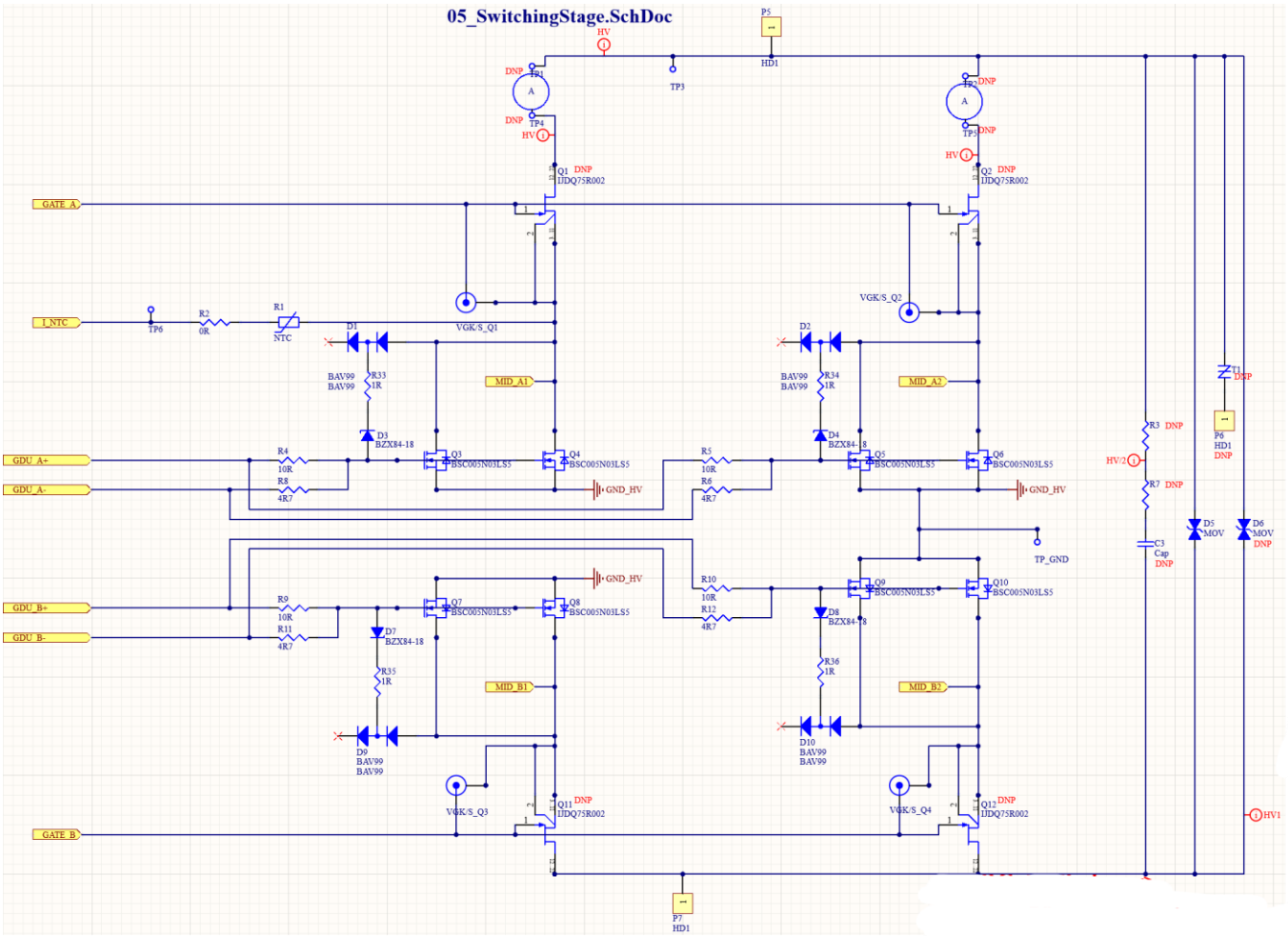

Figure 13 **Power stage schematics**

The power stage has two cascode circuits connected back-to-back to provide blocking capability in positive as well as negative voltage direction as needed for AC applications. It can be used with one set of JFET / LV-MOSFET populated per directions for lower power applications or with two per position.

To reduce the effective R_{DSon} of the full circuit, per on JFET two LV-MOSFETs are connected in parallel.

As it can be seen in Figure 13, the power stage has a metal-oxide varistor installed in parallel to limit the maximum power loss the JFETs are exposed to. This is in particular necessary if used in high inductive environments and with high turn-off current values.

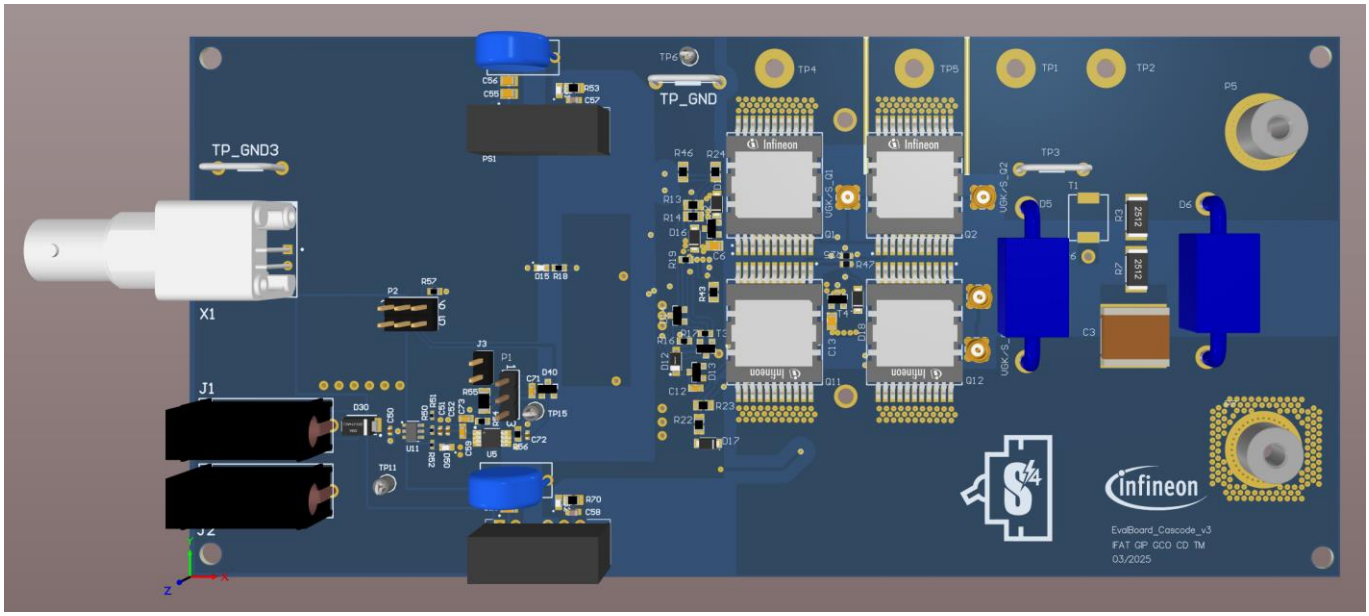

Figure 14 **Evaluation board (photo top-side)**

The top-side shows the CoolSiC™ SiCJFET components in Q-DPAK housing in the middle of the board. On the left side the +24V control power connections and the switching signal connection is located, while the power circuit connections are located on the ride side of the board.

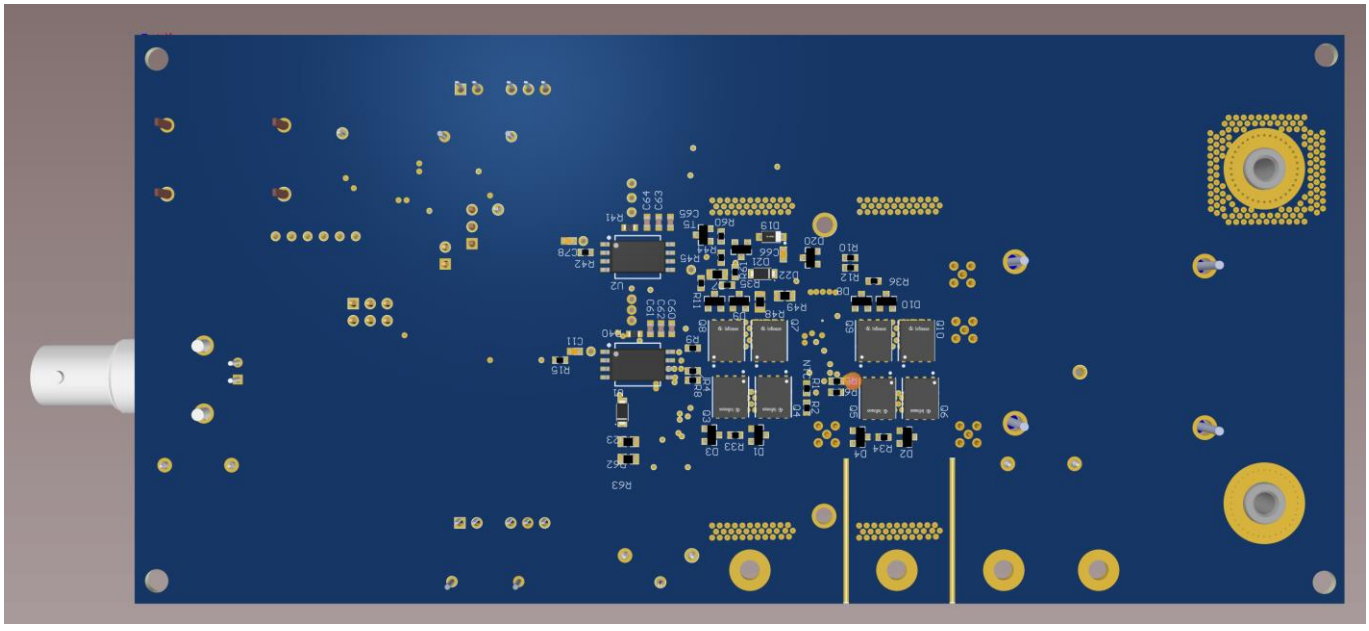

Figure 15 **Evaluation board (photo back-side)**

In the center of the back-side of the board the LV-MOSFET devices are visible. Two LV-MOSFET are used per JFET to reduce the on-resistance to lowest possible values. The LV-MOSFET are placed just below the source connections of the JFET devices to minimize the loop inductance.

3.1 Detailed gate drive circuit

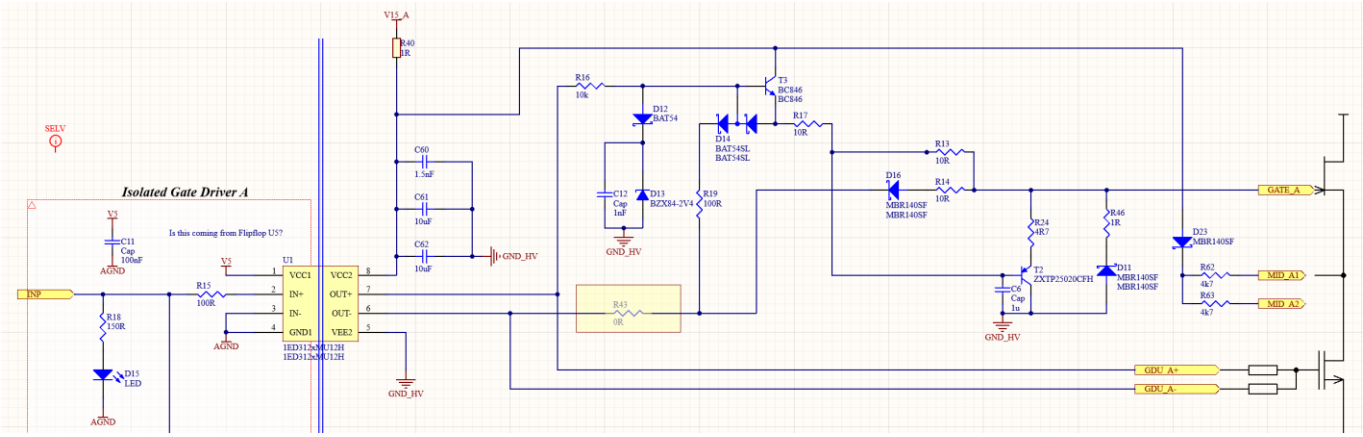

Figure 16 **Detailed gate drive**

The gate drive scheme is based on standard Infineon gate drive device. A component of 1ED312xMU12H family is used. The design provides isolation between the control to power side of the circuit and high pulse current capability.

The two outputs (OUT+ / OUT-) are driving the LV-MOSFET in a conventional way via separate gate resistors. The positive gate drive required to drive the LV-MOSFET (+15V) is way higher compared to the recommended JFET overdrive of +2V. The emitter follower circuit of T3 limits the gate driver output to the JFET required level. The voltage is set by selection of D13.

Even though the CoolSiC™ SiCJFET is a normally-on device, a positive overdrive is recommended to reduce the effective RDSon. Please referred to the JFET datasheet.

Close to the JFET gate connection a clamp circuit is used (T2 / D11). While the gate driver is in on-mode, the transistor T2 enables a positive overdrive of the JFET gate without creating a high gate power consumption. In case the JFET gate potential rises above the set gate voltage level, transistor T2 starts conducting and the JFET gate voltage level is clamped. D11 serves as a standard gate protection to clamp the JFET gate potential to GND.

A special condition can be observed in case the JFET cascode does not block voltage in the load circuit. Assuming no blocking voltage being present, the mid-point potential (MID_A1 / MID_A2) is very low and does not provide a negative bias to the JFET gate. To prevent this unwanted situation, the mid-point is biased via D23 and R62 respectively R63 to +15V. This ensures a secure negative bias of the JFET gate.

3.2 Circuit design and layout considerations

In chapter 1, the main differences between the JFET cell structure and the MOSFET cell structure have been pointed out. Considering the increase in gate-drain capacitance of the JFET cell structure, the gate drive circuit has to be designed to handle higher peak currents compared to MOSFET gate driver circuits.

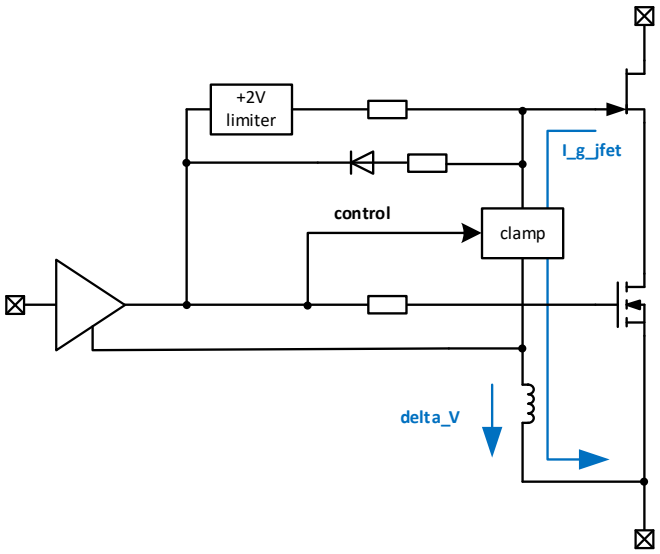

Figure 17 **Not optimized gate driver**

Due to high gate current peaks in the JFET gate loop, special attention has to be paid to the circuit design as well as the board layout of the same. The sketch above (Figure 17) shows a none optimized implementation. When the cascode circuit is turning off, the drain voltage of the JFET will rise to the blocking voltage level. Via the gate-drain capacitance of the JFET, this dV/dt will cause a peak current through the clamp circuit. In case the circuit is not optimized well, the clamp peak current may cause a voltage drop (delta_V) which can turn-on the LV-MOSFET. Re-turn on of the LV-MOSFET causes the JFET to re-turn on and the cascode to oscillate.

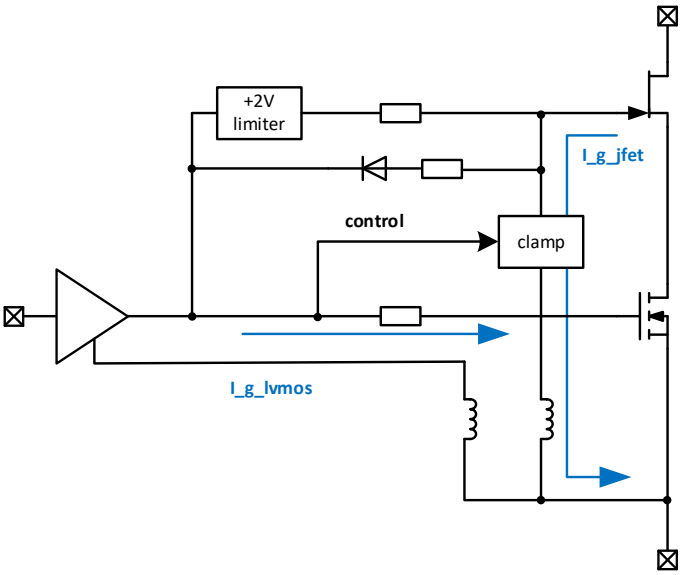

Figure 18 **JFET / MOSFET gate drive loops separated**

An optimized gate circuit shall provide separate loops for JFET gate control and LV-MOSFET gate control with minimal impedance coupling. Furthermore, the components of the gate drive circuit shall be designed to handle the high JFET gate current peaks. When using multiple JFETs in parallel, this may require separate clamp circuit per individual JFET.

4 Test set-up

4.1 Single pulse inductive clamping

In a solid state circuit breaker application or other type of power distribution applications like DC grids or battery disconnects, the semiconductor switch needs to be able to withstand very high surge currents. The semiconductor needs to be able to turn-off the mentioned high surge events even under high inductive operating conditions. The JFET is very well suited here, as it can be driven into avalanche mode to dissipate the inductive energy or to facilitate the commutation of the surge current to a metal-oxide varistor. The CoolSiC™ JFET can operate in avalanche mode at extremely high current rating (> 500A).

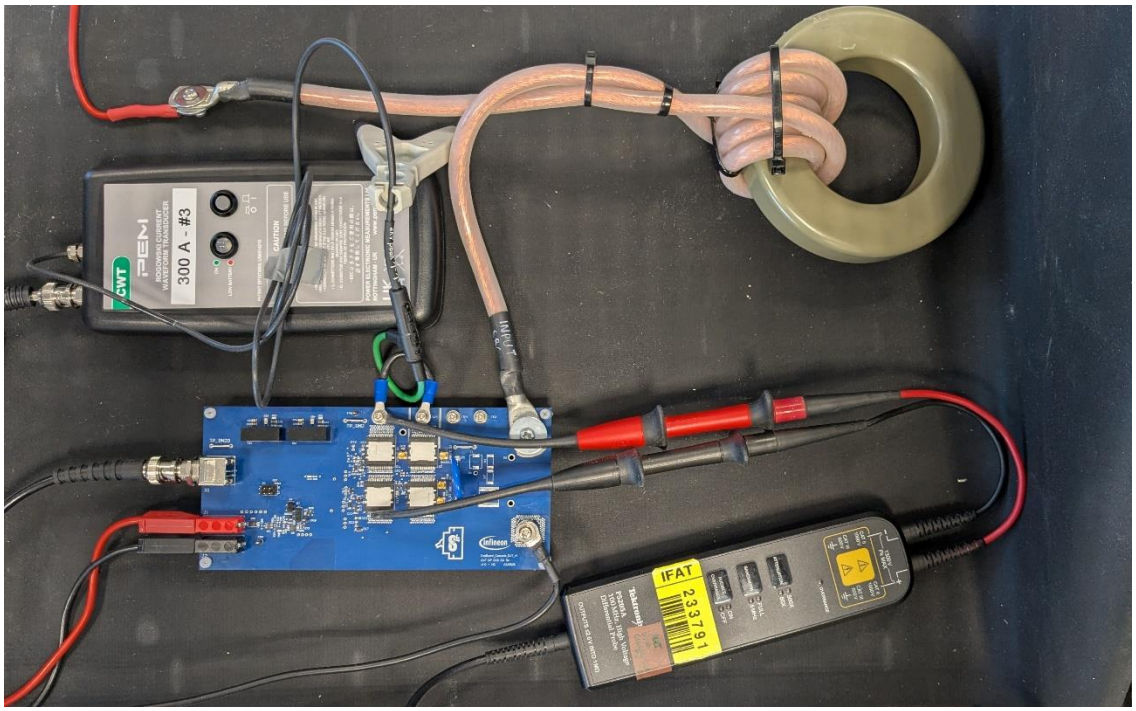

Figure 19 **Test set-up (photo of evaluation board w/ inductor and probes)**

The following test results are considering the CoolSiC™ JFET switching a DC current provided by a DC power supply for easier referencing.

The lab test uses a line/load inductor of ~5µH to represent the inductance under application conditions.

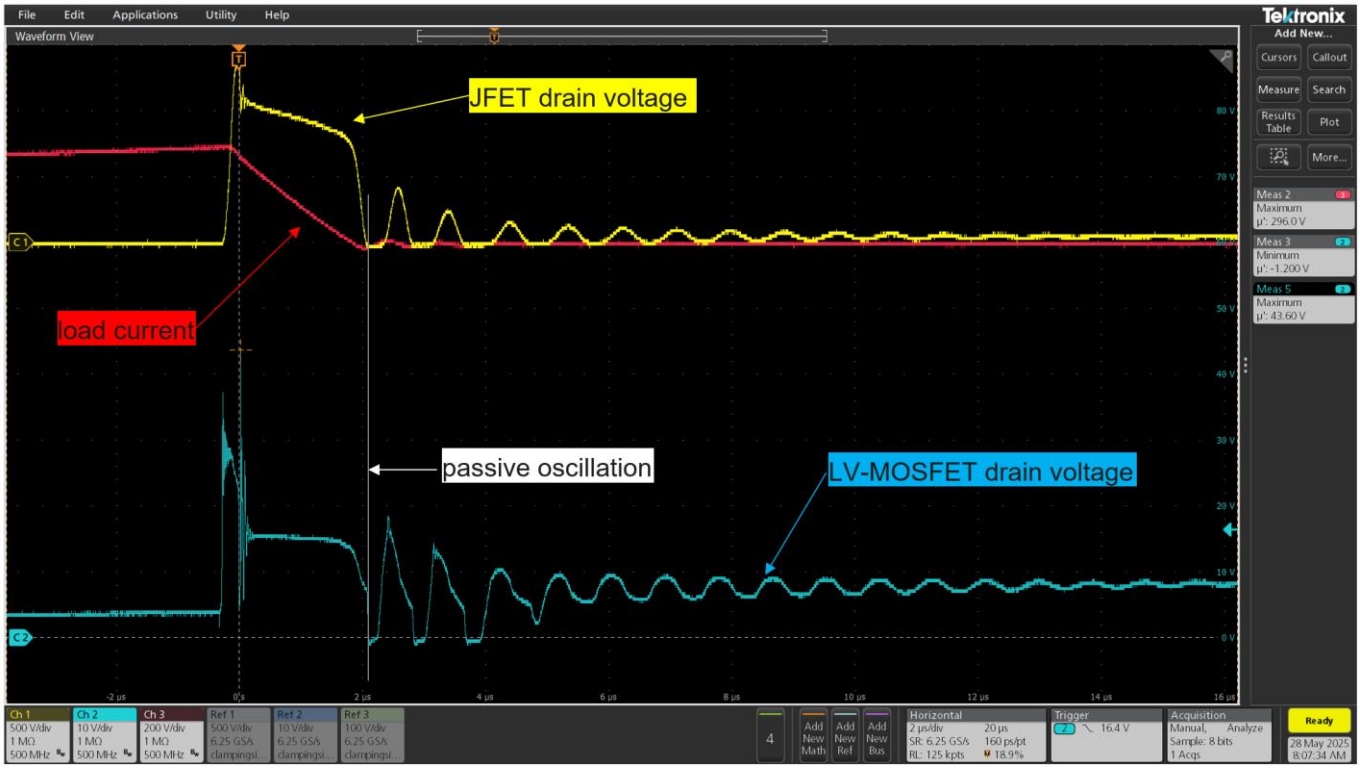

Figure 20 **Scope waveforms**

The waveforms above (Figure 20) show a typical inductive turn-off event. It starts with the JFET cascode in on-mode and the load current ramping up to a level of ~250A. When the cascode turns off, a fast transient on JFET drain voltage is visible, reaching a peak value $V_{PEAK} > V_{DSS}$ (V_{DSS} = 1200V in the example shown). Right after the peak value in JFET drain voltage, it drops to the conduction voltage level of the MOV. This indicates the load current has commutated to the MOV.

From the marked point onwards, a passive oscillation is visible. This oscillation is caused by the output capacitance of the switching semiconductors and the line/load inductance. It is damped and therefore rated not critical, in case not being acceptable in the application a RC snubber can be used to suppress the oscillation.

The LV-MOSFET drain voltage waveform shows the characteristic rise of the drain voltage shortly before the JFET turns off. This rise of drain voltage provides the negative bias for the JFET gate to switch off. After the initial transient, the LV-MOSFET drain voltage drops to the level to the JFET threshold or pinch-off voltage.

4.2 dV/dt ruggedness test

The changing rate of the drain to source voltage over time is a concern if it is too high. High dV/dt could cause an induced turn on event while the device is switched off. Additionally, large dv/dt could lead to ringing in the switch with severe damage.

The main purpose of the test is to evaluate the JFETs in back-to-back configuration while providing external high dV/dt.

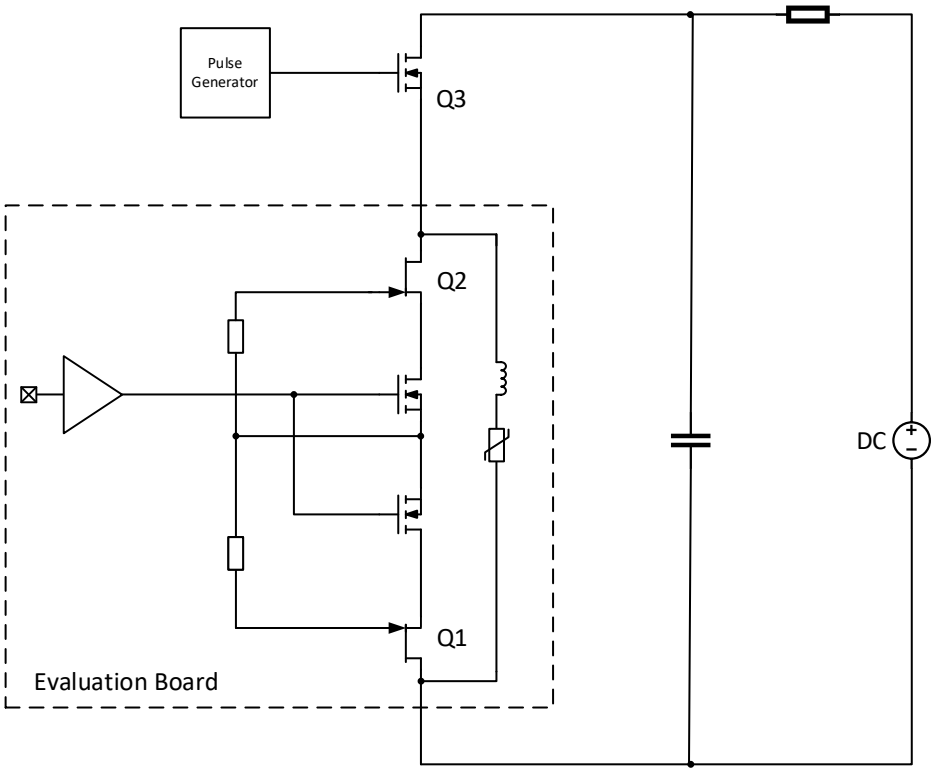

Figure 21 **dV/dt test setup**

While the main switches Q1 and Q2 of the evaluation board are kept in off-mode an auxiliary switch Q3 is turned on in order to create an external high dV/dt the cascode circuit. The capacitor tank C and resistor R are required to provide the required energy for the dV/dt injected into the circuit. The gate driver circuit forces the JFET cascode to be switched off, additionally a pulse generator is required to derive Q3 as shown in Figure 21.

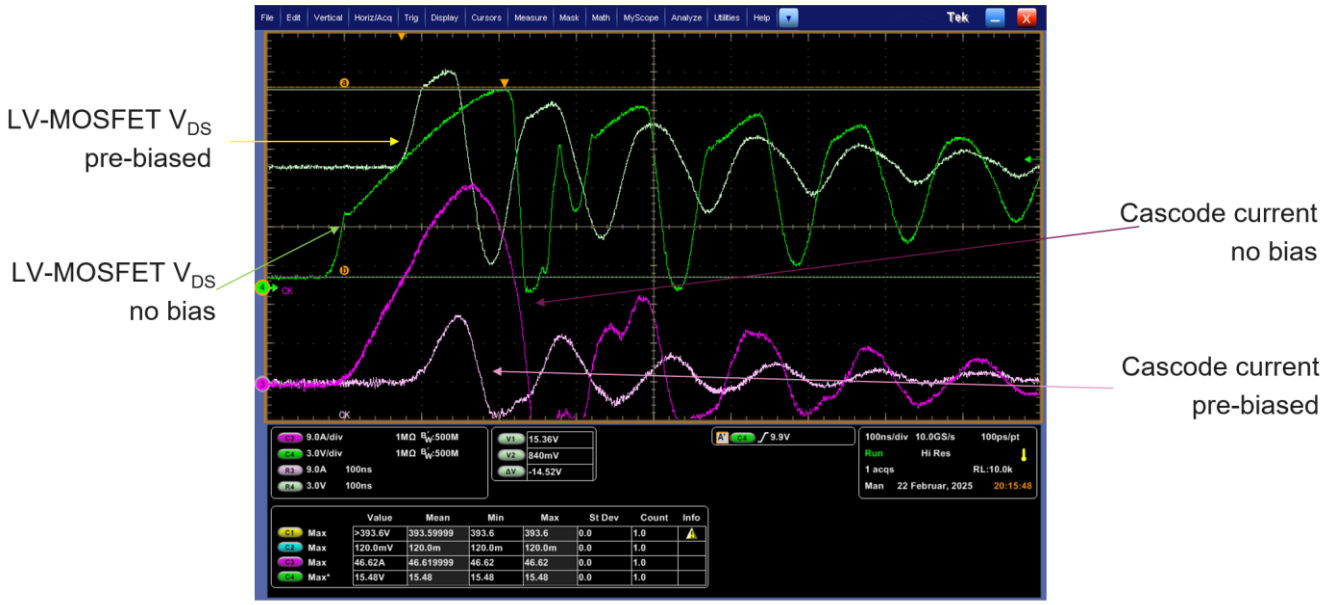

Figure 22 **Scope waveforms**

The above waveforms (Figure 22) are showing two different measurement. First operation with no pre-bias shown substantial inrush current when Q3 from Figure 21 is turned on. As the LV-MOSFET drain is at almost zero volts at that point in time, the JFET gate does not have any negative bias voltage available, therefore the JFET is in on mode.

Second operating point with pre-bias applied shows very much reduced inrush current. The level of inrush current is given by the output capacitance of the cascode assembly and the line/load inductance of the circuitry. Pre-bias is achieved by providing a positive voltage form the gate drive power supply to the cascode middle node (LV-MOS drain / JFET source). This put the JFET gate into a negative pre-bias state and therefore it will be in off mode even before the dV/dt event is triggered by supplying a pulse to Q3.

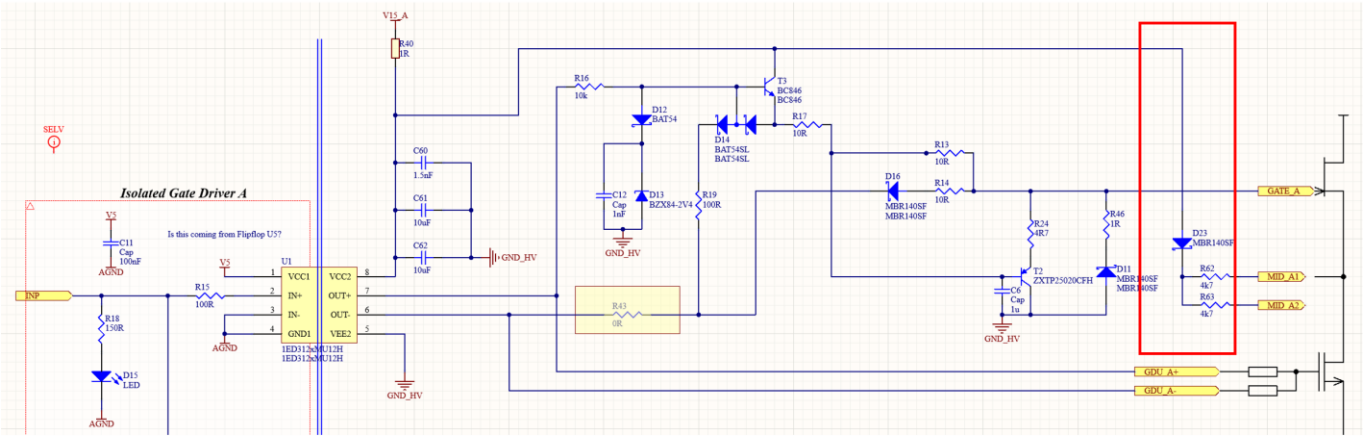

Figure 23 **Pre-bias of cascode mid-point**

5 Summary

This document described the application of the CoolSiC™ JFET technology in cascode configuration. It provides a basic introduction to JFET technology and cascode application. Secondly, it describes the superior performance which can be achieved by using Infineon Technologies newest technology, namely CoolSiC™ JFET. Moreover, application measurements are shown for reference. Single pulse Inductive clamping, repetitive single pulse inductive clamping and dV/dt measurements were performed and results are provided.

Revision history

Document revision	Date	Description of changes
1.0	2025-05-30	Initial release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-05-30

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

AN-2025-06

Important notice

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Warnings

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.