iS15M7R1S1C

SuperQ™ 150-V N-Channel Power MOSFET

FEATURES

- Low on-resistance, $R_{DS(on)}$
- Ultra low energy stored, E_{OSS}
- Ultra low turn-off energy, E_{OFF}
- Optimized Q_{SW} for hard switching
- Low reverse recovery time T_{rr} and Q_{rr}

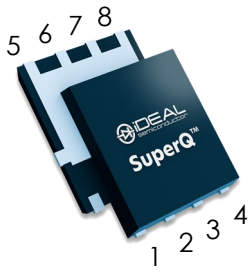
APPLICATIONS

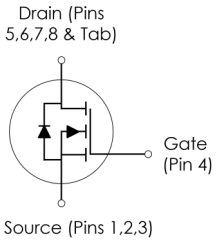
- Boost converters and SMPS control FETs
- Secondary side synchronous rectifier
- Motor control

DESCRIPTION

This 150V, 5.4mΩ$_{TYP}$ SuperQ power MOSFET is designed to minimize losses in SMPS applications through leading Rds,on, ultra low energy storage, fast turn-off time and minimal switching charge.

PRODUCT SUMMARY





PDFN 5x6mm

Parameter T_A = 25°C	Value	Unit
V_{DS}	150	V
$R_{DS(on),max}$	6.4	mΩ
I_D	133	A
Q_G	48	nC
Q_{SW}	4.9	nC
E_{OSS}	1	µJ

ORDERING INFORMATION			
Part Number	**Package**	**Marking**	**Packaging**
iS15M7R1S1C	PDFN 5X6	15M7R1S1	13" 5,000pcs T&R

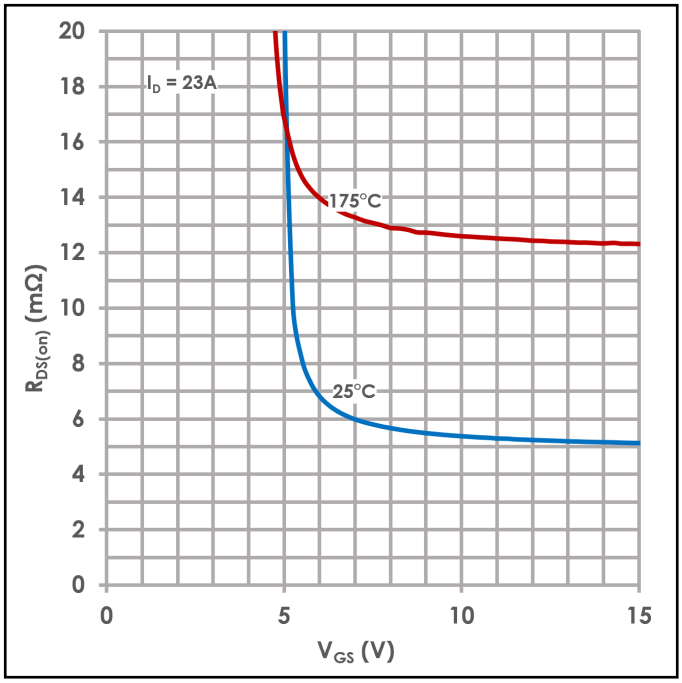


Figure 1: Typical Drain-Source On Resistance

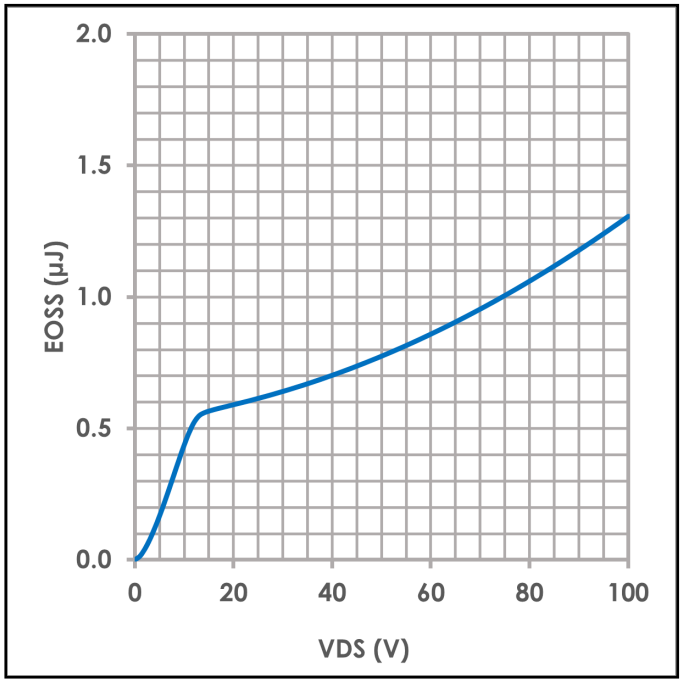


Figure 2: Typical COSS Stored Energy

ABSOLUTE MAXIMUM RATINGS			
SYMBOL	**PARAMETER** (T_A = 25°C unless otherwise specified)	**VALUE**	**UNIT**
V_{GS}	Gate-to-source voltage	± 20	V
I_D	Continuous drain current (silicon limited), T_C = 25°C	133	A
	Continuous drain current (silicon limited), T_C = 100°C	94	
I_{DM}	Pulsed drain current	459	A
P_D	Power dissipation, T_C = 25°C	250	W
T_J, T_{stg}	Operating junction, storage temperature	-55 to 175	°C
E_{AS}	Avalanche energy, single pulse I_D = 11.3A, R_{GS} = 25Ω	641	mJ

THERMAL CHARACTERISTICS					
SYMBOL	**PARAMETER** (T_A = 25°C unless otherwise specified)	**VALUE**			**UNIT**
		MIN	**TYP**	**MAX**	
$R_{\theta JC}$	Junction-to-case thermal resistance - PDFN 5x6	-	-	0.6	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)	-	-	50	°C/W

(1) 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE			UNIT
			MIN	TYP	MAX	
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 1mA	150	-	-	V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 120V, T_J = 25°C	-	0.1	1	µA
		V_{GS} = 0V, V_{DS} = 120V, T_J = 125°C (2)	-	-	100	
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = 20V	-	1	100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 127µA	2.5	3.3	4.1	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 10V, I_D = 23A	-	5.4	6.4	mΩ
		V_{GS} = 8V, I_D = 12A	-	5.8	7.0	mΩ
g_{fs}	Transconductance	V_{DS} = 10V, I_D = 23A	41	82	-	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance (2)	V_{GS} = 0V, V_{DS} = 75V, f = 100kHz	-	2,949	3,893	pF
C_{rss}	Reverse transfer capacitance (2)		-	37	64	
C_{oss}	Output capacitance (2)		-	144	187	
$C_{o(er)}$	Effective output capacitance	V_{DS} = 0 to 75V, V_{GS} = 0V	-	356	-	
R_G	Series gate resistance	f = 1MHz	-	1.1	1.5	Ω
$t_{d(on)}$	Turn-on delay time	V_{DS} = 75V, V_{GS} = 10V, I_{DS} = 23A, $R_{G,EXT}$ = 0 Ω	-	8.5	-	ns
t_r	Rise time		-	1.7	-	
$t_{d(off)}$	Turn-off delay time		-	25	-	
t_f	Fall time		-	8.4	-	
GATE CHARGE CHARACTERISTICS						
Q_{gs}	Gate to source charge	V_{DS} = 75V, I_D = 23A, V_{GS} = 0 to 10V	-	14	-	nC
Q_g	Gate charge total (2)		-	48	63	
Q_{sw}	Switching charge (3)		-	4.9	-	
Q_{gd}	Gate to drain charge (2)		-	13	19	
$V_{plateau}$	Gate plateau voltage		-	5	-	V
Q_{oss}	Output charge (2)	V_{DS} = 0 to 75V, V_{GS} = 0V	-	132	170	nC
E_{oss}	Capacitive stored energy		-	1	-	µJ
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 23A, V_{GS} = 0V	-	0.8	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS} = 75V, I_F = 23A, di/dt = 100A/µs	-	107	-	nC
t_{rr}	Reverse recovery time		-	74	-	ns

(2) Defined by design. Not subject to production test.
(3) Q_{SW} should be used for switching loss calculations. See Figure 16 for Q_{SW} definition.

Ratings and Characteristics Curves

(T_A = 25°C unless otherwise specified)

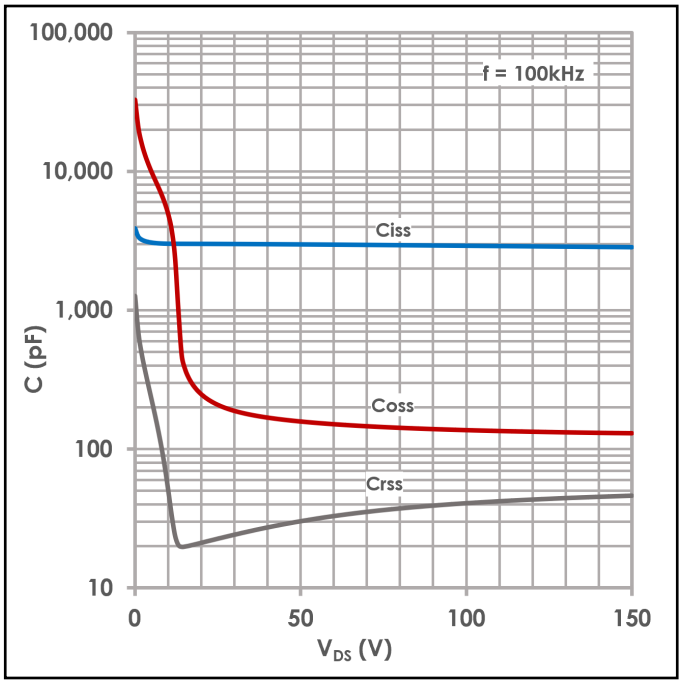


Figure 3: Typical Capacitances

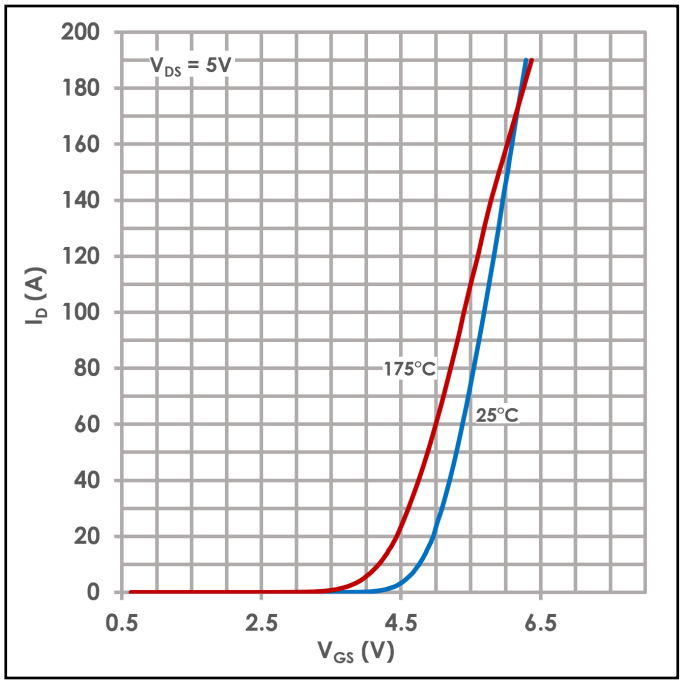


Figure 4: Typical Transfer Characteristics

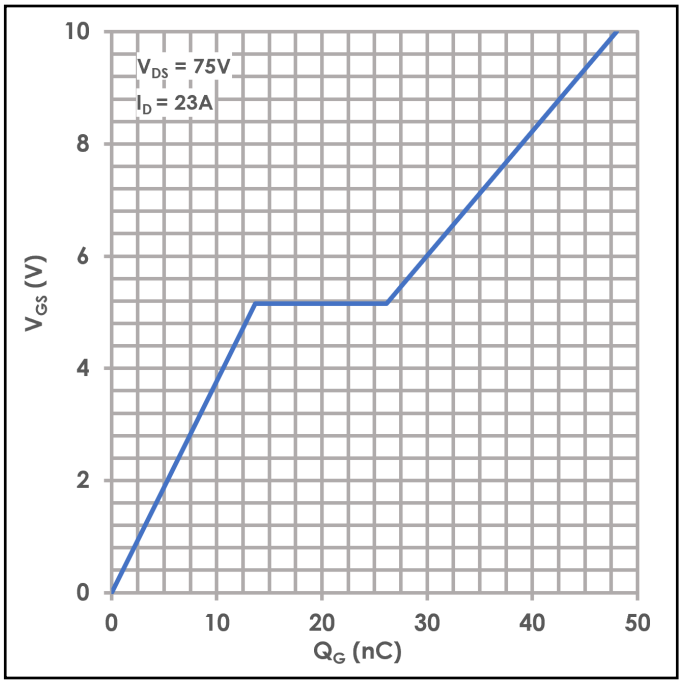


Figure 5: Typical Gate Charge

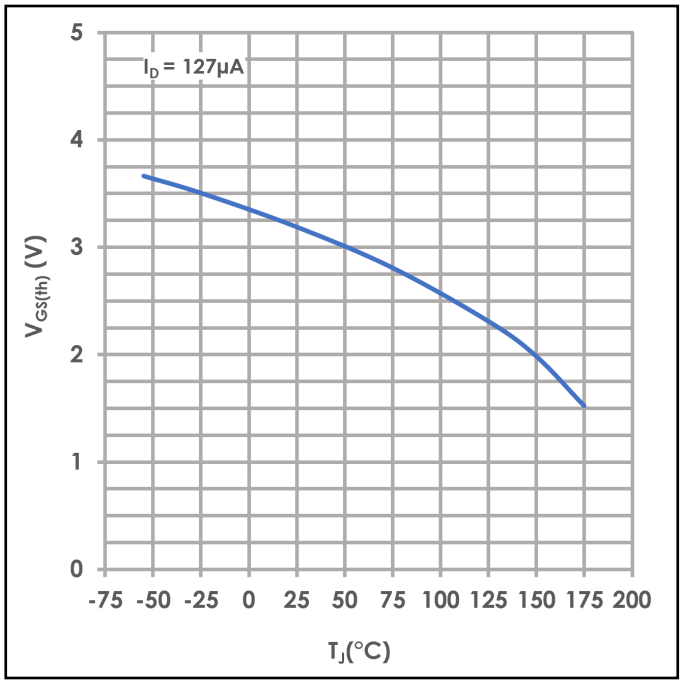


Figure 6: Typical Threshold Voltage

Ratings and Characteristics Curves

(T_A = 25°C unless otherwise specified)

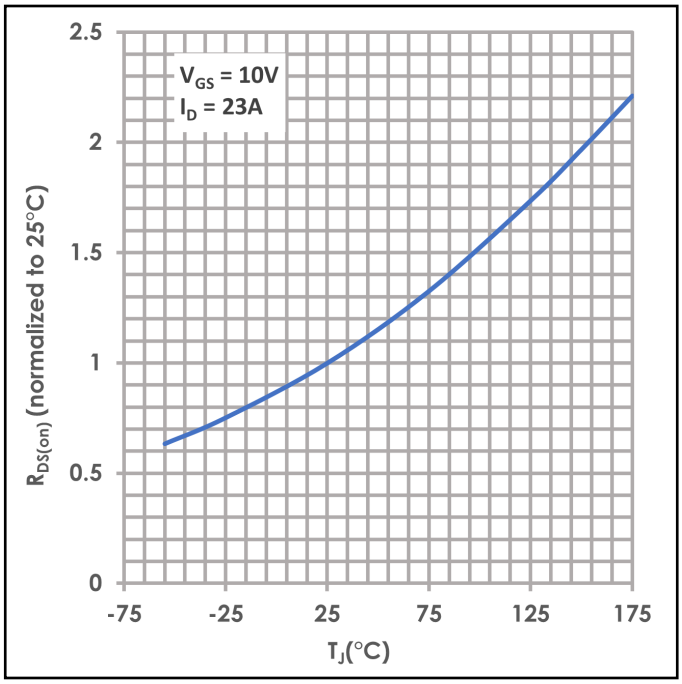


Figure 7: Normalized On-State Resistance vs. Temperature

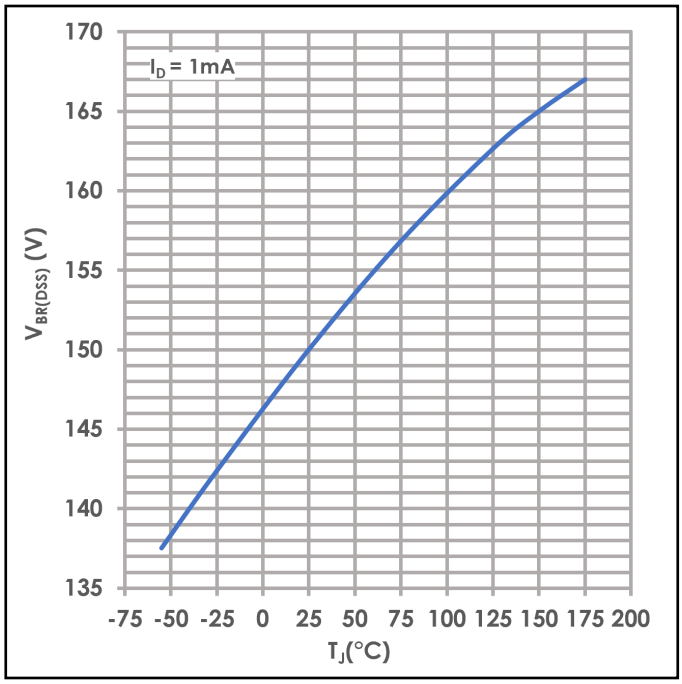


Figure 8: Drain-Source Breakdown Voltage

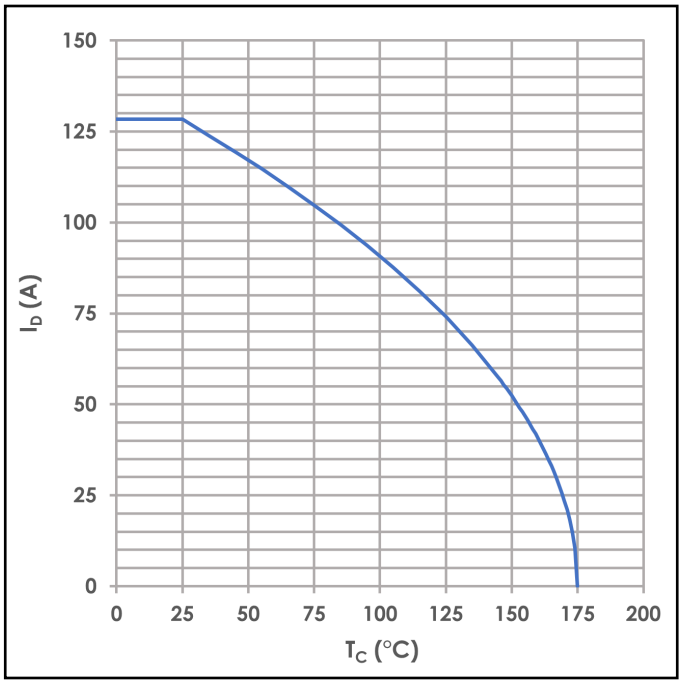


Figure 9: Drain Current

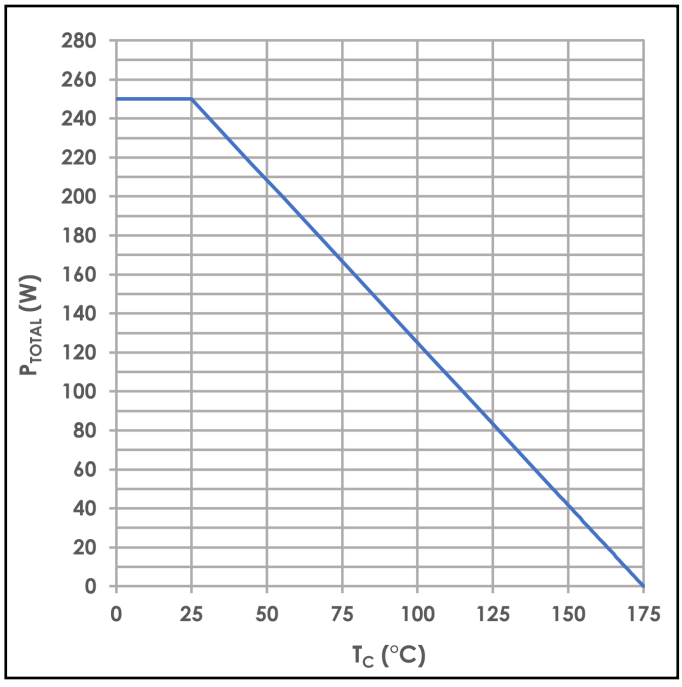


Figure 10: Power Dissipation

Ratings and Characteristics Curves

(T_A = 25°C unless otherwise specified)

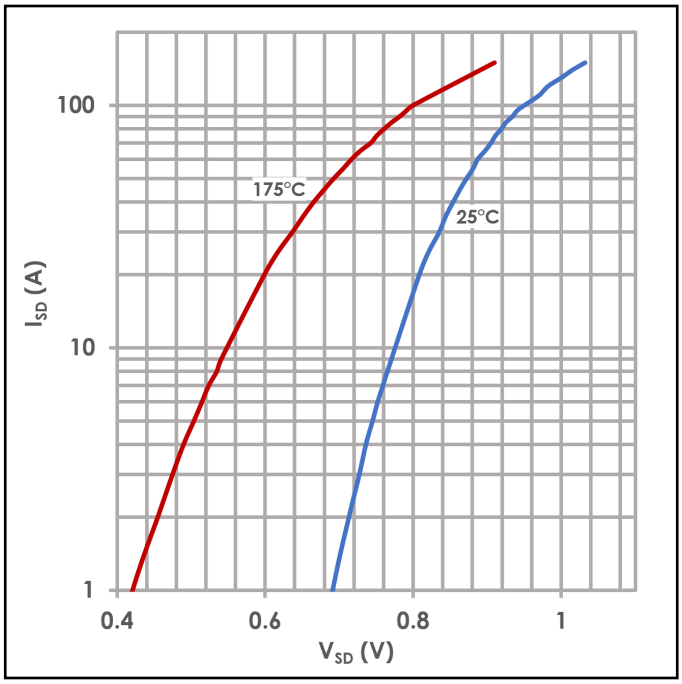


Figure 11: Typical Diode Forward Voltage

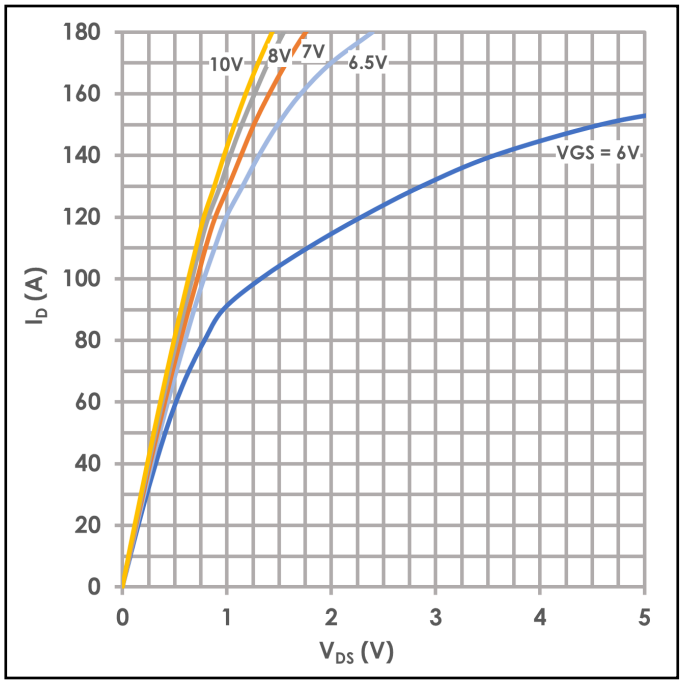


Figure 12: Typical Output Characteristics

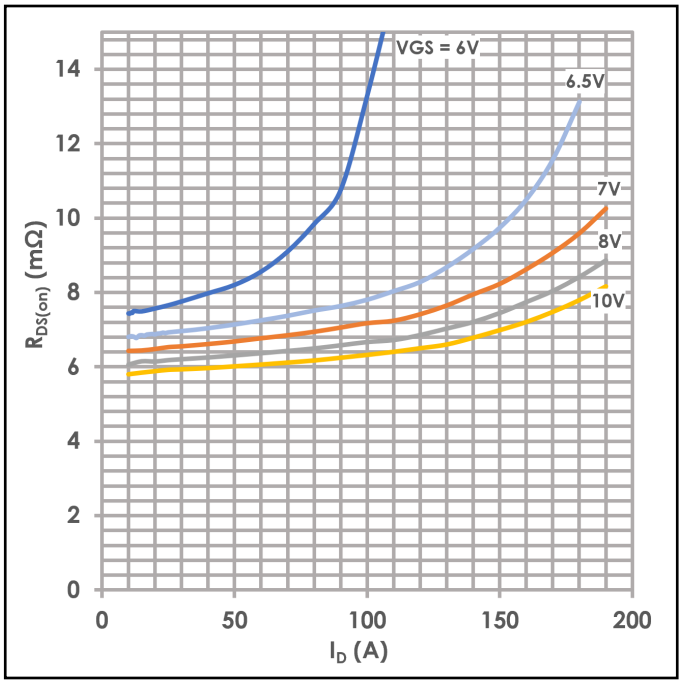


Figure 13: Typical Drain-Source On-Resistance

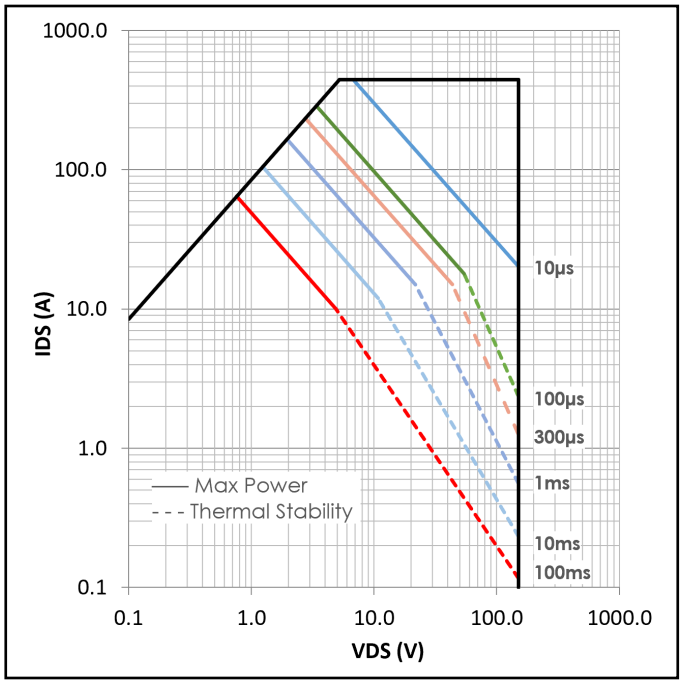


Figure 14: Safe Operating Area

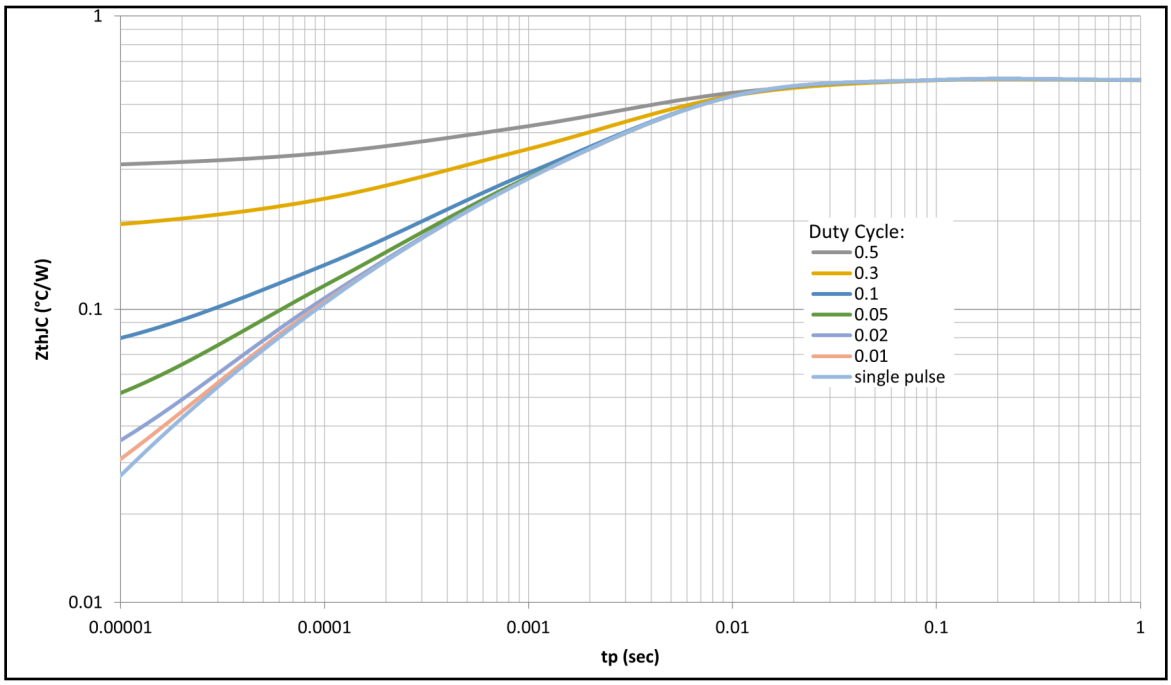


Figure 15: Max Transient Thermal Impedance

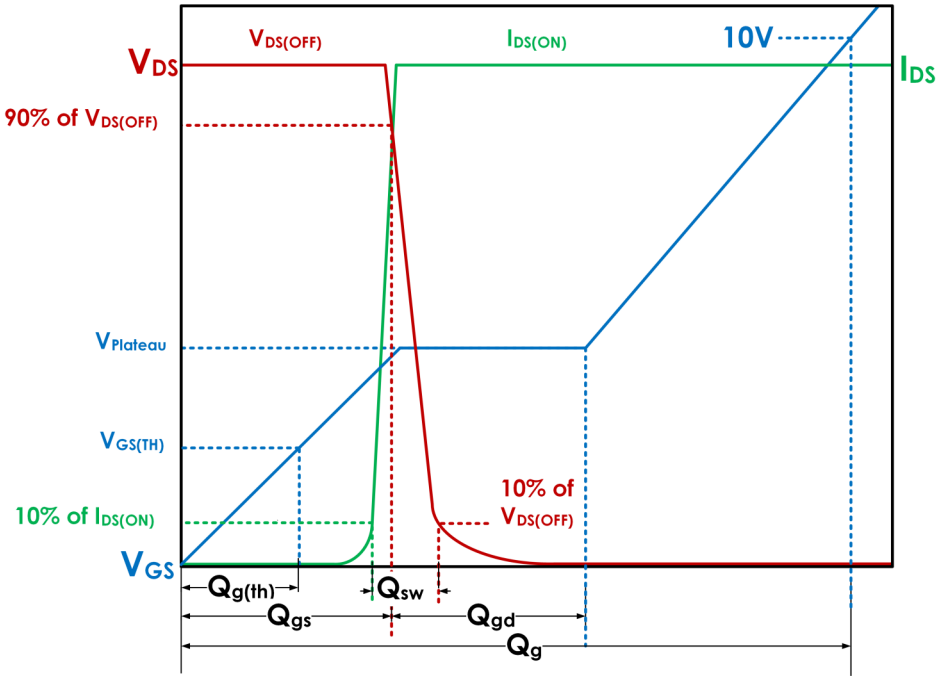
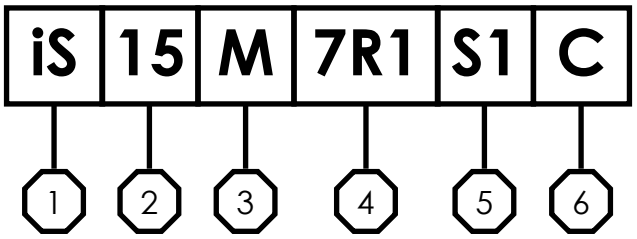


Figure 16: Gate Charge Definitions

DEVICE DECODER RING

Device Code



1 – iDEAL Semiconductor product

2 – Voltage rating divided by 10 (150V)

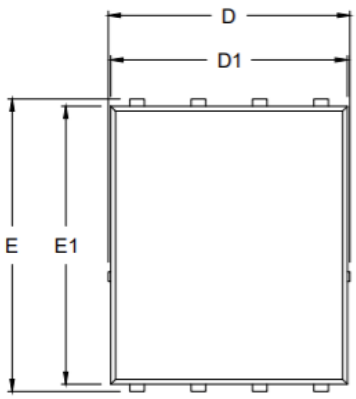
3 – M = N-Channel MOSFET, Standard Threshold

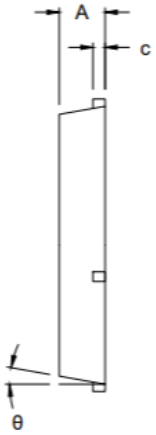
4 – Maximum drain-to-source resistance

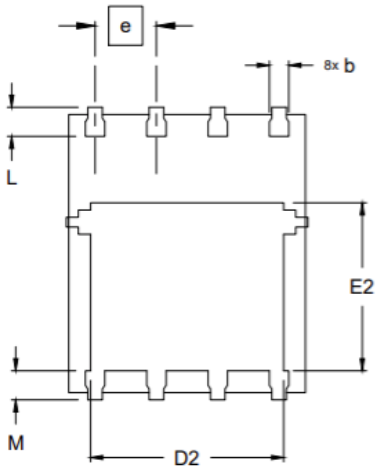
5 – SuperQ™ Generation

6 – C = PDFN 5x6mm

PDFN 5x6mm







SYMBOL	MIN	MAX
A	0.95	1.05
b	0.31	0.51
c	0.25 REF	
D	4.94	5.30
D1	4.80	5.1
D2	3.70	4.10
E	5.97	6.35
E1	5.67	6.10
E2	3.37	3.76
e	1.27 TYP	
L	0.51	0.71
M	0.51	0.73
θ	0°	10°

Revision History		
Version	**Date**	**Comments**
1.0	June 2025	Initial Release

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