TDA38740A Evaluation Board user guide

40 A single-phase buck regulator

About this document

Scope and purpose

This user guide describes the operation, schematic, and bill of materials (BOM) for EVAL_TDA38740A_1.1VOUT, EVAL_TDA38740A_1.2VOUT, and EVAL_TDA38740A_3.3VOUT Evaluation Boards. Detailed application information for TDA38740A is available in the TDA38740A datasheet [1].

Intended audience

This document is intended as a guide for design engineers evaluating TDA38740A performance with EVAL_TDA38740A_1.1VOUT, EVAL_TDA38740A_1.2VOUT, and EVAL_TDA38740A_3.3VOUT Evaluation Boards.

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Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

	Caution: *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	Caution: *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 Introduction

The TDA38740A is a synchronous buck converter with PMBus communication interface, providing a compact, high-performance, and flexible solution in a small 5 mm X 6 mm Power QFN package. This Evaluation Board is to be used during the designing process for evaluating and measuring characteristic curves, and for understanding various features of the part.

The key programmable features offered by the TDA38740A are:

- Soft start
- Thermal protection
- Switching-frequency
- Enable input, output under-voltage lockout
- Over-voltage protection and-current protection,
- High-side short detection
- Load-line, and pre-bias start-up
- All faults have configurable responses via the available XDP Designer GUI from Infineon
- Output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous (low-side) MOSFET for optimum cost and performance and the current limit is thermally compensated.

2 Evaluation Board

EVAL_TDA38740A_1.1VOUT, EVAL_TDA38740A_1.2VOUT, and EVAL_TDA38740A_3.3VOUT Evaluation Boards are synchronous buck converters that steps down 12 V_{in} to 1.1 V_{out}, 1.2 V_{out}, and 3.3 V_{out} respectively. It consists of integrated point-of-load TDA38740A part. The TDA38740A is an easy-to-use, fully-integrated, and highly efficient DC-DC regulator. The onboard pulse width modulation (PWM) controller and OPTIMOS™ FETs with integrated bootstrap diode make TDA38740A a small footprint solution, providing high-efficiency power delivery. Additionally, it uses a fast Constant On-Time (COT) control scheme, which simplifies the design efforts and achieves fast transient response.

This document provides description of all Evaluation Boards mentioned in this document. Figure 1 shows the bench setup of these Evaluation Boards using 1.1 V_{out} configuration as an example:

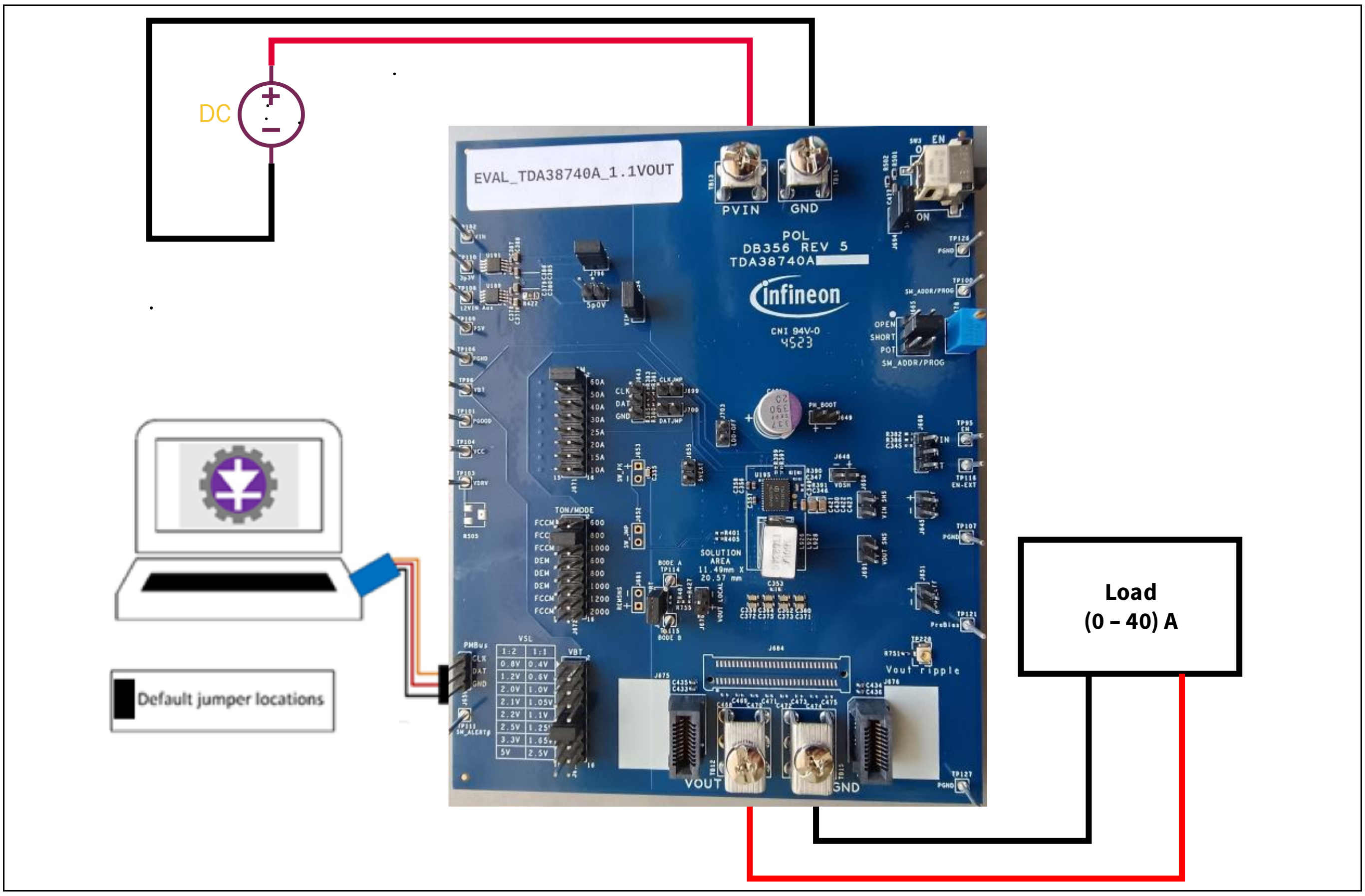

Figure 1 Bench setup block diagram

2.1 Evaluation Kit

The Evaluation Kit consists of only the Evaluation Board. There are three options of Evaluation Board with V_{out} configured to either 1.1 V_{out}, 1.2 V_{out}, and 3.3 V_{out} based on the order requirements of the Evaluation Kit.

The user of this Evaluation Kit should order the USB005 dongle separately. Contact your distribution partner, account managers, or the Infineon support for more information about ordering USB005 dongles.

3 Board information

3.1 Board parameters and technical data

$PV_{in} = V_{in}$ = +12 V

F_{sw}= 800 kHz (this is the default value, but it is configurable using the XDP Designer GUI)

C_{in}= 8 x 22 µF (25 V, Ceramic 0805) + 1 x 2.2 µF (25 V, Ceramic 0402) + 1x 4.7 µF (25 V, Ceramic 0603) + 1 x 390 µF (20 V, Electrolytic, optional)

Table 2 TDA38740A Default output inductor and capacitor bank for each output voltage

Output voltage	Inductor	Output capacitors (C_{out})
1.2 V	150 nH	1880 µF (1x470 µF SP Cap, 2.5 V rated + 20x47 µF Ceramic)
3.3 V	470 nH	1880 µF (1x470 µF POSCAP, 6.3 V rated + 20x47 µF Ceramic)

3.2 Connections and operating instructions

EVAL_TDA38740A_1.1VOUT, EVAL_TDA38740A_1.2VOUT, and EVAL_TDA38740A_3.3VOUT Evaluation Boards require a single +12 V for the input power and can deliver up to 40 A load current. The operation modes and OCP limits are programmable via XDP Designer GUI.

Table 1 Connections

Label		Descriptions
Input	PVIN	Connect input power (+12 V) to this pin.
	GND	Return of input power.
	VIN_Eff (J645)	Sense pins for input voltage.
	VIN_SEN (J690)	Sense pins for the input voltage.
Output	VOUT	V_{out}, connect a load (40 A max) to this pin.
	GND	Return of V_{out}
	VOUT_Eff (J651)	Sense pins for efficiency.
	VOUT_SEN (J691)	Sense pins for the output voltage.
Enable	ENABLE	Connect a scope probe to this pin to monitor Enable Signal. An external Enable signal can be applied to this pin to overdrive the on-board Enable signal by connecting a jumper on EXT-EN header J740. Alternatively, the Enable signal can be generated using PVIN using a resistor divider by connecting a jumper on PVIN-EN header J740.
	GND	
BODE	A	For bode plot measurement.
	B	
SM_ADDR/PROG	I2C Slave Address Offset	Use this jumper to add an offset to the I2C Slave base address of 0x10h. By default, this is set to zero.
I2C/PMbus	J643	This is used to establish communication with the Infineon XDP Designer GUI, which is used to change the default configuration of the part. The dongle USB005 is used for communication.
PGOOD	TP101	This signal is used to indicate that the V_{out} has reached a threshold set by POWER_GOOD_ON PMbus command
SM_ADDR/PROG	J665	This jumper is used to select between 16-programmed files stored in the part. By default, it is set to accept the most recent programmed config file into the part.
ILIM	J671	This jumper is used to select the resistor-programmable current limit.
TON/MODE	J672	This jumper is used to select the resistor-programmable switching frequency and FCCM or DCM mode.
VBT	J674	This jumper is used to set the resistor-programmable boot voltage.
VIN-PVIN	VCC	Connecting a jumper to J751 generates the V_{cc} on board, but removing this jumper and connecting it a 5 V external supply to TP169 will also work.
EN ON/OFF	SW3	This switch is used to enable the part ON and OFF. The switch is pulled up to an onboard 3.3 V regulator.

3.3 Layout

The PCB is an 8-layer board (5.25 inch x4.1 inch) using FR4 material. The PCB thickness is 0.062 inch. TDA38740A and other major power components are mounted on the top side of the board. Table 2 details the layer stack-up order and Copper weight for each layer.

Table 2 PCB layer stack up

Layer	Layer Description	Trace Material
1	Top	0.5-Ounce Copper + 1.5-Ounce plating
2	Ground 1	2-Ounce Copper
3	Signal 1	2-Ounce Copper
4	Power 1	2-Ounce Copper
5	Power ground	2-Ounce Copper
6	Signal 2	2-Ounce Copper
7	Ground 2	2-Ounce Copper
8	Bottom	0.5-Ounce Copper + 1.5-Ounce plating

3.4 PCB Layout

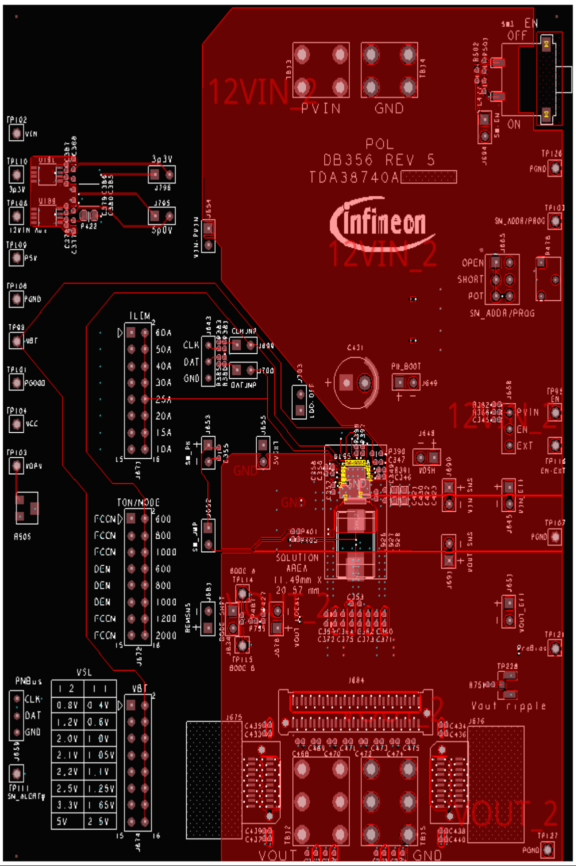

Figure 2 TDA38740A Evaluation Board top layer

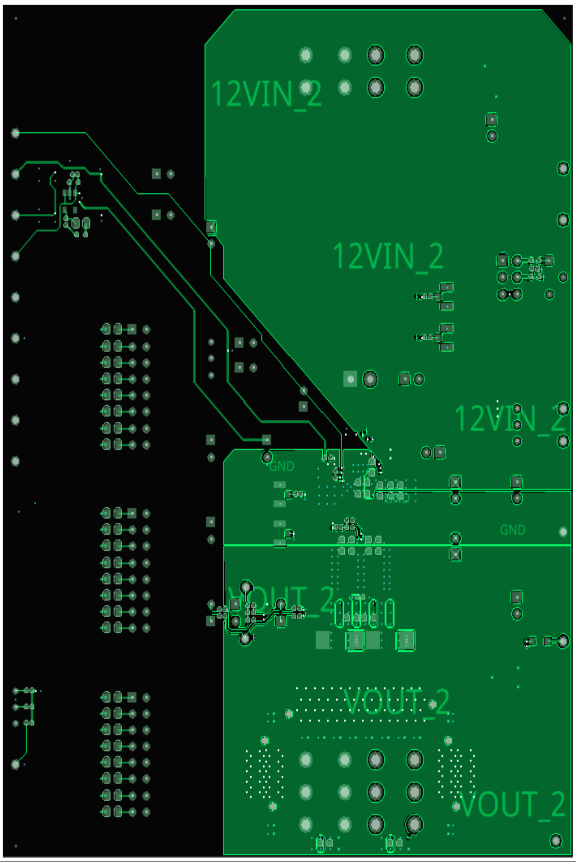

Figure 3 TDA38740A Evaluation Board bottom layer

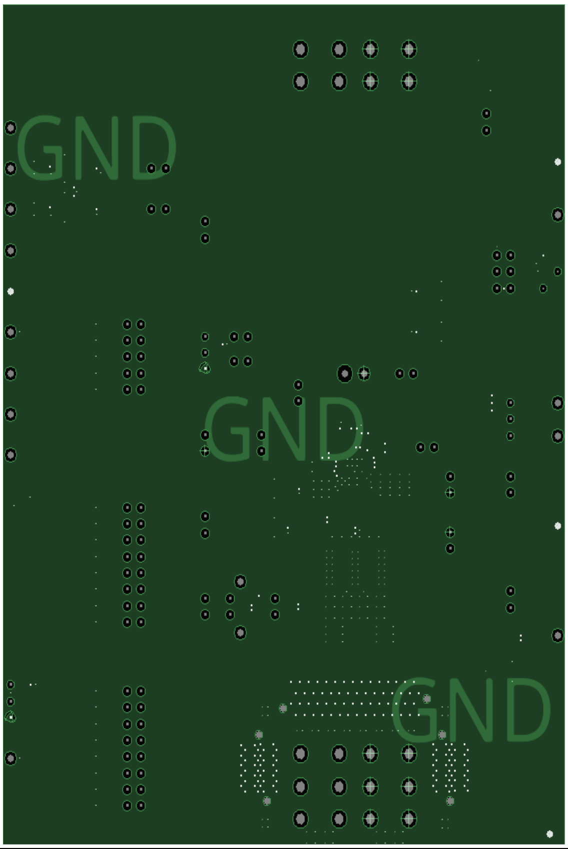

Figure 4 TDA38740A Evaluation Board mid layer 1 (ground)

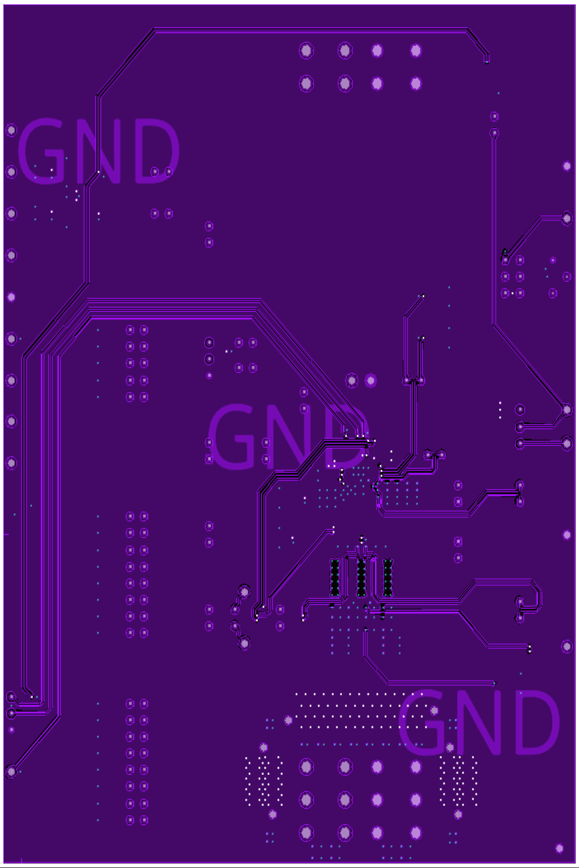

Figure 5 TDA38740A Evaluation Board mid layer 2 (signal 1)

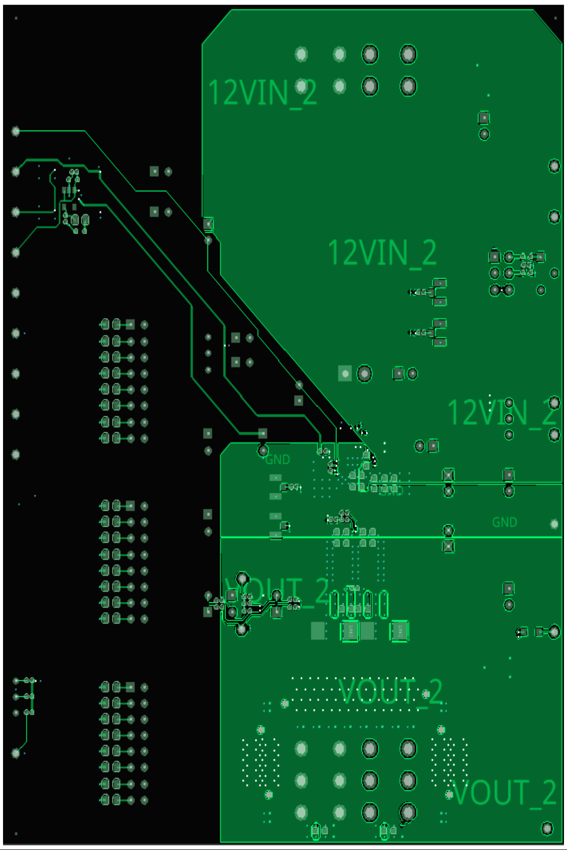

Figure 6 TDA38740A Evaluation Board mid layer 3 (power 1)

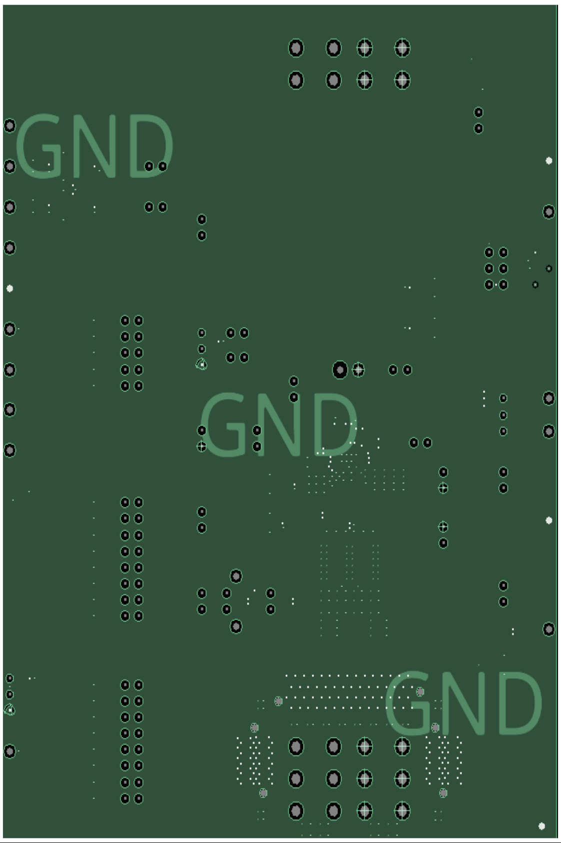

Figure 7 TDA38740A Evaluation Board mid layer 4 (power ground)

Figure 8 TDA38740A Evaluation Board mid layer 5 (signal 2)

Figure 9 TDA38740A Evaluation Board mid layer 6 (ground 2)

3.5 Schematic

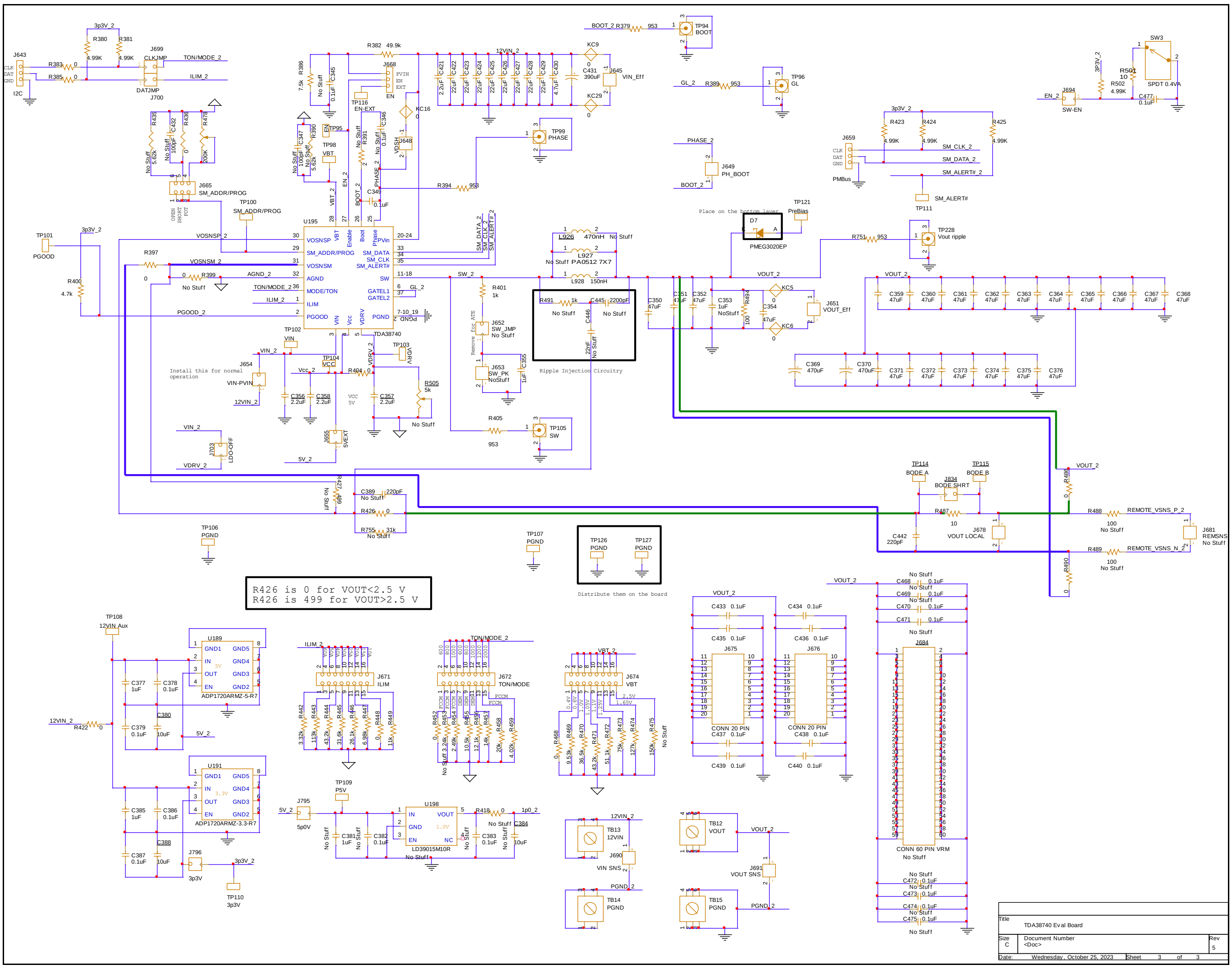

Figure 10 Schematic of EVAL_TDA38740A_1.1VOUT, and EVAL_TDA38740A_1.2VOUT

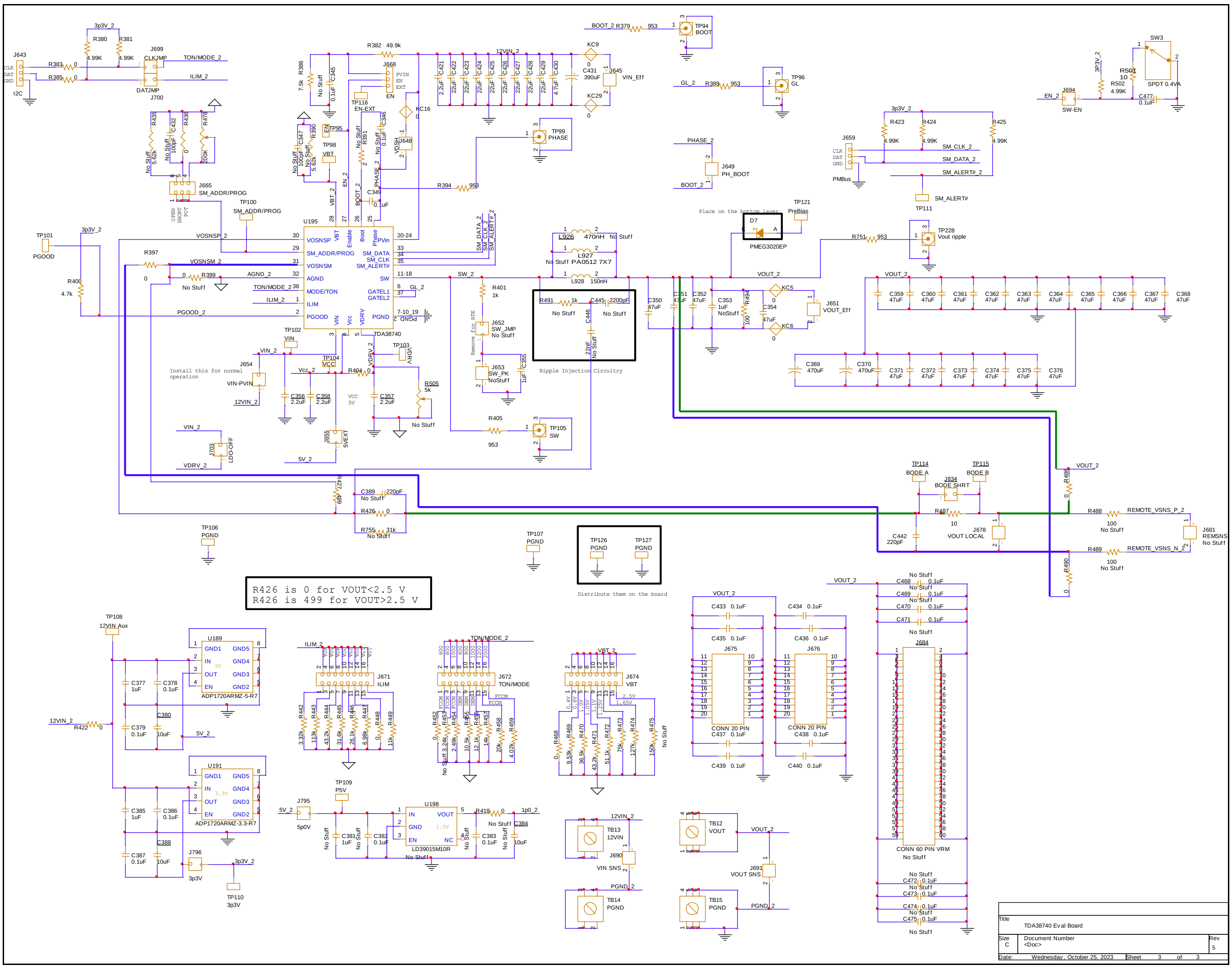

Figure 11 Schematics of EVAL_TDA38740A_3.3Vout

3.6 Bill of materials

Table 3 Optimized bill of materials for 1.1 V_{out} , 1.2 V_{out} , and 3.3 V_{out}

Item	Qty	Reference	Value	Description	Manufacturer	Part Number
1	1	C349	0.1 µF	0.1µF-0402-25V-X7R-10%	TDK	C1005X7R1E104K
2	1	C432	No Stuff	100pF-0402-50V-C0G-5%	JDI	500R07N101JV4T
3	1	C353	No Stuff	1µF-0603-25V-X5R-10%	Samsung	CL10A105KA8NNNC
4	3	C356, C358, C357	2.2 µF	2.2µF-0402-16V-X6S-10%	TDK	C1005X6S1C225K050BC
5	1	C421	2.2 µF	2.2µF-0402-25V-X5R-10%	Murata	GRT155R61E225KE13D
6	8	C422, C423, C424, C425,	22 µF	22µF-0805-25V-X5R-20%	Murata	GRM21BR61E226ME44L

Item	Qty	Reference	Value	Description	Manufacturer	Part Number
		C426, C427, C428, C429				
7	1	C430	4.7 µF	4.7µF-0603-25V-X6S-20%	Murata	GRM188C81E475KE11
8	1	C431	390 µF	CAP, 8 mm, 20 V, TOL%	Panasonic	20SEPF390M
9	12	C359, C360 C361, C362 C363, C364 C371, C372 C373, C374 C375, C376	47 µF	47µF-0603-6.3V-X5R-10%	Murata	GRM188R60J476ME15D
10	1	R382	49.9 k	Res,0402,1/16 W,1%	Yageo	RC0402FR-0749K9L
11	2	R404	0	Res,0402,1/16 W,1%	Yageo	RC0402FR-070RL
12	1	R386	7.5 k	Res,0402,1/16 W,1%	Yageo	RC0402FR-077K5L
13	1	R435, R390	No stuff	Res,0603,1/10 W,1%	Yageo	RC0603FR-07####L
14	1	R391	No stuff	Res,0402,1/16 W,1%	Yageo	RC0402FR-07####L
15	1	R400	4.7 k	Res,0402,1/16 W,1%	Yageo	RC0402FR-074K7L
16	1	R436	0	Res,0603,1/10 W,1%	Yageo	RC0603FR-070RL
17	1	R487	10	Res,0402,1/16 W,1%	Yageo	RC0402FR-0710RL
18	1	R488, R489	No stuff	Res,0402,1/16 W,1%	Yageo	RC0402FR-07####L
19	1	U195	TDA38740A	TDA38740A 40A Single-voltage Synchronous Buck Regulator	Infineon	TDA38740A-0000

Table 4 **Optimized bill of materials based on V_{out}**

V_{out}	Qty	Reference	Value	Description	Manufacturer	Part Number
<2.5 V	8	C350, C351, C352, C354 C365, C366 C367, C368	47 µF	47uF-0805-4V-X6S-20%	Murata	GRT21BC80G476ME13L
	1	C370	470 µF	SP Cap, Dcase,2.5 V,20%	Panasonic	EEFGX0E471R
	1	C369	No stuff	SP Cap, Dcase,2.5 V,20%	Panasonic	EEFGX0E471R
	1	L928	150 nH	IND, SMT,10x6.4 mm,xxA,yymohms	Inter-technical	L101247A-150L
	1	R426	0	Res,0402,1/16 W,1%	Yageo	RC0402FR-07499RL
	1	R755	No Stuff	Res,0402,1/16 W,1%	Yageo	RC0402FR-0730K9L
	1	R427	No Stuff	Res,0402,1/16 W,1%	Yageo	RC0402FR-07499RL
>2.5 V	8	C350, C351, C352, C354 C365, C366 C367, C368	47 µF	47 uF-0805-6.3 V-X5R-20%	TDK	C2012X5R0J476M
	1	C370	470 µF	POSCAP, Dcase, 6.3 V,20%	Panasonic	6TPF470MAH

V_{out}	Qty	Reference	Value	Description	Manufacturer	Part Number
	1	C369	No stuff	POSCAP, Dcase, 6.3 V,20%	Panasonic	6TPF470MAH
	1	L926	470 nH	IND, SMT,10x7 mm, xxA,yy mohms	Inter-technical	SLQ40407A-R47MHF
	1	R426	499	Res,0402,1/16 W,1%		RC0402FR-07499RL
	1	R755	30.9 k	Res,0402,1/16 W,1%	Yageo	RC0402FR-0730K9L
	1	R427	499	Res,0402,1/16 W,1%	Yageo	RC0402FR-07499RL

3.7 XDP Designer GUI

Infineon XDP Designer GUI is needed to communicate with the TDA38740A part via I2C. The GUI is a part of the Infineon XDP Designer.

Note that Dongle driver v59.4 or higher is necessary to communicate with the TDA38740A.

Installing and configuring XDP Designer

1. Launch the Infineon Developer Center.
2. Locate and click on the **Manage tools** Section.
3. In the search bar of the **Manage tools** Section, search for **XDP Designer**.
4. Install the **XDP designer** from the search results.
5. Once the installation is complete, launch the XDP Designer.

Configure the XDP Designer

1. Power the Evaluation Board with +12 V V_{in} and connect to your computer with the USB005 dongle.
2. Update system or scan devices: There are two ways to establish connection with your board:

- Click the **Tuning & Debugging** button within XDP Designer. This should automatically update the system section with the connected device and its configuration.
- If the automatic update doesn't work, click the **Scan Devices** button.

  The device will show with the part number and I2C address, with green circles (if the connection is correct and there are no faults).

3. Use the **XDP Designer toolbar** to alter any system configurations or read the telemetry.

   See Figure 12 for an annotated version of the XDP Designer home screen shown for EVAL_TDA38740A_1.1VOUT.

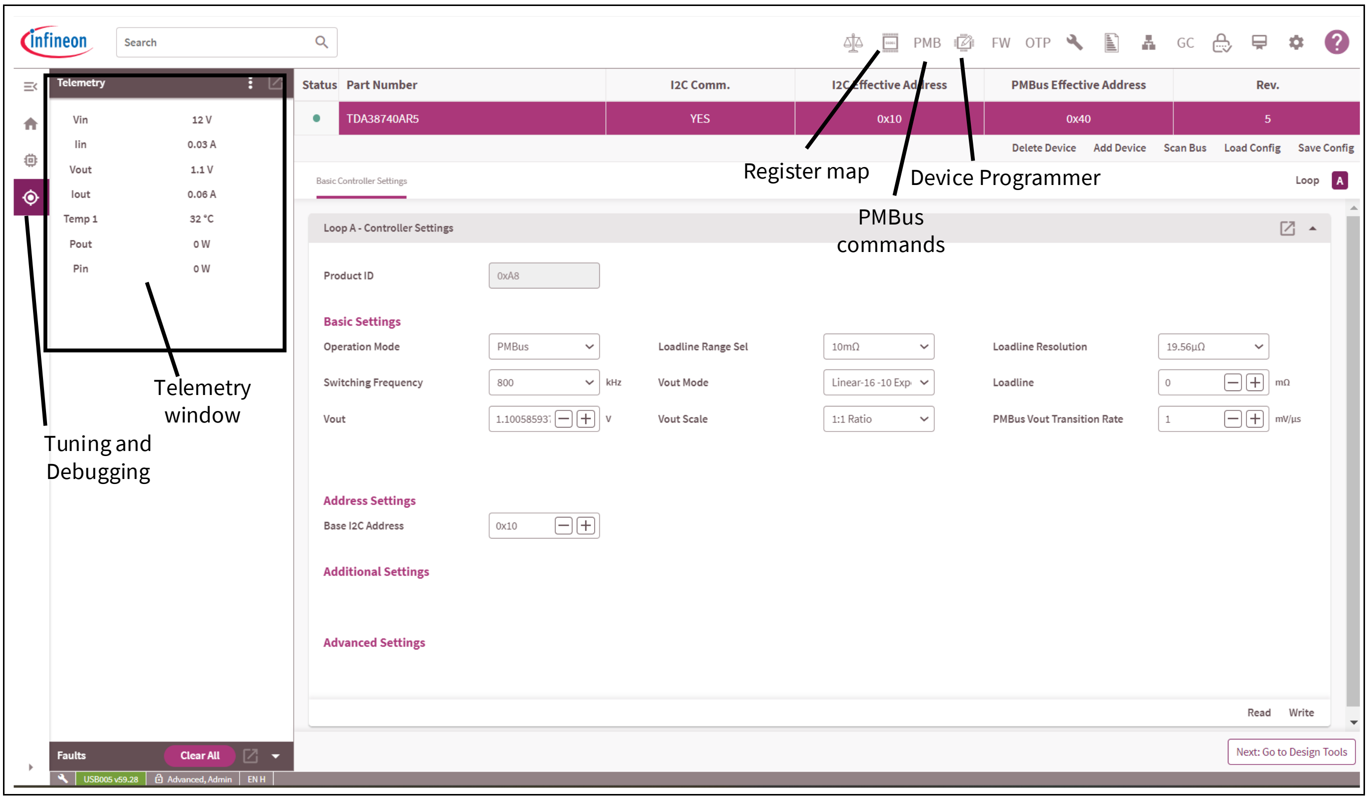

Figure 12 XDP Designer GUI 1.1 V_{out}

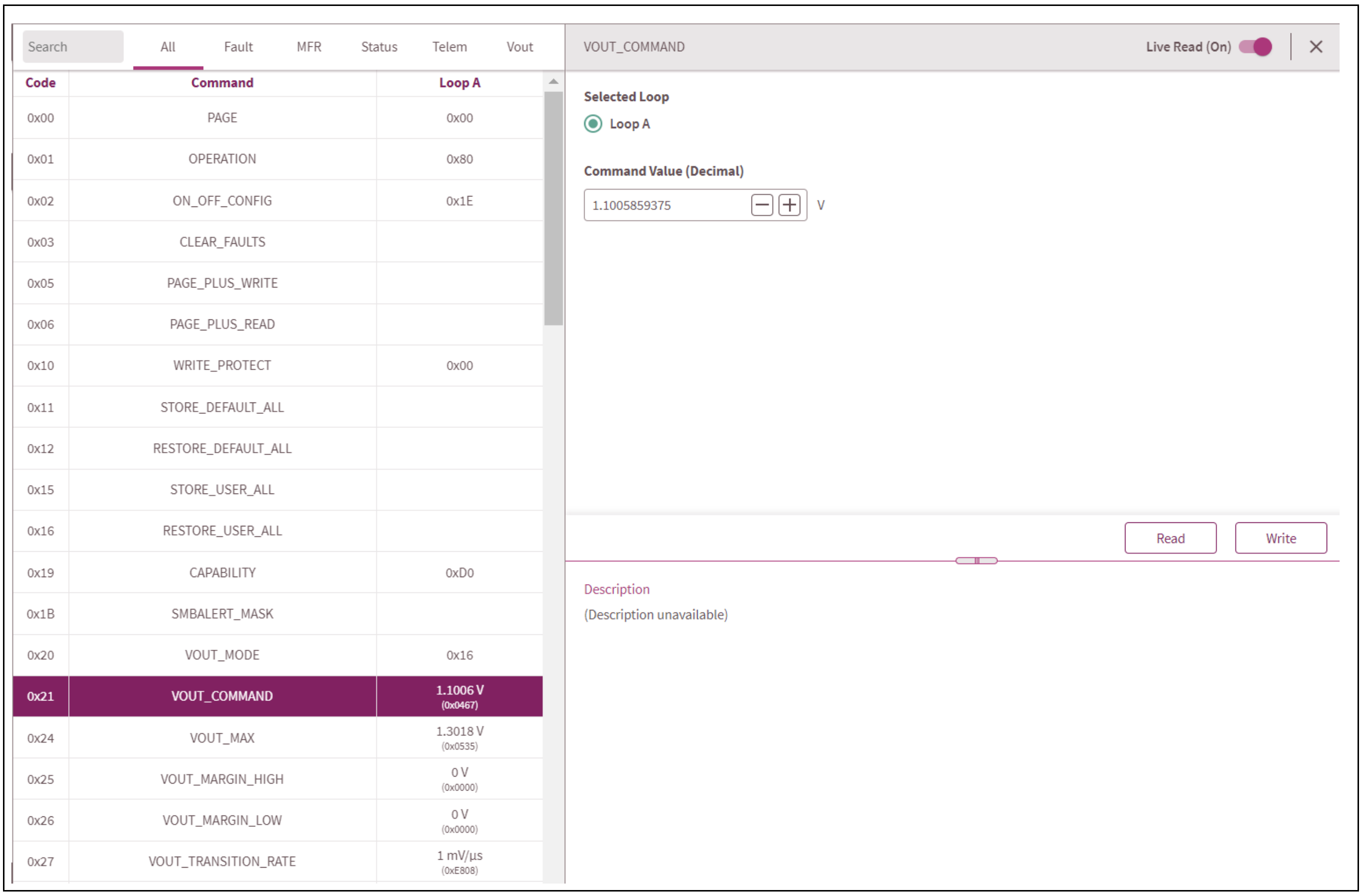

Figure 13 PMBus command window

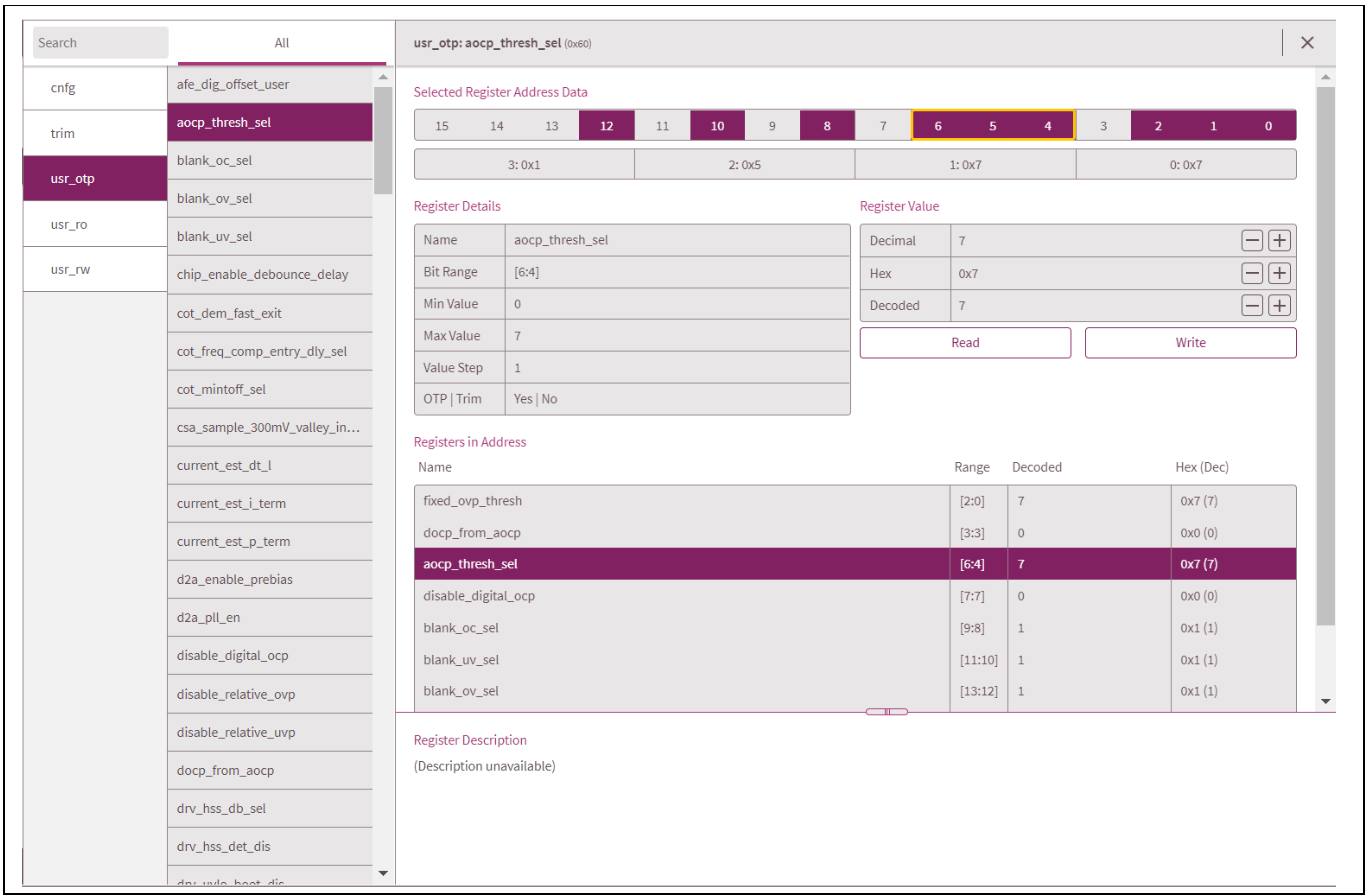

Figure 14 Register map window

4 Typical operating waveforms

Operating conditions: PV_{in} = 12.0 V, V_{out} = 1.2 V, I_{out} = 0 - 40 A, room temperature, no airflow.

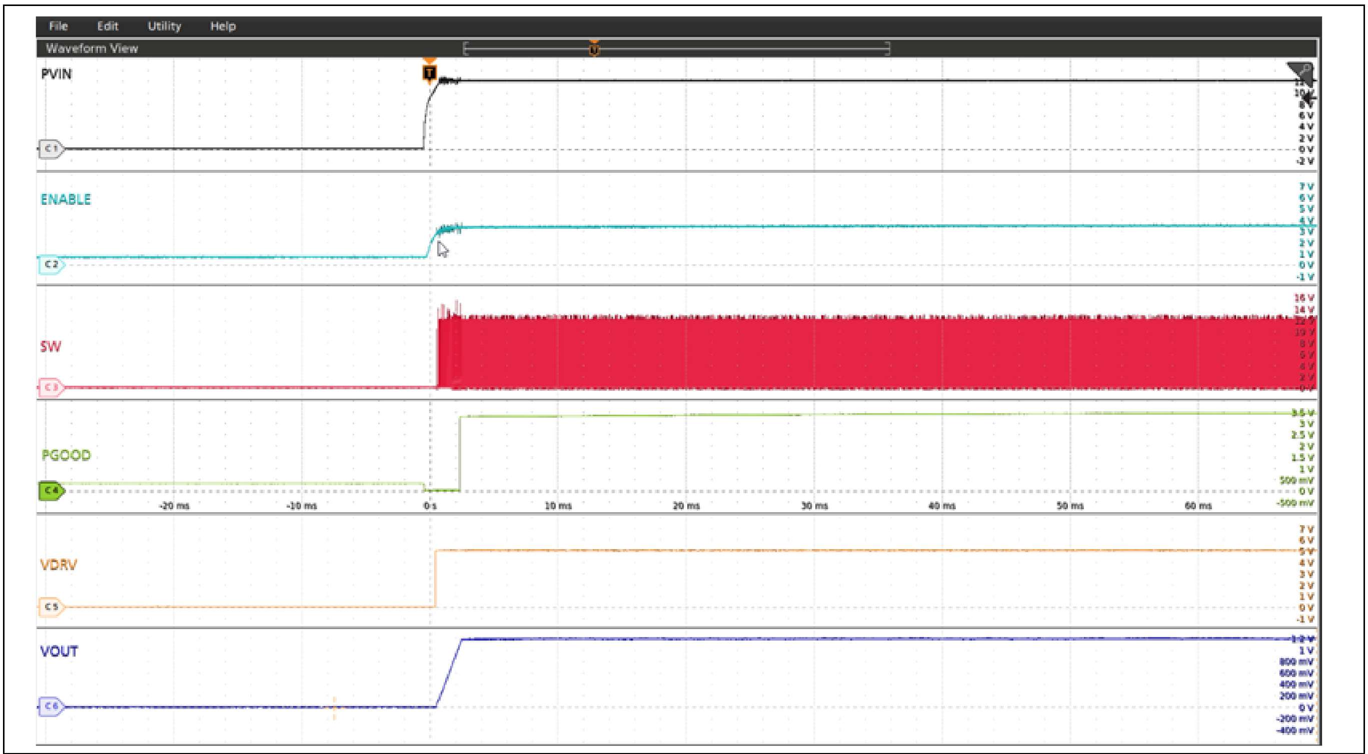

Figure 15 Start up at 0 A load (Ch_1: PVin, Ch_2: Enable, Ch_3: Switch node, Ch_4: PGOOD, Ch_5: VDRV, Ch_6: V_{out})

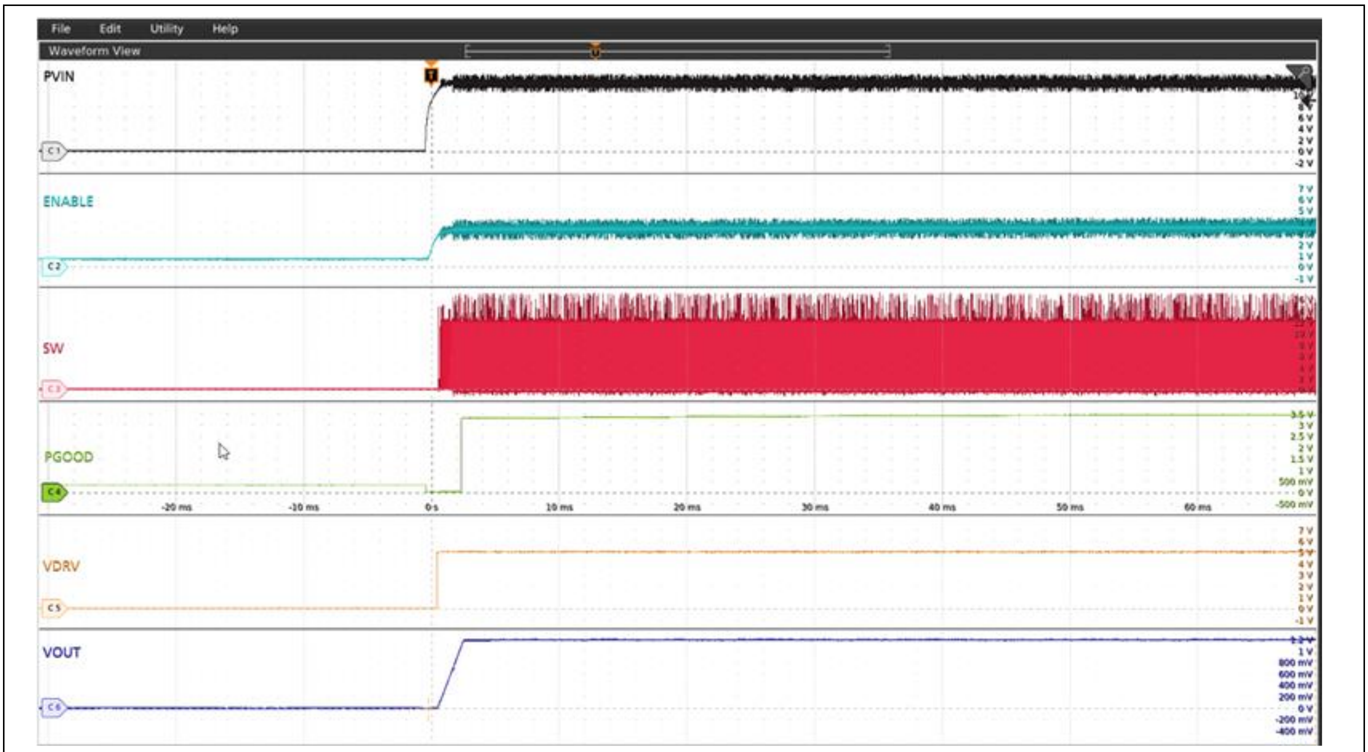

Figure 16 Start up at 20 A load (Ch_1:PV_{in}, Ch_2: Enable, Ch_3: Switch node, Ch_4: PGOOD, Ch_5: VDRV, Ch_6: V_{out})

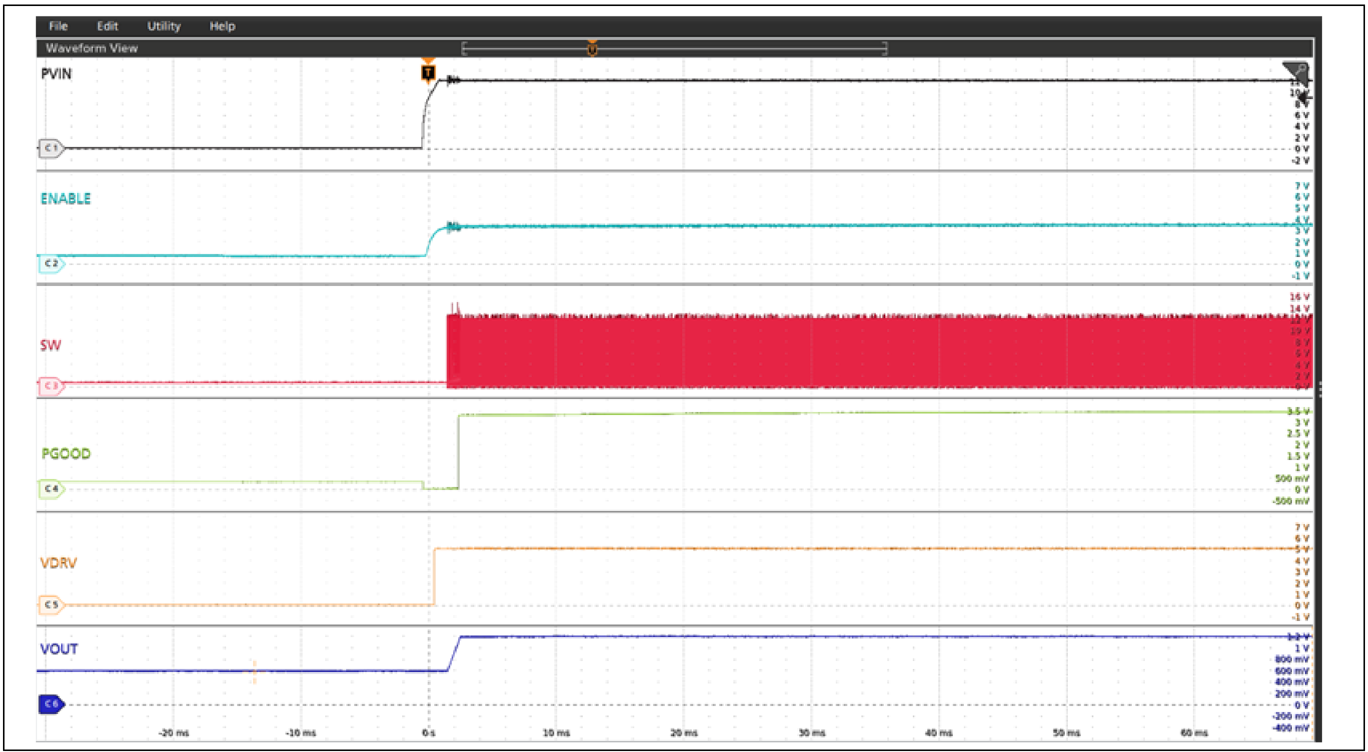

Figure 17 Pre-bias start up at 0 A, pre-bias voltage = 0.6 V (Ch_1: PV_{in}, Ch_2: Enable, Ch_3: Switch node, Ch_4: PGOOD, Ch_5: VDRV, Ch_6: V_{out})

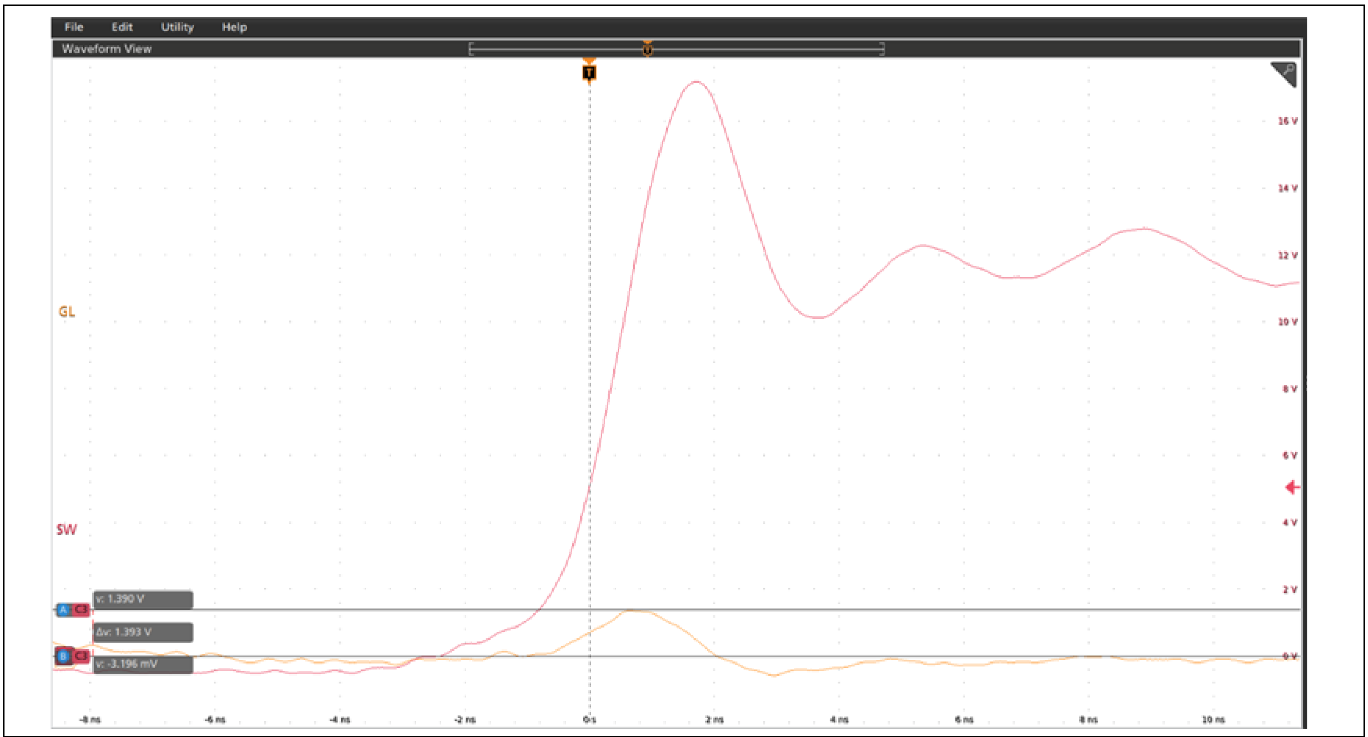

Figure 18 SW and GL, 25 A load, f_{sw} = 800 kHz

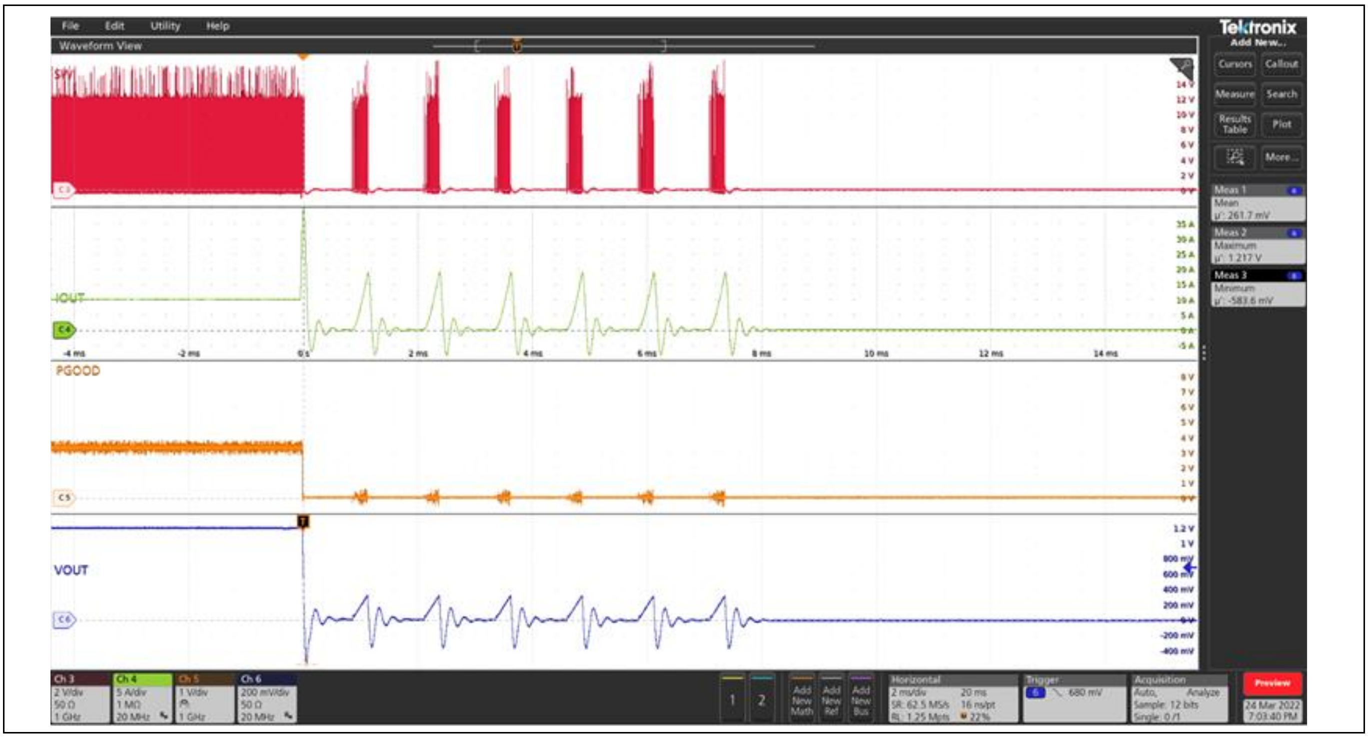

Figure 19 Short circuit and retry 6-times and shutdown (Ch$_1$: Switch node, Ch$_2$: V_{out}, Ch$_3$: PGOOD, Ch$_4$: I_{out})

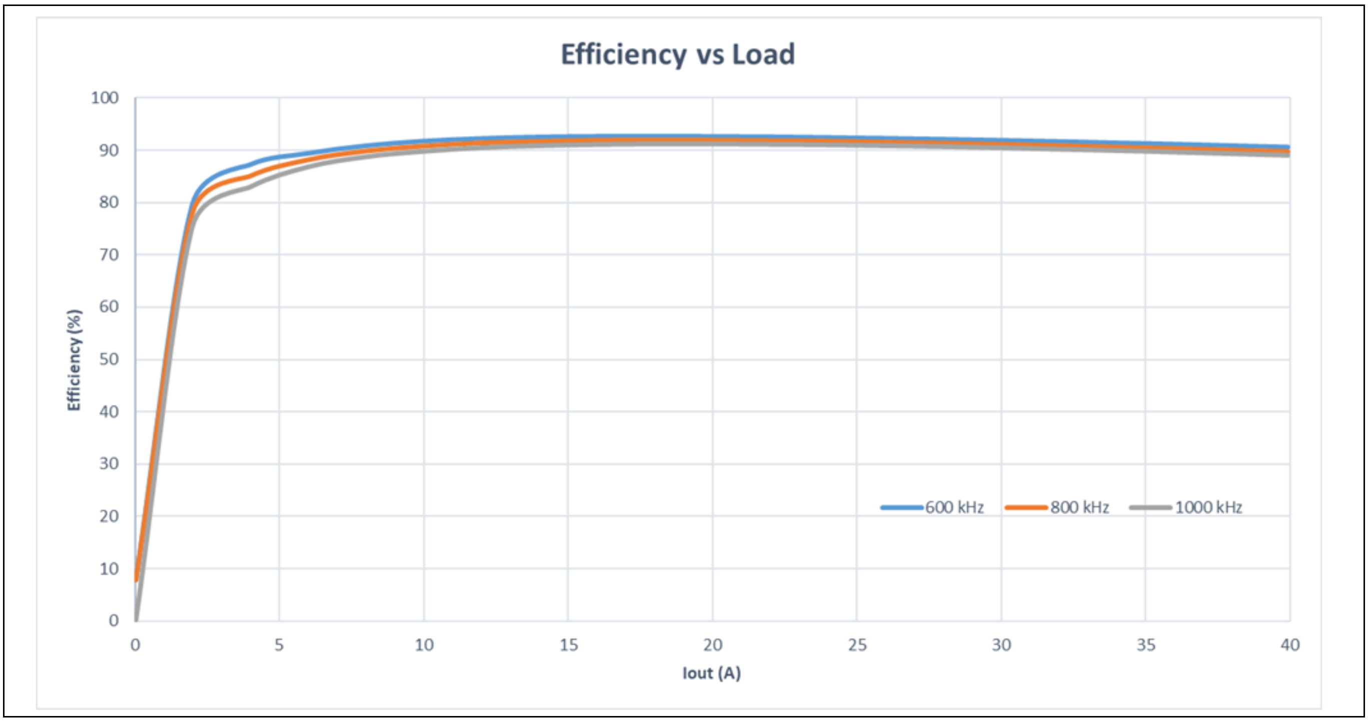

Figure 20 TDA38740A efficiency versus load current without airflow in FCCM with external V_{cc} (12 V_{in}, 1.2 V_{out}, no air flow, 150 nH, 600 kHz/800 kHz/1000 kHz, T_a = 25 °C)

Figure 21 Power loss versus load current without airflow in FCCM with external V_{cc} (12 V_{in}, 1.2 V_{out}, no air flow, 150nH, 600 kHz/800 kHz/1000 kHz, T_a = 25 °C)

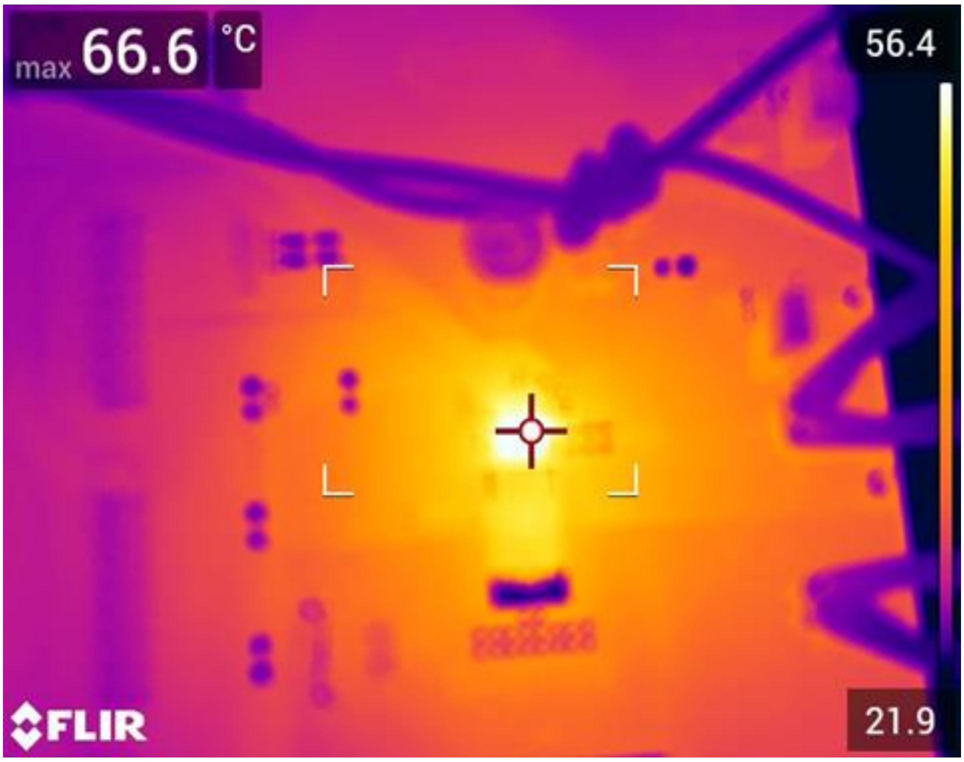

Figure 22 Thermal image of the board at 1.2 V, 40 A load, TDA38740A = 66.6 °C, L = 47.3 °C, Amb = 21.9 °C, natural convection, f_{sw} = 1000 kHz

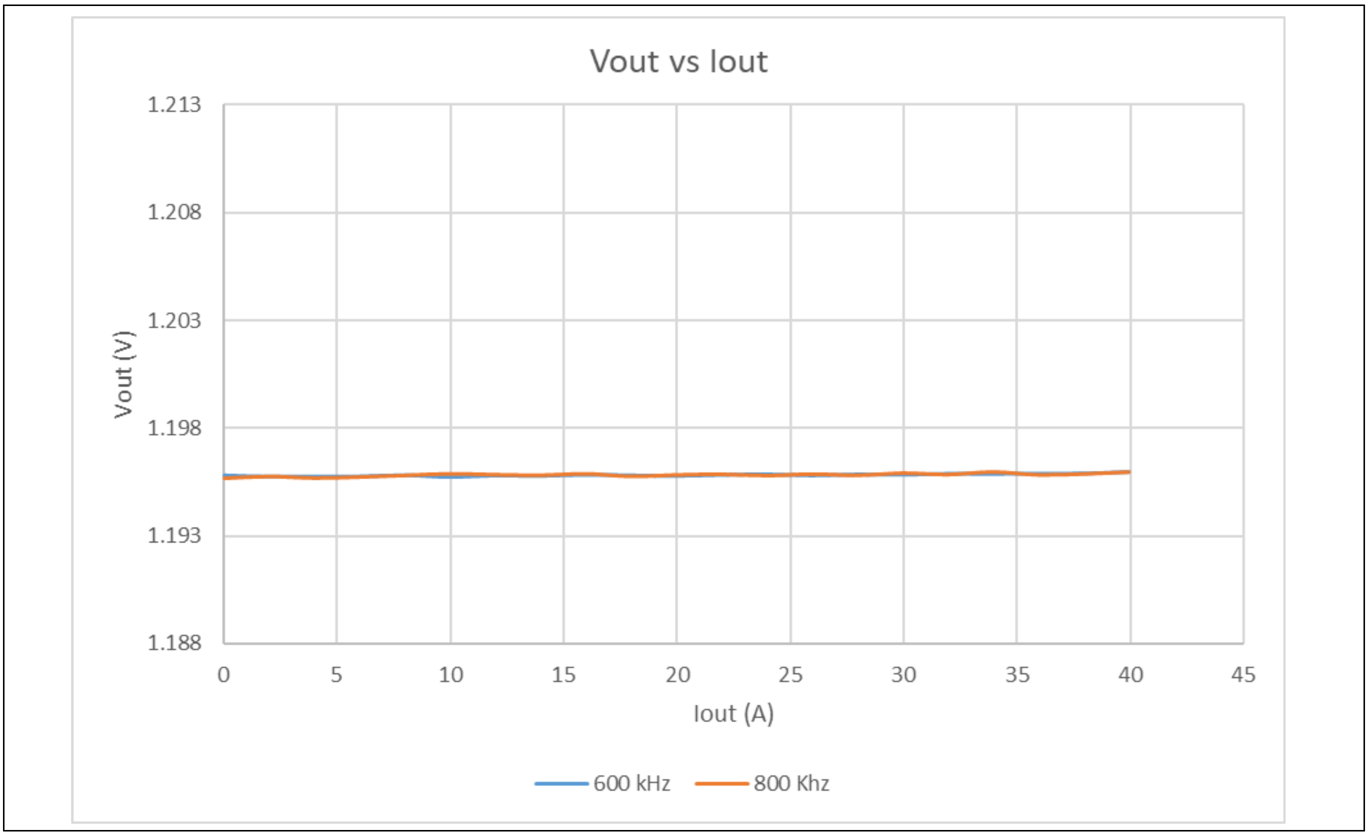

Figure 23 **TDA38740A V_{out} regulation (12 V_{in}, 1.2 V_{out}, no air flow, 150 nH, 600/800 kHz, T_a = 25 °C)**

Operating conditions: PV_{in} = 12.0 V, V_{out} = 3.3 V, I_{out} = 0 – 40 A, room temperature, no airflow.

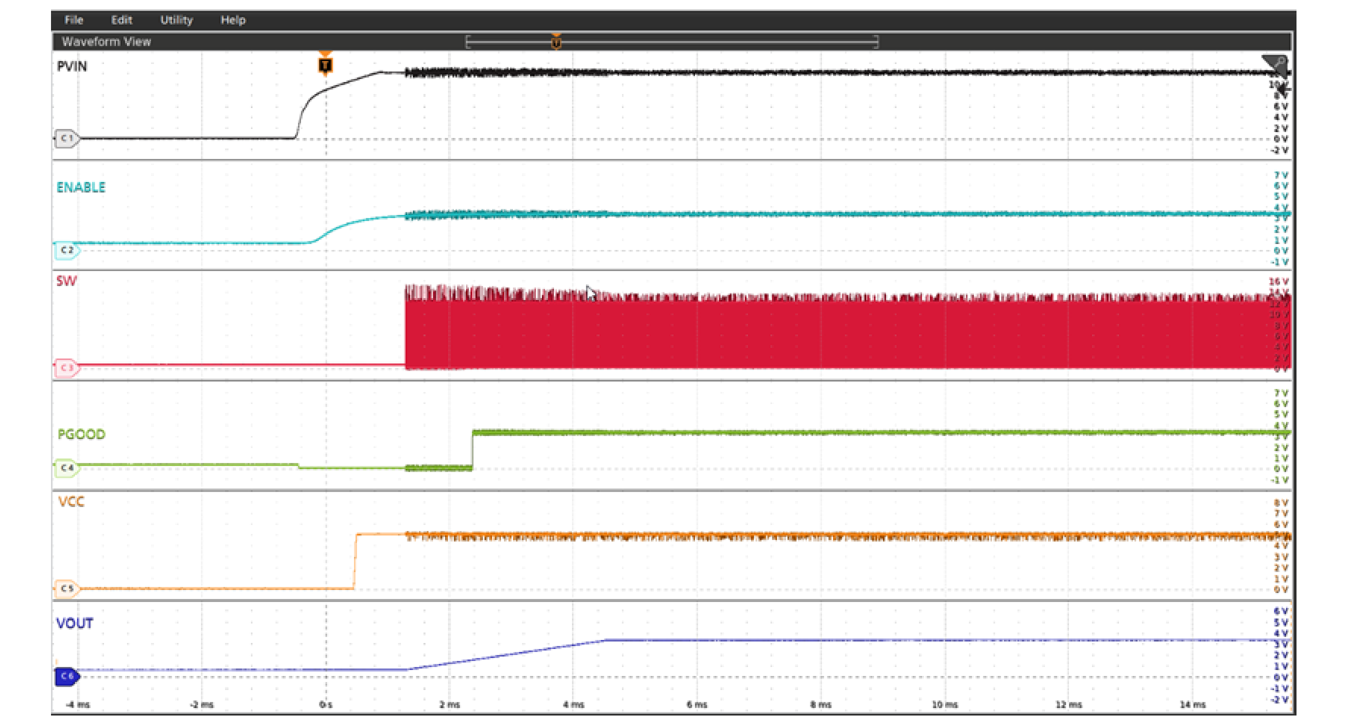

Figure 24 **Start up at 0 A load (Ch₁: PV_{in}, Ch₂: Enable, Ch₃: Switch node, Ch₄: PGOOD, Ch₅: VDRV, Ch₆: V_{out})**

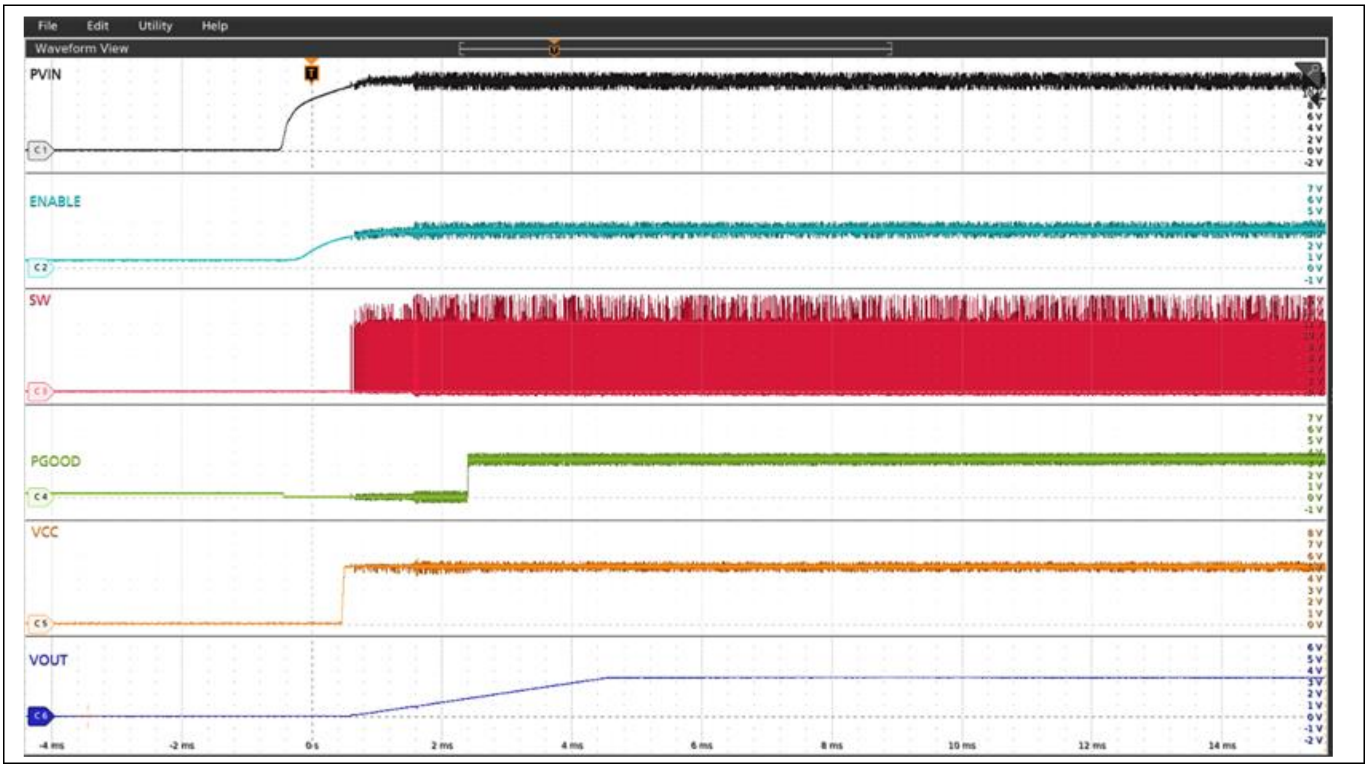

Figure 25 **Start up at 20 A load (Ch₁: PV_{in}, Ch₂: Enable, Ch₃: Switch node, Ch₄: PGOOD, Ch₅: VDRV, Ch₆: V_{out})**

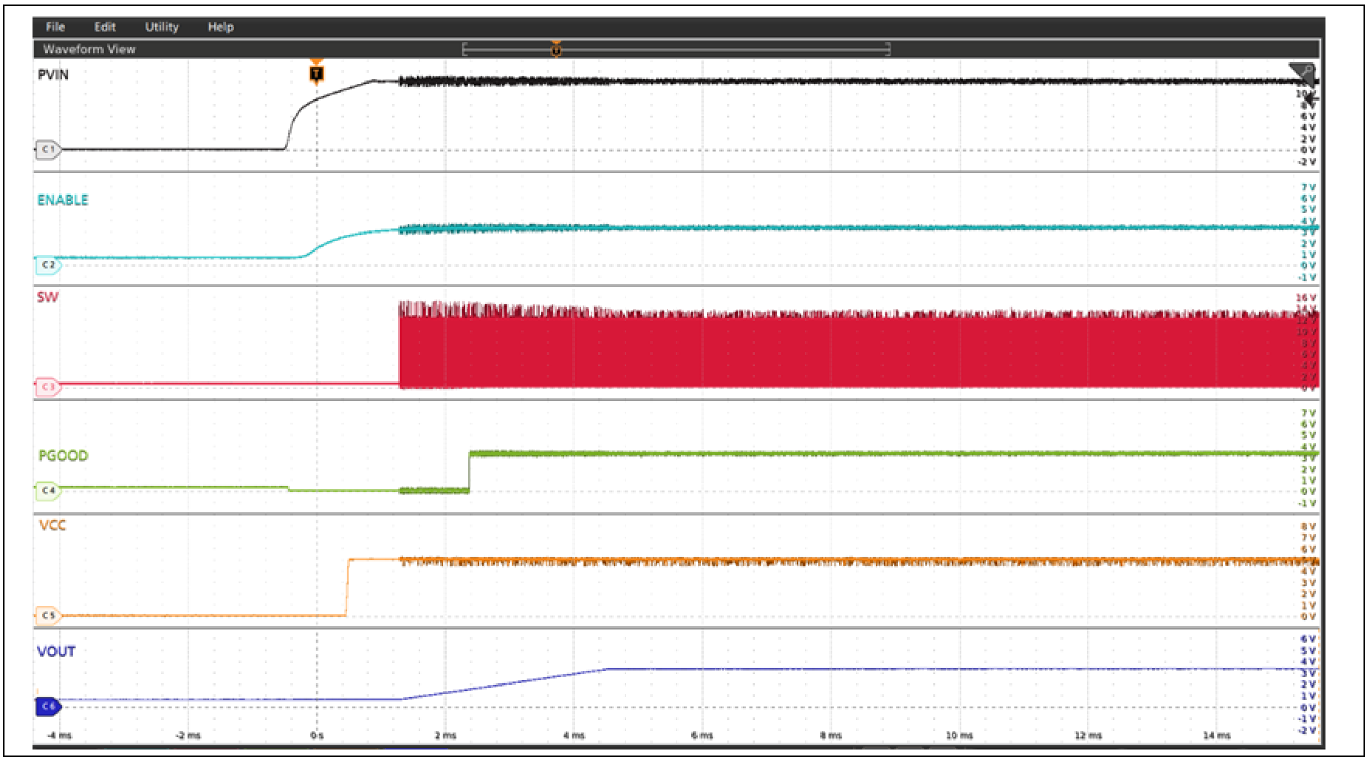

Figure 26 Pre-bias start up at 0 A, pre-bias voltage = 0.6 V (Ch_1: PV_{in}, Ch_2: Enable, Ch_3: Switch node, Ch_4: PGOOD, Ch_5: VDRV, Ch_6: V_{out})

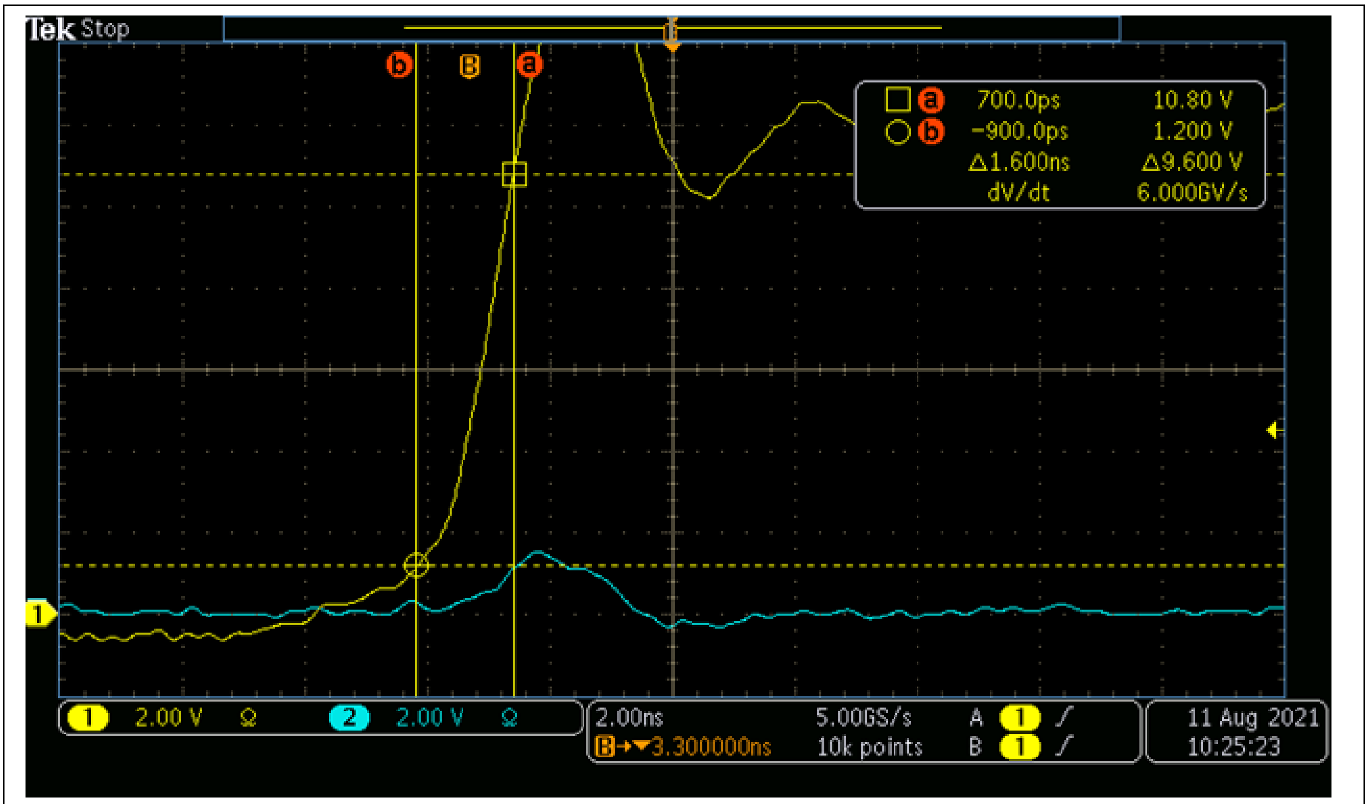

Figure 27 SW and GL, 30 A load, f_{sw} = 800 kHz

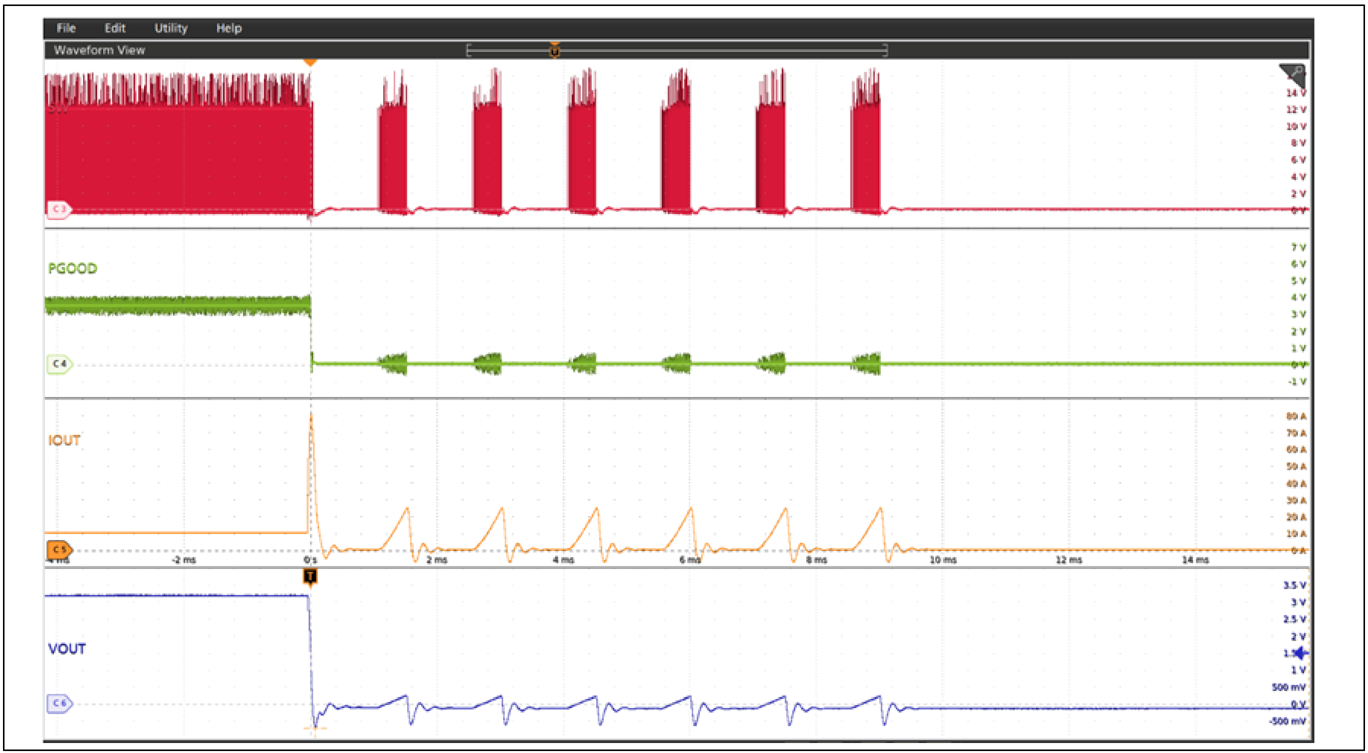

Figure 28 Short circuit and retry 6-times and shutdown (Ch_1: Switch node, Ch_2: V_{out}, Ch_3: PGOOD, Ch_4: I_{out})

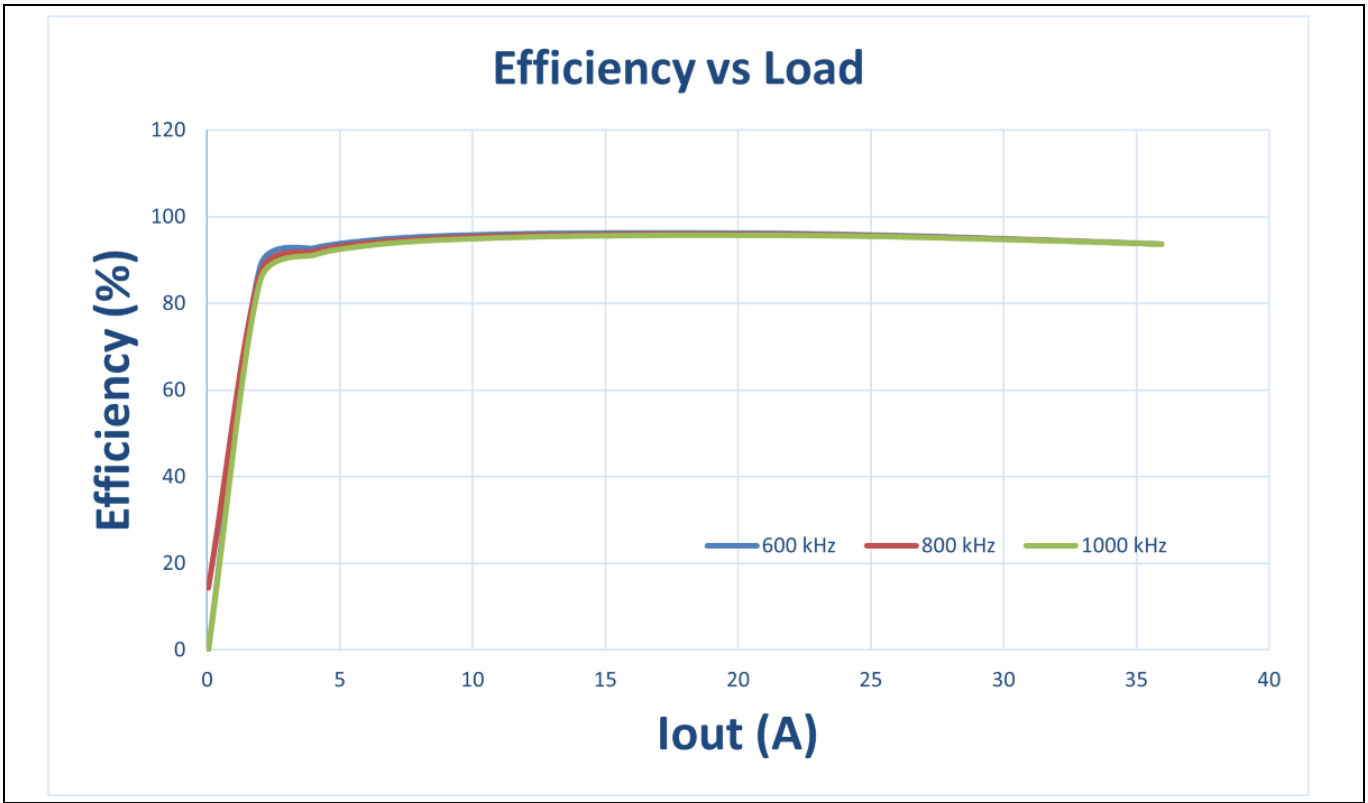

Figure 29 TDA38740A efficiency versus load current without airflow in FCCM with external V_{cc} (12 V_{in}, 3.3 V_{out}, no air flow, 470 nH, 600 kHz/800 kHz/1000 kHz, T_a = 25 °C)

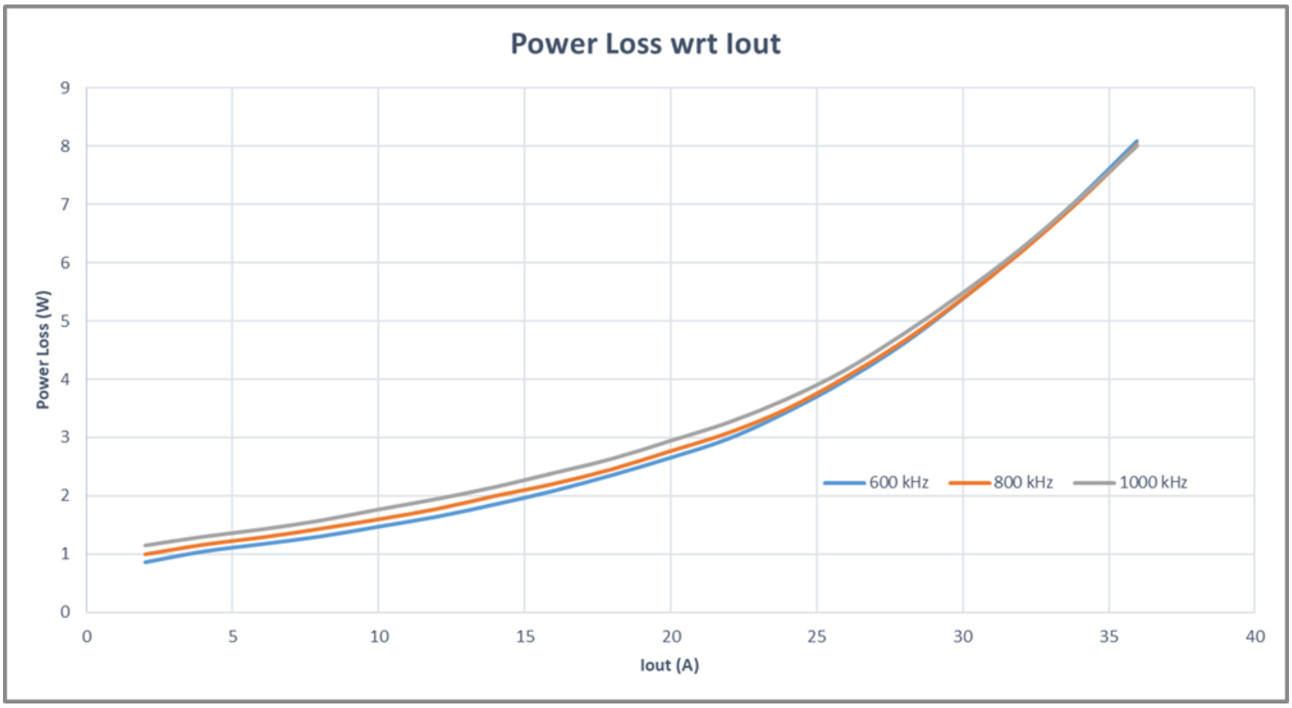

Figure 30 Power loss versus load current without airflow in FCCM with external V_{cc} (12 V_{in}, 1.2 V_{out}, no air flow, 470 nH, 600 kHz/800 kHz/1000 kHz, T_a = 25 °C)

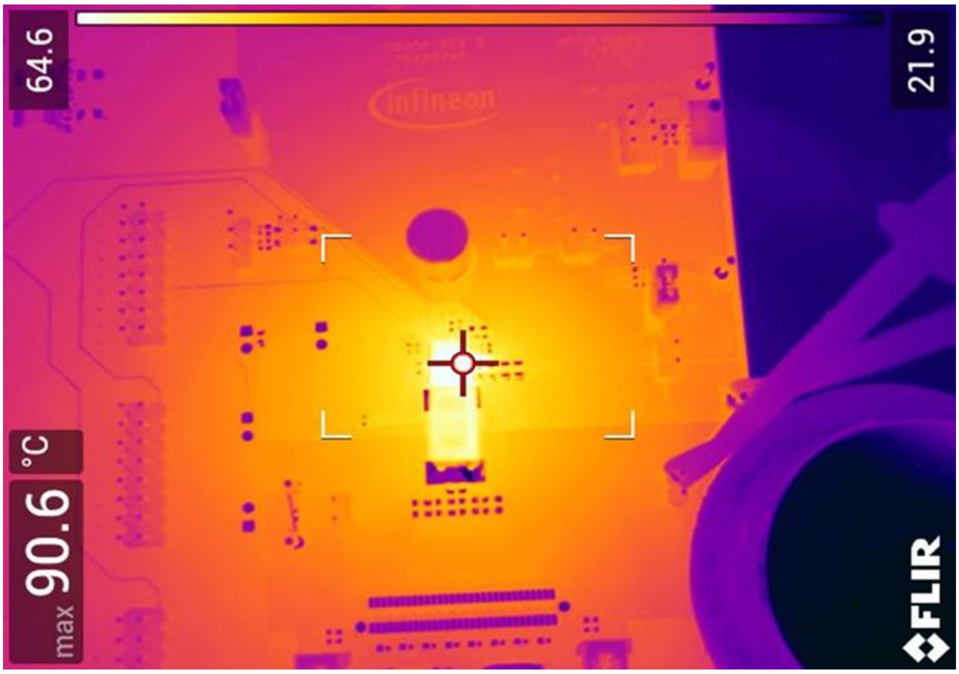

Figure 31 Thermal image of the board at 3.3 V, 35 A load, TDA38740A = 90.6 °C, L = 61.3 °C, Amb = 22.3 °C, natural convection, f_{sw} = 1000 kHz

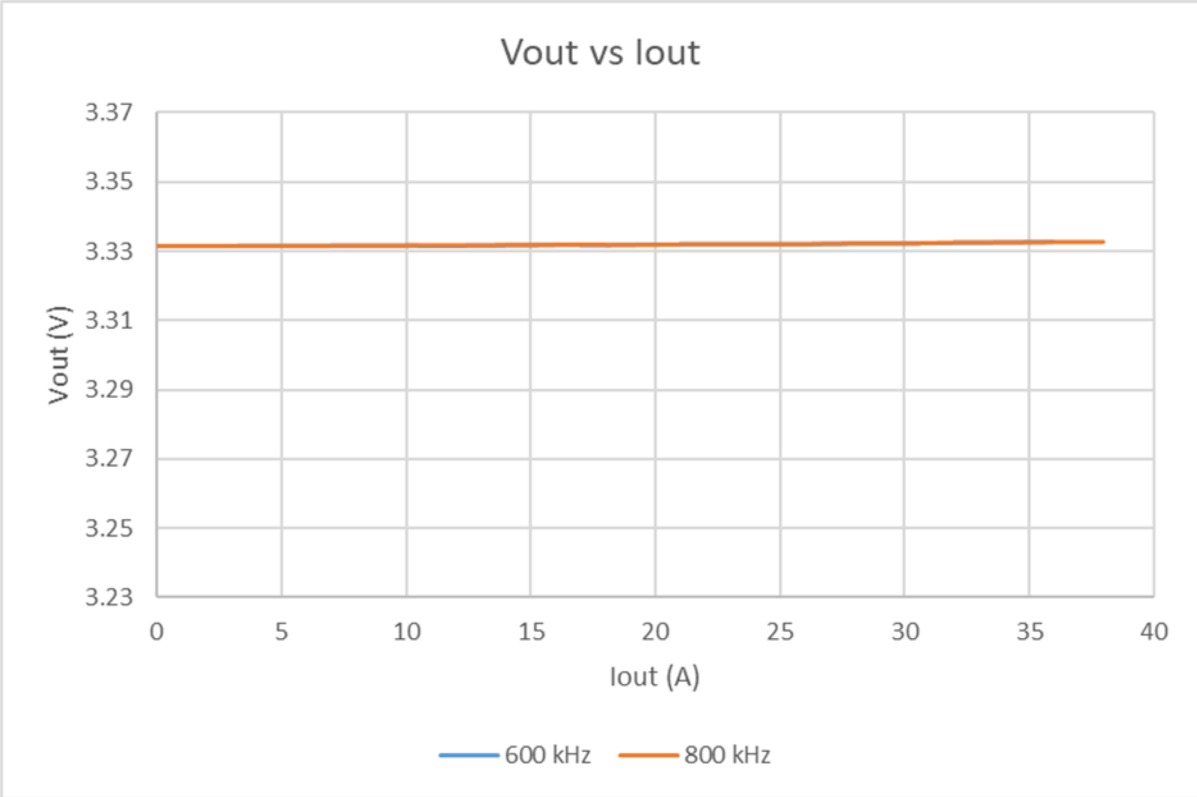

Figure 32 TDA38740A V_{out} regulation (12 V_{in}, 3.3 V_{out}, no air flow, 470 nH, 600/800 kHz, T_a = 25 °C)

References

[1] Infineon Technologies AG: TDA38740A OptiMOS™ IPOL 40 A single-voltage synchronous buck regulator datasheet.

Revision history

Document revision	Date	Description of changes
V 1.0	2024-06-30	Initial release

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