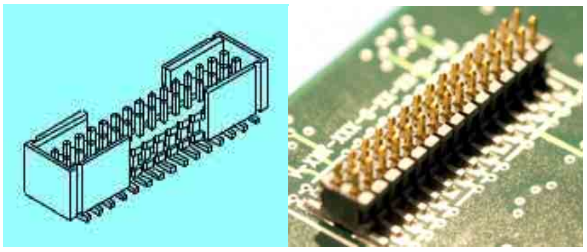
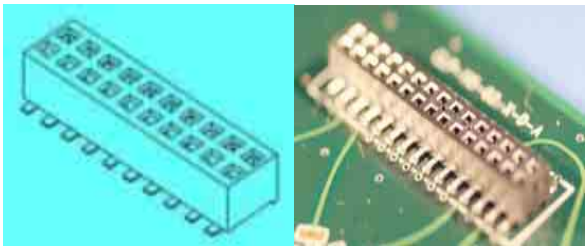
High Speed Characterization Report

FTSH-115-03-L-DV-A



Mated With



CLP-115-02-L-D-A

Description:

Parallel Board-to-Board, 0.050” [1.27mm] Pitch, 5.13mm (0.202”) Stack Height

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Report Revision: 9/29/2005

Series: FTSH/CLP Low Profile Socket and Terminal Strip
Description: Parallel Board-to-Board, 0.050" [1.27mm] Pitch, 5.13mm (0.202") Stack Height

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Connector Overview

Micro 1.27mm (.050”) pitch socket and terminal strip interfaces (CLP/FTSH Series’) are available with up to 50 contacts per row and board-to-board spacings of 5.13mm (0.202"), 5.18mm (0.204"), and 7.47mm (0.294) between boards. The data in this report is applicable only to the standard 5.13mm (0.202") board-to-board stack height version.

Connector System Speed Rating

FTSH/CLP Series, Parallel Board-to-Board, 1.27mm Pitch, 5.13mm (0.202") Stack Height

Signaling	Speed Rating
Single-Ended:	**7.0 GHz / 14 Gbps**
Differential:	**8.5 GHz / 17 Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

To calculate the Speed Rating, the measured -3 dB point is rounded up to the nearest half-GHz level. The up-rounding corrects for a portion of the test board’s trace loss, since trace losses are included in the loss data in this report. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

For example, a connector with a -3 dB point of 7.8 GHz would have a Speed Rating of 8 GHz/ 16 Gbps. A connector with a -3 dB point of 7.2 GHz would have a Speed Rating of 7.5 GHz/ 15 Gbps.

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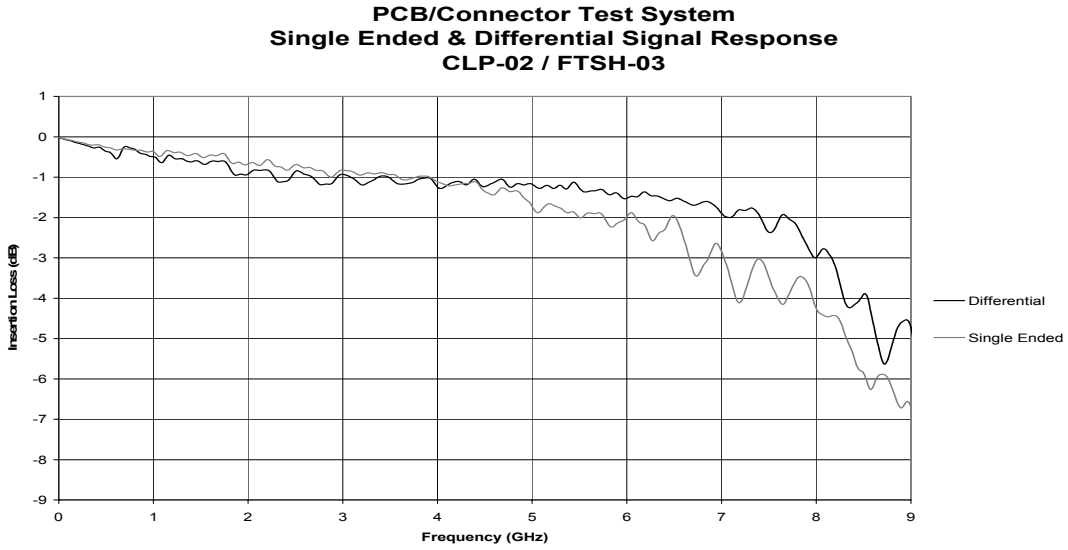
Frequency Domain Data Summary

Table 1 - Single-Ended Connector System Performance		
Test Parameter	**Configuration**	
Insertion Loss	GSG	**-3dB @ 6.68 GHz**
Return Loss	GSG	≤ -5dB to 6.68 GHz
Near-End Crosstalk	GAQG	≤ -8dB to 6.68 GHz
	GAGQG	≤ -20dB to 6.68 GHz
	Xrow, GAG to GQG	≤ -10dB to 6.68 GHz
Far-End Crosstalk	GAQG	≤ -10dB to 6.68 GHz
	GAGQG	≤ -12dB to 6.68 GHz
	Xrow, GAG to GQG	≤ -18dB to 6.68 GHz

Table 2 - Differential Connector System Bandwidth		
Test Parameter	**Configuration**	
Insertion Loss	GSSG	**-3dB @ 8.18 GHz**
Return Loss	GSSG	≤ -5dB to 8.18 GHz
Near-End Crosstalk	GAAQQG	≤ -15dB to 8.18 GHz
	GAAGQQG	≤ -28dB to 8.18 GHz
	Xrow, GAASS to GQQG	≤ -15dB to 8.18 GHz
Far-End Crosstalk	GAAQQG	≤ -15dB to 8.18 GHz
	GAAGQQG	≤ -25dB to 8.18 GHz
	Xrow, GAASS to GQQG	≤ -15dB to 8.18 GHz



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Time Domain Data Summary

Table 3 - Single-Ended Impedance (Ω)							
Signal Risetime	**30±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	57.1	51.3	51.1	50.4	50.3	50.1	50.0
Minimum Impedance	35.3	39.8	42.0	45.0	47.0	48.0	48.6

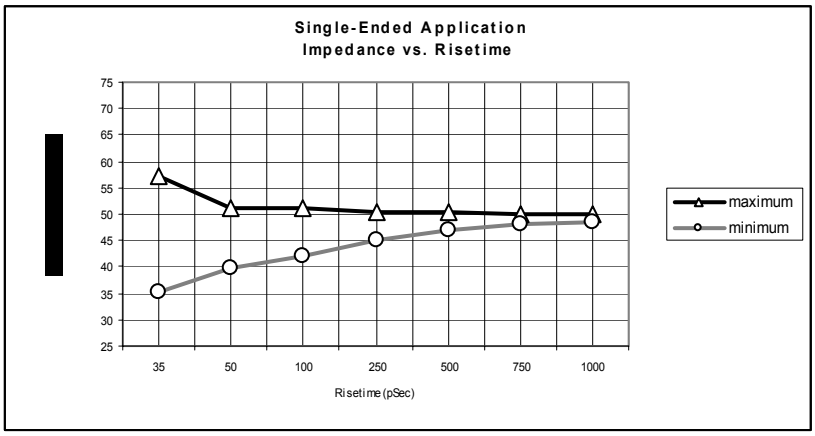

Table 4 - Differential Impedance (Ω)							
Signal Risetime	**30±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	101.3	100.7	100.7	100.6	100.6	100.5	100.4
Minimum Impedance	63.6	71.3	76.0	82.8	89.3	92.3	94.1

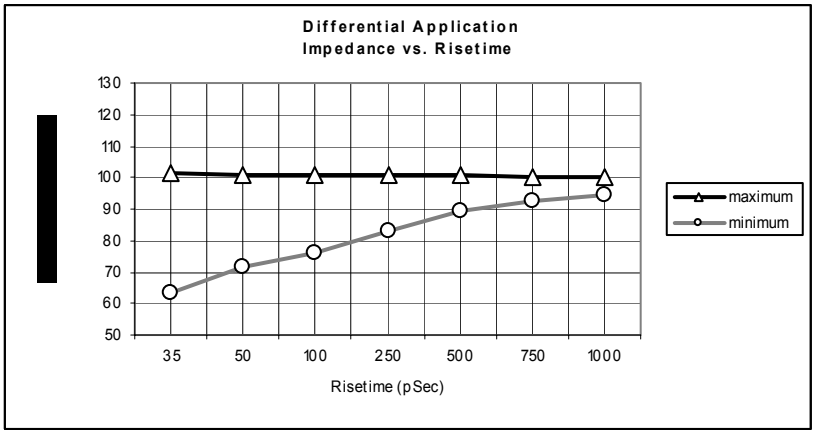

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Table 5 - Single-Ended Crosstalk (%)								
Input (t_r)		**30±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
NEXT	GAQG	13.9	12.2	9.5	4.6	2.5	1.7	1.3
	GAGQG	4.9	2.5	1.6	< 1.0	< 1.0	< 1.0	< 1.0
	$Xrow^{se}$	8.9	7.0	5.4	2.5	1.3	< 1.0	< 1.0
FEXT	GAQG	8.2	6.0	3.7	1.3	< 1.0	< 1.0	< 1.0
	GAGQG	3.5	2.3	1.5	< 1.0	< 1.0	< 1.0	< 1.0
	$Xrow^{se}$	7.0	4.5	2.6	< 1.0	< 1.0	< 1.0	< 1.0

Table 6 - Differential Crosstalk (%)								
Input (t_r)		**30±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
NEXT	GAAQQSS	4.6	3.9	2.9	1.4	< 1.0	< 1.0	< 1.0
	GAAGQQG	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0
	$Xrow^{diff}$	4.4	3.7	2.6	1.1	< 1.0	< 1.0	< 1.0
FEXT	GAAQQSS	2.0	1.1	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0
	GAAGQQG	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0
	$Xrow^{diff}$	1.9	1.3	< 1.0	< 1.0	< 1.0	< 1.0	< 1.0

Table 7 - Propagation Delay (Mated Connector)	
Single-Ended	78ps
Differential	72ps

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Characterization Details

This report presents data which characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the test PCB from drive side probe tips to receive side probe tips. PCB effects are not removed or de-embedded from the test data. PCB designs with impedance mismatch, large losses, skew, cross talk, or similar impairments can have a significant impact on observed test data. Therefore, great design effort is put forth to limit these effects in the PCB utilized in these tests. Some board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. But other effects, such as via coupling or stub resonance, are not evaluated here. Such effects are addressed and characterized fully by the Samtec Final Inch® products.

Additionally, intermediate test signal connections can mask the connectors' true performance. Such connection effects are minimized by using high performance test cables, adapters, and microwave probes. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differential and single-ended drive scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications, and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield is used as the signal return, while in others, connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. So care must be taken when choosing signal/ground ratios in cost- or density-sensitive applications.

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For this connector, the following configurations were evaluated:

Single-Ended Impedance:

- GSG (ground-signal-ground)

Single-Ended Crosstalk:

- Electrical "worst case": GAQG (ground-active-quiet-ground)
- Electrical "best case": GAGQG (ground-active-ground-quiet-ground)
- Across row: $Xrow^{se}$ (from one row of terminals to the other row or across the ground blade when applicable)

Differential Impedance:

- GSSG (Ground-positive signal-negative signal-ground)

Differential Crosstalk:

- Electrical "worst case": GAAQQG (ground-active-active-quiet-quiet-ground)
- Electrical "best case": GAAGQQG (ground-active-active-ground-quiet-quiet-ground)
- Across row:$Xrow^{diff}$ (from one row of terminals to the other row or across the ground blade when applicable) (ground-active-active-static-static-ground) across the row of terminals to (ground-quiet-quiet-ground)

In all cases where a center ground blade is present in the connector it is always grounded to the PCB. Only one single-ended signal or differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of "SSSS", or four adjacent single ended signals, might be encountered, as opposed to the "GSG" and "GSSG" configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

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Signal Edge Speed (Rise Time):
In pulse signaling applications, the perceived performance of an interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 +/-5 ps. Generally, this should demonstrate worst case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 1.0 ns.

For this report, rise times were measured at 10%-90% signal levels.

Frequency Domain Data
Frequency domain parameters are helpful in evaluating the connector system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the frequency domain are insertion loss, return loss, and near-end and far-end crosstalk. Other parameters or formats, such as VSWR or S-parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated from time domain measurements using Fourier Transform calculations. Procedures and methods used in generating the SUT's frequency domain data are provided in the frequency domain test procedures in Appendix E of this report.

Time Domain Data
Time Domain parameters indicate impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. Time Domain data is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Reference plane impedance is 50 ohms for single-ended measurements and 100 ohms for differential measurements. The fastest risetime signal exciting the SUT is 30 ± 5 picoseconds.

In this report, propagation delay is defined as the signal propagation time through the PCB connector pads and connector pair. It does not include PCB traces. Delay is measured at 30 ± 5 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

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Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

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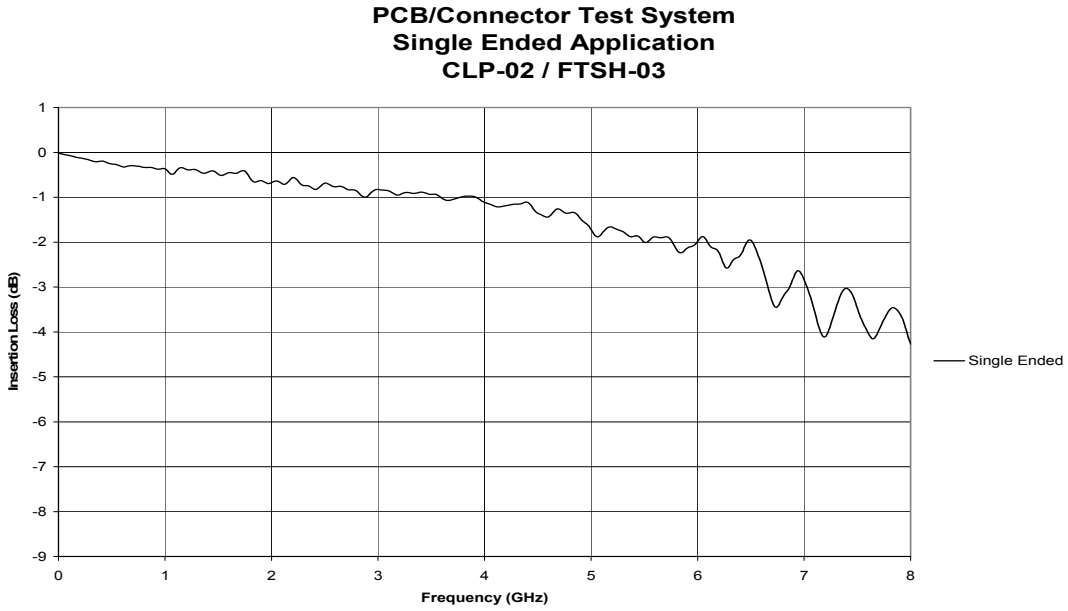
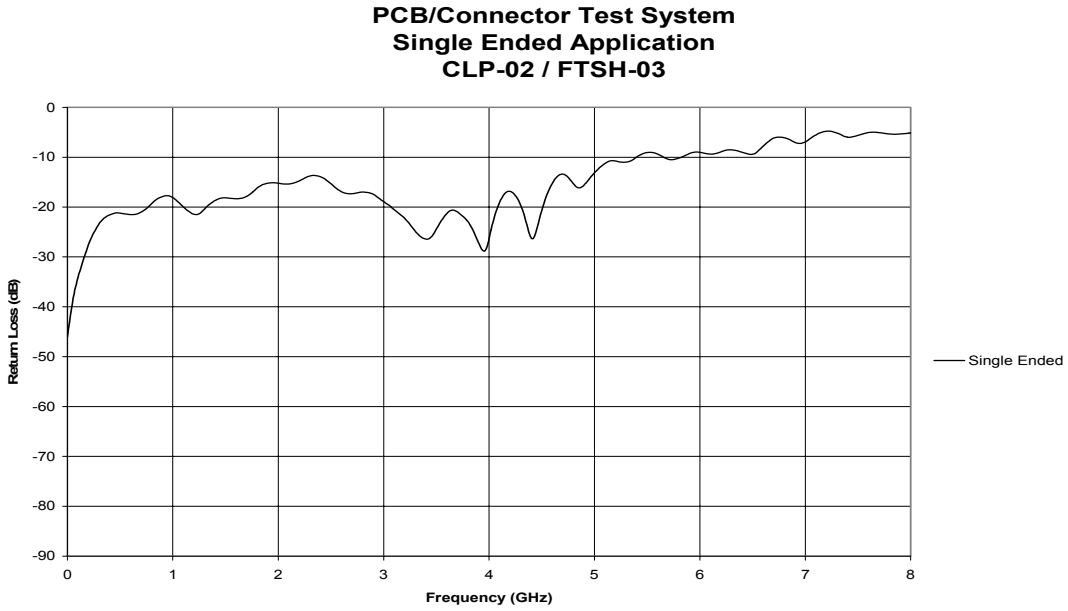
Appendix A – Frequency Domain Response Graphs

Single-Ended Application – Insertion Loss



Single-Ended Application – Return Loss



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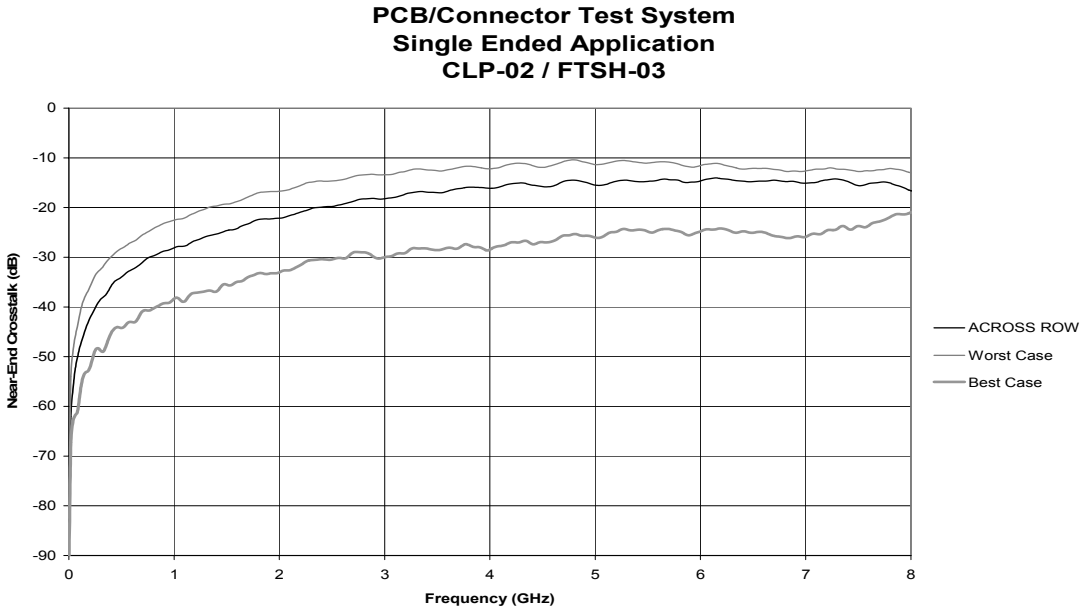
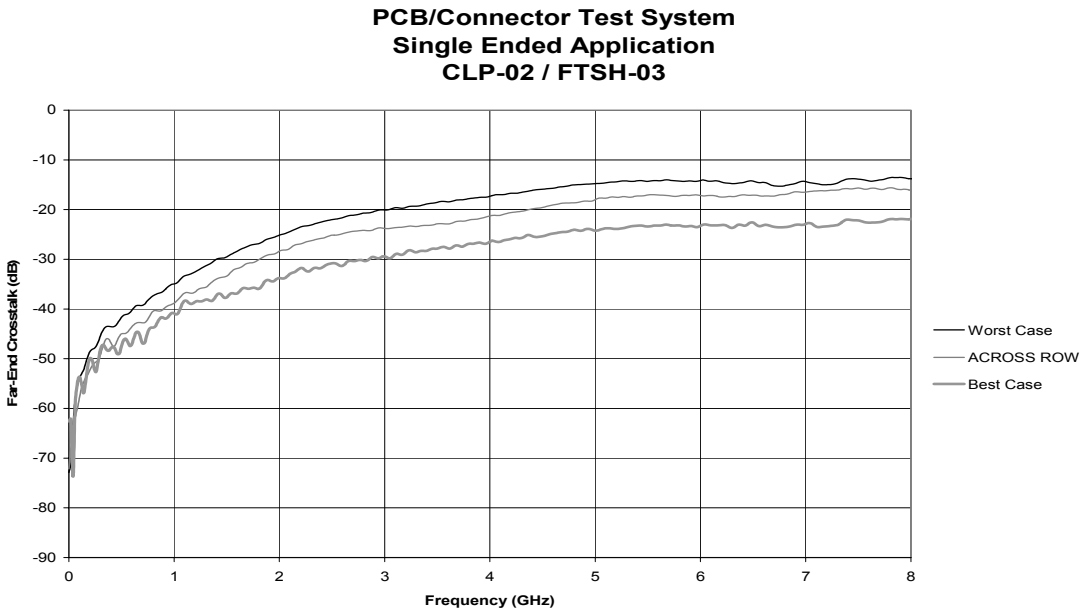
Single-Ended Application – NEXT



Single-Ended Application – FEXT



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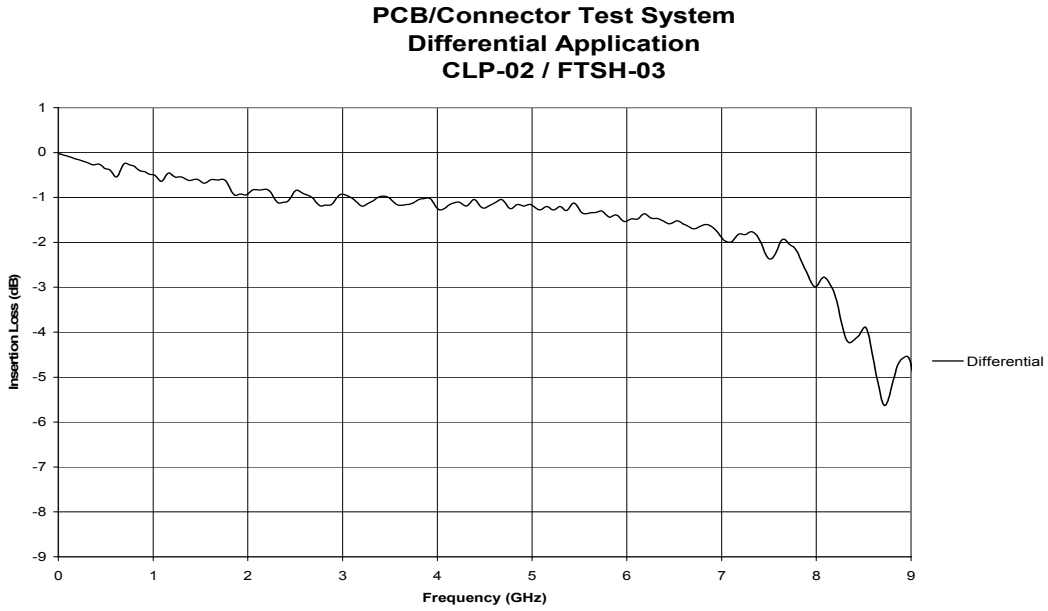
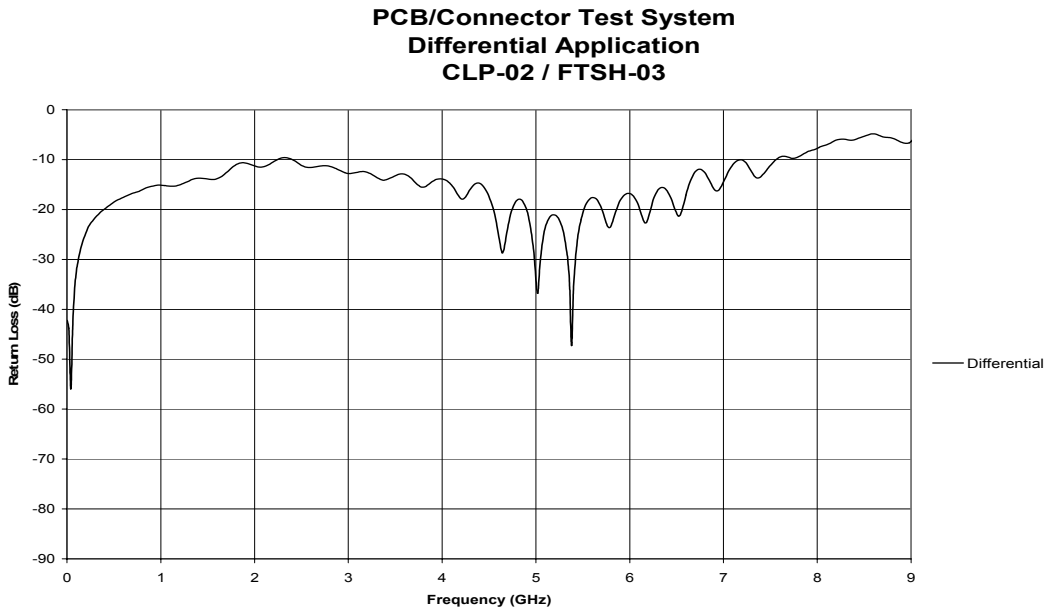
Differential Application – Insertion Loss



Differential Application – Return Loss



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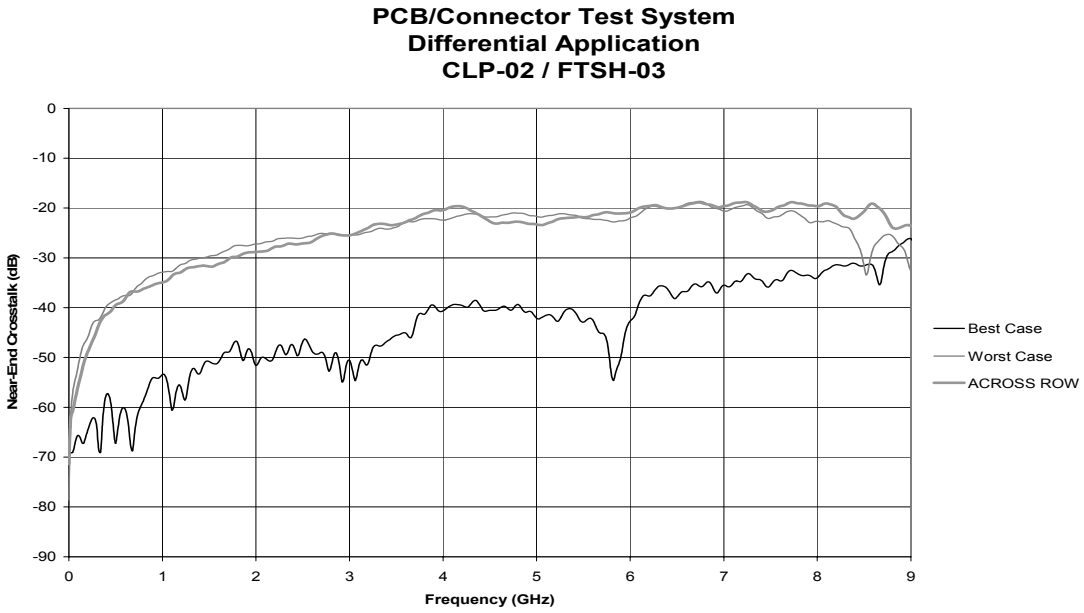
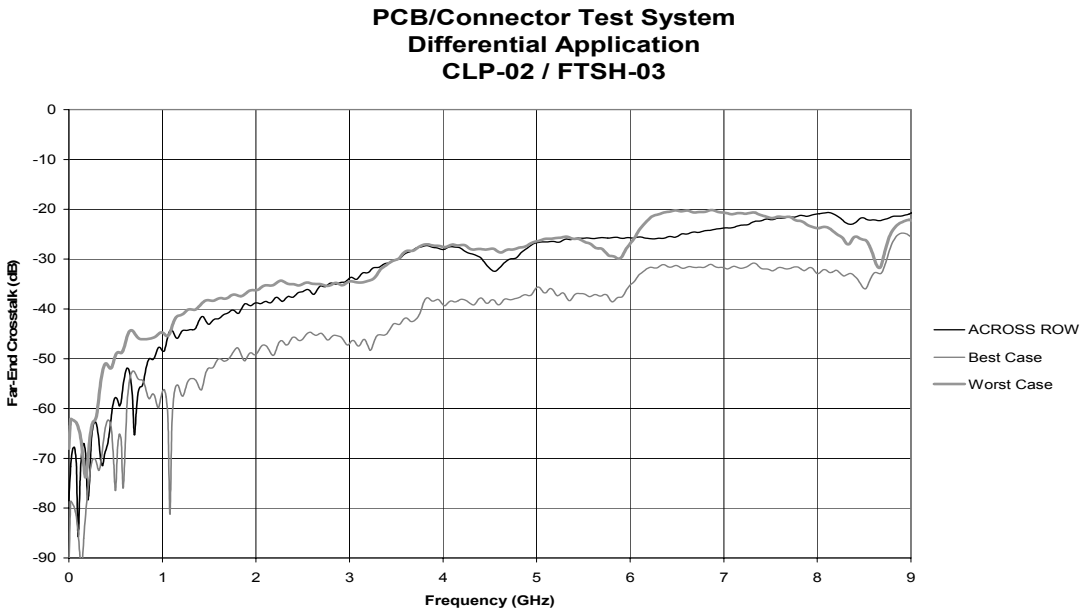
Differential Application – NEXT



Differential Application – FEXT



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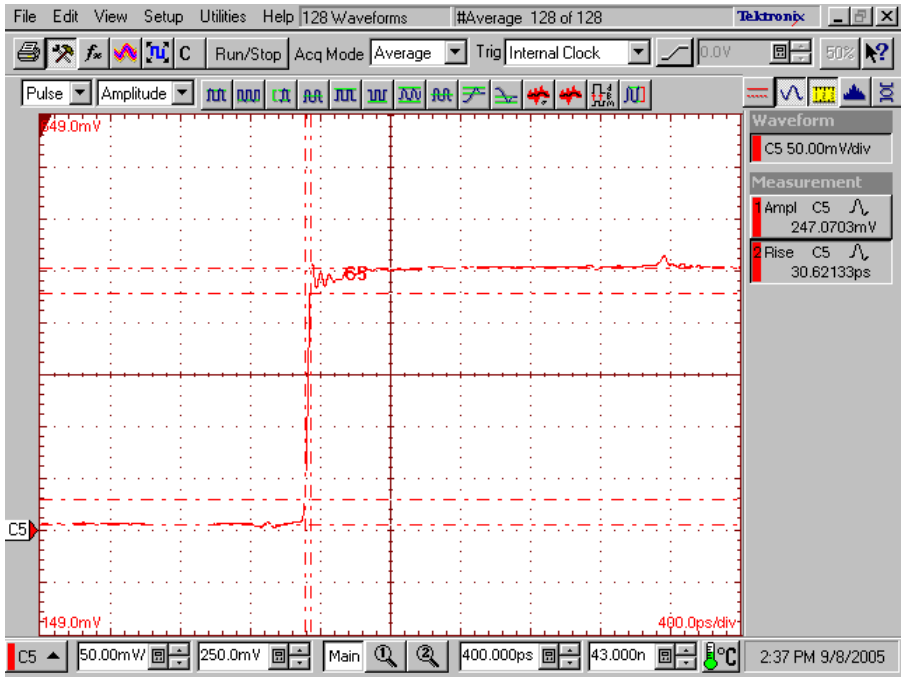
Appendix B – Time Domain Response Graphs

Single-Ended Application – Input Pulse



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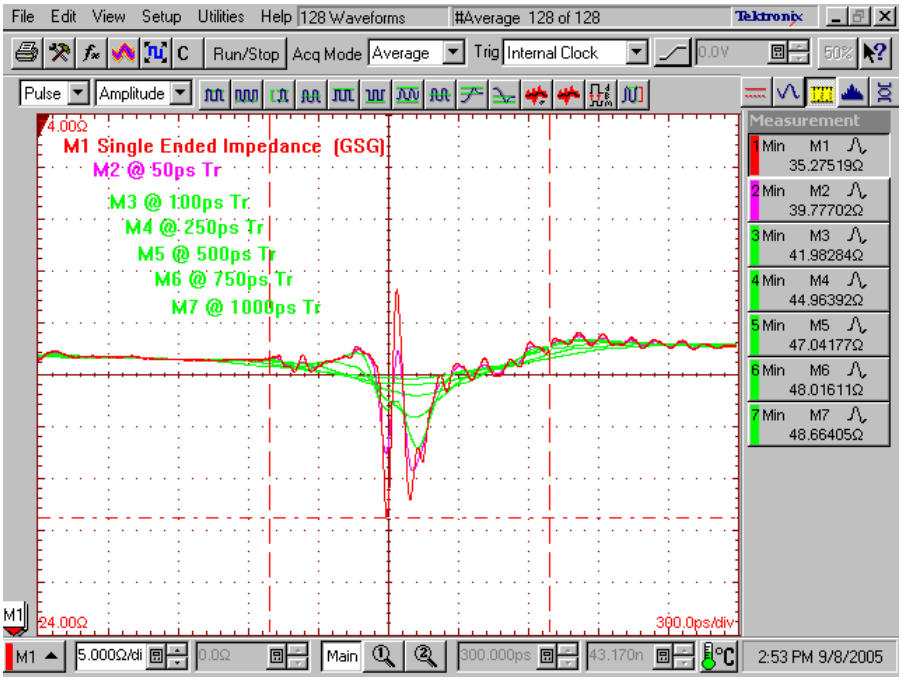
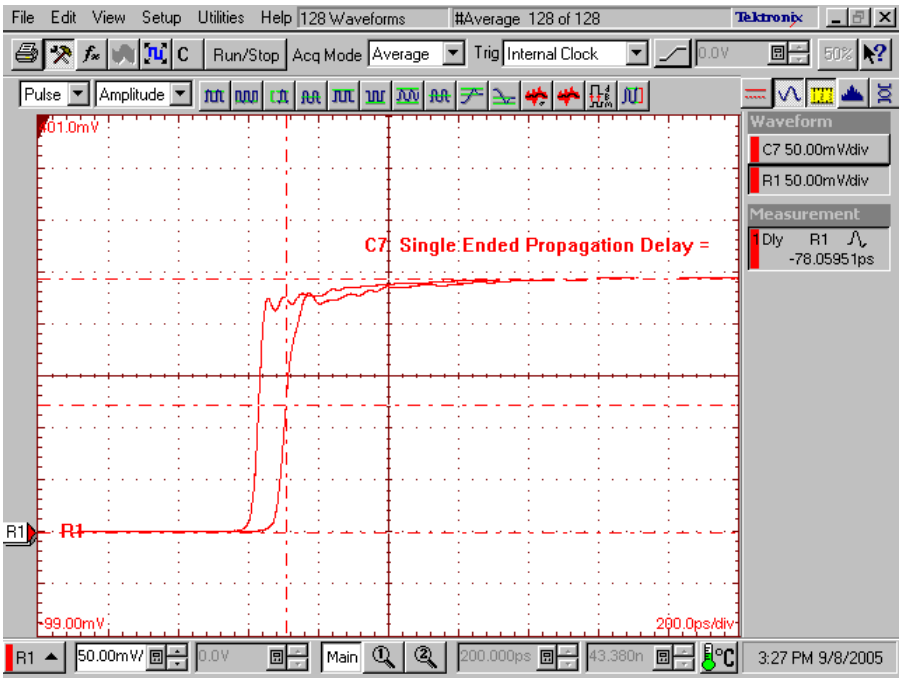
Single-Ended Application – Impedance



Single-Ended Application – Propagation Delay



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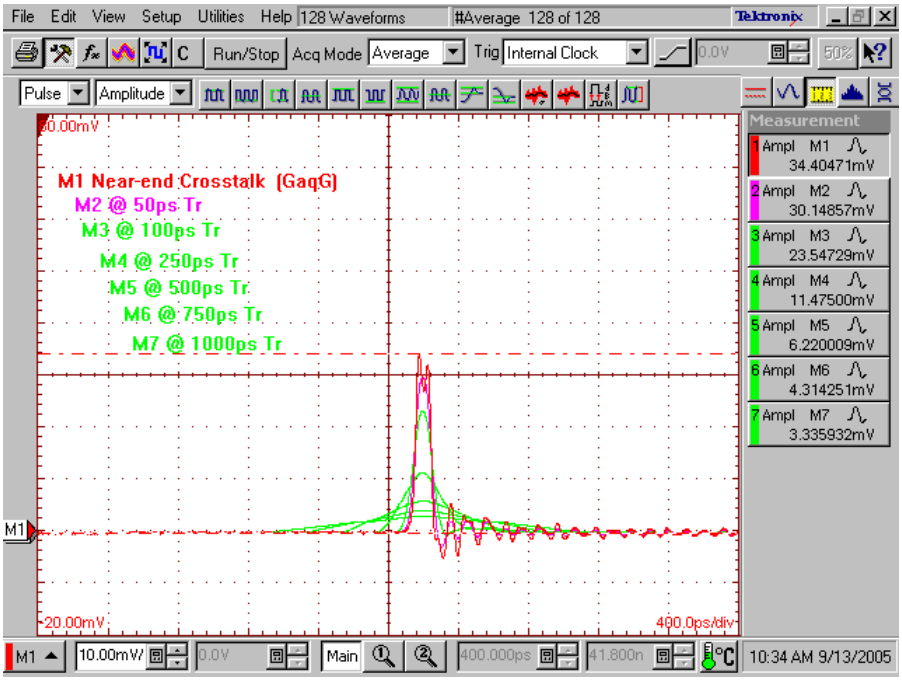
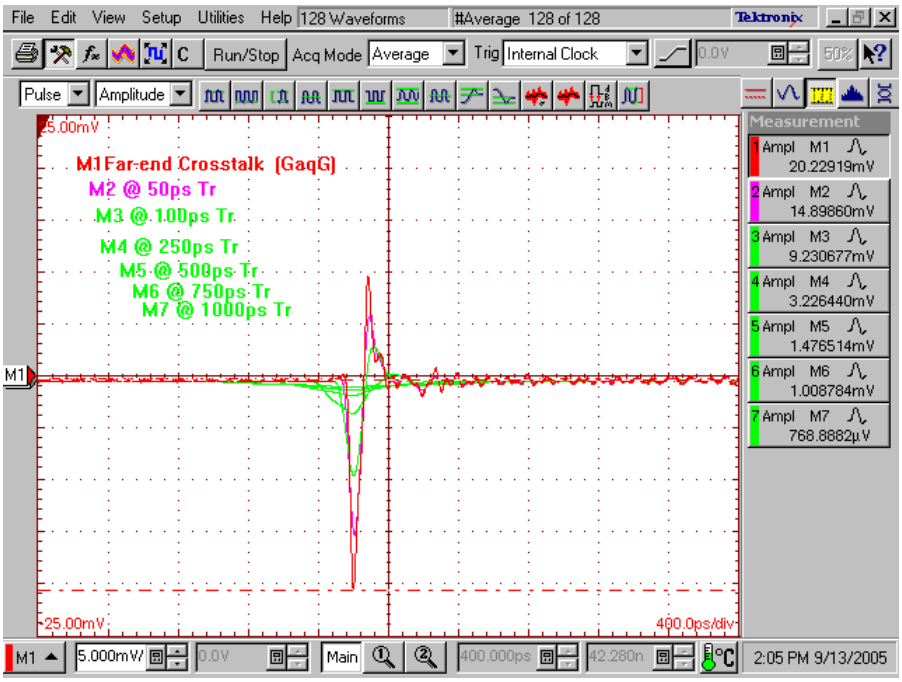
Single-Ended Application – NEXT, "Worst Case In Row" Configuration



Single-Ended Application – FEXT, "Worst Case In Row" Configuration



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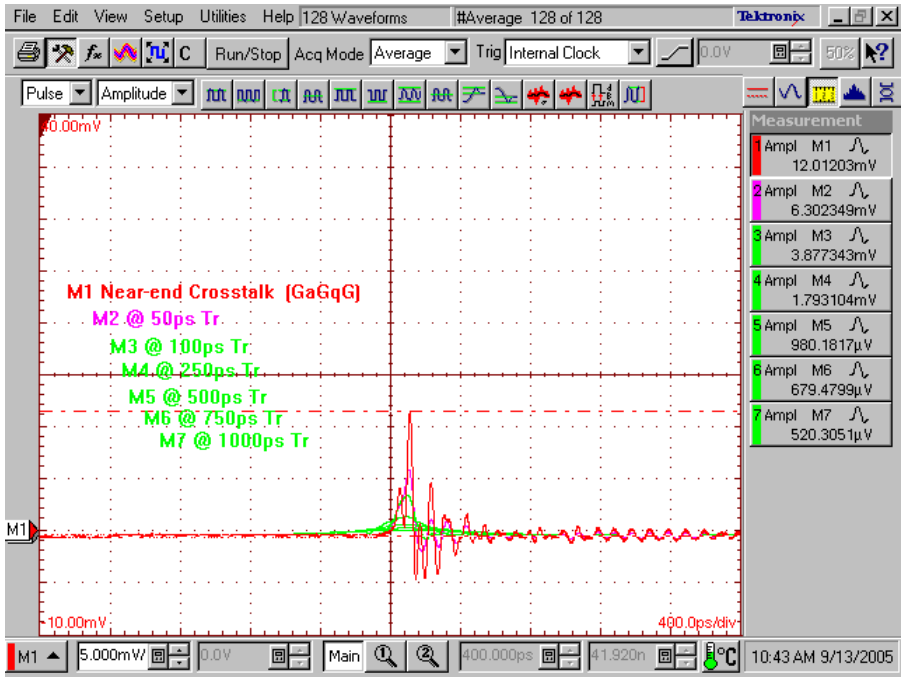
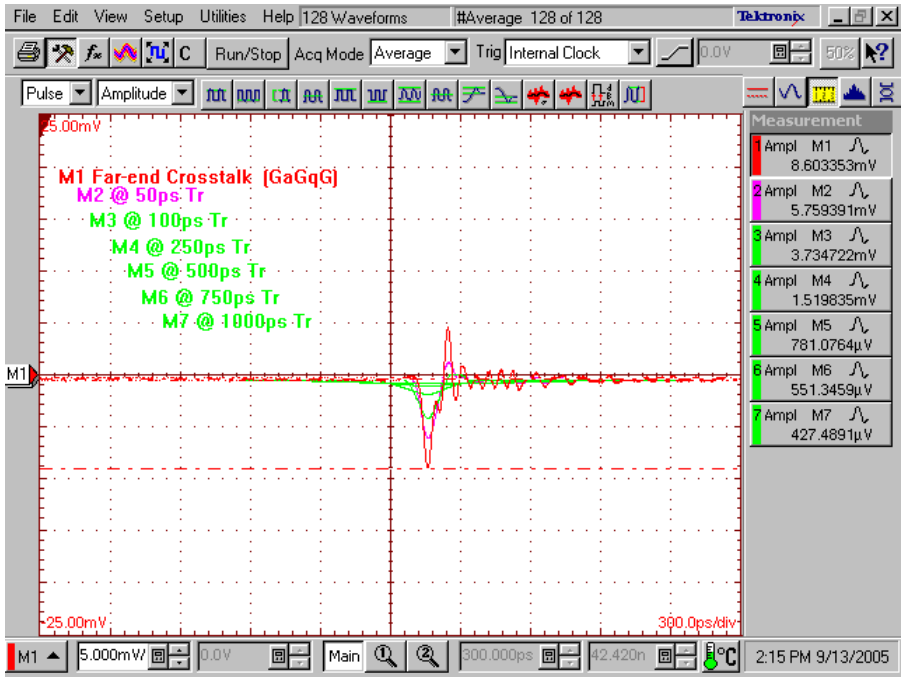
Single-Ended Application – NEXT, "Best Case In Row" Configuration



Single-Ended Application – FEXT, "Best Case In Row" Configuration



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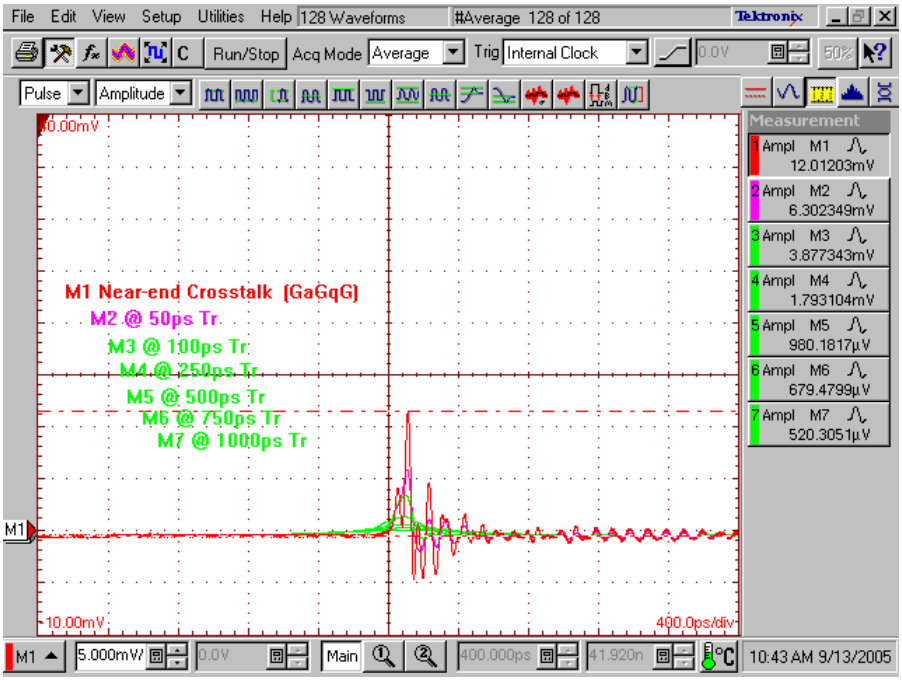
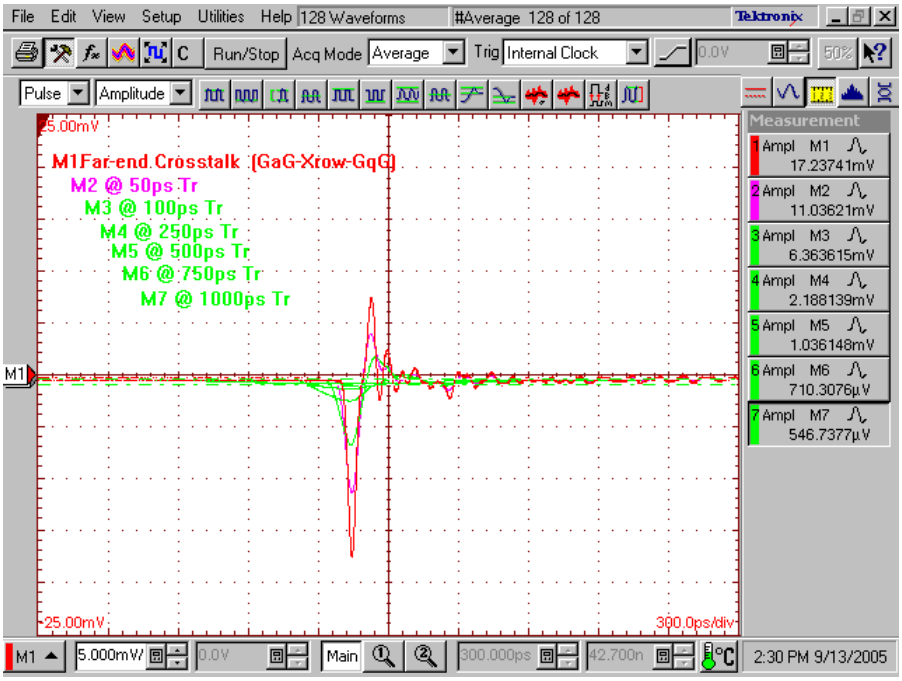
Single-Ended Application – NEXT, "Across Row" Configuration



Single-Ended Application – FEXT, "Across Row" Configuration



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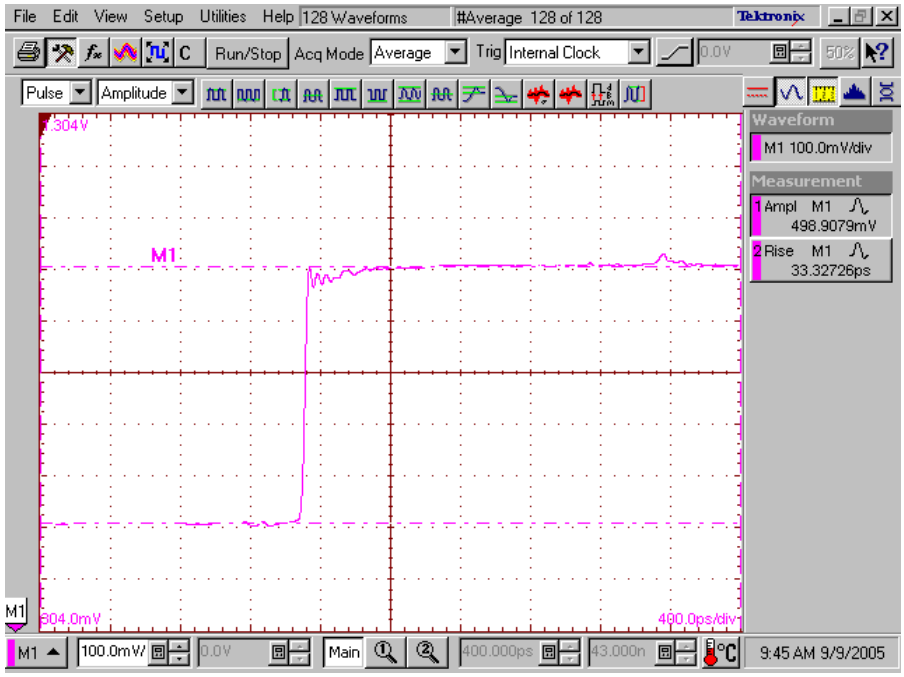
Differential Application – Input Pulse



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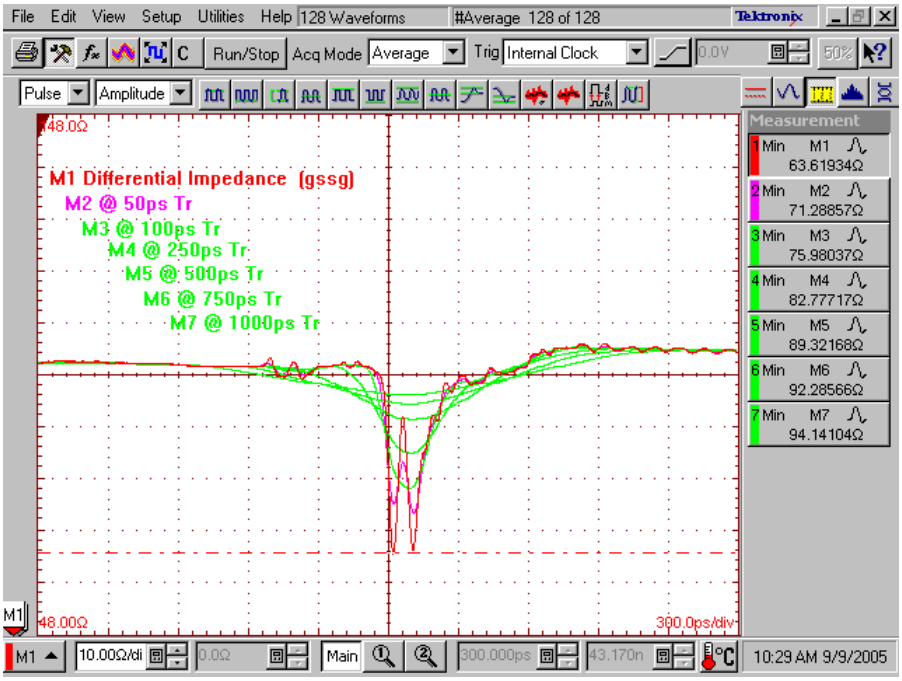
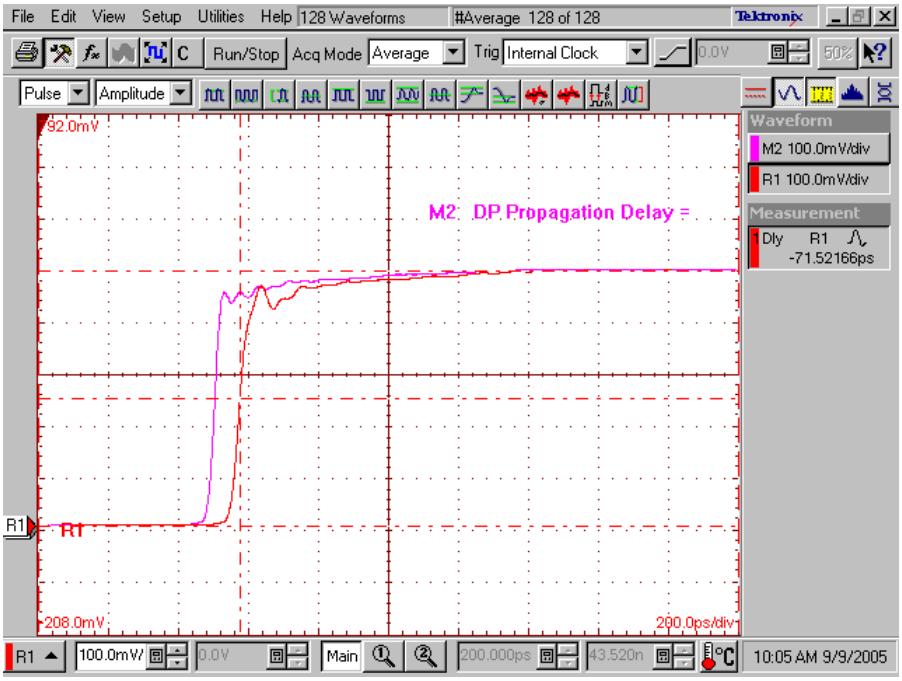
Differential Application – Impedance



Differential Application – Propagation Delay



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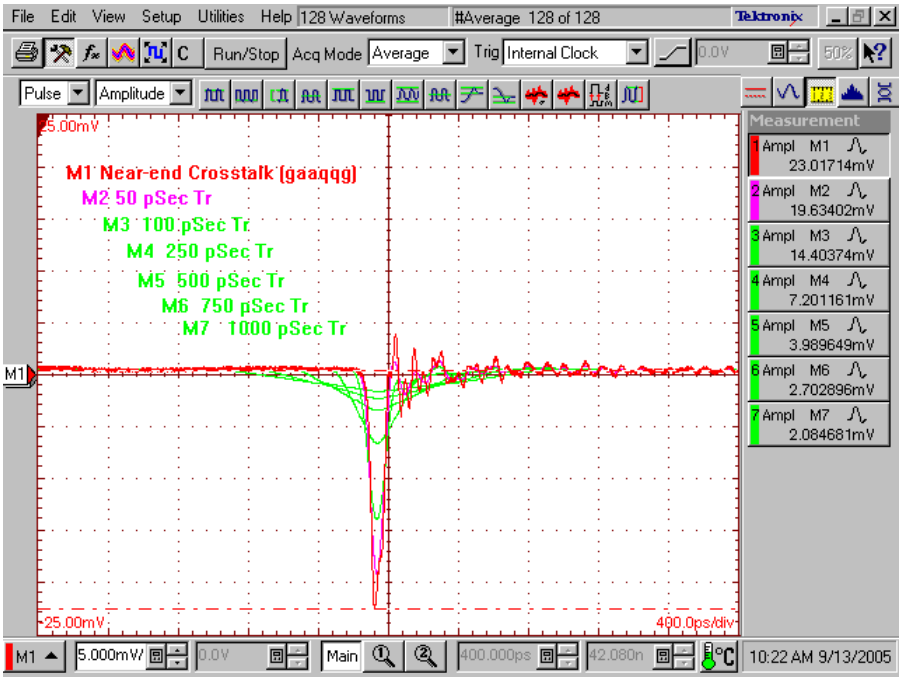
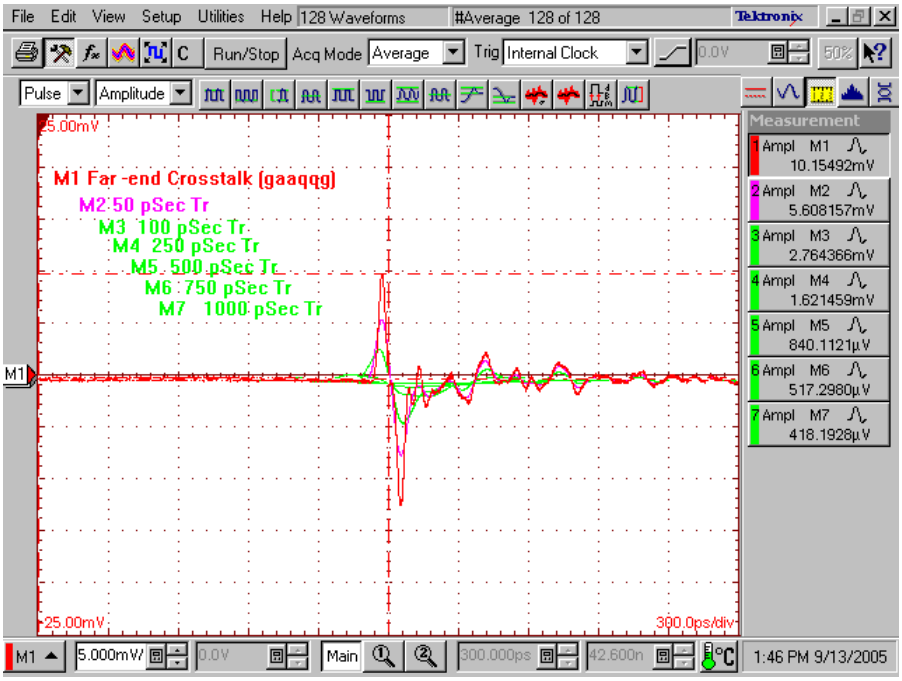
Description: Parallel Board-to-Board, 0.050” [1.27mm] Pitch, 5.13mm (0.202”) Stack Height

Differential Application – NEXT, “Worst Case In Row ” Configuration

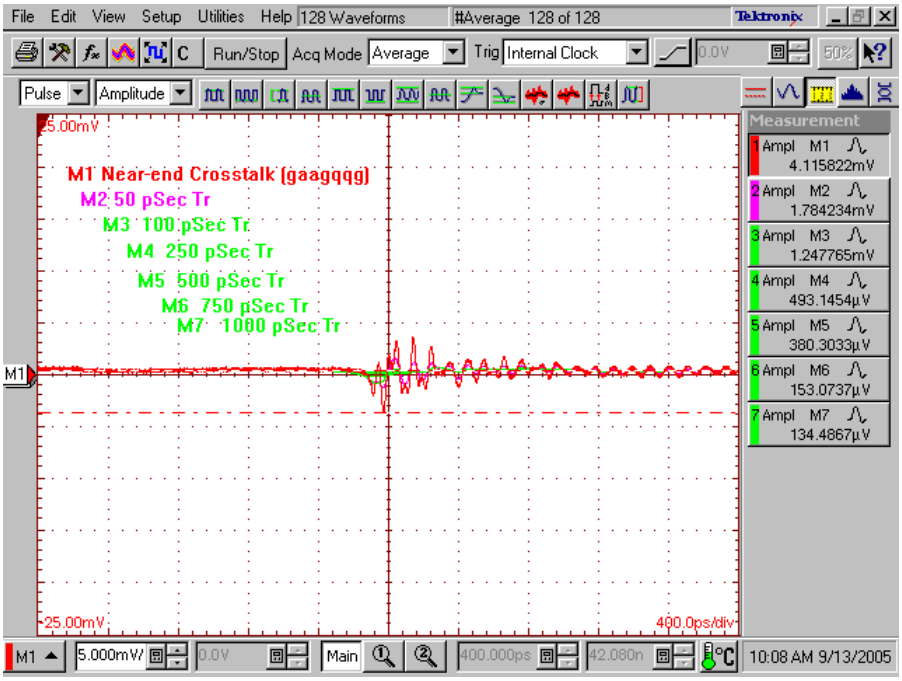


Differential Application – FEXT, “Worst Case In Row” Configuration

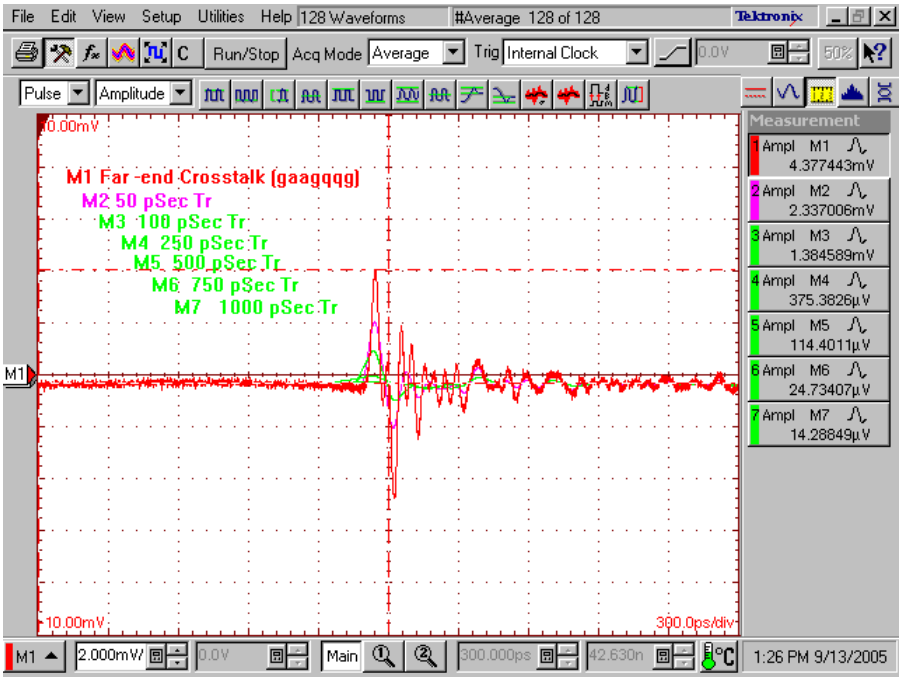


Series: FTSH/CLP Low Profile Socket and Terminal Strip
Description: Parallel Board-to-Board, 0.050" [1.27mm] Pitch, 5.13mm (0.202") Stack Height

Differential Application – NEXT, "Best Case In Row" Configuration

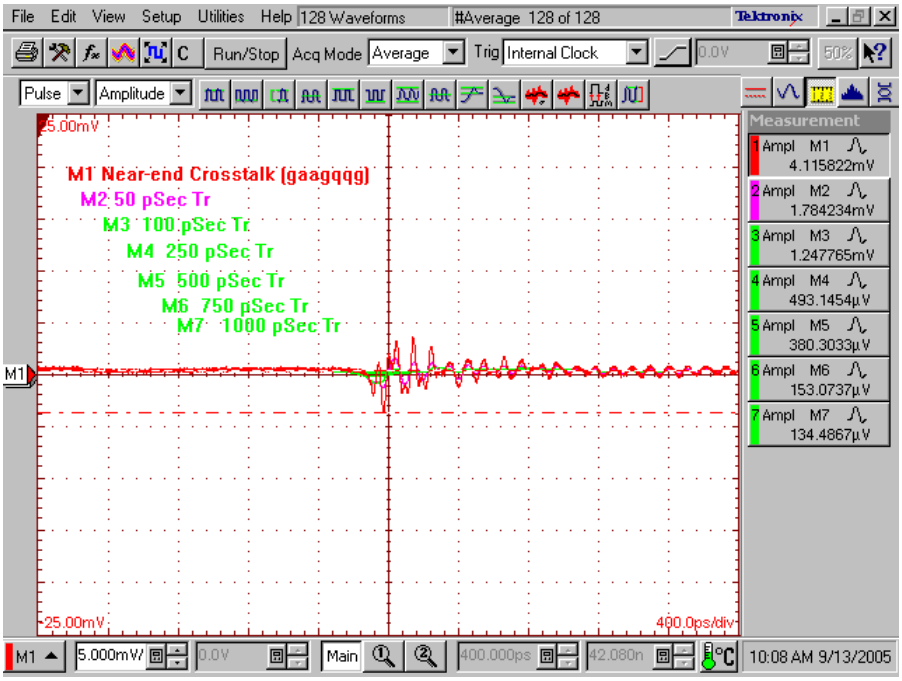


Differential Application – FEXT, "Best Case In Row" Configuration

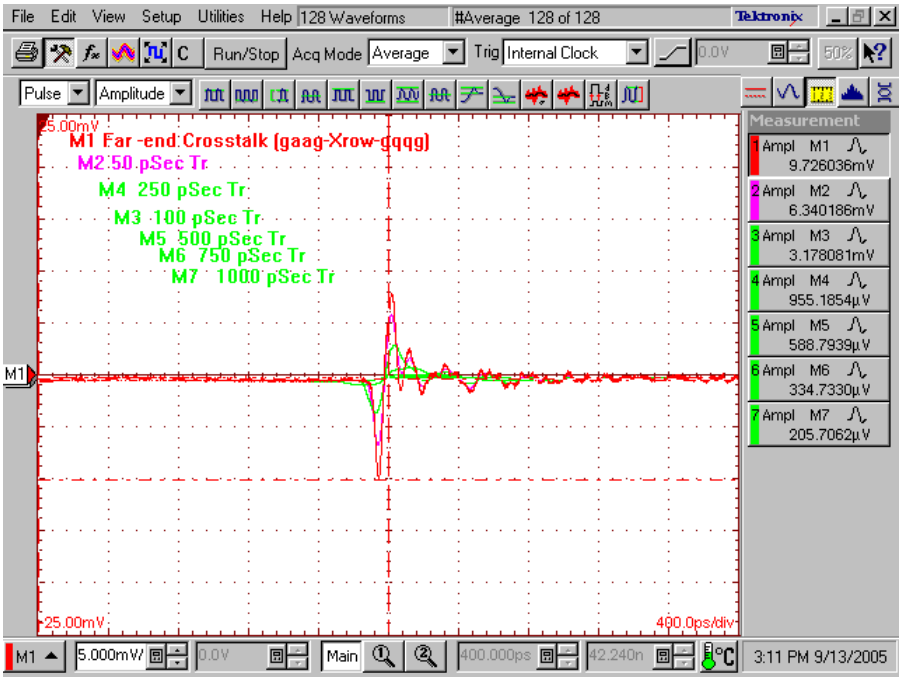


Series: FTSH/CLP Low Profile Socket and Terminal Strip
Description: Parallel Board-to-Board, 0.050" [1.27mm] Pitch, 5.13mm (0.202") Stack Height

Differential Application – NEXT, "Across Row" Configuration



Differential Application – FEXT, "Across Row" Configuration



Series: FTSH/CLP Low Profile Socket and Terminal Strip
Description: Parallel Board-to-Board, 0.050" [1.27mm] Pitch, 5.13mm (0.202") Stack Height

Appendix C – Product and Test System Descriptions

Product Description

Product samples are the micro low profile socket strip CLP-115-02-L-D-A and CLP-125-02-L-D-A. The mating FTSH terminal strips headers are P/N FTSH-115-03-L-D-A and FTSH-125-03-L-D-A respectively. When mated a 5.13mm (.202") stack height exists between PC boards

Each connector structure consists of 2 rows of 15 or 25 surface mount terminal positions mounted into a plastic housing. The contacts are evenly spaced at a 1.27mm (.050") pitch.

Test System Description

The test fixtures are composed of a 4-layer FR-4 material with 50Ω and100Ω signal trace and pad configurations designed for the electrical characterization of Samtec hi-speed connector products. The pictured fixtures are specific to the CLP/FTSH surface mount series connector and are identified by Samtec P/N PCB-100278-TST-01 and P/N PCB-100278-TST-02 (Figure 1)

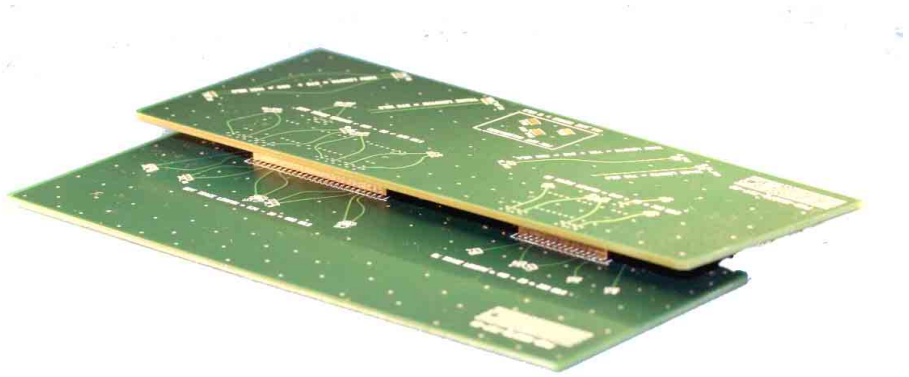


Figure 1 Mated PCB Test Fixture with Mounted Test Connectors

PCB-100278-TST-01 (Figure 1, bottom PCB) is designated as the test signal launch board and contains the two CLP socket series connectors. The 15 signals/row connector (right) is used in characterizing single ended (GSG) test signals and the 25 signals/row connector (left) is used to characterize differential test signals(GSSG). PCB-100278-TST-02 provides the reference plane and/or calibration standards used in generating time delay and s-parameter information. Test fixture PCB-100278-TST-02 contains the mating FTSH terminal connectors (Figure 1, top pcb) and is the main signal

Series: FTSH/CLP Low Profile Socket and Terminal Strip
Description: Parallel Board-to-Board, 0.050" [1.27mm] Pitch, 5.13mm (0.202") Stack Height

monitoring section of the fixture. When the two board fixtures are mated the labeled probe points coordinate to create continuous electrical transmission paths between the signal launch pads and monitoring junctions. Both the single-ended and differential fixtures "J" number represents each signal terminal's designated position within the connector. Signals can also be launched from the terminal side of the connector but the response may not necessarily correlate with a socket side launch All data and waveforms presented in the report are results from a socket side signal launch. Table 8 below identifies the launch, monitoring and adjacent line termination points used in generating characterization data for this report.

Table 8 – PCB Fixture Characterization & Termination Matrix

	Single Ended				Differential			
	Launch	Monitor	50Ω to Gnd. Termination		Launch	Monitor	100Ω Across Signal Pair Termination	
USE PCB	**TST-01**	**TST-02**	**TST-01**	**TST-02**	**TST-01**	**TST-02**	**TST-01**	**TST-02**
IL, RL Z, PD	J-7	J_7	J-3 J-8	J_3 J8	J43_45	J43-45	J38_40 J37_39	J37-38 J38-40
USE PCB	**TST-01**	**TST-01**	**TST-01**	**TST-02**	**TST-01**	**TST-01**	**TST-01**	**TST-02**
NEXT(worst)	J-25	J-23		J_23 J25	J9_11	J5_7		J5-7 J9-11
NEXT(best)	J-7	J-3	J-8	J_3 J_7 J8	J43_45	J37_39	J38_40	J37-39 J38-40 J43-45
NEXT(xrow)	J-7	J-8	J-3	J_3 J_7 J8	J38_40	J37_39	J43_45	J37-39 J38-40 J43-45
USE PCB	**TST-01**	**TST-02**	**TST-01**	**TST-02**	**TST-01**	**TST-02**	**TST-01**	**TST-02**
FEXT(worst)	J-25	J_23	J-23	J25	J9_11	J5-7	J5_7	J9-11
FEXT(best)	J-7	J_3	J-3 J-8	J_7 J8	J43_45	J37-39	J37_39 J38_40	J43-45 J38-40
FEXT(xrow)	J-7	J8	J-3 J-8	J_3 J_7	J38_40	J37-39	J43_45 J37_39	J38-40 J43-45

Series: FTSH/CLP Low Profile Socket and Terminal Strip
Description: Parallel Board-to-Board, 0.050" [1.27mm] Pitch, 5.13mm (0.202") Stack Height

Signal Conditioning, Calibration Standards And Signal Launch/Monitoring

Figure 2 represents the layout of the footprint, connector, and signal trace transitions where test signal configuration conditions can be determined. In general these GSG or GSSG conditions are spelled out in the characterization details section of the report. Be aware that the geometry or signal conditioning adjacent to active or monitored test points may have aggressive or response changing behaviors and should be terminated to the SUT's characteristic impedance as specified in Table 8.

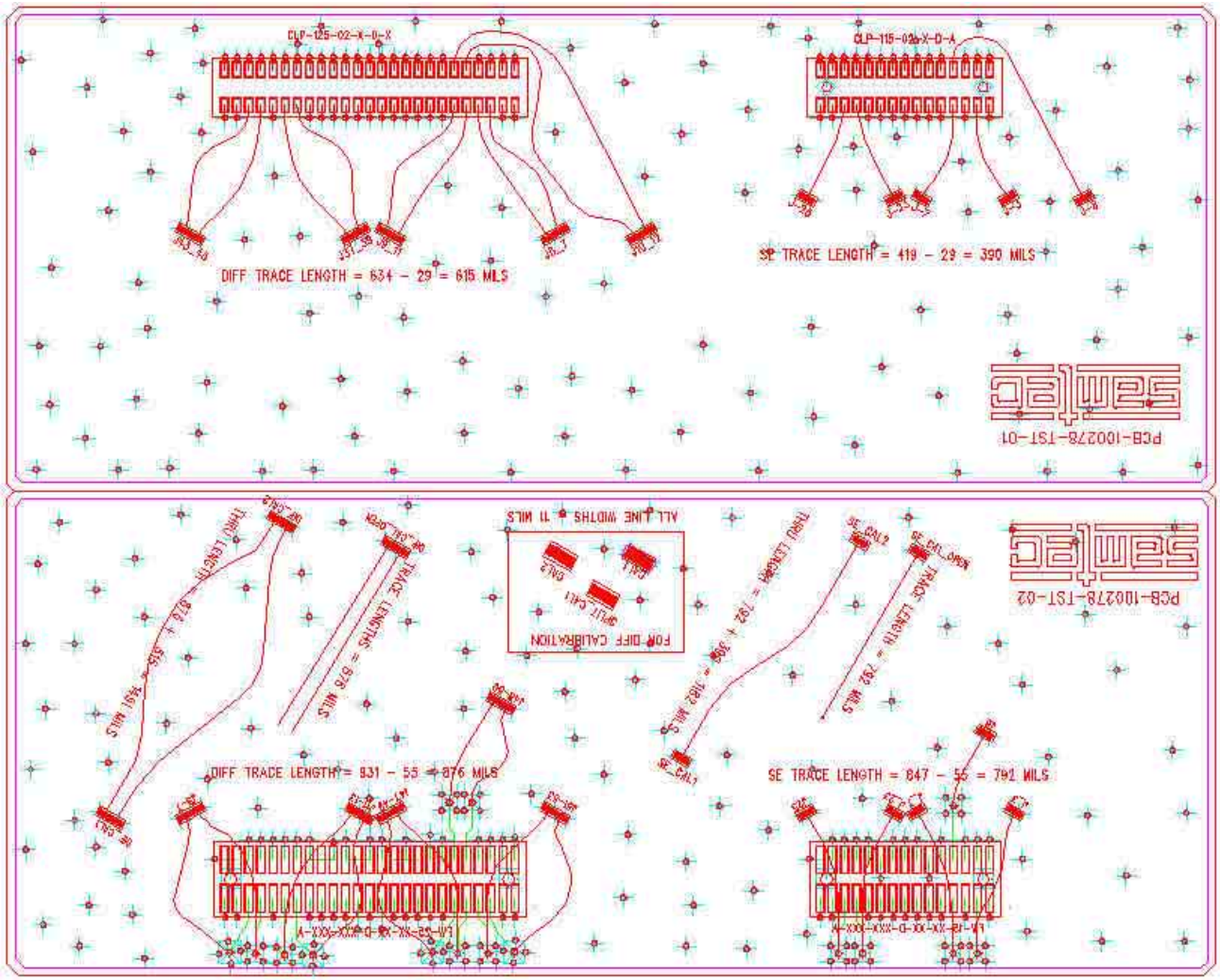


Figure 2 Signal Conditioning, Calibration Standards And Signal Launch/Monitoring Map

Series: FTSH/CLP Low Profile Socket and Terminal Strip
Description: Parallel Board-to-Board, 0.050" [1.27mm] Pitch, 5.13mm (0.202") Stack Height

Appendix D – Test and Measurement Setup

Test instruments are a Tektronix CSA8000 Communication Signal Analyzer Mainframe and the Agilent 8720ES Vector Network Analyzer. Four bays of the CSA8000 are occupied with three Tektronix 80E04 TDR/Sampling Heads and one Tektronix 80E03 Sampling Head. For this series of tests, four of the eight TDR/Sampling Head capability is used *(Figure 3)*. The 8720ES serves as a supporting test instrument for verification or troubleshooting results obtained from the TDA Systems IConnect Software package. IConnect is a TDR based measurement software tool used in generating frequency domain related responses from high speed interconnects.

The probe stations illuminated video microscopy system, microprobe positioners, and 40GHz capable probes provide both the mechanical properties and electrical characteristics for obtaining the precise signal launch and calibrations that are critical in obtaining accurate high speed measurements. The 450 micron pitch probes are located to PCB launch points with 25X to 175X magnification and XYZ fine positioning adjustments available from both the probe table and micro-probe positioners. Electrically the microwave probes rate a < 1.0 dB insertion loss, a < 18 dB return loss, and an isolation of 38 dB to 40 GHz *(Figure 4)*. Test cables and interconnect adapters are high quality and insure high-bandwidth and low parasitic measurements.

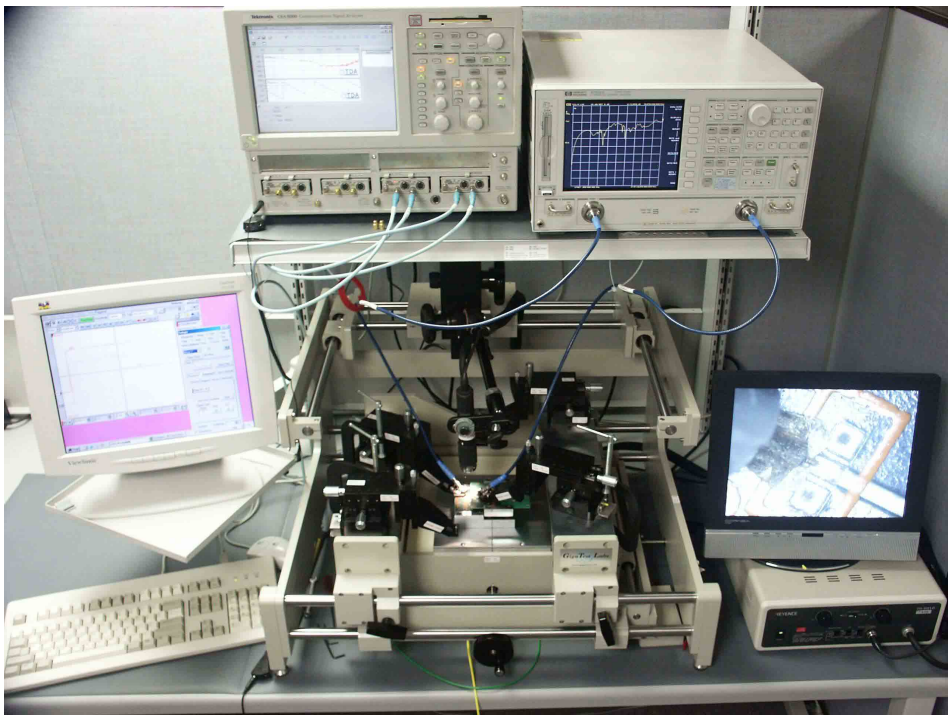


Figure 3– Probe Station Measurements Capability

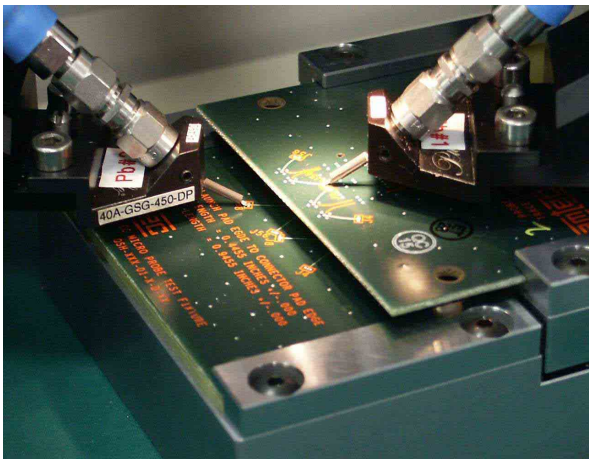
Series: FTSH/CLP Low Profile Socket and Terminal Strip
Description: Parallel Board-to-Board, 0.050" [1.27mm] Pitch, 5.13mm (0.202") Stack Height

Test Instruments

QTY	Description
1	Tektronix CSA8000 Communication Signal Analyzer
3	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module
1	Tektronix 80E03 Dual Channel 20 GHz Sampling Module
2	Tektronix 012-1568-00 1 Meter Module Extender

Measurement Station Accessories

QTY	Description
1	GigaTest Labs Model (GTL3030) Probe Station
4	GTL Micro-Probe Positioners
2	Picoprobe by GGB Ind. Model 40A GSG (single ended applications)
2	Picoprobe by GGB Ind. Dual Model 40A GSG-GSG (differential applications)
1	Keyence VH-5910 High Resolution Video Microscope
1	Keyence VH-W100 Fixed Magnification Lens 100 X
1	Keyence VH-Z25 Standard Zoom Lens 25X-175X



Test Cables & Adapters

QTY	Description
4	Pasternack .086" Semi Rigid Cable Assembly 6" SMA Male to SMA Male 26.5 GHz
2	Huber-Suhner Cable Assembly 36" SMA Female to SMA Female 26.5 GHz (IL = .34 dB @ 10 GHz)
4	Pasternack Precision Adapters, 3.5 mm Male to 2.9(K) Male, Max.VSWR 1.25 @ 34GHz

Series: FTSH/CLP Low Profile Socket and Terminal Strip
Description: Parallel Board-to-Board, 0.050" [1.27mm] Pitch, 5.13mm (0.202") Stack Height

Appendix E - Frequency and Time Domain Measurements

It is important to note before gathering measurement data that TDA Systems IConnect measurements and CSA8000 measurements are virtually the same measurements with diverse formats. This means that the operator, being extremely aware, can obtain SI time and frequency characteristics in an almost simultaneous fashion.

Since IConnect setup procedures are specific to the frequency information sought, it is mandatory that the sample preparation and CSA8000 functional setups be consistent throughout the waveform gathering process. If the operators test equipment permits recall sequencing between the various test parameter setups, it insures IConnect functional setups remain consistent with the TDR/TDT waveforms previously recorded. Related time and frequency test parameter data recorded for this report were gathered simultaneously.

Frequency (S-Parameter) Domain Procedures
Frequency data extraction involves two steps that first measure the frequency related time domain waveform followed by post-processing of the time domain waveforms into loss and crosstalk response parameters versus frequency. The first step utilizes the Tektronix CSA8000 time based instrument to capture frequency related single-ended or differential signal types propagating through an appropriately prepared SUT. The second step involves a correlation of the time based waveforms using the TDA Systems IConnect software tool to post-process these waveforms into frequency response parameters. TDA Systems labels these frequency related waveform relationships as the *Step* and *DUT* reference. This report establishes the setup procedures for defining the *Step* and *DUT* reference for frequency parameters of interest. Once established, the *Step* and *DUT* references are post-processed in IConnect's S-parameter computations window.

CSA8000 Setup
Listed below are the CSA 8000 functional menu setups used for single-ended and differential frequency response extractions. Both signal types utilize I-Connect software tools to generate S-parameter upper and lower frequency boundaries along with the step frequency. These frequency boundaries are determined by a time domain instruments functional settings such as window length, number of points and averaging capability. Once window length, number of points and averaging functions are set, maintain the same instrument settings throughout the extraction process.

Series: FTSH/CLP Low Profile Socket and Terminal Strip
Description: Parallel Board-to-Board, 0.050" [1.27mm] Pitch, 5.13mm (0.202") Stack Height

	Single-Ended Signal	Differential Signal
Vertical Scale:	100 mV/ Div:	100 mV/ Div:
Offset:	Default / Scroll	Default / Scroll
Horizontal Scale:	1nSec/ Div = 20 MHz step frequency	1nSec/ Div = 20 MHz step frequency
Max. Record Length:	4000 = Min. Resolution	4000 = Min. Resolution
Averages:	≥ 128	≥ 128

Insertion Loss

SUT Preparation - For signal launch and monitoring path guidelines reference table 8. Terminate all the suggested active or adjacent signal lines at the impedance values recommended in the table. Signal trace locations and configurations can be verified using figure 2.

Step Reference - Establish this waveform by making a TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. The transmission path is completed by inserting a negligible length of transmission standard between the microwave probes. *(**Note:** Use the split-cal1 standard in TDT mode located on Samtec PCB100278-TST-02 fixture).*

DUT Reference - Establish these waveforms by making an active TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. Insert the SUT between the probes in place of the transmission standard and record the measurement.

Return Loss

SUT Preparation – For signal launch and monitoring path guidelines reference table 8. Terminate all the suggested active or adjacent signal lines at the impedance values recommended in the table. Signal trace locations and configurations can be verified using figure 2.

Step Reference - Establish the waveform by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems electrical path up to and including an open standard. *(**Note:** Use split-cal1 standard in TDR mode located on Samtec PCB100278-TST-02 fixture).*

DUT Reference – Retain same signal paths and test setup used in obtaining insertion loss waveforms. Establish these waveforms by making a TDT (matched) reflection measurement that includes all cables, adapters, and probes connected in the test systems transmission path. For this condition the quality cables and adapters located on

the far-end of the inserted SUT serves as the resistive load impedance closely matching the test system input impedance of 50Ω single-ended and100Ω differential.

Near-End Crosstalk (NEXT)

SUT Preparation – For signal launch and monitoring path guidelines reference table 8. Terminate all the suggested active or adjacent signal lines at the impedance values recommended in the table. Signal trace locations and configurations can be verified using figure 2.

Step Reference - Establish these waveforms by making an active measurement that includes all cables, adapters, and probes connected in the test systems electrical path up to and including an open standard. *(**Note:** Use split-cal1 standard in TDR mode located on Samtec PCB100278-TST-02 fixture).*

DUT Reference - Establish these waveforms by driving the suggested signal line and monitoring the TDR coupled energy at the adjacent near-end signal line. Establish {6} measurement waveforms of worst case, best case and across row (xrow) coupling conditions for both signal types.

Far-End Crosstalk (FEXT)

SUT Preparation - For signal launch and monitoring path guidelines reference table 8. Terminate all the suggested active or adjacent signal lines at the impedance values recommended in the table. Signal trace locations and configurations can be verified using figure 2.

Step Reference - Establish these waveforms by making a TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path. The transmission path is completed by inserting a negligible length of transmission standard *(**Note:** Use the split-cal1 standard in TDT mode located on Samtec PCB100278-TST-02 fixture).*

DUT Reference - Establish these waveforms by driving the suggested signal line and monitoring the TDR coupled energy at the adjacent near-end signal line. Establish {6} measurement waveforms of worst case, best case and across row (xrow) coupling conditions for both signal types.

Series: FTSH/CLP Low Profile Socket and Terminal Strip
Description: Parallel Board-to-Board, 0.050" [1.27mm] Pitch, 5.13mm (0.202") Stack Height

Time Domain Procedures

Measurements involving digital type pulses are performed utilizing either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. For this series of tests, TDR methods are employed for the impedance and propagation delay measurements. Crosstalk measurements utilize TDT methods. The Tektronix 80E04 TDR/ Sampling Head provide both the signaling type and sampling capability necessary to accurately and fully characterize the SUT.

Impedance

The signal line(s) of the SUT's signal configuration is energized with a TDR pulse. The far-end of the energized signal line is terminated in the test systems characteristic impedance (e.g.; 50Ω or 100Ω terminations). By terminating the adjacent signal lines in the test systems characteristic impedance, the effects on the resultant impedance shape of the waveform is limited. For signal launch and monitoring path guidelines reference table 8.

Propagation Delay

This connector series uses the fastest edge rate (30ps) of the TDR impedance waveform to measure propagation delay. . Differential or single ended signal delay is the measured difference of propagation between the known signal trace length delay *(reference PCB100278-TST-02 for each mated connectors referenced signal trace length).* and the combined delay through the input signal traces and output signal traces of the mated SUT. The measurement is a one-way propagation result. Termination of the adjacent signal lines into the test systems characteristic impedance eliminate alternate current paths providing for better measurement accuracy. For signal launch and monitoring path guidelines reference table 8.

Crosstalk

An active pulsed waveform is transmitted through a selected SUT signal line. The adjacent quiet signal lines are monitored for the coupled energy at the near-end and far-end. Active and quiet lines not being monitored are terminated in the test systems characteristic impedance. Signal lines adjacent to the quiet lines remain terminated on both ends throughout the test sequence. Failing to terminate the active near or far end, quiet lines, or in some cases, signal lines adjacent to the quiet line may have an effect on amplitude and shape of the coupled energy. For signal launch and monitoring path guidelines reference table 8.

Series: FTSH/CLP Low Profile Socket and Terminal Strip
Description: Parallel Board-to-Board, 0.050" [1.27mm] Pitch, 5.13mm (0.202") Stack Height

Appendix F – Glossary of Terms

BC – Best Case crosstalk configuration

DP – Differential Pair signal configuration

DUT – Device under test; TDA IConnect reference waveform

FEXT – Far-End Crosstalk

GSG – Ground–Signal-Ground; geometric configuration

NEXT – Near-End Crosstalk

PCB – Printed Circuit Board

SE – Single-Ended

SI – Signal Integrity

SUT – System under test

TDR – Time Domain Reflectometry

TDT – Time Domain Transmission

WC – Worst Case crosstalk configuration

Xrow^{se} – Cross ground/ power bar crosstalk, single-ended signal

Xrow^{diff} – Cross ground/ power bar crosstalk, differential signal

Z – Impedance (expressed in ohms)

Static (S) – connector terminals with no connection to PCB ground