Evaluation of the ADRF5050 Nonreflective, Silicon SP4T Switch, 100 MHz to 20 GHz

FEATURES

- Full featured evaluation board for the ADRF5050
- Easy connection to test equipment
- Additional through line for calibration

EQUIPMENT NEEDED

- DC power supplies
- Network analyzer

GENERAL DESCRIPTION

The ADRF5050 is a nonreflective, SP4T switch manufactured in the silicon on insulator (SOI) process.

This user guide describes the ADRF5050-EVALZ evaluation board, which is designed to simply evaluate the features and performance of the ADRF5050. A photograph of the evaluation board is shown in Figure 1.

The ADRF5050 data sheet provides full specifications for the ADRF5050. Refer to the ADRF5050 data sheet with this user guide when using the ADRF5050-EVALZ.

ADRF5050-EVALZ EVALUATION BOARD PHOTOGRAPH

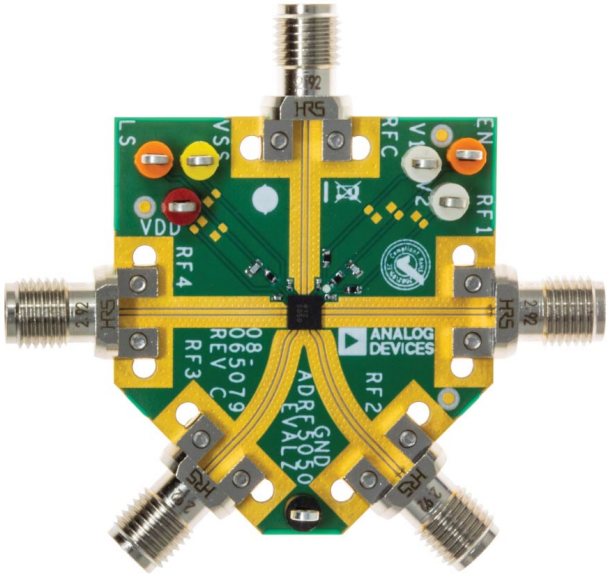

Figure 1. ADRF5050-EVALZ Evaluation Board Photograph

TABLE OF CONTENTS

REVISION HISTORY

2/2023—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The ADRF5050-EVALZ is a connectorized board, assembled with the ADRF5050 and its application circuitry. All components are placed on the primary side of ADRF5050-EVALZ. An assembly drawing for the ADRF5050-EVALZ is shown in Figure 11, and an evaluation board schematic is shown in Figure 10.

BOARD LAYOUT

The ADRF5050-EVALZ is designed using RF circuit design techniques on a 4-layer printed circuit board (PCB). The PCB stack-up is shown in Figure 2.

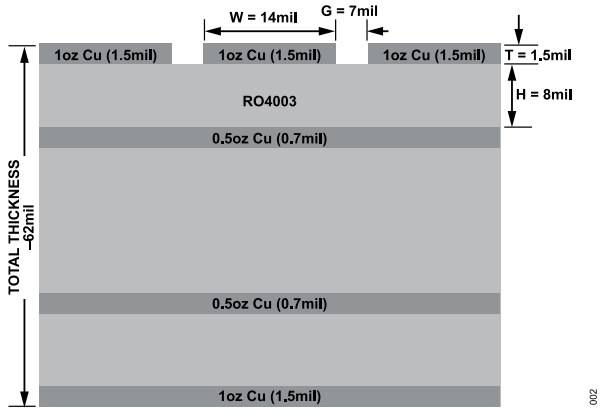

Figure 2. Evaluation Board Stack-Up

The outer copper layers are 1 oz (1.5 mil) thick and the inner layers are 0.5 oz (0.7 mil) thick.

The top dielectric material is 8 mil Rogers 4003, which provides 50 Ω controlled impedance and optimizes the high frequency performance. All RF traces are routed on the top layer, and the second layer is used as the ground plane for RF transmission lines. The remaining two layers are also ground planes filled with FR4 material to manage the thermal rise during high power operations and are supported with dense and filled vias to the PCB bottom for thermal relief. The overall board thickness is approximately 62 mil for mechanical strength.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 14 mil and ground spacing of 7 mil to have a characteristic impedance of 50 Ω. Ground via fences are arranged on both sides of the CPWG to improve isolation between nearby RF lines and other signal lines.

The exposed ground pad of the ADRF5050, which is soldered on the PCB ground pad, is the main thermal conduit for heat dissipation. The PCB ground pad is densely populated with filled, through vias to provide the lowest possible thermal resistance path from the top to the bottom of the PCB. The connections from the package ground leads to ground are kept as short as possible.

POWER SUPPLY AND CONTROL INPUTS

The ADRF5050-EVALZ has two power-supply inputs, four control inputs, and a ground, as shown in Table 1. The DC test points are populated on VDD, VSS, V1, V2, LS, EN, and GND. A 3.3 V supply is connected to the DC test points on VDD, and the −3.3 V supply is connected to the DC test points on VSS. Ground reference can be connected to GND. Connect the control inputs, V1, V2, LS, and EN, to 3.3 V or 0 V. The typical total current consumption for the ADRF5050 is 0.68 mA.

The VDD and VSS supply pins and control pins of the ADRF5050 are decoupled with 100 pF capacitor.

Table 1. Power Supply and Control Inputs

Test Point	Description
VDD	+3.3 V supply voltage
VSS	−3.3 V supply voltage
V1	Control Input 1
V2	Control Input 2
EN	Enable
LS	Logic select
GND	Ground

EVALUATION BOARD HARDWARE

RF INPUTS AND OUTPUTS

The ADRF5050-EVALZ has five edge-mounted, 2.92 mm connectors for the RF inputs and outputs, as shown in Table 2.

Table 2. RF Inputs and Outputs

SMA Connector	Description
RFC	RF common port
RF1	RF Throw Port 1
RF2	RF Throw Port 2
RF3	RF Throw Port 3
RF4	RF Throw Port 4

The ADRF5050-EVALZ is shipped together with a through line that calibrates out the board loss effects from the measurements determining the device performance at the pins of the IC. Figure 3 shows the typical board loss for the ADRF5050-EVALZ at room temperature, as well as the embedded and de-embedded insertion loss for the ADRF5050.

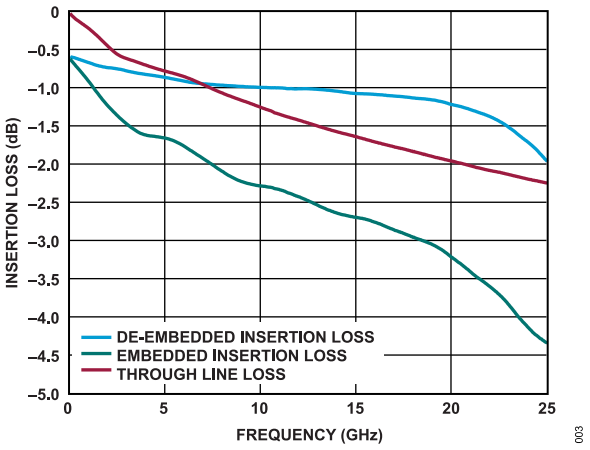

Figure 3. Insertion Loss vs. Frequency

TEST PROCEDURE

BIASING SEQUENCE

To bias up the ADRF5050-EVALZ, perform the following steps:

1. Ground the GND test point.
2. Bias up the VDD test point.
3. Bias up the VSS test point.
4. Bias up the V1, V2, LS, and EN test points.
5. Apply an RF input signal.

The ADRF5050-EVALZ is shipped fully assembled and tested. Figure 4 provides a basic test setup diagram to evaluate the s-parameters using a network analyzer. Perform the following steps to complete the test setup and to verify the operation of the ADRF5050-EVALZ:

1. Connect the GND test point to the ground terminal of the power supply.
2. Connect the VDD test point to the voltage output terminal of the 3.3 V supply.
3. Connect the VSS test point to the voltage output terminal of the −3.3 V supply. Note that the current from VDD test point is around 155 µA and from VSS test point is around 530 µA.
4. Connect the V1, V2, EN, and LS test points to the voltage output terminal of the 3.3 V supply. The ADRF5050 can be configured in different modes by connecting the control test points to 3.3 V or 0 V, as shown in Table 3.
5. Connect a calibrated network analyzer to the RFC, RF1, RF2, RF3, and RF4 2.92 mm connectors. If the network analyzer port count is not enough, terminate unused RF ports with 50 Ω. Sweep the frequency from 100 MHz to 20 GHz and set the power to –5 dBm.
6. The ADRF5050-EVALZ is expected to have an insertion loss of 1.20 dB at 20 GHz. See the expected results in Figure 5.

Additional test equipment is needed to fully evaluate the device functions and performance.

For third-order intercept point evaluation, use two signal generators and a spectrum analyzer. A high isolation power combiner is also recommended.

For power compression and power handling evaluations, use a 2-channel power meter and a signal generator. A high enough power amplifier is also recommended at the input. Test accessories, such as couplers and attenuators, must have enough power handling.

The ADRF5050-EVALZ comes with a support plate attached to the bottom side. To ensure maximum heat dissipation and to reduce thermal rise on the board during high power evaluations, this support plate must be attached to a heat sink using thermal grease.

Note that the measurements performed at the 2.92 mm connectors of the ADRF5050-EVALZ include the losses of the 2.92 mm connectors and the PCB. The through line must be measured to calibrate out the effects on the ADRF5050-EVALZ. The through line is the summation of an RF input line and an RF output line that are connected to the device and equal in length.

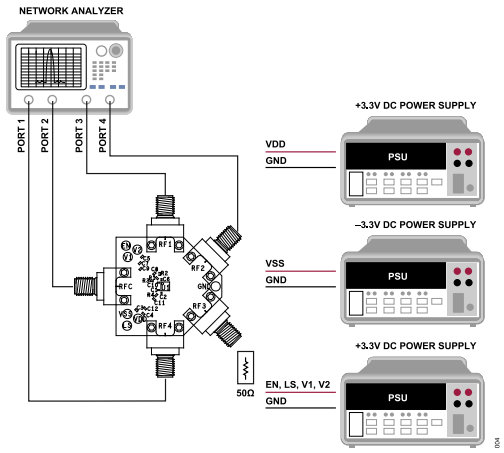

Figure 4. Test Setup Diagram

Table 3. Control Voltage Truth Table

Digital Control Inputs				RFx Paths			
EN	LS	V1	V2	RF1 to RFC	RF2 to RFC	RF3 to RFC	RF4 to RFC
Low	Low	Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	Low	High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	Low	Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	Low	High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	High	Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	High	High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
High	Low or high	Low or high	Low or high	Isolation (off)	Isolation (off)	Isolation (off)	Isolation (off)

TEST PROCEDURE

EXPECTED RESULTS

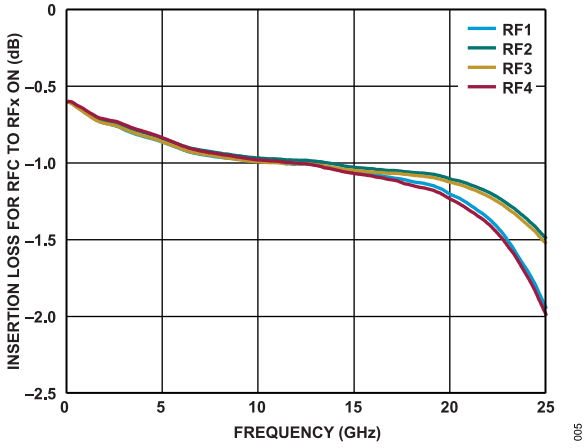

Figure 5. Insertion Loss for RFC to RFx On vs. Frequency

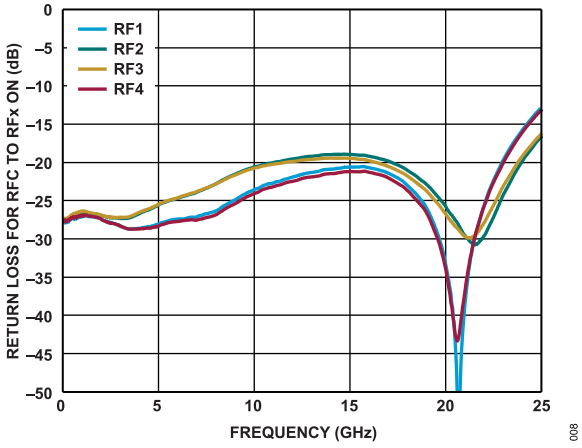

Figure 8. Return Loss for RFC to RFx On vs. Frequency

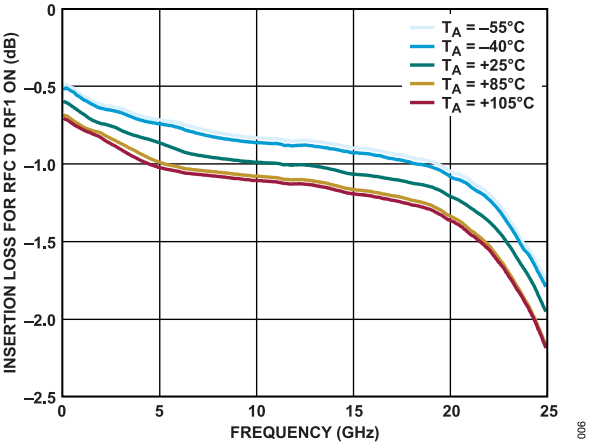

Figure 6. Insertion Loss for RFC to RF1 On vs. Frequency over Various Temperatures

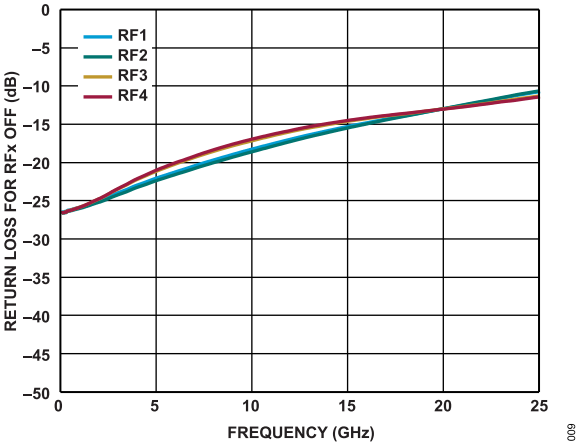

Figure 9. Return Loss for RFx Off vs. Frequency

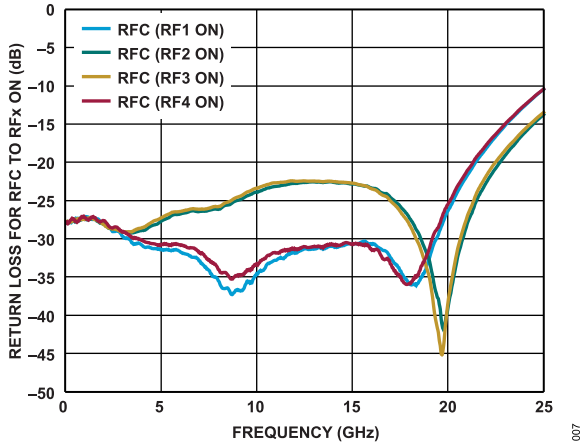

Figure 7. Return Loss for RFC to RFx On vs. Frequency

EVALUATION BOARD SCHEMATIC AND ARTWORK

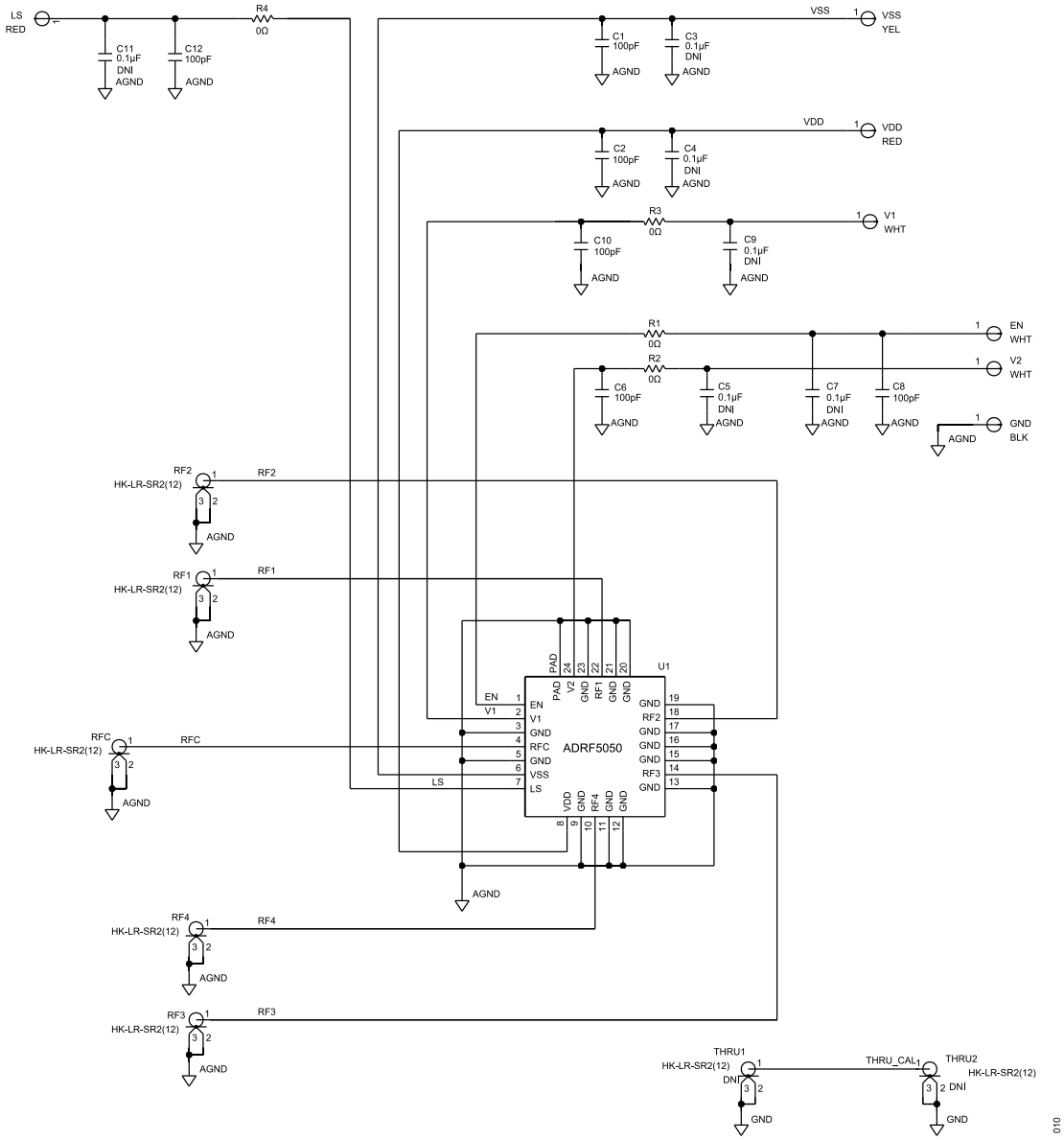

Figure 10. ADRF5050-EVALZ Evaluation Board Schematic

EVALUATION BOARD SCHEMATIC AND ARTWORK

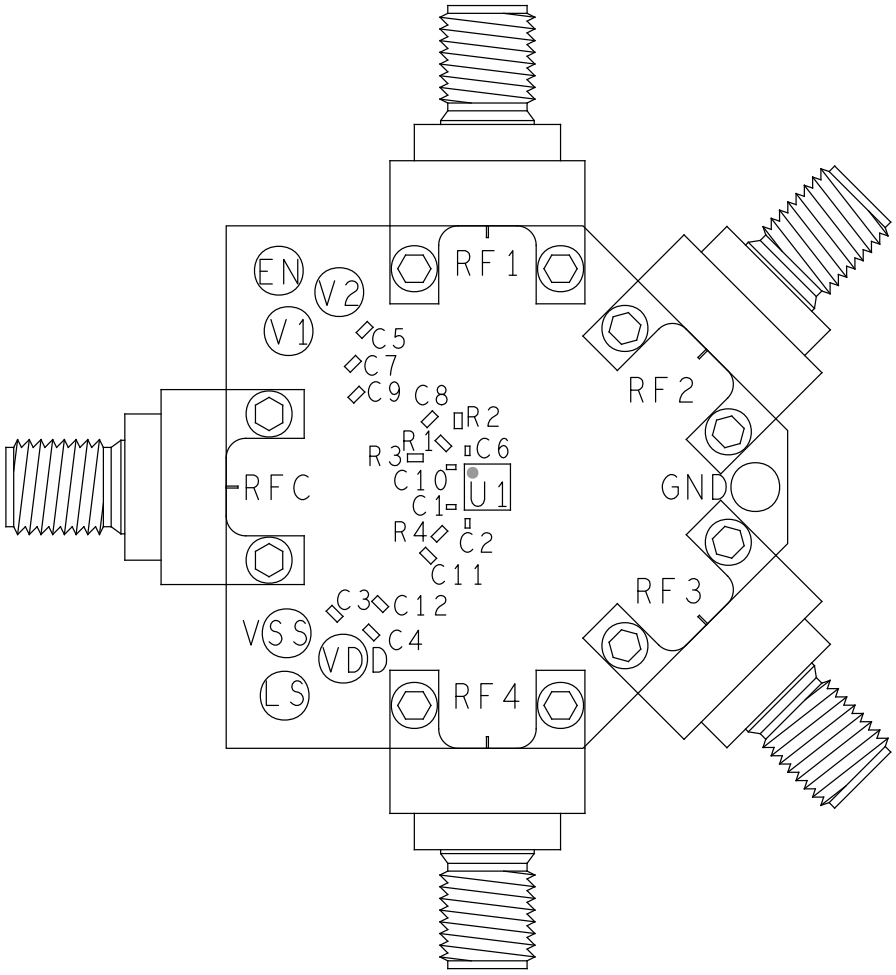

Figure 11. ADRF5050-EVALZ Evaluation Board Assembly Diagram

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. Bill of Materials for ADRF5050-EVALZ

Qty	Reference Designator	Description	Manufacturer	Part Number
4	C1, C2, C6, C10	Capacitors, 100 pF, 25 V, C0201 package	Murata	GRM033R71E101KA01D
2	C8, C12	Capacitors, 100 pF, 50 V, C0402 package	Murata	GCM1555C1H101JA16D
5	R1, R2, R3, R4	Resistors, 0 ohm, 1/10 W, R0402 package	Panasonic	ERJ-2GE0R00X
5	RF1, RF2, RF3, RF4, RFC	Edge-mount 2.92 mm connectors	Hirose Electronic Co.	HK-LR-SR2(12)
7	EN, V1, V2, GND, LS, VDD, VSS	Surface-mount test points	Keystone Electronics	500x
1	U1	Nonreflective, silicon SP4T switch, 100 MHz to 20 GHz	Analog Devices, Inc.	ADRF5050
1	PCB	ADRF5050-EVALZ	Analog Devices	

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.