ADPL42005

Evaluates the ADPL42005 20V, 500mA, Low Noise, CMOS LDO Linear Regulator

General Description

The ADPL42005 evaluation boards evaluate the ADPL42005, a 20V, 500mA, low noise, complementary metal oxide semiconductor (CMOS), low dropout (LDO) linear regulator.

See the *Ordering Information* section for the two types of evaluation boards that evaluate the ADPL42005. There is an evaluation board that features an 8-lead, 3mm x 3mm LFCSP package, and another evaluation board that features an 8-lead SOIC package.

The evaluation boards provide a 3.3V output over an input range of 4.0V to 20V. The maximum output current is 500mA, but the output current is also limited by the thermal dissipation of the ADPL42005. The evaluation boards use the adjustable version of the ADPL42005. A resistor divider programs the output of the adjustable ADPL42005 to 3.3V. Noise performance for the adjustable ADPL42005 can be made comparable to a fixed output ADPL42005 by installing optional RC network components into placeholders provided by the evaluation board printed circuit board (PCB) designs. The evaluation boards can easily be configured with a jumper for fixed output versions of the ADPL42005 that normally have their SENSE/ADJ pin connected directly to the output.

In addition to connectors for the input voltage, output voltage, EN control signal, and ground, the evaluation boards provide test points for the input, output, and PG pin voltages. A jumper normally connects the EN pin to the V_{IN} input, but the jumper can be repositioned so EN can be driven externally at its connector instead.

For more details, refer to the ADPL42005 data sheet. Consult it with this user guide when using the ADPL42005 evaluation boards.

Features and Benefits

- Input voltage range: 4V to 20V
- Resistor programmed 3.3V output voltage
- Jumper turns regulator on or connects the EN pin to a connector to turn the regulator on or off externally
- Jumper connects the SENSE/ADJ pin to the output through a resistor divider or directly
- V_{IN}, V_{OUT}, and GND test points for regulation and dropout voltage monitoring
- PG test point for power good voltage monitoring that helps to indicate the status of the output
- 8-lead (3mm x 3mm) LFCSP package or 8-lead SOIC package

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Quick Start

Required Equipment

- A DC power supply
- Multimeters for voltage and current measurements
- Electronic or resistive loads

Procedure

The ADPL42005 evaluation boards are simple to set up to evaluate the performance of the ADPL42005. See *Figure 1* or *Figure 2* for the evaluation board connections, and follow these steps.

1. Connect the load between the V_{OUT} and GND terminals.
2. With the input power supply off and turned down, connect the input supply to the V_{IN} and GND terminals. Ensure the JP1 shunt connects EN to V_{IN} according to the jumper connection guide. Also ensure the JP2 shunt allows the resistor divider to program the output to 3.3V according to the jumper connection guide.
3. With the load turned down, turn the input power supply on and increase the voltage to 4V or higher.
4. Vary V_{IN} from 4V to 20V and the load current from 0A to 500mA. **Observe conservative power dissipation limits** and note the following when setting V_{IN} and the load current.
   - An input voltage too close to the programmed output voltage (too low) can cause dropout operation and a loss of output-voltage regulation.
   - The amount of output current combined with an input voltage too high above the output can increase power dissipation to an unacceptable level.
5. Monitor regulation and dropout voltage at the V_{IN}, V_{OUT}, and GND test points.
6. To apply an EN signal externally, reposition jumper JP1 and apply the EN signal to the EN connector.
7. If an output voltage other than 3.3V is desired, change resistors R1 and R2.
8. JP2 is a convenient way to connect the SENSE/ADJ pin directly to the output if a fixed-output ADPL42005 is installed. The bottom feedback divider resistor R2 may be removed as well.
9. Monitor the power good voltage through the PG test point to see the status of the output.

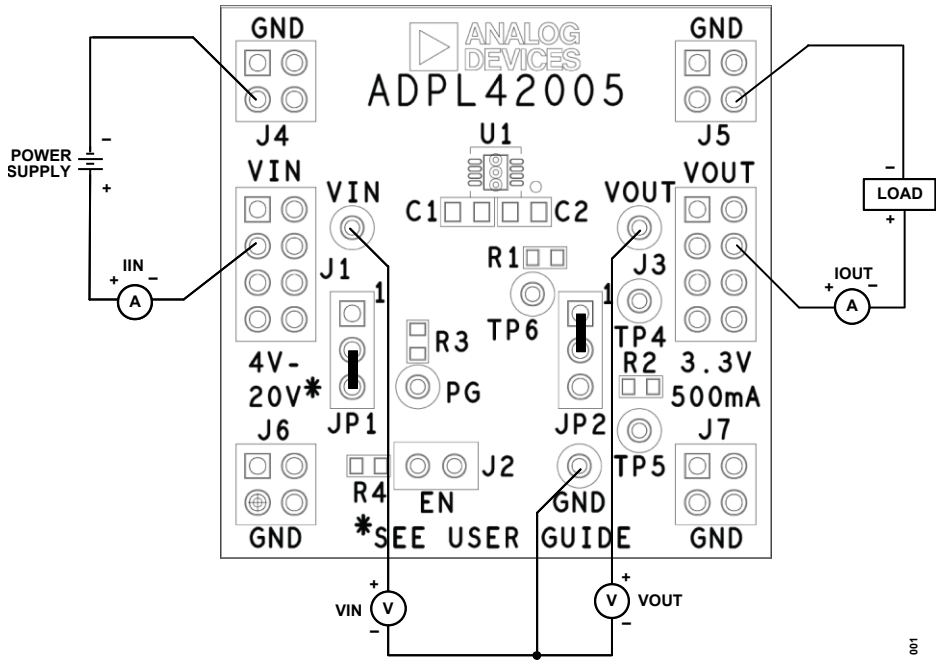


Figure 1. LFCSP Package Evaluation Board Connections

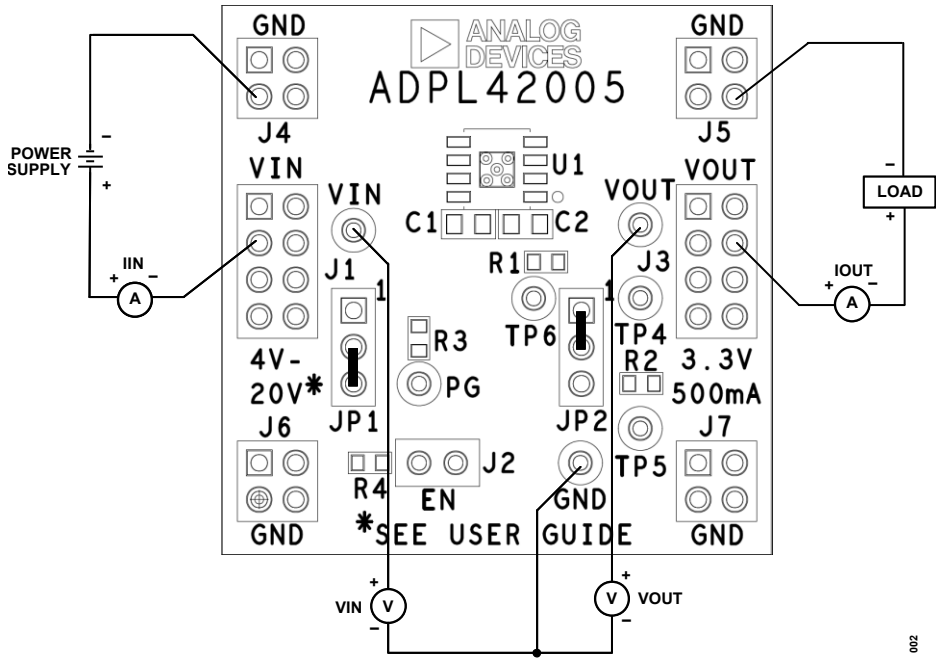


Figure 2. SOIC Package Evaluation Board Connections

Performance Summary

Specifications are at T_A = +25°C, unless otherwise noted.

Table 1. Performance Summary of the LFCSP Package Evaluation Board\

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}	I_{OUT} = 10mA, V_{OUT} = 3.3V	4		20	V
Input Voltage Range	V_{IN}	I_{OUT} = 500mA, V_{OUT} = 3.3V	4		6.3[1]	V
Output Voltage	V_{OUT}	V_{IN} = 5V, I_{OUT} = 500mA, R1 = 24kΩ, R2 = 14kΩ	3.22	3.29	3.36	V
Feedback Divider Current	I_{FB}	JP1 = Pins 2 to 3, JP2 = Pins 1 to 2, R1 = 24kΩ, R2 = 14kΩ		87		µA
Shutdown Input Current	I_{GND_SD}	JP1 = Pins 1 to 2, V_{IN} = 12V, EN = GND		40	75	µA

[1] The maximum power dissipation and, consequently, the maximum input voltage for an output programmed to 3.3V with a 500mA load is determined by the 60°C temperature rise of the ADPL42005 on the evaluation board. In addition, consider the effect of ambient temperature and the maximum junction temperature that may occur. Refer to the ADPL42005 data sheet for more information.

Table 2. Performance Summary of the SOIC Package Evaluation Board

PARAMETER	SYMBOL	TEST CONDITIONS/COMMENTS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}	I_{OUT} = 10mA, V_{OUT} = 3.3V	4		20	V
Input Voltage Range	V_{IN}	I_{OUT} = 500mA, V_{OUT} = 3.3V	4		5.77[1]	V
Output Voltage	V_{OUT}	V_{IN} = 5V, I_{OUT} = 500mA, R1 = 24kΩ, R2 = 14kΩ	3.22	3.29	3.36	V
Feedback Divider Current	I_{FB}	JP1 = Pins 2 to 3, JP2 = Pins 1 to 2, R1 = 24kΩ, R2 = 14kΩ		87		µA
Shutdown Input Current	I_{GND_SD}	JP1 = Pins 1 to 2, V_{IN} = 12V, EN = GND		40	75	µA

[1] The maximum power dissipation and, consequently, the maximum input voltage for an output programmed to 3.3V with a 500mA load is determined by the 60°C temperature rise of the ADPL42005 on the evaluation board. In addition, consider the effect of ambient temperature and the maximum junction temperature that may occur. Refer to the ADPL42005 data sheet for more information.

Printed Circuit Board (PCB) Layout

The printed circuit boards (PCBs) for these evaluation boards are 0.062 inches thick and 1.5 inches square. There are two copper layers, and the finished copper thickness is 1.5 ounces. The input capacitor, ADPL42005, and output capacitor are all placed on the upper side of the PCB. The input and output capacitors are placed near the ADPL42005 with their ground terminals close to each other. The bottom side of the PCB is a solid ground plane that connects to the ground on the top PCB layer by thermal vias under or near the ADPL42005 and at other points. The layout may significantly affect circuit electrical performance and reliability.

Jumper Connection

JUMPER	DEFAULT CONNECTION	FEATURE
JP1	Pins 2 to 3	Turns the regulator on.
JP2	Pins 1 to 2	Connects the SENSE/ADJ pin to the output through a resistor divider.

Ordering Information

MODEL [1, 2]	PACKAGE DESCRIPTION
EVAL-ADPL42005CP-AZ	LFCSP Package Evaluation Board
EVAL-ADPL42005RD-AZ	SOIC Package Evaluation Board

[1] *Z = RoHS compliant part*

[2] *The evaluation boards are preconfigured with an adjustable ADPL42005.*

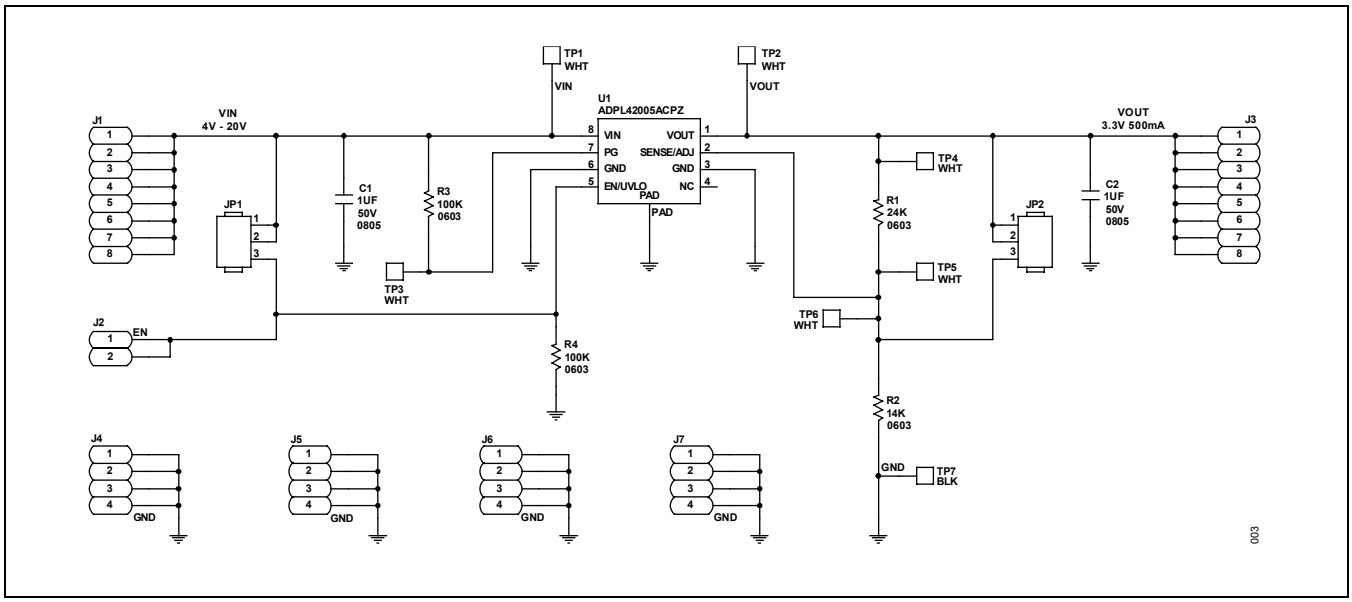
LFCSP Package Evaluation Board Bill of Materials

ITEM	QUANTITY	REFERENCE DESIGNATOR	PART DESCRIPTION	MANUFACTURER, PART NUMBER
Required Circuit Components				
1	2	C1, C2	1µF capacitor, X5R, 50V, 10%, 0805	Murata, GRM219R61H105KA73D
2	1	R1	24kΩ resistor, 0.1%, 1/10W, 0603	Panasonic, ERA-3AEB243V
3	1	R2	14kΩ resistor, 0.1%, 1/10W, 0603	Panasonic, ERA-3AEB1402V
4	2	R3, R4	100kΩ resistor, 1%, 1/10W, 0603	Yageo, RC0603FR-07100KL
5	1	U1	20V, 500mA, low noise, CMOS, LDO linear regulator	Analog Devices, ADPL42005ACPZ-R7
Hardware				
1	2	J1, J3	Connector, header, male, 2 x 4, 2.54mm, vertical, straight, through hole	Sullins, PEC04DAAN
2	1	J2	Connector, header, male, 1 x 2, 2.54mm, vertical, straight, through hole	Sullins, PEC02SAAN
3	4	J4 to J7	Connector, header, male, 2 x 2, 2.54mm, vertical, straight, through hole	Sullins, PEC02DAAN
4	2	JP1, JP2	Connector, header, male, 1 x 3, 2.54mm, vertical, straight, through hole	Sullins, PEC03SAAN
5	2	XJP1, XJP2	Connector, shunt, female, 2 position, 2.54mm	Sullins, SPC02SYAN

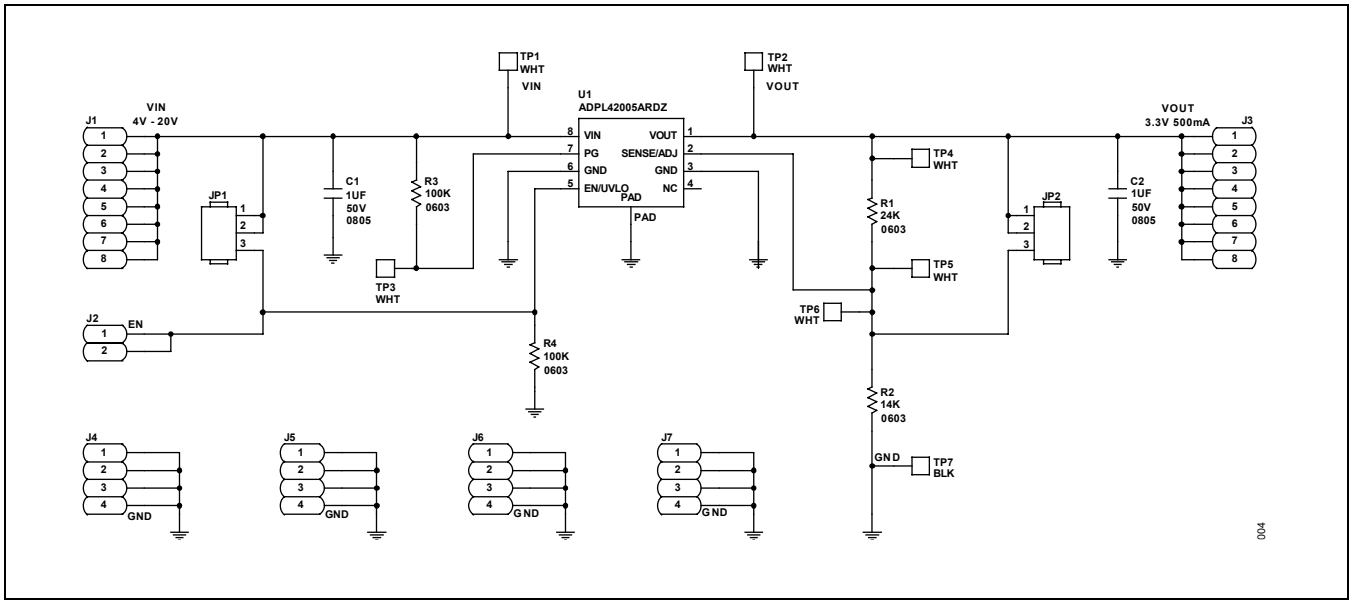
SOIC Package Evaluation Board Bill of Materials

ITEM	QUANTITY	REFERENCE DESIGNATOR	PART DESCRIPTION	MANUFACTURER, PART NUMBER
Required Circuit Components				
1	2	C1, C2	1µF capacitor, X5R, 50V, 10%, 0805	Murata, GRM219R61H105KA73D
2	1	R1	24kΩ resistor, 0.1%, 1/10W, 0603	Panasonic, ERA-3AEB243V
3	1	R2	14kΩ resistor, 0.1%, 1/10W, 0603	Yageo, RT0603BRD0714KL
4	2	R3, R4	100kΩ resistor, 1%, 1/10W, 0603	Yageo, RC0603FR-07100KL
5	1	U1	20V, 500mA, low noise, CMOS, LDO linear regulator	Analog Devices, ADPL42005ARDZ-R7
Hardware				
1	2	J1, J3	Connector, header, male, 2 x 4, 2.54mm, vertical, straight, through hole	Sullins, PEC04DAAN
2	1	J2	Connector, header, male, 1 x 2, 2.54mm, vertical, straight, through hole	Sullins, PEC02SAAN
3	4	J4 to J7	Connector, header, male, 2 x 2, 2.54mm, vertical, straight, through hole	Sullins, PEC02DAAN
4	2	JP1, JP2	Connector, header, male, 1 x 3, 2.54mm, vertical, straight, through hole	Sullins, PEC03SAAN
5	2	XJP1, XJP2	Connector, shunt, female, 2 position, 2.54mm	Sullins, SPC02SYAN

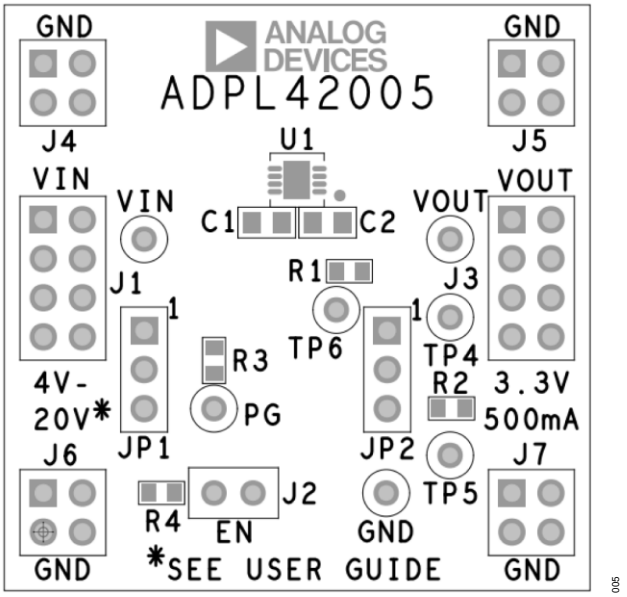
LFCSP Package Evaluation Board Schematic



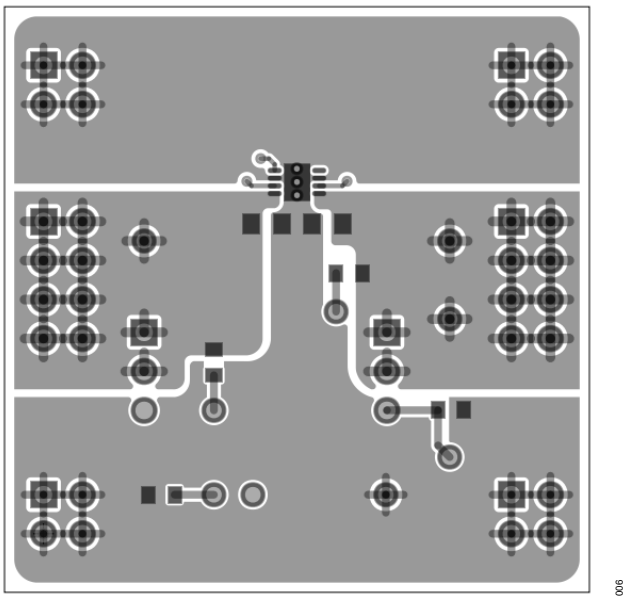
SOIC Package Evaluation Board Schematic



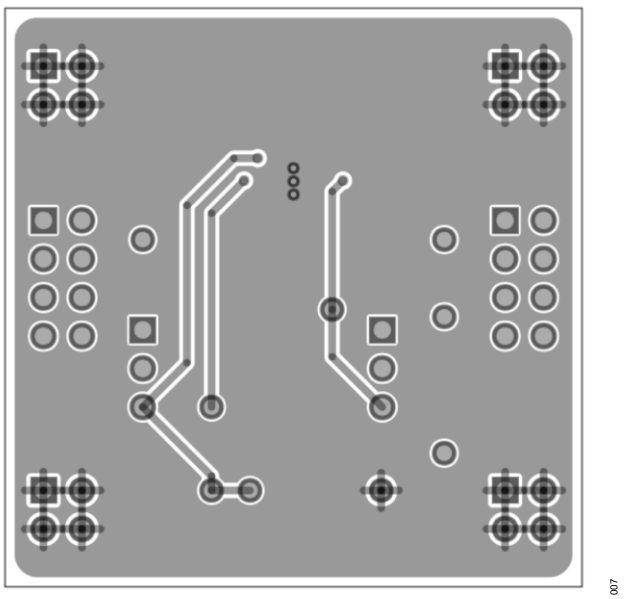
LFCSP Package Evaluation Board PCB Layout



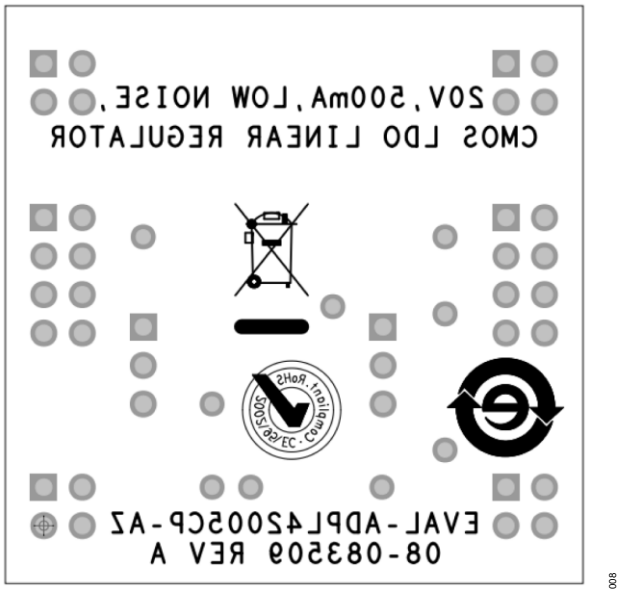
LFCSP Package Evaluation Board—Top Silkscreen



LFCSP Package Evaluation Board—Top

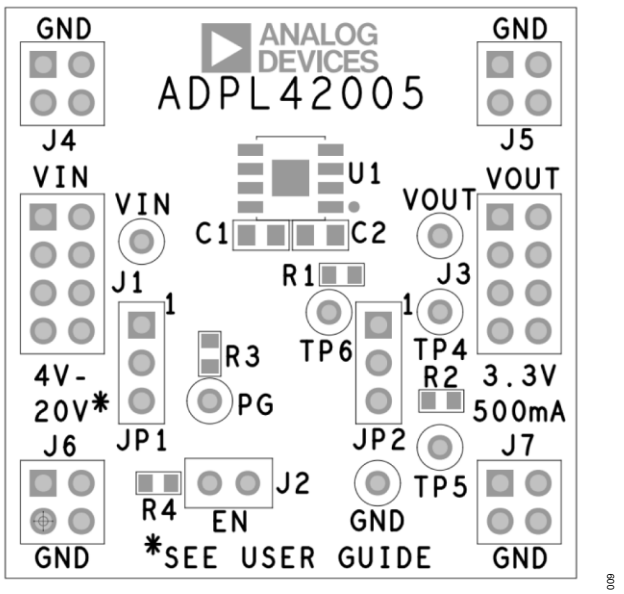


LFCSP Package Evaluation Board—Bottom

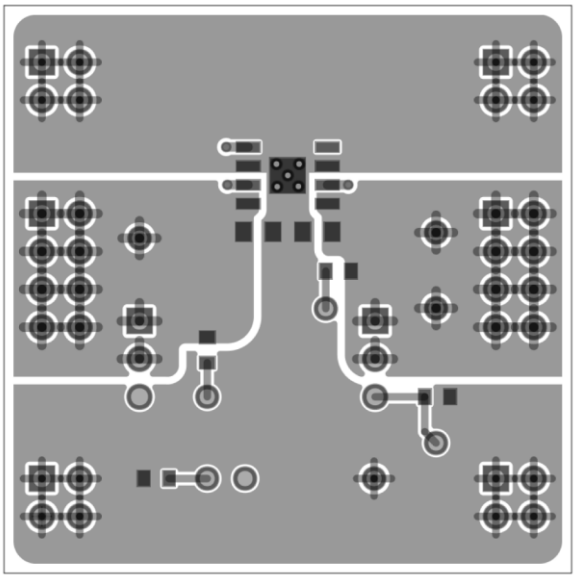


LFCSP Package Evaluation Board—Bottom Silkscreen

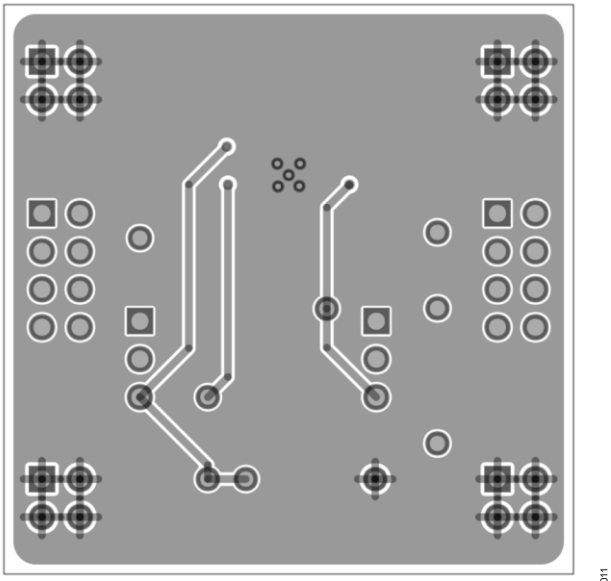
SOIC Package Evaluation Board PCB Layout



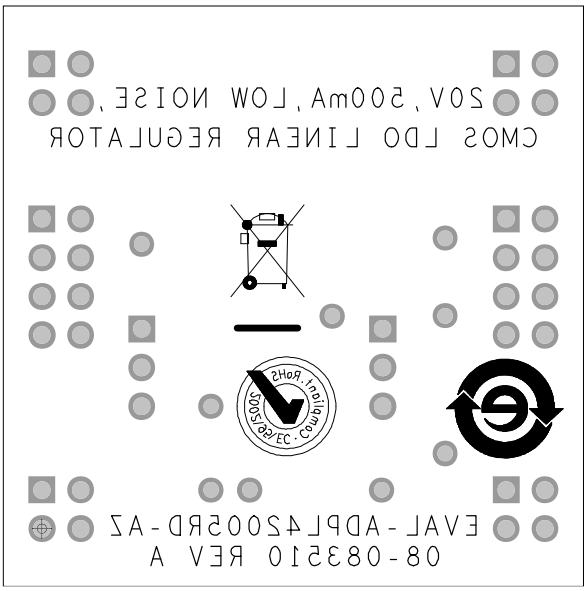
SOIC Package Evaluation Board—Top Silkscreen



SOIC Package Evaluation Board—Top



SOIC Package Evaluation Board—Bottom



SOIC Package Evaluation Board—Bottom Silkscreen

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	02/25	Initial release	—

Notes