

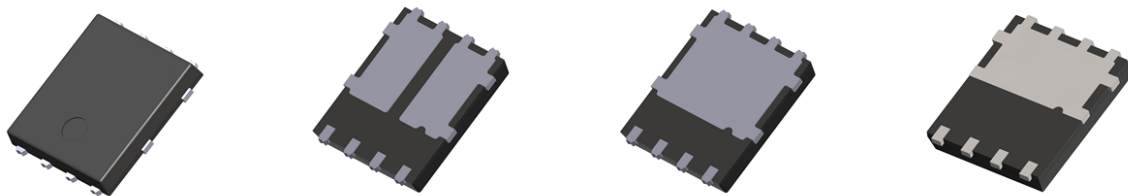
## Printed circuit board assembly recommendations for STMicroelectronics PowerFLAT packages

### Introduction

The PowerFLAT package (5x6) was created to allow a larger die to fit in a standard SO8 footprint, as well as to minimize package height and weight (lead-frame design is done in such a way that die and wire bond pads are on the same plane). After mounting on a PCB (printed circuit board), leads and body are directly soldered to the board without space-consuming standoff, which is inherent to leaded packages.

There are 2 main configurations for this package: one is single island, and the other one is dual island. Each allow different electrical functions. For the single island package configuration, one option is available for high voltage products, with greater distance between body pads and leads to ensure higher clearance. These options are shown in [Figure 1](#) below:

**Figure 1. PowerFLAT package configurations**



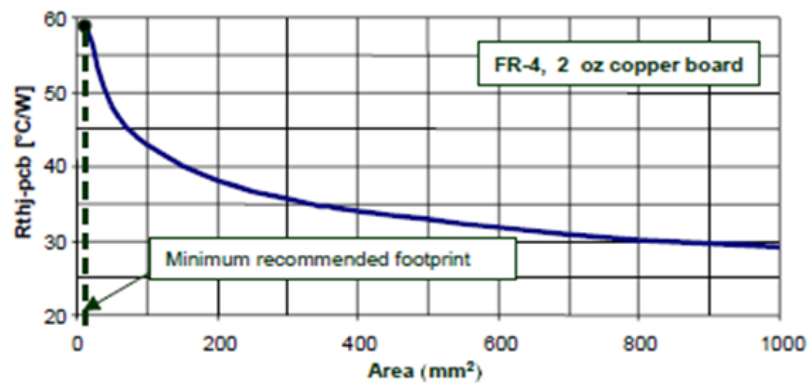
# 1 Thermal considerations

## 1.1 Thermal resistance

The thermal resistance of a semiconductor device characterizes the device's capability to dissipate the heat generated by the chip during operation. This parameter allows us to calculate the junction temperature, taking into account the device environment (load current, ambient temperature, mounting conditions, etc.).

For SMDs (surface mount devices), the thermal resistance between junction and ambient, called  $R_{th(j-a)}$  or  $R_{th(j-pcb)}$ , highly depends on the copper surface used under the tab. Figure 2. PowerFLAT  $R_{th}$  below shows an example of the relationship between  $R_{th(j-a)}$  and the copper surface under the tab for an FR4 board - 35  $\mu m$  copper thickness for a PFLAT package.

Figure 2. PowerFLAT  $R_{th}$

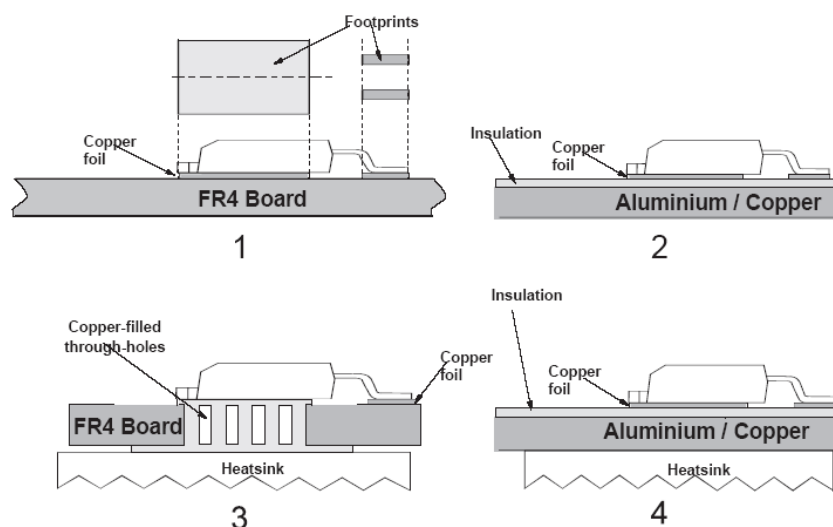


## 1.2 Mounting techniques and $R_{th(j-a)}$

$R_{th(j-a)}$  varies based on the printed circuit board technology employed. As shown in Figure 3. Mounting techniques for power SMDs, several technologies can be used depending on the performance required in the design. Four techniques are commonly used:

- FR4 - copper
- IMS (insulated metal substrate)
- FR4 board with copper-filled through-holes + heatsink
- IMS + heatsink

Figure 3. Mounting techniques for power SMDs



As the FR4 board is commonly used in surface mounting techniques, there are several ways of overcoming its low thermal performance:

- The use of large heat spreader areas (heatsink) at the copper layer of the PCB
- The use of copper-filled through-holes in addition to an external heatsink for even better thermal management

However, due to its power dissipation limitation, using the FR4 board with these techniques is only advisable for currents up to 8 A max.

Another technology available today is IMS - Insulated Metallic Substrate. This offers greatly enhanced thermal characteristics for surface mount components. IMS consists of three different layers:

- (I) base material which is available as an aluminum or copper plate
- (II) thermal conductive dielectric layer
- (III) copper foil, which can be etched as a circuit layer

If a higher power must be dissipated, an external heatsink can be applied, which allows a significant reduction of  $R_{th(j-a)}$ .

The designer should carefully examine the appropriate mounting method to be used based on the power dissipation requirements. The board type will influence the thermal performance of the system. Table 1.  $R_{th(j-a)}$  for DPAK shows the  $R_{th(j-a)}$  for each mounting technique. The  $R_{th(j-a)}$  values were not measured in similar conditions for PowerFLAT packages, but similar values can be expected.

Table 1.  $R_{th(j-a)}$  for DPAK

| Mounting method                                    | $R_{th(j-a)}$ |
|----------------------------------------------------|---------------|
|                                                    | DPAK          |
| FR4                                                | 70 °C/W       |
| FR4 with 10 cm <sup>2</sup> heatsink on board      | 40 °C/W       |
| FR4 with copper filled holes and external heatsink | 13 °C/W       |
| IMS (40 cm <sup>2</sup> ) floating in air          | 9 °C/W        |
| IMS with external heatsink                         | 4.5 °C/W      |

## 2 PowerFLAT PCB mounting process

The surface mount assembly is a 5-step process:

- Solder paste printing
- Component placement on the board
- Reflow soldering
- Cleaning (optional)
- Final solder joint inspection

### 2.1 Printed circuit board recommendations

- PCB solderable metallization

There are two common plated solderable metallization finishes which are used for PCB surface mount devices. In either case, it is required that the plating is uniform, conforming, and free of impurities to ensure consistent solderability.

The first metallization finish consists of an organic solderable preservative (OSP) coating over the copper pad. The organic coating assists in reducing oxidation to preserve the copper metallization for soldering.

The second metallization is NiAu (electroless nickel plating over the copper pad, followed by immersion gold). The thickness of the nickel layer is determined by the allowable internal material stresses and the temperature excursions the board will be subjected to throughout its lifetime. For the immersion gold process, the gold thickness is self-limited, but should be thick enough to prevent Ni oxidation (typically above 0.05  $\mu\text{m}$ ) and thin enough to represent more than 5% of the overall solder volume. Having excessive gold in the solder joint can create gold embitterment, which may affect the reliability of the solder joint.

- PCB design

We recommend closed vias in the design, in order to control the amount of solder paste during screen printing.

Position of tracks and open vias in the solder area should be well balanced. Symmetrical layout is recommended to avoid tilt caused by asymmetrical solder paste quantities.

- PCB pad design

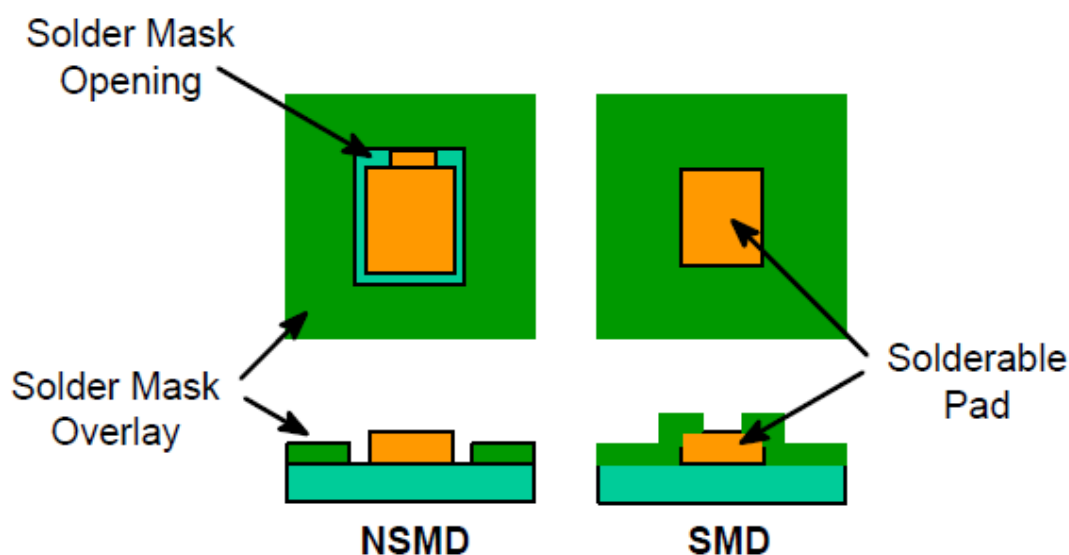
There are 2 different types of PCB pad configurations commonly used for surface mount packages:

- Non solder mask defined (NSMD)
- Solder mask defined (SMD)

As their title indicates, NSMD contact pads have the solder mask pulled away from the solderable metallization, while the SMD pads have the solder mask over the edge of the metallization, as shown in [Figure 4. Comparison between SMD and NSMD pads](#).

With SMD pads, the solder mask restricts the flow of solder paste to the top of the metallization, preventing the solder from flowing along the sides of the metal pad. This is different from the NSMD pads, where the solder will flow around both the top and the sides of the metallization.

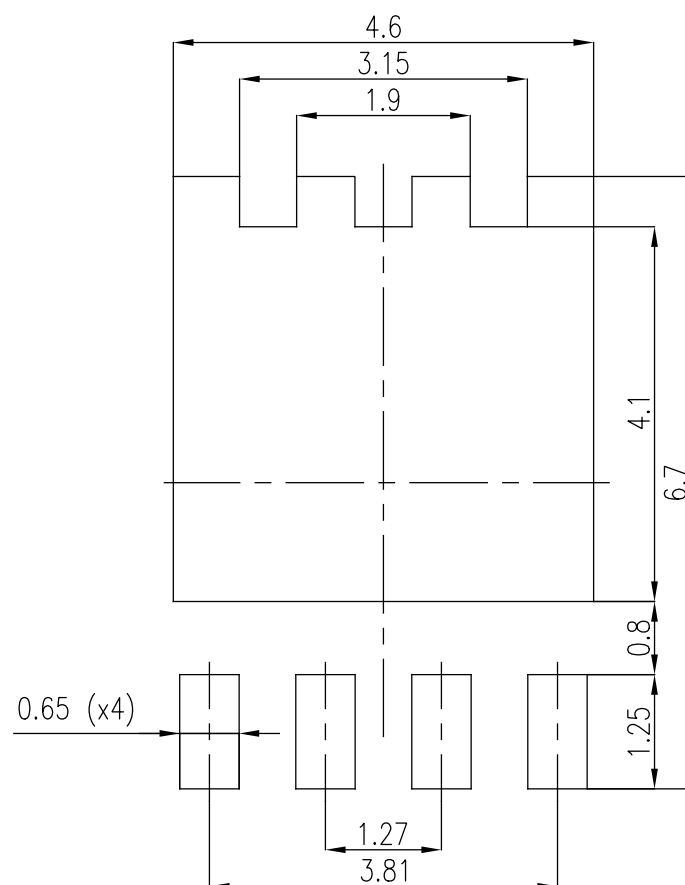
Figure 4. Comparison between SMD and NSMD pads



Both configurations can be used.

Typically, NSMD pads are preferred since defining the location and size of the copper pad is easier to control than the solder mask. This is based on the fact that the copper etching process is capable of tighter tolerance than the solder masking process.

PCB solderable pad design recommendations for PFLAT packages are shown in [Figure 5. PowerFLAT single pad PCB footprint](#), [Figure 6. PowerFLAT dual pad PCB footprint](#) and [Figure 7. PowerFLAT high voltage PCB footprint](#).

**Figure 5. PowerFLAT single pad PCB footprint**


**Figure 6. PowerFLAT dual pad PCB footprint**

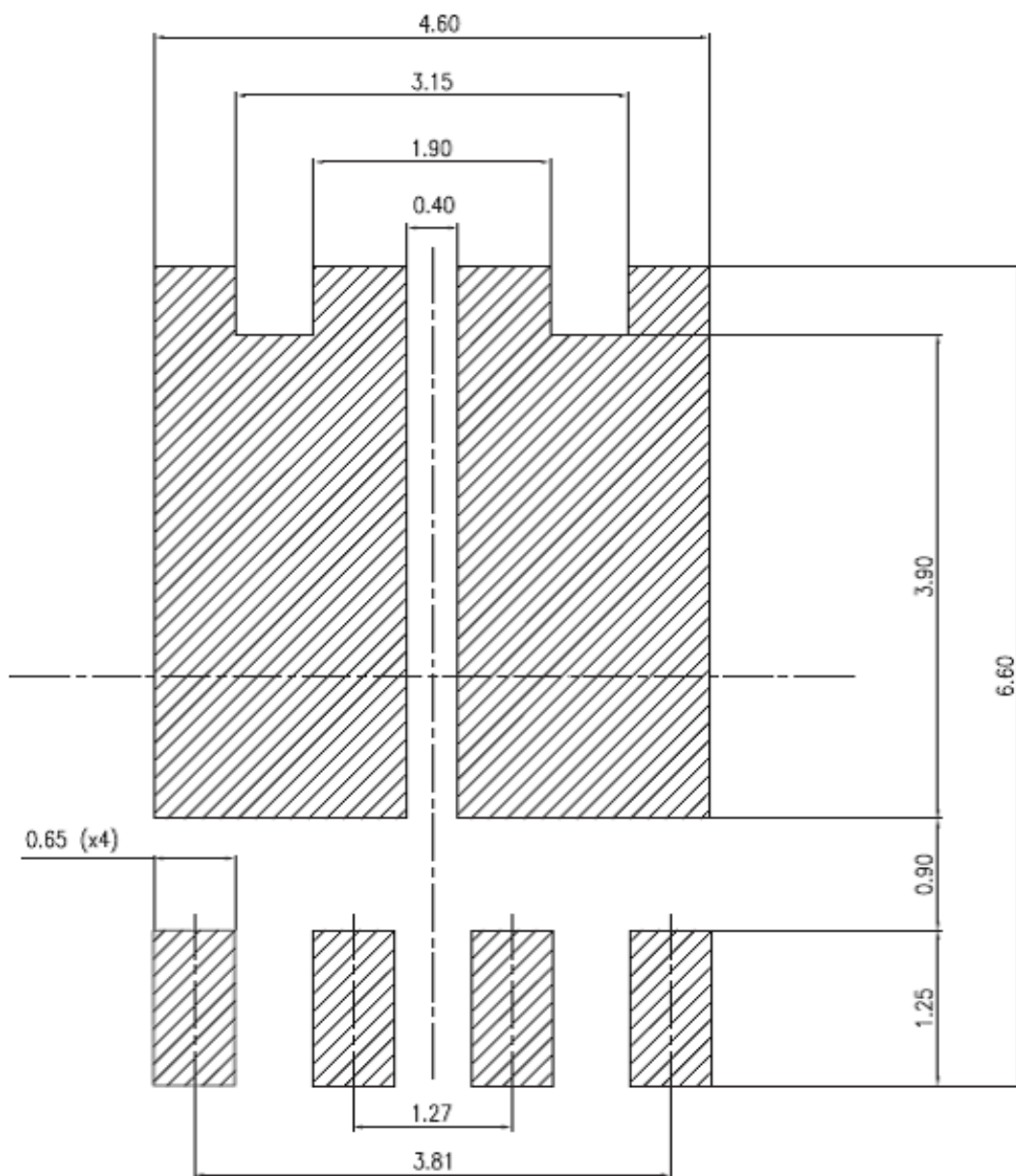
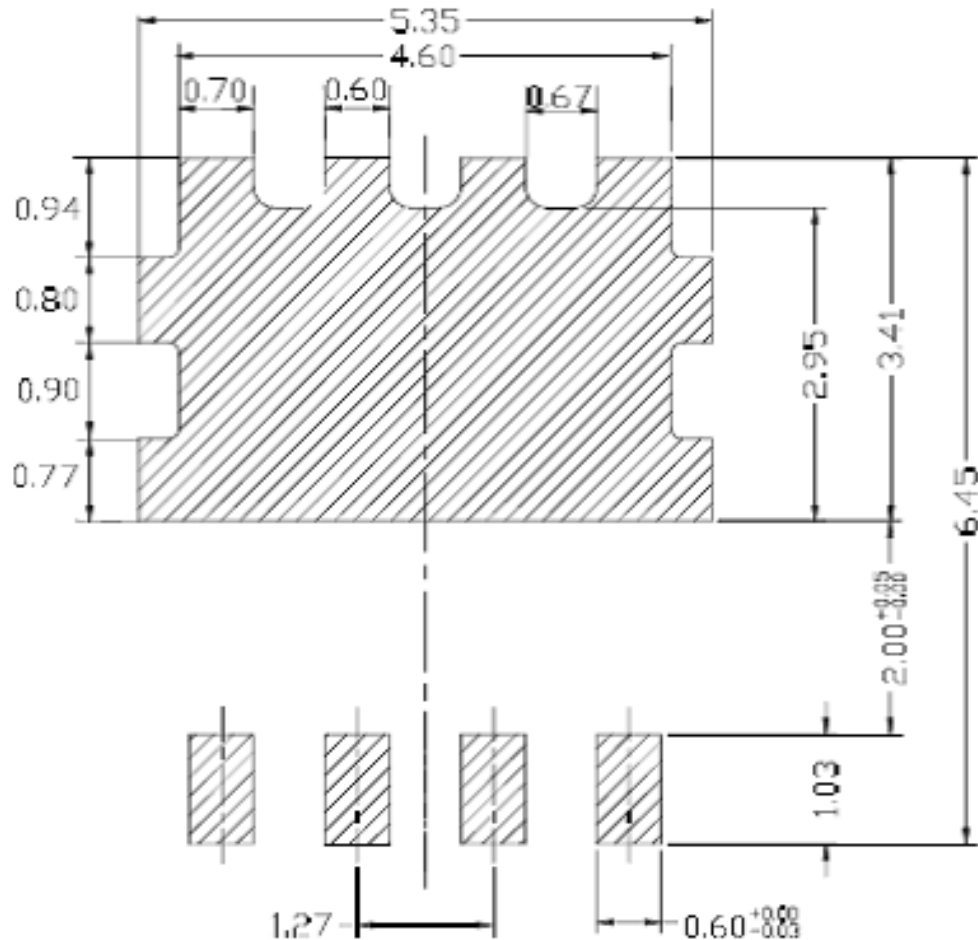


Figure 7. PowerFLAT high voltage PCB footprint



The dimensions of the PCB solderable pads should be greater than the device footprint to ensure correct solder fillet aspect. The ratio between the package's pad configuration and that of the PCB is designed for optimal reliability, and to allow component self-centering during reflow.

## 2.2 Solder paste printing

- Solder type

We recommend the use of solder paste with fine particles (type 3 or type 4, meaning particle dimensions from 20 to 45  $\mu\text{m}$ ), as well as solder paste containing halide-free flux ROL0 in accordance with ANSI/J-STD-004. For lead-free solders Sn-Ag-Cu, alloy SnAg1.0Cu0.5 is preferred, but any SnAgCu alloys with 1 to 4% Ag and <1% Cu should be suitable.

- Solder screening on the PCB

Stencil screening the solder on the PCB is commonly used in the industry. Recommended stencil thicknesses are 0.075 mm to 0.127 mm (0.003 inch to 0.005 inch) and the sidewalls of the stencil openings should be tapered approximately 5° to ease the release of the paste when the stencil is removed from the PCB.

For a typical lead PCB terminal, we recommend a stencil opening to footprint ratio of 90%. For central exposed pad, it may vary depending on package dimensions, but solder coverage should vary from 50 to 80%.

For PowerFLAT, as described later in this document, we evaluated an opening from 45 to 75%, without significant differences in terms of voids (but of course solder thickness differs depending on stencil opening and stencil thickness).



The stencil opening under the package's exposed pad must be divided into smaller openings. This reduces the risk of solder voiding, and allows the solder joint for the leads to be at the same height as the exposed pad. To ensure a safe and repeatable stencil printing process, some generic design rules for stencil design should be followed, as described here below.

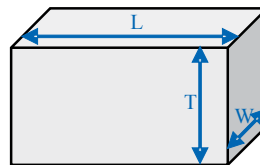
- General design rule
  - Stencil thickness (T) = 75 ~ 125 µm
  - Aspect ratio =

$$\frac{W}{T} \geq 1.5 \quad (1)$$

- Aspect area =

$$\frac{L \times W}{2T(L + W)} \geq 0.66 \quad (2)$$

**Figure 8. Stencil opening dimensions**



Recommended stencil design openings for PFLAT single and dual pad packages are shown in [Figure 9. PowerFLAT single pad stencil opening recommendation](#), [Figure 10. PowerFLAT dual pad stencil opening recommendation](#) and [Figure 11. PowerFLAT high voltage stencil opening recommendation](#). Stencil openings are drawn in blue dotted lines (PCB solderable pads are in black).

Figure 9. PowerFLAT single pad stencil opening recommendation

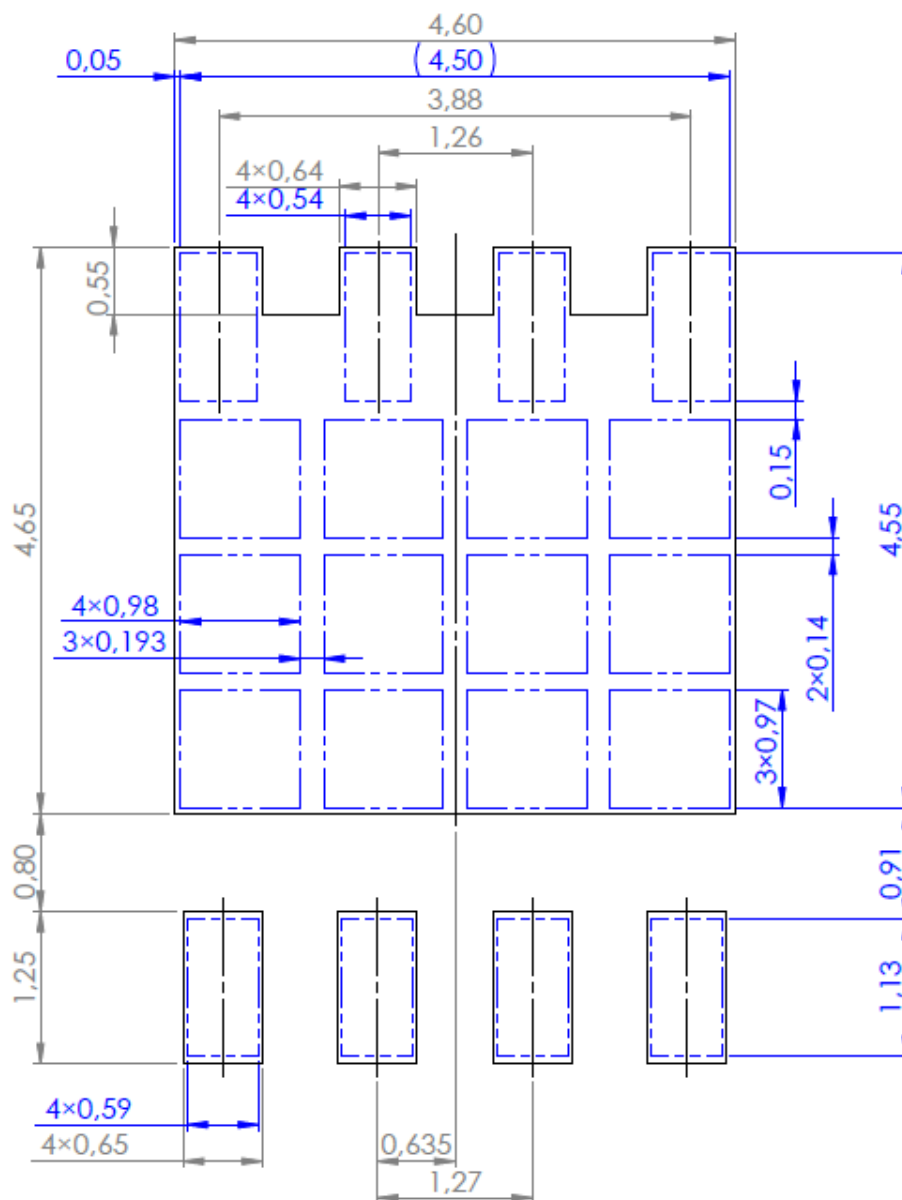
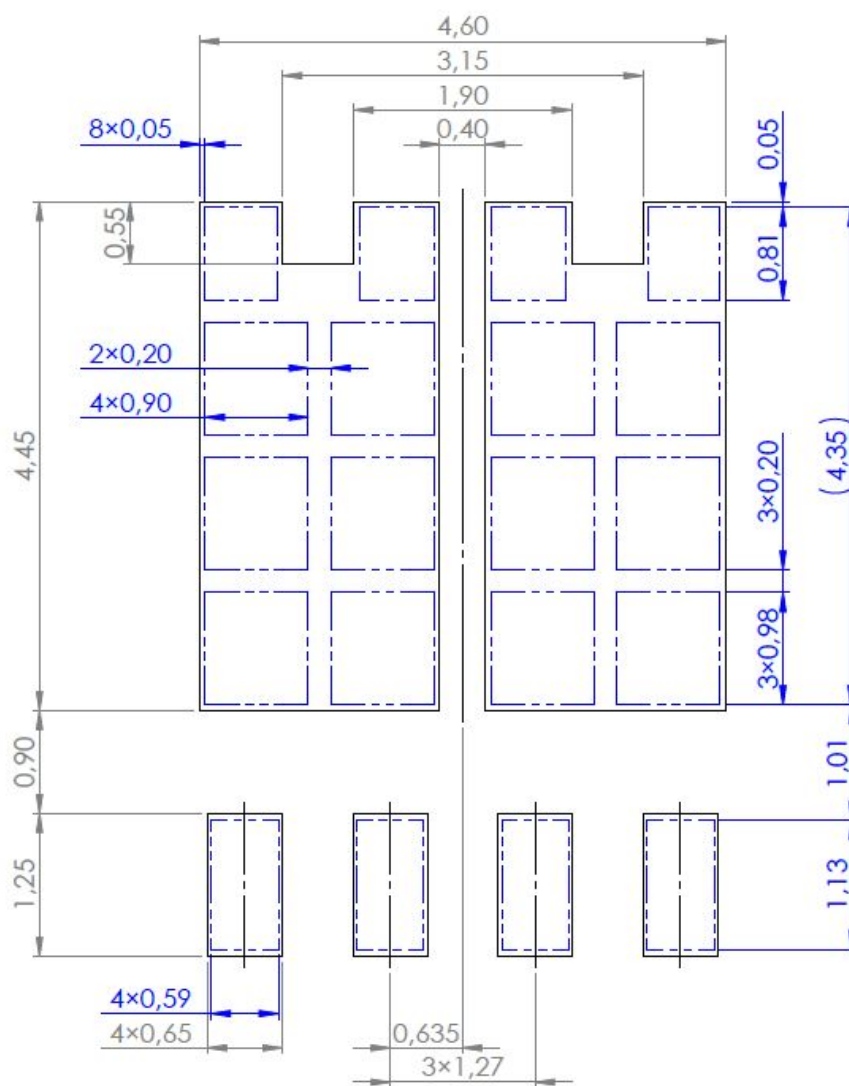
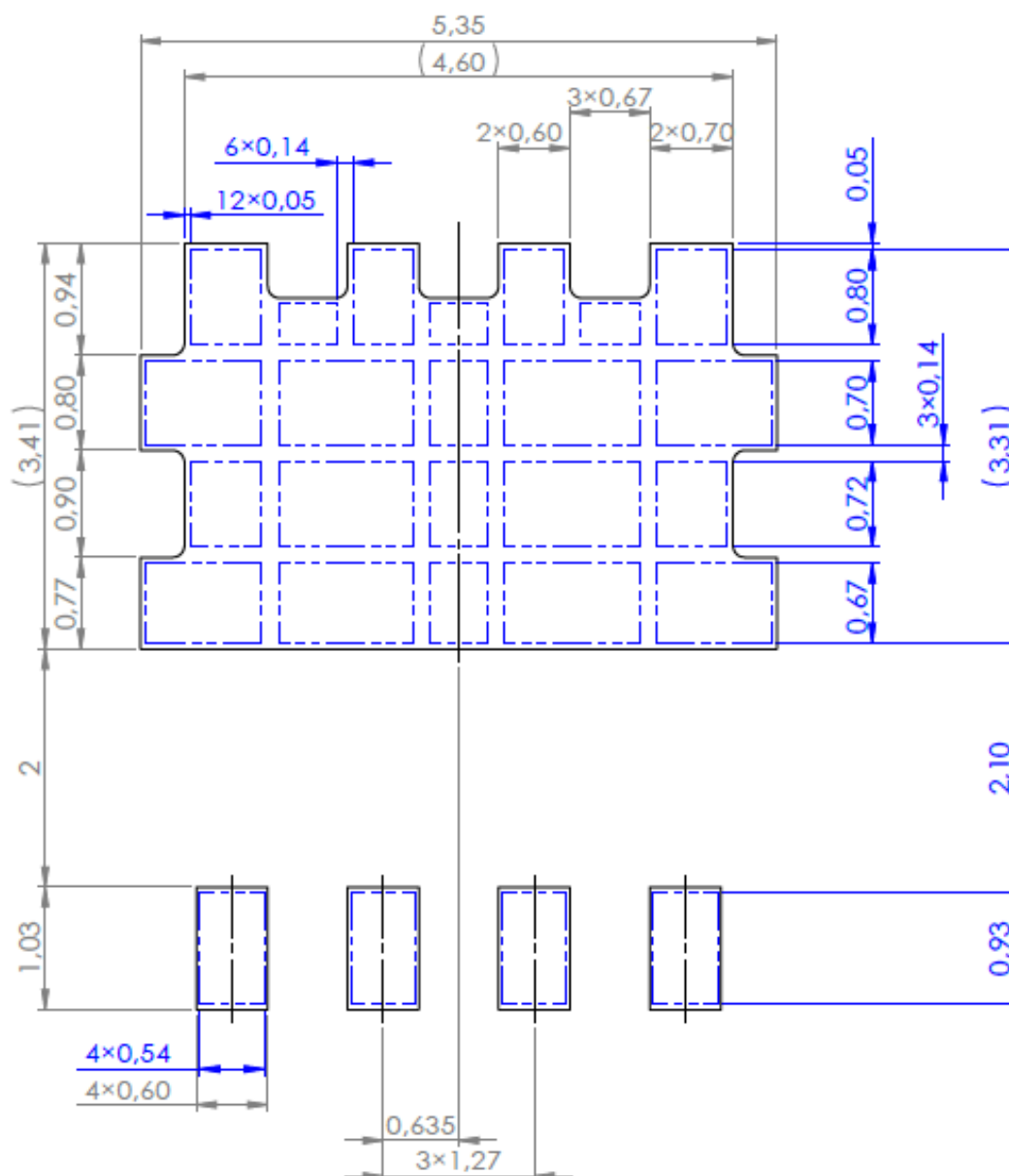


Figure 10. PowerFLAT dual pad stencil opening recommendation



**Figure 11. PowerFLAT high voltage stencil opening recommendation**



## 2.3 Component placement

Manual placement is not recommended.

We recommend to use pick-and-place equipment with the standard tolerance of  $\pm 0.05$  mm or better. The package will tend to center itself and correct for slight placement errors during the reflow process due to surface tension of the solder joint.

Adequate placement force should be used (3.5 N for example for most of packages). Too strong a placement force can lead to squeezed-out solder paste and cause solder joint to short. Too low a placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or non-centered packages.

## 2.4 Reflow profile recommendation

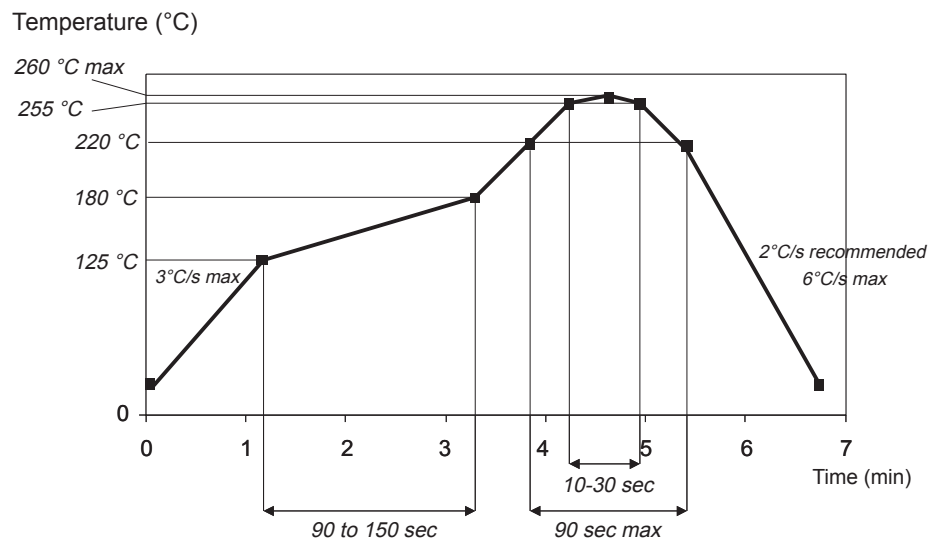
The soldering process causes significant thermal stress to a semiconductor component. This has to be minimized to assure a reliable and extended lifetime of the device.

PowerFLAT, like many other SMD plastic packages, can be exposed to a maximum temperature of 260 °C for 10 seconds. Overheating during the reflow soldering process may damage the device, therefore any solder temperature profile should be within these limits. As reflow techniques are most common in surface mounting, typical heating profiles for lead-free solder (ST Ecopack) are given in [Figure 12. ST Ecopack recommended soldering reflow profile for PCB mounting](#) for small packages, either for mounting on an FR4 or on metal-backed boards (IMS). Please refer to the IPC / JEDEC J-STD-020E standard for further information about “small” and “large” component definitions.

**Note:** *The soldering profile defined in the JEDEC J-STD-020E standard are used for reliability assessment and typically describe the warmest profiles used for component mounting, not the necessary temperatures to achieve good soldering.*

Wave soldering is not advisable for SMD power packages (and thus for PowerFLAT) because it is almost impossible to contact the whole package slug during the process.

**Figure 12. ST Ecopack recommended soldering reflow profile for PCB mounting**



For each individual board, the appropriate heat profile has to be adjusted experimentally. The current proposal is just a starting point. In every case, the following precautions have to be considered:

- Always preheat the device. The purpose of this step is to minimize the rate of temperature rise to less than 3 °C per second (recommended 2 °C/s) in order to minimize the thermal shock on the component.
- Dry out section, after preheating, to ensure that the solder paste is fully dried before starting the reflow step. Also, this step allows the temperature gradient on the board to be evened out.
- Peak temperature should be at least 30 °C higher than the melting point of the solder alloy chosen to ensure reflow quality. In any case the peak temperature should not exceed 260 °C.

Lead-free devices are described in an internal specification defining:

- Their characteristics: lead-free connection coating, solderability and identification features
- Their reliability, such as soldering resistance, reliability, whisker risk prevention

This specification is available for ST customers upon request (title: ECOPACK components definition and characteristics). Please consult this specification for further reflow and wave soldering information.

Voids pose a difficult reliability problem for large surface mount devices. Voids under the package result in poor thermal contact and the high thermal resistance can lead to component failure.

## 2.5 Thermal cycling evaluations performed by STMicroelectronics

Evaluations were performed to assess ability of PowerFLAT package mounted on PCB to fulfill AECQ101 requirements.

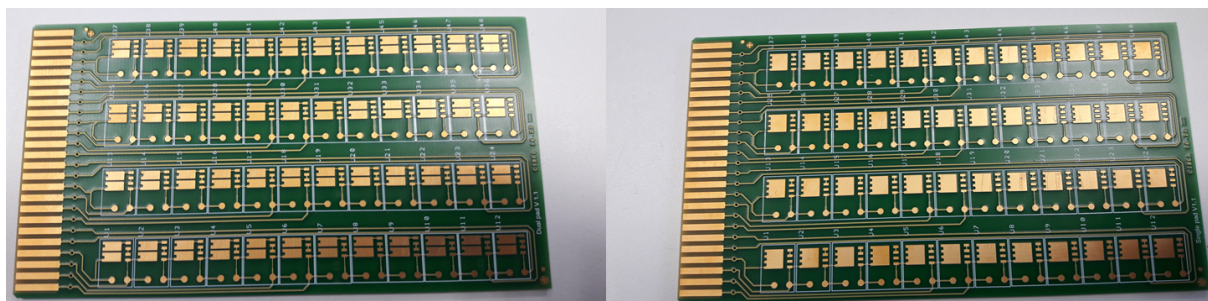
### 2.5.1 Evaluation description

The PCBs were designed for PowerFLAT single and dual pad, with solderable pad dimensions recommended in this document. PCBs with 2 and 6 layers were designed (70  $\mu\text{m}$  Cu layer thickness on external sides, 35  $\mu\text{m}$  Cu internal layers for 6 layer PCBs), to evaluate PCBs with different mechanical characteristics. Solderable pads were designed as NSMD, and covered with NiAu plating.

PCB and PowerFLAT components generate a daisy chain, resistance was measured at initial stage, and resistance drift was measured every 500 cycles.

Figure 13. PCB pictures provides photos of the PCBs (before and after component mounting).

Figure 13. PCB pictures



Components were mounted on the PCBs with different stencil designs, described in Figure 14. Stencil openings single pad. Various pad openings were evaluated for central exposed pad, in order to evaluate pad opening impact on reliability.

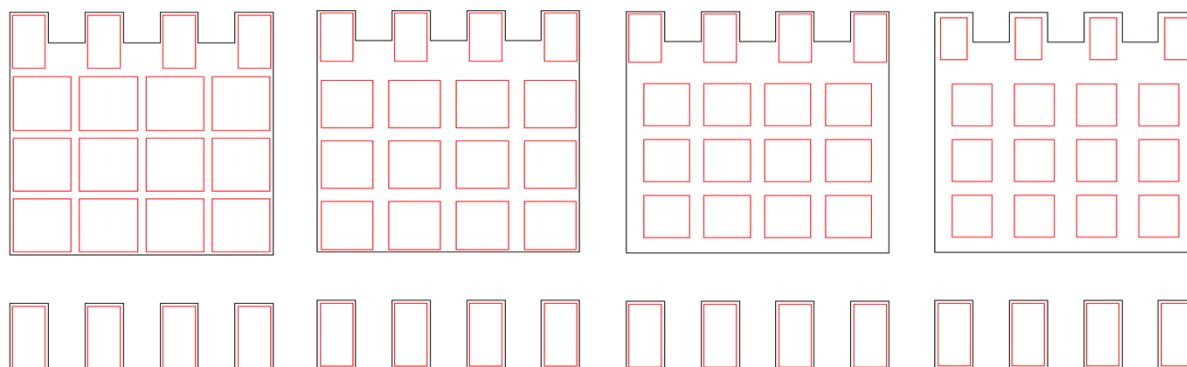
For the single pad package, opening ratios of 73%, 61%, 49% and 41% were designed (opening ratio is the ratio between stencil opening and PCB land dimension).

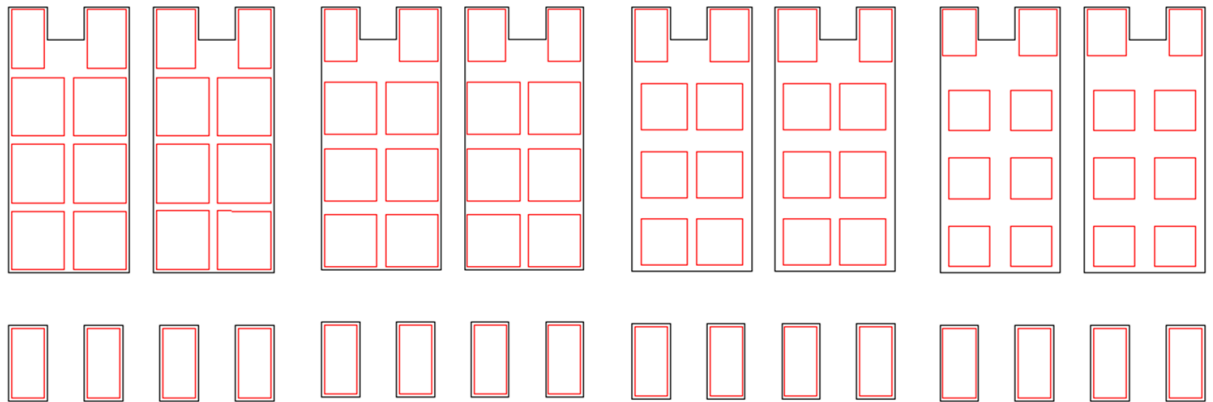
For dual pad package, opening ratios of 74%, 66%, 55% and 43% were designed. These designs are shown in Figure 14. Stencil openings single pad and Figure 15. Stencil openings dual pad.

Stencils with 100 and 125  $\mu\text{m}$  thickness were evaluated.

The solder paste used was SnAg1.0Cu0.5 solder alloy, type 4 paste.

Figure 14. Stencil openings single pad



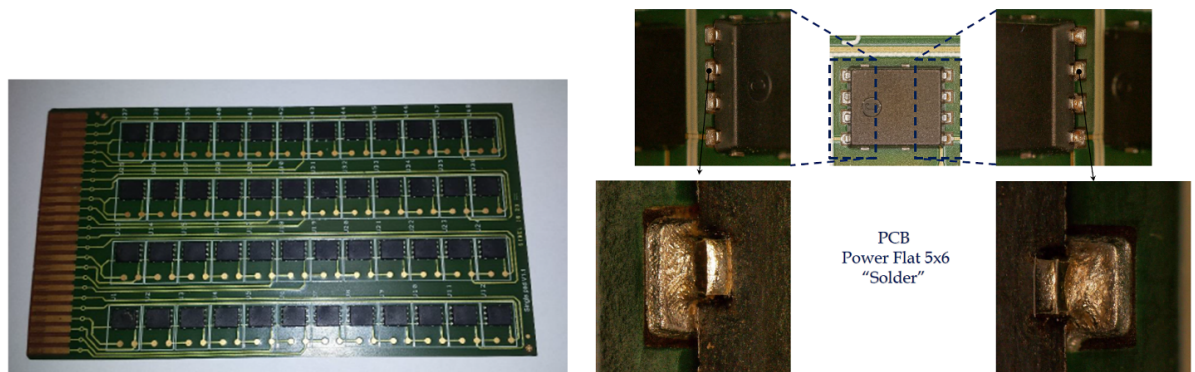
**Figure 15. Stencil openings dual pad**


The reflow profile used was the standard JEDEC profile, without any optimization. For this reason, void level was quite high (up to 30% voids under a single pad) in our evaluation, but it was intentionally not optimized to reflect reliability behavior of a solder joint in conditions not necessarily optimized for a PowerFLAT package.

## 2.5.2

### Results

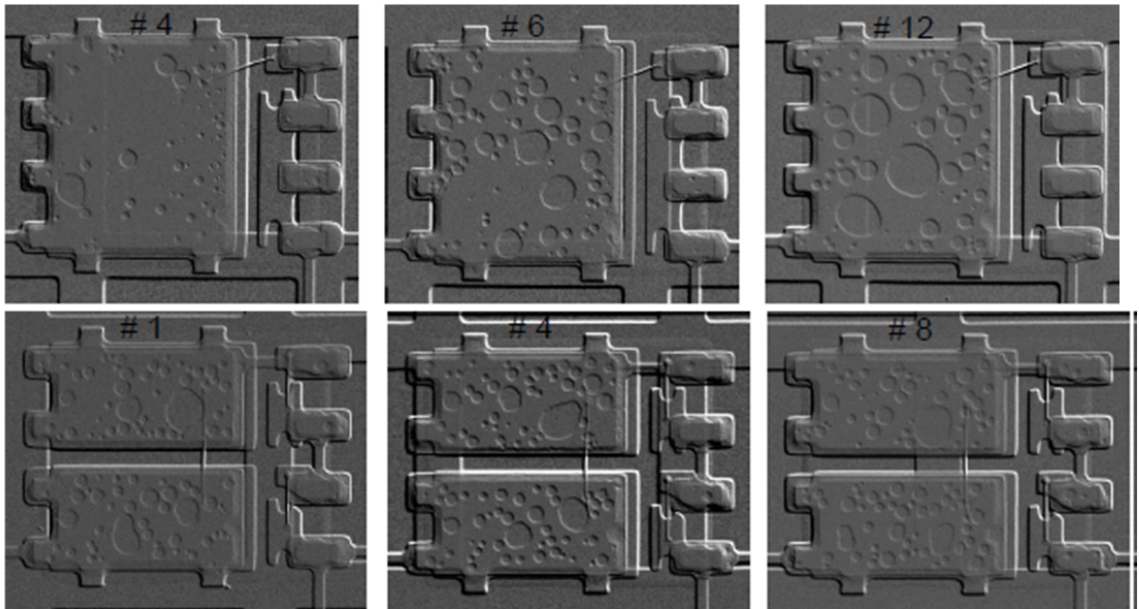
Assembly on PCB yield was 100%; no issues encountered.

**Figure 16. Assembly pictures**


As mentioned earlier, the reflow profile was not optimized, so void level was quite high. Below are some pictures of voids inside the solder joint layer (up to 30% voids in central pad).

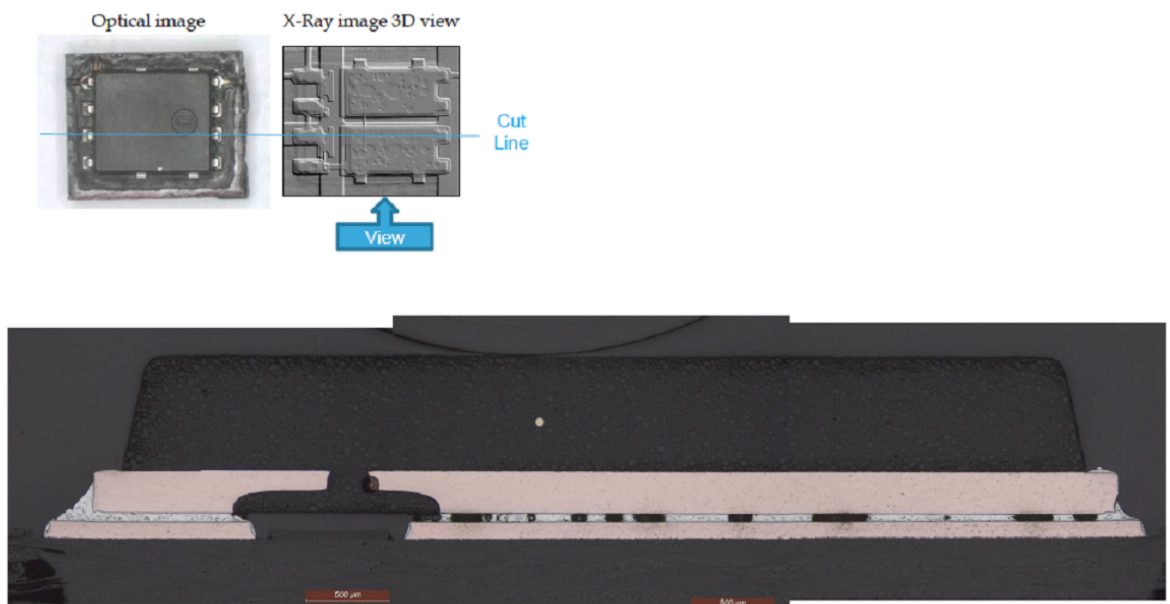


**Figure 17. X-rays showing solder joint voids**



Cross section views of the package mounted on a PCB show correct solder joints, without significant tilt, even if tilt was higher for stencil openings with the lowest opening ratio.

**Figure 18. Cross section view**



After MSL1 preconditioning level (as per IPC/JEDEC J-STD-033\*), and 1500 cycles of thermal cycling (-55/150 °C), no failures were noted.

On dual island PFLAT, no failures occurred after 2000 cycles, in any of the configurations evaluated. Evaluation was stopped after 2000 cycles.

On single island PFLAT, the first failures occurred at 2000 cycles, as described in the table below.



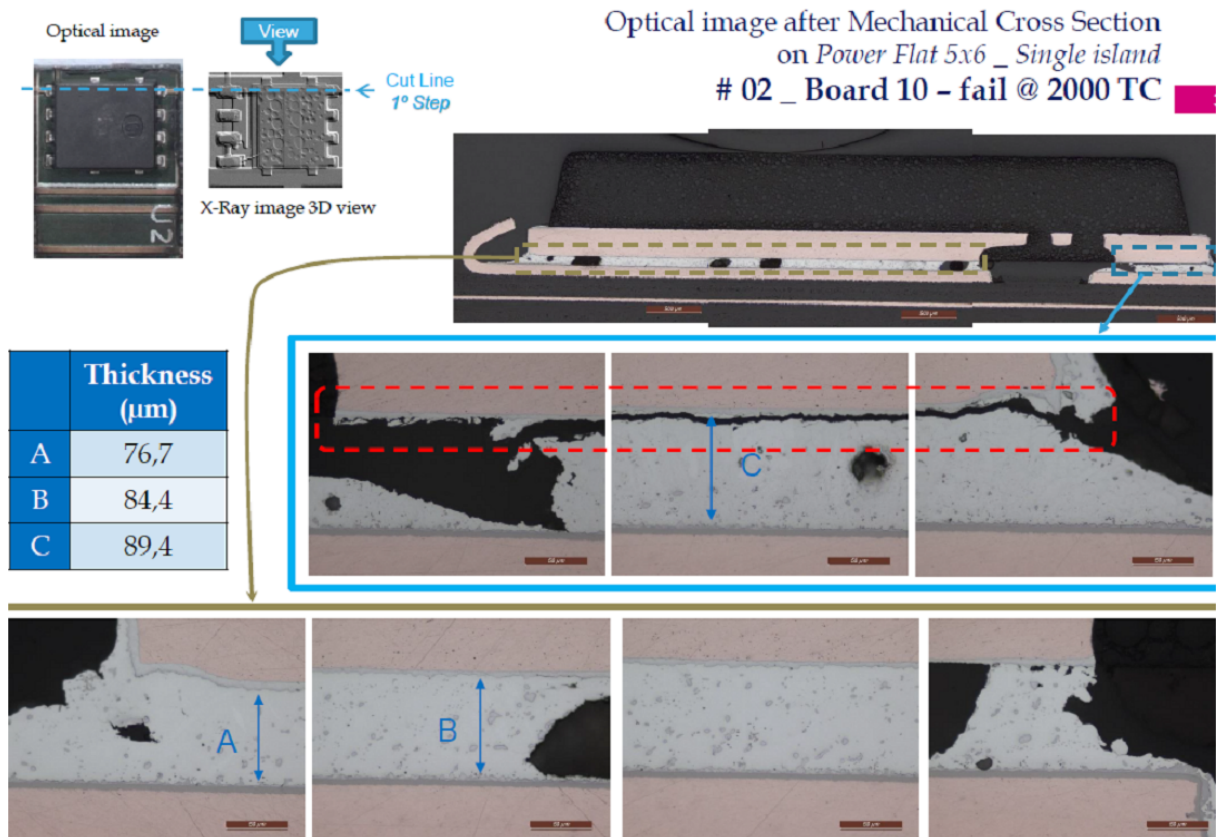
**Table 2. Thermal cycling results: 2 layer PCB**

| PCB 2 layers design |                          |                              |                              |
|---------------------|--------------------------|------------------------------|------------------------------|
| Stencil thickness   | Stencil pad opening in % | Results MSL1 + TC 1500 cycle | Results MSL1 + TC 2000 cycle |
| 100 µm              | 73%                      | 0/24 fail                    | 0/24                         |
| 100 µm              | 61%                      | 0/24                         | 0/24                         |
| 100 µm              | 49%                      | 0/24                         | 0/24                         |
| 100 µm              | 41%                      | 0/24                         | 0/24                         |
| 125 µm              | 73%                      | 0/24                         | 0/24                         |
| 125 µm              | 61%                      | 0/24                         | 0/24                         |
| 125 µm              | 49%                      | 0/24                         | 0/24                         |
| 125 µm              | 41%                      | 0/24                         | 0/24                         |

**Table 3. Thermal cycling results: 6 layer PCB**

| PCB 6 layers design |                          |                              |                              |
|---------------------|--------------------------|------------------------------|------------------------------|
| Stencil thickness   | Stencil pad opening in % | Results MSL1 + TC 1500 cycle | Results MSL1 + TC 2000 cycle |
| 100 µm              | 73%                      | 0/24 fail                    | 1/24                         |
| 100 µm              | 61%                      | 0/24                         | 0/24                         |
| 100 µm              | 49%                      | 0/24                         | 0/24                         |
| 100 µm              | 41%                      | 0/24                         | 1/24                         |
| 125 µm              | 73%                      | 0/24                         | 0/24                         |
| 125 µm              | 61%                      | 0/24                         | 0/24                         |
| 125 µm              | 49%                      | 0/24                         | 0/24                         |
| 125 µm              | 41%                      | 0/24                         | 1/24                         |

Failure analysis was conducted for each reject and showed full cracks in the solder joint under the lead (no crack under drain pad), as highlighted in [Figure 19. Failure analysis sample after 2000 cycles](#) below.

**Figure 19. Failure analysis sample after 2000 cycles**


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### 3 Conclusion

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This evaluation confirmed that PowerFLAT assembly on a printed circuit board is a safe and reliable process, and allows at least 1500 thermal cycles (-55/+150 °C) without issues. For applications requiring better behavior, some optimization may still be done (reflow profile fine tuning, stencil design and thickness) to ensure a stronger solder joint (thicker and with fewer voids).

We noticed also that the stencil opening ratio under the central pad does not have a major influence on void levels, although we recommend a design with more than 50% opening ratio to avoid excessive tilt.

## Revision history

**Table 4. Document revision history**

| Date        | Revision | Changes                                                                                                                                                                                                                                     |
|-------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17-Aug-2017 | 1        | First release                                                                                                                                                                                                                               |
| 29-Aug-2017 | 2        | Updated Figure 2. PowerFLAT $R_{th}$ , Figure 3. Mounting techniques for power SMDs, Figure 8. Stencil opening dimensions, Figure 12. ST Ecopack recommended soldering reflow profile for PCB mounting.<br>Removed Fig 9, replaced by text. |
| 04-Oct-2018 | 3        | Updated Figure 5. PowerFLAT single pad PCB footprint and Figure 9. PowerFLAT single pad stencil opening recommendation.                                                                                                                     |
| 15-Mar-2019 | 4        | Updated ST trademark management.<br>Minor text changes.                                                                                                                                                                                     |

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